Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters

Ze Ni, *Student Member, IEEE*, Xiaofeng Lyu, *Member, IEEE*, Om Prakash Yadav, Brij N. Singh, *Senior Member, IEEE*, Sheng Zheng, *Senior Member, IEEE*, and Dong Cao, *Member, IEEE*

***Abstract*—Remaining useful lifetime prediction and extension of Si power devices have been studied extensively. Silicon carbide (SiC) power devices have been developed and commercialized. Specifically, SiC MOSFETs have been utilized for the next generation high-voltage, high-power converters with smaller size and higher efficiency, covering various mainstream applications, including photovoltaic systems, electric vehicles, solid-state transformers, and more electric ships and airplanes. However, the SiC-based devices have different failure modes and mechanisms compared with Si counterparts. Therefore, a comprehensive review is critical to develop accurate lifetime prediction and extension strategies for SiC power converter systems. The SiC power device component-level failure modes and mechanisms are first investigated. Different accelerated lifetime tests and component-level lifetime models are then compared. Power converter system-level offline lifetime modeling techniques and software tools are further summarized. Besides, the SiC power converter condition monitoring strategies and health indicators are surveyed. The online measurement challenges are also studied. Furthermore, the system-level lifetime extension strategies are reviewed. By integrating device physics, statistical modeling, reliability engineering, and mechanical engineering with power electronics, this article is intended to provide a comprehensive overview, address existing challenges, and unfold new research opportunities regarding the SiC power converter real-time lifetime prediction and extension.**

***Index Terms*—Accelerated lifetime test (ALT), active thermal control, ageing indicator, condition monitoring, failure mode, lifetime control, lifetime modeling, reliability, remaining useful lifetime (RUL), silicon carbide (SiC) MOSFET, temperature-sensitive electrical parameter (TSEP).**

Manuscript received August 16, 2019; revised November 7, 2019; accepted December 12, 2019. Date of publication December 26, 2019; date of current version April 22, 2020. This work was supported in part by ND EPSCoR under Award no. FAR0029766, in part by NASA EPSCoR Research Cooperative Agreement under Award no. 80NSSC19M0081, and in part by the Center of Quality, Reliability, and Maintainability Engineering (CQRME), NDSU. Recommended for publication by Associate Editor A. Lindemann. *(Corresponding author: Dong Cao.)*

Z. Ni is with the ECE Department, North Dakota State University, Fargo, ND 58108 USA (e-mail: ze.ni@ndsu.edu).

X. Lyu is with Navitas Semiconductor, Inc., Los Angeles, CA 90245 USA (e-mail: xiaofeng.lyu@ndsu.edu).

O. P. Yadav is with the IME Department, North Dakota State University, Fargo, ND 58108 USA (e-mail: om.yadav@ndsu.edu).

B. N. Singh is with the John Deere, Inc., Fargo, ND 58102 USA (e-mail: SinghBrijN@JohnDeere.com).

S. Zheng is with the National Transportation Research Center, Oak Ridge National Laboratory, Knoxville, TN 37932 USA (e-mail: zhengs@ornl.gov).

D. Cao is with the ECE Department, University of Dayton, Dayton, OH 45469 USA (e-mail: dcao02@udayton.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2962503

NOMENCLATURE

C_{OX}	Oxide capacitance.
dI_d/dt	Drain–source current switching rate.
$\Delta\varepsilon_p$	Plastic strain change in thermal cycles.
ΔT	Temperature range in the entire thermal cycle.
ΔT_0	Elastic temperature range.
ΔT_j	Junction temperature swing.
ΔT_{on}	Turn-ON time duration.
ε_s	Bond wire strain.
ε_p	Bond wire plastic strain.
E_a	Activation energy.
f_{sw}	Switching frequency.
I_d	Drain–source current.
I_{dss}	Drain leakage current.
I_{gp}	Gate current plateau.
I_{gss}	Gate leakage current.
k_b	Boltzmann's constant.
L_G	Gate length.
L_S	Solder crack length.
LT (V_{normal})	Lifetime of components under normal use.
LT (V_{stressed})	Lifetime of components under voltage stress.
λ_C	Channel length modulation factor.
λ_i	Failure rate of the *i*th individual component.
$\lambda_{\max}$	Maximum failure rate among all components.
Λ	System failure rate.
μ_N^*	Electron mobility.
N_f	Number of cycles to failure.
$R_{\mathrm{ds_on}}$	Drain–source ON-state resistance.
R_{on}	Body diode ON-state resistance.
$R_{\mathrm{th_jc}}$	Junction-case thermal impedance.
$R(t)$	System reliability.
T_j	Junction temperature.
$T_{j_\max}$	Maximum junction temperature.
T_{j_mean}	Average junction temperature.
$V_{\mathrm{ce_on}}$	ON-state collector–emitter voltage.
V_{ds}	Drain–source voltage.
$V_{\mathrm{ds_on}}$	ON-state drain–source voltage.
V_F	Body diode forward voltage.
V_{gs}	Gate–source voltage.
$V_{\mathrm{gs_mp}}$	Gate–source voltage Miller plateau amplitude.
V_{normal}	Normal voltage amplitude.
V_{stressed}	Stressed voltage amplitude.
V_{th}	Threshold voltage.
Acronyms	
ALT	Accelerated lifetime test.

BN	Bayesian network.
CTBN	Continuous-time BN.
CTE	Coefficient of thermal expansion.
DBN	Dynamic BN.
DCB	Direct copper bonding.
DFTA	Dynamic fault tree analysis.
DPWM	Discontinuous PWM.
DRBD	Dynamic reliability block diagram.
DTBN	Discrete-time BN.
DUT	Device under test.
EKF	Extended Kalman filter.
FTA	Fault tree analysis.
GaN	Gallium nitride.
HTGB	High-temperature gate bias.
HTRB	High-temperature reverse bias.
KF	Kalman filter.
MC	Markov chain.
MTTF	Mean time to failure.
PC	Power cycling.
PF	Particle filter.
PoF	Physics of failure.
PWM	Pulsewidth modulation.
RBD	Reliability block diagram.
RUL	Remaining useful lifetime.
SiC	Silicon carbide.
TC	Temperature cycling.
TDDB	Time-dependent dielectric breakdown.
THD	Total harmonic distortion.
TS	Thermal shock.
TSEP	Temperature-sensitive electrical parameter.

I. Introduction

POWER converters are the key power-processing components for many emerging applications including renewable energy generation and storage systems, electric or hybrid electric vehicle drives, solid-state transformers, more electric ships and airplanes, etc. To reduce the total design and maintenance cost, and to guarantee the uninterrupted power delivery system operation and the human safety, two generalized approaches have been extensively studied. One is from the perspective of the design for reliability [1] through integrating the reliability and durability analysis into the design period. Most recent research in this area has adopted artificial intelligence methods such as artificial neural network to optimize the balance between design parameters and reliability indexes [2]. Another more widely researched method is regarding the accurate remaining useful lifetime (RUL) prediction of power converters, which can help prevent unwanted failures and generate better maintenance plans. This work will focus on the second one. The reliability and lifetime prediction of silicon (Si) semiconductor device based power converters have been commonly investigated [3]–[11]. Over the past decade, power converters based on silicon carbide (SiC) semiconductor devices such as SiC MOSFETs have demonstrated superior performance in terms of efficiency and power density [12]–[15]. Compared with Si devices, SiC MOSFETs feature higher withstand voltage, higher operating temperature, higher switching frequency, and smaller ON-state resistance [16]–[19]. Nevertheless, SiC MOSFETs are facing new reliability challenges compared with Si devices [20], [21]. Therefore, to design more reliable SiC power converters, an understanding of additional SiC MOSFET failure modes, lifetime prediction approaches, and online monitoring strategies is needed for real-time lifetime prediction.

SiC MOSFETs have the chip-level and package-level failure modes. The chip-level failure modes are mainly related to gate oxide and body diode. Compared with Si devices, the gate oxide of SiC MOSFETs has a higher probability of time-dependent dielectric breakdown (TDDB) according to the following three aspects.

1) Higher electric field is normally used to achieve lower channel resistance.
2) Higher temperature operation is preferred to shrink the cooling systems.
3) Higher Fowler–Nordheim tunneling current exists due to smaller conduction band offset between SiC and SiO_2 [22]–[25].

The body diode failure of SiC MOSFETs is primarily caused by stacking faults. Most of the package-level failure modes appear at bond wires and solder layers. The bond wires between the SiC die and the direct copper bonding (DCB) are less reliable compared with those in Si-based devices, due to worse flexibility caused by about ten times hardness of SiC material [26]. Besides, both the bond wires and solder layers in SiC devices are more possibly subjected to thermomechanical degradation caused by coefficient of thermal expansion (CTE) mismatch during commonly higher temperature operation. Therefore, the SiC MOSFET failure modes, mechanisms, and indicators are essential to develop the component-level lifetime models.

Traditionally, to generate a lifetime prediction, offline lifetime models are developed. These models need statistical methods such as Monte Carlo analysis for the parameter estimation [3], [4], [6], [7]. To verify the validity of the lifetime models, accelerated lifetime tests (ALTs) to stress certain failure modes should be performed [6], [7], [10]. The lifetime prediction of power converters could be investigated from the component level to the system level. The main components of power converters include active switches, capacitors, and inductors. The lifetime models of these components have been developed based on PoF, data-driven, and hybrid methods. They are verified by ALTs [27]–[32]. Based on component-level lifetime models, the system-level lifetime models could be developed by RBD, failure tree analysis (FTA), and Markov chain (MC) [4]–[11], [33]. However, the offline system lifetime model accuracy is limited, since it cannot be dynamically adjusted during the system operation. A more accurate real-time lifetime model with data updating features is needed through condition monitoring. How to combine the monitored degradation indicator information and the ALT-based statistical models is the major challenge.

The semiconductor device reliability has been reviewed systematically [34]. Failure mechanisms and lifetime prediction techniques have also been summarized in [35]. But these papers have not covered the RUL estimation modeling methods of the power converter systems. Besides, the RUL estimation models have been thoroughly analyzed in [36]–[38]. But they are presented in a generally statistical way. Therefore, it can be

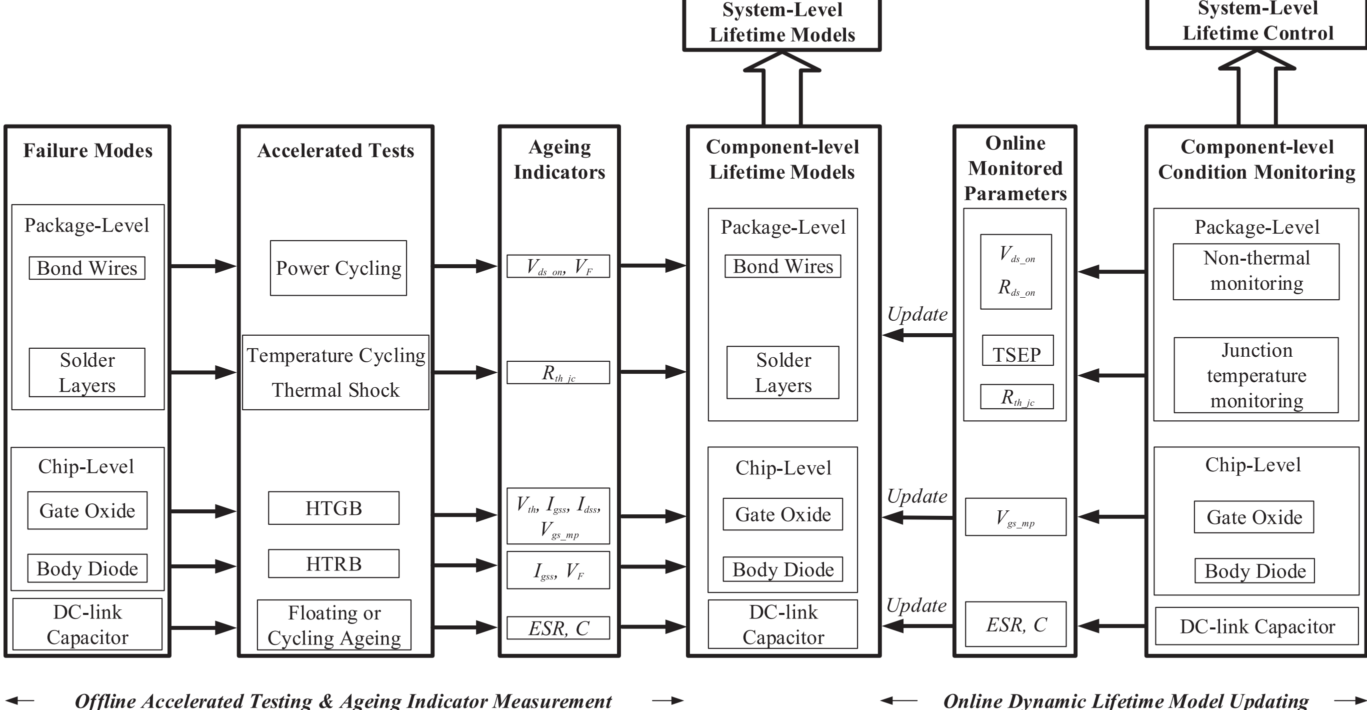


Fig. 1. Online and offline system lifetime modeling summary for power converters.

concluded that there is no dedicated overview on system-level RUL estimation and extension for SiC power converters.

This article intends to address these challenges and provide a comprehensive overview of the real-time lifetime prediction and extension strategies for SiC MOSFET-based power converters. Fig. 1 shows the organization of this overview. Due to the space limitation in this figure, only typical ageing indicators and online monitored parameters have been included. More health indicators will be explained further. As shown in this figure, lifetime modeling can be conducted either offline or online. By combining the static offline lifetime models with real-time data through online monitoring, it is possible to generate a more accurate real-time estimation method for RUL.

This real-time SiC power converter lifetime prediction methodology could be explained in the following four steps.

A. Health Indicator Monitoring and Calculation

Both the chip-level and the package-level failure indicators could be monitored online. By measuring these parameters, the lifetime models derived from the ALTs could be updated, and the corresponding real-time lifetime models could be developed. For example, the ON-state device voltage has been measured in real time to reflect the package-level degradation such as the bond wire liftoff [39], [40]. The Miller plateau amplitude has been measured to detect gate oxide ageing [41]. Equivalent series resistance (ESR) and capacitance have been monitored to tell the dc-link capacitor health condition [42]. Section II will be dedicated to more detailed health indicators.

To estimate the model parameters in the lifetime models of each component, algorithms such as the Kalman filter (KF), the extended KF (EKF), and the particle filter (PF) could be used. Section III will analyze more in this modeling part.

B. Component Health Indicator Integration

Since a component could have more than one health indicator, an integration should be conducted for each component. In this procedure, all the monitored health indicators of each component are integrated to reflect the health condition for this specific component. For example, 11 health indicators have been collected and processed through principle component analysis to detect unsupervised degradation in the SiC MOSFETs [43].

C. Component Interdependence Consideration

Different failure indicators can be the cause and result of each other. For instance, the negative bias temperature stress results in negative shift of V_{th}, which induces the increase of I_{dss} [44]. Besides, when solder-fatigue happens, the thermal impedance increases, which causes T_j to rise. This, in turn, results in an increase of $V_{\mathrm{ds_on}}$, which indicates another failure mode—bond wire liftoff. Likewise, bond wire liftoff induces uneven current distribution, which generates higher power loss and corresponding higher junction temperature. Hence, more thermal stress is put onto the solder layers [45].

Thus, the failure-mode interdependence among different components in the system should be included in this procedure.

D. System-Level RUL Prediction

Based on the widely investigated system-level lifetime modeling techniques, the SiC power converter system-level lifetime

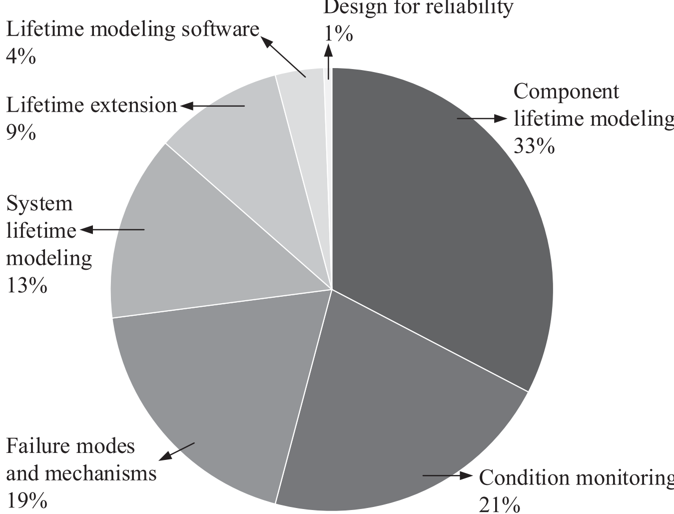


Fig. 2. Classification and statistical analysis of the referenced papers.

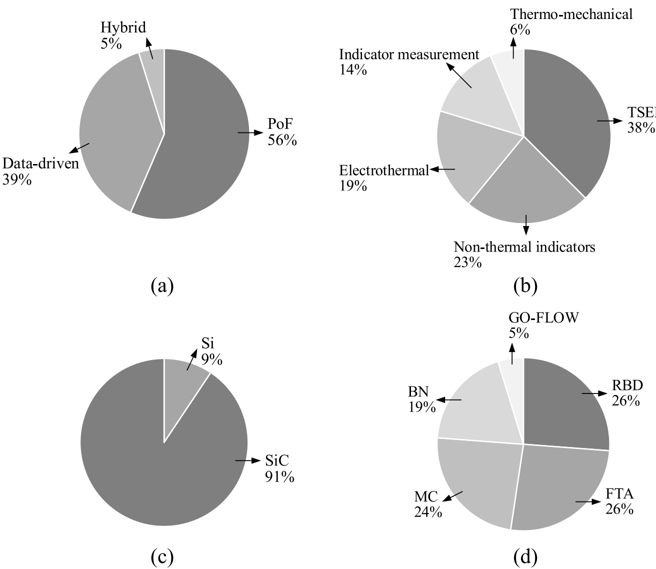


Fig. 3. Paper percentage in (a) component-level lifetime modeling, (b) condition monitoring, (c) failure modes, and (d) system-level lifetime modeling.

modeling could be further made and the lifetime prediction could be conducted in real time more accurately. Further details in this part will be presented in Section IV.

The online monitored data could be further used for active lifetime extension. A tradeoff between reliability improvement and system performance has to be cautiously considered [46]–[49]. Section VII will summarize these techniques.

To make the more than 300 cited papers more illustrative, a statistical analysis has been made. Fig. 2 shows the percentage of the papers in each investigated category. The papers concerning the component lifetime modeling takes the largest proportion, which is 33% among all the categories. In areas of condition monitoring as well as failure modes and mechanisms, the percentage is 21% and 19%, respectively. Papers regarding the system lifetime modeling take about 14%.

Fig. 3 further classifies the four main categories into detailed subcategory percentage. Fig. 3(a) shows that in this overview, the papers regarding the PoF models contribute most to the component lifetime modeling domain. From Fig. 3(b), in the condition monitoring area, about 38% and 23% of this research focuses on temperature-sensitive electrical parameters (TSEPs) and non-thermal indicators, respectively. Fig. 3(c) presents around 91% of the cited papers in the failure-mode domain are related to the SiC MOSFETs. In Fig. 3(d), regarding the system lifetime modeling, the mostly cited papers are related to RBD, failure tree analysis (FTA), and MC.

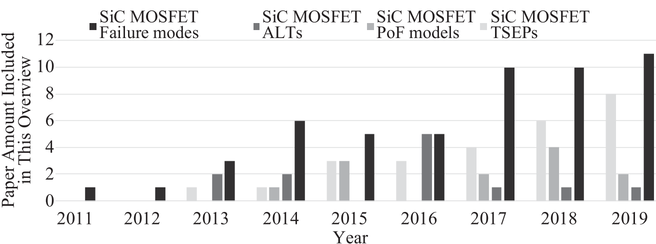


Fig. 4. Amount of the included SiC MOSFET-based papers by the year.

Furthermore, from the literature review, the main reliability domains based on SiC MOSFETs, such as failure modes, ALTs, PoF models, and TSEPs, have not been investigated extensively compared with the Si counterparts. Therefore, Fig. 4 lists the amount of the SiC MOSFET-based papers included in this overview by the year. It shows a trend of the number of SiC MOSFET-based papers these years, especially in the areas of failure modes and TSEPs.

This article will be organized as follows. Section II reviews the failure modes, mechanisms of SiC MOSFETs, and the corresponding aging indicators. Section III first covers the ALTs relevant to the presented specific indicators. Component-level static RUL models are then presented. The cycle counting and fatigue damage accumulation approaches are also analyzed as necessary procedures of deriving lifetime models. Section IV summarizes system-level static lifetime modeling. Section V lists the component-level and system-level lifetime modeling software. Section VI gives a comprehensive analysis of the SiC power converter real-time condition monitoring methods and the corresponding parameters. These online measured parameters could be utilized to make the models more accurate through dynamically updating the initial system-level models. Section VII reviews the system-level lifetime extension strategies to actively improve the RUL. Finally, Section VIII provides the conclusion and recommendations for future work.

II. SiC MOSFET Failure Modes and Mechanisms

To derive the lifetime models, the failure modes and mechanisms of SiC MOSFETs should be investigated first. This physical understanding would lay the foundation for identifying the indicators of various failure modes. Furthermore, the failure criteria could be developed based on these indicators.

The frequently encountered failure modes of SiC MOSFETs are located at the gate oxide, body diode, bond wire, chip-substrate solder layer, and substrate–baseplate solder layer [50]. Among them, the gate oxide and the body diode are considered as the device chip level, whereas the bond wire, chip solder-substrate layer, and substrate–baseplate solder layer are considered as

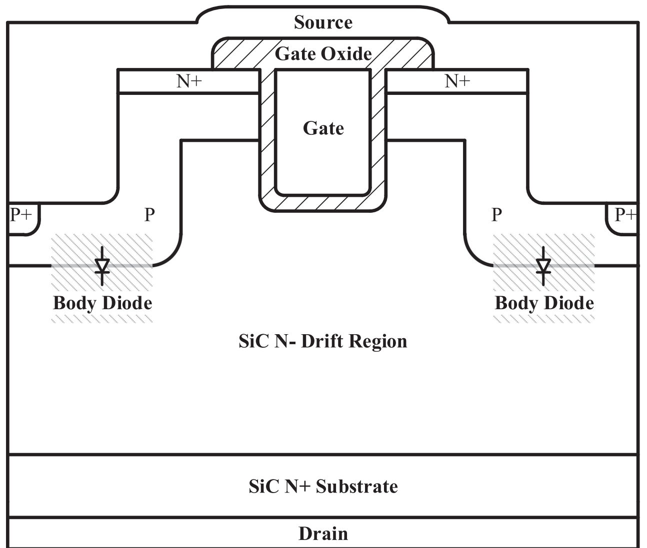


Fig. 5. Up-to-date typical SiC MOSFET chip-level structure.

the device package level. These chip-level and package-level failure modes are challenging to be monitored directly due to their inaccessible locations. In the following, these two groups of failure modes and mechanisms as well as the corresponding indicators will be summarized.

A. Chip-Level Failure Modes of SiC MOSFETS

Fig. 5 shows an up-to-date typical chip-level SiC MOSFET trench structure [51] with low ON-state resistance and improved gate oxide reliability especially at the bottom of the gate trench [52], [53]. The most common chip-level failure modes of SiC MOSFETs occur at the gate oxide and body diode.

Gate oxide degradation failure is basically caused by the tunneling current into the gate oxide layer [54]. Two stresses contribute to the gate oxide degradation, i.e., high electric field stress and high temperature stress. Compared with Si devices, three aspects have counteracted the gate oxide reliability of SiC MOSFETs. First, SiC MOSFETs have lower inversion channel mobility [23]. As a result, higher electric field is needed to realize smaller channel resistance. So, a tradeoff exists between smaller ON-state resistance and better gate oxide reliability. Second, higher interface state density occurs at SiC–SiO_2 interface [23], [55], which brings in lower barrier height. Thus, more mobile hot carriers are injected from doped SiC to oxide. Therefore, it is more likely for the carrier nonequilibrium to induce the gate oxide dislocation. Third, smaller conduction band offset between SiC and SiO_2 [24] introduces higher Fowler–Nordheim tunneling current at similar gate electric field and temperature. Hence, there is higher probability of TDDB. In sum, the more possibly degraded gate oxide in SiC MOSFETs would further lead to the failures such as short circuit [56].

The intrinsic body diode failure is normally due to the recombination-induced stacking fault mechanism [57]. The forward voltage bias stress has been reported to be the primary cause of the body diode degradation [16], [57], [58].

1) Gate Oxide: There are two main failure mechanisms for SiC MOSFET gate oxide. One is the TDDB, which is caused by high temperature and high electric field stress [24]. Compared with Si counterparts, SiC MOSFETs are more often applied with higher $V_{\rm gs}$ and higher temperature to achieve lower ON-state resistance and smaller heat sink. This would make the gate oxide more vulnerable [59]. The other is the avalanche breakdown, which is caused by high electric field stress [59], [60]. The most extensively studied indicators of gate oxide degradation include Miller plateau voltage amplitude [61], [62], Miller plateau time duration [62], drain leakage current [63], threshold voltage [44], gate leakage current [63], and ON-state resistance [62].

1) Miller plateau voltage amplitude $V_{\rm gs_mp}$ increases with the $V_{\rm gs}$ stress, and is identified as a more obvious indicator than threshold voltage $V_{\rm th}$ for Si MOSFET gate oxide degradation [61]. In SiC MOSFETs, $V_{\rm gs_mp}$ is verified to be an indicator of gate oxide degradation by high electric field stress test and positive bias temperature stress test [64]. As shown in (1), with higher electric field stress, the μ_N^* decrease caused by electron scattering [65] and the $V_{\rm th}$ increase caused by the electrons confined to the SiC–SiO_2 interface [66] will lift up $V_{\rm gs_mp}$. The second stress of the Miller plateau shift is caused by the temperature dependence of $V_{\rm th}$ and electron mobility [59]

$$V_{\rm gs_mp} = \sqrt{\frac{2 \cdot I_d \cdot L_G}{\mu_N^* \cdot C_{\rm OX} \cdot W_G \cdot (1 + \lambda_C \cdot V_{\rm ds})}} + V_{\rm th} \quad (1)$$

where μ_N^* is the electron mobility, $C_{\rm OX}$ is the oxide capacitance, W_G, L_G are the gate width and length, respectively, and λ_C is the channel length modulation factor.

2) Miller plateau time duration $T_{\rm gs_mp}$ has been shown to have a larger positive shift in Si MOSFETs compared with $V_{\rm gs_mp}$ and $V_{\rm th}$ under the high electric field test [62].

3) Both the drain leakage current $I_{\rm dss}$ and threshold voltage $V_{\rm th}$ tend to increase with stress time under the high temperature gate bias (HTGB) test [44], [63], [67]. The change of $I_{\rm dss}$ and threshold voltage $V_{\rm th}$ fundamentally appears together due to the same shift mechanism [68]. Their shift is mainly caused by high electric field stress and high temperature stress [44], [69]–[71]. When a continuous positive $V_{\rm gs}$ is applied, the electrons are gradually trapped at the SiC–SiO_2 interface. This results in an increase in $V_{\rm th}$. Contrarily, with a continuous negative $V_{\rm gs}$, the holes are trapped at the SiC–SiO_2 interface, which causes $V_{\rm th}$ to decrease [72]. This $V_{\rm th}$ instability issue is mainly caused by the active charge traps in the near-interfacial region in the gate oxide [73]. Besides, due to a larger portion of the capture and emission in the holes and electrons, the $V_{\rm th}$ hysteresis effect has been measured and verified to be more obvious in SiC MOSFETs compared with Si counterparts [74].

4) Gate leakage current $I_{\rm gss}$ increases with stress time under the high-temperature reverse bias (HTRB) test [63]. Under the operating condition of the high electric field and high temperature, the localized heat stresses the polycrystalline silicon gate metal. As a result, the voids are formed and

cracks appear in the gate metal, through which I_{gss} flows between the source and gate. Thus, I_{gss} could be an indicator of SiC MOSFETs gate oxide breakdown. Since SiC MOSFETs have thinner gate oxide layer compared with Si counterparts for the sake of a desirably lower V_{th} value [75], they are more easily affected by large variations of V_{ds} and T_j. So, there is higher probability to induce larger I_{gss} for SiC MOSFETs [67].

5) ON-state resistance $R_{\text{ds_on}}$ is an indicator for Si MOSFET gate oxide degradation [62], [67], [76], [77], although it has been mostly used to indicate the package-related failures. SiC $R_{\text{ds_on}}$ mainly consists of the channel resistance due to mobile carriers, resistance in the N^+ source layer, resistance in source and drain electrodes, and resistance in the N^- drift region between two adjacent wells of p-type semiconductor [78]. Higher electric field stress increases the oxide charge density and further enlarges the overall $R_{\text{ds_on}}$. So, $R_{\text{ds_on}}$ could indicate the SiC MOSFET gate oxide degradation.

2) Body Diode: Formed by the N^- drift region and the well of p-type semiconductor, the SiC MOSFET body diode degradation is caused by the forward voltage bias stress [16], [57], [58] owing to the stacking fault mechanism [57], [79]. The continuous forward current flowing through SiC MOSFET p-n junction results in accumulated hole–electron recombination energy [16], [58], which forms the stacking fault extended at the body diode. Since the forward current pathway is blocked by these faults, both the ON-resistance and forward voltage of the body diode would rise [80]. The larger body diode ON-resistance brings in the thermal-design challenges. The increase of forward voltage drop could degrade the blocking voltage. Therefore, in the topologies with current commutation occurring at the body diode, such as full-bridge inverters, these stacking faults play a significant role in reducing the system lifetime.

Three indicators of the body diode degradation have been the body diode ON-resistance R_{on} [16], forward voltage V_F [81], and drain leakage current I_{dss} [59]. They are fundamentally attributed to the high-density basal plane dislocation in the lightly doped N^- drift layer [57], [82]. V_F of body diode has been demonstrated to be influenced by the forward stress duration [57], [58], [82] based on the ALT results. Similarly, I_{dss} has been shown to increase with the forward stress duration as well [57].

B. Package-Level Failure Modes of SiC MOSFET

From the perspective of package-level failure modes, most literature focuses on Si IGBT modules. SiC MOSFET package-level failure modes have not been well studied. Fig. 6 shows one typical SiC MOSFET power module package with bond wires. It is mainly composed of three parts, i.e., the SiC chip die, the DCB, and the baseplate. DCB is composed of two layers of substrate conductors and a substrate insulator layer in between. The substrate conductor is usually made of copper. Substrate insulator could be made of ceramics by using Al_2O_3, AlN, or Si_3N_4 [83]–[85]. Bond wires connect the SiC die and the DCB. The chip die and the DCB, as well as the baseplate and the DCB, are commonly attached by solder. The baseplate could be made of copper or AlSiC [84], [85].

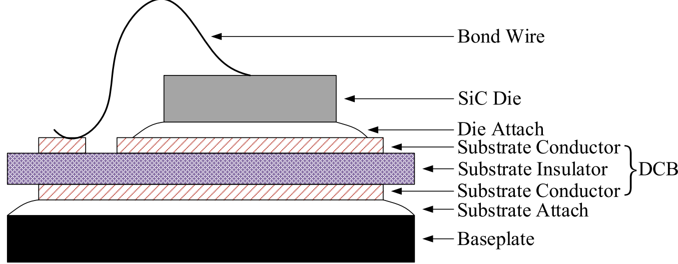


Fig. 6. SiC MOSFET package-level structure.

Compared with that of the Si counterparts, the package-level reliability of the SiC MOSFETs is not so promising. It will be analyzed in detail from three perspectives regarding the semiconductor fabrication, mechanical, and material properties.

1) From the semiconductor fabrication perspective, SiC-based dies have smaller active die areas compared with Si-based ones assuming the same current rating [86]. It means that SiC dies have higher current density than Si ones. As a result, the electromigration would be more likely to occur in SiC devices [87]. Hence, there is higher probability for the electromigration to generate more internal voids inside the bond wires [87]. These voids would increase the imbalanced current density among the bond wires and strengthen the unequal self-heating effect [88]. The electromigration could also generate more solder voids and induce worse interconnect failures [89]. In summary, at the same temperature and the same current rating, higher current density in SiC devices induces higher probability of degradation at both bond wires and solder layers. One way of alleviating this issue is to have more bond wires in parallel, thereby relieving stresses caused by high current density [87].
2) From the mechanical property perspective, SiC is stiffer and has much larger Young's modulus than Si [90]. It would bring in higher stress on the interface between the SiC die attached solder and the substrate conductor during PC. Larger Young's modulus would also result in more significant accumulated creep strain and creep energy concentration on the interface between SiC die solder and the substrate conductor at the same junction temperature [91]. Correspondingly, for SiC MOSFETs, the crack initiation would be more likely to occur on the interface between the SiC die solder and substrate conductor compared with Si counterparts.
3) From the material property perspective, SiC has higher thermal conductivity than Si. Correspondingly, the larger temperature variation has been reported in SiC devices compared to Si ones at the same current [86], [92]. This higher temperature swing could increase the stress on the interface between SiC die solder and substrate conductor.

The detailed package-level failure will be discussed further.

Bond wires and solder layers are the two mostly studied package-level failure locations of SiC MOSFET modules [93]. Package-level failures are mainly caused by three stresses. First, thermomechanical stress is induced by the CTE mismatch

among different materials. The resulted temperature swing results in solder-fatigue, crack growth, and bond wire failures [45], [94]–[96]. Second, relative humidity stress intensifies the effects of mechanical stresses, which reduces the metal atom bonding energy. Thus, the atom corrosion increases the crack growth rate at the tail of the bond wire [97]. Third, high current density stress caused by the relatively small SiC die-size could accelerate electromigration-related degradation [87], [97].

1) Bond Wires: Two types of failure mechanisms have been identified in the bond wires [98]. One is the bond wire fracture at the interface between bond wire and DCB upper surface. The other one is the bond wire liftoff at the interface between bond wire and SiC die. The bond wire fracture is caused by its alternate heating and cooling [43], [99]. The TC leads to repeated expansion and contraction on bond wires. When the thermomechanical deformation is accumulated to a certain extent, the cracks would occur. As a result, the fracture is identified at the bond wire tail interfaced with the DCB upper surface. The other type of failure is the bond wire liftoff caused by the CTE mismatch between the bond wire copper and SiC, as well as ohmic self-heating effects [87]. The thermomechanical stress changes the surface structure through the chip metallization [100]. When the chip surface structure change is accumulated to separate bond wires from the SiC die, the bond wire liftoff occurs. Furthermore, due to the parasitic resistance and high SiC current density, the internal voids and cracks would also gradually induce the bond wire liftoff [87].

Bond wire fracture happens more slowly than its liftoff [101]. Thus, the bond wire liftoff has been investigated more extensively. Following five indicators have been studied for the bond wire liftoff.

1) ON-state voltage has been identified to indicate bond wire liftoff as thermal cycles accumulate [102], [103].
2) SiC MOSFET ON-state resistance $R_{\mathrm{ds_on}}$ increases with the thermal cycles [104].
3) The voltage between the Kelvin source and power source has been used to reflect the online SiC MOSFET bond wire liftoff [105].
4) Bond wire resistance increases when SiC MOSFET bond wire liftoff deteriorates [87].
5) The eddy current in bond wires generated by pulsed electromagnetic induction heating has been used as an indicator of the IGBT bond wire liftoff [88], which could be employed to monitor SiC MOSFETs in the induction heating-related applications.

2) Solder Layers: Solder layers include the die attach between SiC die and DCB as well as substrate attach connecting DCB and baseplate [50], [106]. Due to the CTE mismatches between the SiC and solder material, between the DCB upper layer copper and solder material, shear stress gradually generates the cracks and voids in the solder layer [107]. These cracks and voids reduce the effective heat conduction area between the die and DCB copper. As a result, the thermal resistance of the chip die-to-DCB solder increases, which leads the die-attach temperature to rise. As the voids grow, this localized die-attach heating process accelerates the chip damage [108]–[110]. Two indicators have been studied in the SiC MOSFET solder layer degradation. First, the junction-case thermal impedance has been shown to increase with the degradation of die-DCB solder layer [111], substrate–baseplate solder layer [102] in the Si IGBTs and SiC MOSFETs [112]. Second, the solder layer resistance has been verified to be related to the SiC MOSFET solder-fatigue [106]. As analyzed in the chip-level failure modes, V_{th} shifts as SiC gate oxide degrades. To exclude this degradation from solder-fatigue evaluation, the body diode could be utilized to conduct the load current. Therefore, the die-attach solder layer resistance increase is not associated with SiC die degradation.

C. Summary of Failure Modes of SiC MOSFETs

The typical failure locations, causes, and indicators of SiC MOSFETs are summarized in Table I. Failure locations show where the corresponding failure modes occur. Two chip-level and two package-level failure modes are summarized. Failure causes list the stresses of different failure modes. Indicators are the external electrical parameters reflecting the corresponding internal failure modes. The indicators are identified to determine the number of cycles to failure in ALTs when the indicator values reach to the defined failure criteria [113].

For the gate oxide failure, the two causes are related to high electric field and high temperature. Higher electric field results in more localized heat, which generates more polycrystalline silicon voids between the gate and source [63]. As a result, the gate leakage current I_{gss} [63], [75] would increase. Twice the nominal value of I_{gss} has been used as a gate oxide degradation criterion [63]. Higher electric field and temperature stresses also result in more charge trapping at the SiC–SiO_2 interface [116]. It leads to the increase of both the threshold voltage shift ΔV_{th} [44], [69]–[71], [114], [115] and drain leakage current I_{dss} [114], [116]. The 20% higher than the initial V_{th} [114], or five times the initial I_{dss} [116] has been applied as the failure criterion. Higher electric field and temperature stresses also lead to the increase of both the fixed charge of the gate oxide and the charge in interface states, which uplifts the $V_{\mathrm{gs_mp}}$ [61], [62].

For the body diode failure, the forward bias is the main stress. It induces expansion of basal plane dislocations in the SiC epitaxial layer [57], [58], [82], which further causes forward voltage V_F and drain leakage current I_{dss} to increase. Thus, the body diode V_F [81] and I_{dss} [59] have been used as indicators.

For the bond wire and solder layer failures, the thermomechanical stresses are the main contributors to the failure. It causes high junction temperature in bond wires, which further leads to the increase of ON-state parameters $V_{\mathrm{ds_on}}$ and $R_{\mathrm{ds_on}}$. Thermomechanical stresses also cause crack propagation in the solder, which increases thermal impedance $R_{\mathrm{th_jc}}$. Thus, $R_{\mathrm{th_jc}}$ could be used as an indicator of the solder layer failures [113].

III. Offline Component-Level Lifetime Modeling

To obtain the component-level lifetime models, it is necessary to conduct the ALTs first. Then, the component-level SiC MOSFET lifetime estimation models are extrapolated using the information obtained from the ALTs. To analyze the irregular thermal cycles in ALT results, cycle counting techniques are applied. After that, the fatigue-accumulation approaches need

TABLE I
FAILURE LOCATIONS, CAUSES, AND INDICATORS OF SiC MOSFETS

Failure location	Failure Cause	Failure Indicator
Gate oxide	High electric field, high temperature	Gate leakage current I_{gss} [63], [75]
		Threshold voltage shift ΔV_{th} [44], [69]–[71], [114], [115]
		Drain leakage current I_{dss} [114], [116]
		Miller Plateau V_{gs_mp} [64]
Body diode	Forward bias [57], [58], [82]	Drain leakage current I_{dss} [59]
		Body diode forward voltage V_F [81]
Bond wires	Thermo-mechanical stresses	On-state drain-source voltage V_{ds_on} [103]
		Drain-source on-state resistance R_{ds_on} [104]
		Voltage between Kelvin, power sources [105]
		Bond wire resistance [87]
Solder layers		Thermal resistance R_{th_jc} [112]
		Solder layer resistance [106]

TABLE II
COMPARISON OF DIFFERENT ALTS

Test	Test condition		Test location	Failure indicator
HTGB	V_{gs} stressed to maximum voltage at maximum T_j		Gate oxide	I_{gss}
				V_{th}
HTRB	V_{ds} reversely biased to the maximum voltage at maximum T_j		Edge channel structure and solid-state junction surface	I_{dss}
PC	The device is heated and cooled by pulses		Bond wire	V_{ds_on} / V_F
				V_{th}
				R_{ds_on}
				I_{gss}
				C_{ds}
TC	External heat and cooling	Short cycle time	Solder joint, bond wire	R_{ds_on}
TS		Long cycle time	Interface between DCB and baseplate	R_{th_jc}

to be used to consider the accumulative stress effect based on the mission profiles.

A. SiC MOSFET ALTs and Indicators

To acquire reliability and lifetime data efficiently, ALTs are commonly adopted. In SiC MOSFET-based ALTs, gate oxide, solder layer, and bond wire have been subjected to higher-than-normal accelerated temperature stress and voltage stress. The test results are further applied to lifetime prediction at normal use conditions. The widely used reliability test methods for SiC MOSFETs are HTGB [117], [118], HTRB [117], [118], PC [104], [119], [120], TC [121] and thermal shock (TS) [99]. Their test conditions, locations, and failure indicators are summarized in Table II.

1) HTGB test is designed to detect the gate oxide degradation caused by the random oxide defects and the ionic-oxide contamination [117], [122]. In this test, the gate oxide is subjected to the maximum positive or negative $V_{\rm gs}$ stress at the maximum operating junction temperature $T_{j_\max}$ for a long enough period, such as 1000 h [123]. The drain and source are shorted. Gate leakage current $I_{\rm gss}$ [99], threshold voltage $V_{\rm th}$ [117], [118], [124] have been used for indicating the gate oxide degradation. The HTGB test is regarded to be passed when $I_{\rm gss}$ or $V_{\rm th}$ shift is within twice the initial value [117]. Considering the bias temperature instability in SiC MOSFETs, the $V_{\rm th}$ shift occurs due to the device self-heating in the HTGB test. By measuring the body diode forward voltage with a small drain current flowing through it, the self-heating related $V_{\rm th}$ shift is avoided [125]. So, more accurate ageing condition is indicated.
2) HTRB test is used to evaluate the stability and integrity of the edge channel structure and solid-state junction surface [117], [124]. The drain-to-source junction is reversely biased [122] by stressing $V_{\rm ds}$ at 80%–100% maximum voltage rating at $T_{j_\max}$ for a sufficiently long period, such as 1000 h [117]. The gate and source are shorted. The drain leakage current $I_{\rm dss}$ is used as the indicator [123]. HTRB test is regarded to be passed when $I_{\rm dss}$ is within twice the initial value [117].
3) PC test is intended to detect the degradation of bond wires [99]. PC test can be classified into dc and ac tests based on different heating sources [126]. The heating of dc PC tests is from only conduction power loss $P_{\rm cond}$. The device under test (DUT) in ac PC tests is heated by both the conduction loss $P_{\rm cond}$ and switching loss $P_{\rm sw}$. In this test, the gate is triggered either continuously or alternately, so that the DUT is heated with load current flowing through the junction. Then, the DUT is cooled down shortly by turning OFF the power and using external cooling such as typically chosen water cooling. Threshold voltage $V_{\rm th}$ [120], ON-state resistance $R_{\rm ds_on}$ [104], [120], [127], gate leakage current $I_{\rm gss}$ [120], drain–source capacitance $C_{\rm ds}$ [120], ON-state voltage $V_{\rm ds_on}$ [120], [122] and body diode forward voltage V_F [99] can be used for the indicators. One criterion for the pass is that $V_{\rm ds_on}$ or V_F should be within +5% the initial value [99]. As temperature rises, for either Si or SiC MOSFETs, the decrease of mobility in the drift region [128] results in an increase of drift region resistance. For SiC MOSFETs, the channel mobility increase leads to channel resistance decrease [129]. This

would counteract the increase of the drift region resistance. As a result, $R_{\text{ds_on}}$ is less temperature-relevant [130], [131] and, thus, is not an ideal indicator in SiC MOSFET PC test. Also, due to smaller die-size in SiC and resulted less apparent change of Miller capacitance compared with Si devices, the discharge time of Miller capacitor is not so sensitive to be an indicator in SiC PC tests [132], [133]. Considering these constraints, the TSEPs for the SiC MOSFETs have been explored. One promising dc PC TSEP is identified as body diode's voltage drop at low current and negative gate bias, which is shown to be independent of the ageing effect [134], [135].

4) TC test is also used for the acceleration of the packaging interconnection degradation. But the heating and cooling sources are from the eternal hot plate or thermal chamber. Compared with PC test, TC test is able to achieve more precise temperature control of $T_{j_\max}$, T_{j_mean}, and ΔT_j.

5) TS test is similar to TC test, but with longer thermal cycling time. The DUT is heated in one chamber for a sufficient time and then cooled in another chamber for another enough period. The time should be long enough to guarantee that the DUT has a uniform temperature distribution. The transfer time between these two chambers does not contribute to the accelerated ageing in this test, and thus, should be short.

The aforementioned ALTs could also be combined with other characterization tests to realize specific functions. A double pulse test has been integrated with a PC test platform to acquire multiple health indicators in real time [136].

Commonly adopted reliability test standards for power devices have been published by Joint Electron Device Engineering Council (JEDEC) [137], Automotive Electronics Council (AEC) [116], [138], International Electrotechnical Commission (IEC) [44], and Military Standard (MIL STD) 750 [138]. The transfer characteristics are sensitive to both the measurement sweep speed and direction for SiC MOSFETs [138]. However, none of the existing standards has considered this issue. Besides, V_{th} shift in SiC MOSFETs tends to recover when the temperature rapidly decreases under a positive bias thermal stress [122]. The minimum uninterrupted bias duration in the MIL-STD-750F standard [139] is defined as 8 h [140]. The maximum interrupted bias duration in the JEDEC JESD22-A108D standard [36] is regulated as 96 h for devices working at the voltage larger than 10 V, or 168 h for all other devices. Nevertheless, these minimum uninterrupted and maximum interrupted bias durations need to be reconsidered for SiC MOSFETs. JEDEC is now working on JC-70.2 standards to clarify the qualification procedures and characterization methods for SiC MOSFETs [140].

B. Component-Level Lifetime Modeling Methods

Lifetime models are used to estimate the reliability under normal operating conditions based on the failure data obtained from ALTs. Every acceleration model has its own application conditions [101]. The component-level statistical models have been reviewed in [141]. The data obtained from ALTs are discrete numbers. To use them in the fully parametric RUL estimation, extrapolation is typically conducted based on PoF models, data-driven models, and hybrid models for both chip-level and package-level RUL modeling.

1) PoF Models: The PoF models are based on the physical parameters reflecting corresponding failure mechanisms. They use statistical methods for parameter identification, which requires experiments and tested data. The PoF models are classified based on different failure modes, such as gate oxide failure, bond wire fracture and liftoff, and solder-fatigue.

Gate oxide failure could be caused by voltage stress related to high electric field. The corresponding lifetime model is based on stressed and normal voltage [97], [115], as shown in (2). It has advantages in predicting long-term damage behaviors due to their damage accumulation mathematical description

$$\text{LT}(V_{\text{Stressed}}) = (V_{\text{Stressed}}/V_{\text{normal}})^{\beta_1} \cdot \text{LT}(V_{\text{normal}}) \quad (2)$$

where V_{stressed} and V_{normal} are the stressed and normal voltage amplitude, respectively, LT(V_{stressed}) and LT(V_{normal}) are the lifetime of the component under voltage stress and under normal use conditions, respectively, and β_1 is a negative constant depending on the acceleration test results.

Gate oxide degradation could also be associated with the high temperature stress. A Weibull–Arrhenius model, shown in (3), has been used to model the SiC MOSFET failure rate in terms of the junction temperature [142]. Gate leakage current is monitored to indicate the ageing-extent

$$\lambda(t, T_j) = \left[\beta_2/\left(C_1 \cdot e^{E_a/(k_b \cdot T_j)}\right)\right] \cdot \left[t/\left(C_1 \cdot e^{E_a/(k_b \cdot T_j)}\right)\right]^{\beta_2 - 1} \quad (3)$$

where λ is the instantaneous failure rate, t is the time, E_a is activation energy, k_b is Boltzmann's constant, β_2 is the form factor, and C_1 is a constant related to the material.

With a simplified form, the aforementioned SiC MOSFET gate oxide time to failure could also be represented by [143]

$$\tau_{\text{BD}} = \tau_0 \cdot e^{-\gamma \cdot E_{\text{OX}}} \cdot e^{-E_a/(k_b \cdot T_j)} \quad (4)$$

where τ_{BD} is time to break down for SiC MOSFET gate oxide, τ_0 is the constant dependent on accelerated tests, γ is the electric field acceleration factor, and E_{OX} is gate oxide electric field.

Bond wire fracture is caused by the alternate expansion and contraction at the wire interfaced with DCB upper surface. Equation (5) shows the Schafft model to analyze the relationship between N_f and wire bending stress [140], [144]. Thus, the fracture related bond wire lifetime could be predicted

$$N_f = a_1 \cdot (\varepsilon_s)^{n_1} \quad (5)$$

where ε_s is the bond wire strain, and a_1 and n_1 are constants based on the bond wire material.

PoF lifetime models of bond wire liftoff and solder-fatigue are based on the fundamental form of the Coffin–Manson model [107], [145]–[147] in (6). The SiC MOSFET bond wire lifetime has also been estimated with this model [148], [149]

$$N_f = a_2 \cdot (\Delta T - \Delta T_0)^{-n_2} \quad (6)$$

where N_f is the number of cycles to failure, ΔT is the temperature range in the entire thermal cycle, ΔT_0 is the elastic

temperature range, which is normally regarded as insignificant, and a_2 and n_2 are defined by the database of PC tests.

However, it fails to consider the impact of the average junction temperature T_{j_mean} on cycles to failure. By Arrhenius approach [107], [144], [150], more accurate Coffin–Manson based lifetime model for bond wire liftoff and solder-fatigue is improved [29], [151], as shown in

$$N_f = a_3 \cdot (\Delta T_j)^{-n_3} \cdot e^{E_a/(k_b \cdot T_{j_\text{mean}})}. \quad (7)$$

A bond wire lifetime comparison between the Si IGBT and SiC MOSFET has been conducted using the previous model [152]. With $R_{\text{ds_on}}$ as the degradation indicator in thermal cycling tests, SiC MOSFETs are shown to achieve more cycles to failure than Si IGBTs, especially at low junction temperature swing.

By further considering other parameters such as power-ON time t_{on}, current flowing through the wire I_w, blocking voltage V_B, and wire diameter D_w, the bond wire lifetime model is improved in the Bayerer model in [146], [153]–[156]

$$N_f = a_4 \cdot (\Delta T_j)^{-\beta_2} \cdot e^{\beta_3/(T_j+273)} \cdot t_{\text{on}}^{\beta_4} \cdot I_w^{\beta_5} \cdot V_B^{\beta_4} \cdot D_w^{\beta_7}. \quad (8)$$

It has been verified to predict the lifetime of SiC MOSFETs under thermal cycling mission profiles [157].

The bond wire liftoff could also be modeled from the perspective of material science. Following equation shows a plastic strain based Coffin–Manson model, which can illustrate the physical failure process caused by the CTE mismatch between the bond wire copper and SiC [158], [159]

$$N_f = C_2 \cdot (\Delta \varepsilon_p)^{-C_3} \quad (9)$$

where ε_p is the plastic strain put on the bond wire. C_2 and C_3 are defined by the thermal test results.

Solder-fatigue is caused by the CTE mismatch. The PoF lifetime models can be based on stress, plastic strain, creep strain, stress–strain hysteresis energy, and crack propagation damage [160]. The Coffin–Manson model based on plastic strain [161] is shown in (10). Norris–Landzberg model [160], [162] leads to more precise lifetime estimation by further considering cycling frequency and maximum temperature

$$N_f = L_S / [a_5 \cdot (\Delta \varepsilon_p)^{n_4}] \quad (10)$$

where L_S is solder crack length, $\Delta\varepsilon_p$ is plastic strain change in thermal cycles, and a_5 and n_4 are decided by thermal cycling tests.

The following equation presents an SiC MOSFET solder layer lifetime model based on the exponential relationship between the lifetime and creep strain energy accumulated in one cycle [91]:

$$\Delta W_c = W_f \cdot (2N_f)^m \quad (11)$$

where ΔW_c is the creep energy accumulated in one cycle, W_f is the fatigue energy coefficient of solder material, and *m* is the fatigue energy index.

$R_{\text{ds_on}}$ has been measured to reflect the overall RUL of the SiC MOSFET-based on PC test results [163]. The corresponding lifetime model is shown in

$$\Delta R_{\text{ds_on}}(t) = \theta_1 \cdot e^{\theta_2 \cdot t} + \theta_3 \quad (12)$$

where θ_1, θ_2, and θ_3 are the model parameters dependent on the specific prognostic algorithms.

To estimate the model parameters in the PoF models, algorithms such as the PF [160], [164], [165], the KF [164], and the EKF [165] have been used. These algorithms are based on Bayesian inference to generate probability density function. Since the posterior distributions of PF algorithm parameters are expressed by particles and weights, it is more suitable for the prognostics of the nonlinear systems with non-Gaussian noise compared to KF and EKF methods [166]. The correlation between the parameters and the noise in the sensor data needs to be considered in the model-parameter identification process.

PoF models have a direct physical meaning. But it is difficult to obtain accurate models in real systems considering the different failure modes [36]. Besides, as the model becomes more complex, laborious experiments are needed to identify the model coefficients. Thus, PoF models are not universally applicable to different types of power converter systems.

2) Data-Driven Models: Data-driven models estimate the RUL based on available data without need of any physics mechanisms [36], [167]. The uncertainty margins are large by using this method. Thus, it is not suitable to predict long-term lifetime [168]. The data can be collected from either recorded failure data or real-time condition monitoring. Considering relatively scarce failure events, condition monitored data are the more realizable source. This real-time data can either directly reflect or indirectly indicate the system-health status. For the former case, the RUL estimation is regarded as the prediction of the condition monitored data to reach a predefined threshold level. For the latter case, failure event data are probably needed along with the condition monitored data for RUL estimation [36]. This article focuses only on the former case. Both a threshold and a model to represent the condition monitored data are required to determine the RUL. The decision of the threshold is normally based on the engineering experience and related standards.

Data-driven models are dependent on observed data in both healthy and faulty states [169], [170]. RUL is estimated normally in a form of probability density functions [171]. They include the models based on regression, Wiener process, Gamma process, MC, and artificial intelligence. The models based on Wiener, Gamma, and MC are related to stochastic processes capturing degradation dynamics. Thus, these three models are suitable to model the lifetime of the power inverters with multiple steady states.

1) Regression-based models are most commonly used. By using this method, the system-health condition is reflected by the monitored variables. Hence, the RUL is estimated by modeling these variables with a predefined threshold.
2) Modeling through Wiener process or Brownian motion with drift [36] is appropriate when the degradation develops bidirectionally over the time with Gaussian noises.
3) Gamma process [172] based models are applicable for the cases in which the degradation occurs gradually over time in a sequence of small positive increments. These models have relatively straightforward mathematical calculations. Besides, they take the temporal variability into consideration.

TABLE III
SUMMARY OF LINEAR AND NONLINEAR DATA-DRIVEN MODELS

Model group	Parameter estimation method	Monitored component / location	Failure indicator
Linear model	Bayesian Interference [178]	Power MOSFETs / Solder layers	R_{ds_on}
	Bayesian Interference [179]	Discrete IGBTs / Solder layers	V_{ce_on}
	Random sample and consensus [180]	Si Power MOSFETs and IGBTs / Gate oxide	V_{th}
	KF with least square fitting [117]	Power MOSFETs / Bond wires, solder layers	R_{ds_on}
Nonlinear model	EKF [166]	SiC MOSFETs / N/A	R_{ds_on}
	Exponential model [176], [177]	Si MOSFETs / N/A	R_{ds_on}, V_{th}
		Si IGBTs / N/A	V_{ce_on}

4) MC-based models assume that the future degradation state depends only on the current degradation state, and the system state can be reflected directly by observed data.
5) Artificial intelligence-based methods have mostly applied machine learning to estimate the RUL of power devices and converters, such as relevance vector machines [169], artificial neural networks [166], [173], deep learning algorithms [171], [174], genetic algorithms [175], [176], and supervised learning [177].
   a) A relevance vector machine has been utilized to train the power MOSFET ageing data to obtain representative vectors [169], which are fitted by a degradation model to predict the RUL.
   b) A time-delay neural network failure model has been combined with the probabilistic function by using the maximum likelihood method for IGBT model optimization [171].
   c) A recurrent neural network scheme has been applied in the system prognostics [166].
   d) A deep learning algorithm based on stacked long short-term memory has been used to conduct the training and inference for Si MOSFETs and corresponding power converters by detecting $R_{\mathrm{ds_on}}$ change [171], [174]. It derives a more accurate lifetime model compared to KF and PF methods.
   e) A genetic algorithm has been adopted to select the valuable principal components for GaN device behavioral modeling [176].
   f) Supervised learning has assisted in predicting the switching voltage and current waveforms so that a GaN RUL model is built to realize better device lifetime prediction [177].

From another perspective, the parameter estimation could be conducted through different mathematical means based on the data derived from thermal cycling tests. Therefore, the data-driven models could also be classified into the linear and nonlinear groups, as shown in Table III.

a) Linear data-driven models: The maximum likelihood estimation is the most basic linear data-driven modeling method [177]. The least square approximation has been used to predict the gate oxide lifetime as a function of V_{gs} stress based on the HTGB test data [166]. However, the estimation accuracy is discounted due to the outliers present in the beginning part of the data [177]. To address this issue, some ideas in other disciplines could be applied. Random sample consensus is a way to remove the data outliners and improve estimation accuracy [178]. But the nonlinearity in the initial part of the data still remains.

Bayesian interference is another way to improve accuracy by considering prior knowledge into estimation [160]. Furthermore, KF has been used to minimize the mean square errors by estimating the posterior state [27], [179].

b) Nonlinear data-driven models: Bayesian tracking algorithms such as EKF and exponential models are commonly adopted for the nonlinear data-driven techniques [178]. First, EKF nonlinear algorithm has been applied in SiC MOSFET junction temperature estimation. This is based on a state-space model describing the relationship between $R_{\mathrm{ds_on}}$ and T_j [166]. The experimental result shows the robustness to load change. Second, EKF could also be utilized together with other techniques such as PF to model the RUL. The battery RUL estimation has been conducted with relevance vector machine by combining these two approaches [167], [181]. EKF is shown to be robust but suffers from fast divergence [182]. The PF is presented to improve the estimation accuracy. But resampling of the particles is carried out in each iteration, which increases the computational burden [6]. Third, exponential models have been applied to relate the ON-state resistance and Si device lifetime [176], [177]. The exponential lifetime model could also be utilized in the V_{th}-related degradation [177]. Furthermore, the matrix–vector-based exponential lifetime model has been used to create a connection between the lifetime and ON-state device voltage [176].

c) Data-driven models in both linear and nonlinear systems: Some models can be applied in either linear or nonlinear circumstances. Monte Carlo simulation method [36] is especially useful when analytical approaches are not feasible. Since it performs stochastic iterations of the independent component variables [27] to conduct the simulation, a weighted average value is normally used to calculate the lifetime. So, it cannot generate an exact prediction [183]. Besides, machine learning is an alternative in either linear or nonlinear cases by applying the statistical techniques such as least square approximation [36] or Bayesian inference [37]. But the RUL probability density function is unavailable in this method [37].

3) Hybrid Models: The hybrid models could combine the physics of failure and data-driven models [184], [185].

TABLE IV
SUMMARY OF SiC MOSFET COMPONENT-LEVEL LIFETIME MODELS

Model Categories	Failure Modes	Model Descriptions	Features	
PoF models	Gate oxide breakdown	Stressed and normal voltage based	Suitable for long-term damage behavior prediction	
		Weibull-Arrhenius exponential model and its derivatives	Capable of modeling temperature stress	
	Bond wire fracture	Schafft Model	Capable of modeling wire bending stress	
	Bond wire lift-off	Coffin-Manson model	Fails to consider the impact of T_{j_mean}	
		Coffin-Manson model by Arrhenius approach	Shows SiC MOSFETs achieve more cycles to failure than Si IGBTs, especially at low ΔT_j	
		Bayerer model	Includes power-on time t_{on}, current I_w, blocking voltage V_B, and wire diameter D_w	
		Plastic strain based Coffin–Manson model	Capable of modeling CTE mismatch between the bond wire copper and SiC	
	Solder fatigue	Coffin-Manson model by Arrhenius approach	Capable of including the impact of T_{j_mean}	
		Plastic strain based Coffin–Manson model	Capable of modeling CTE mismatch between the DCB-die solder attach and SiC	
		Norris–Landzberg model	Considers TC frequency and maximum temperature	
		Creep strain energy	Shows exponential relationship between lifetime and creep strain energy in a cycle	
	Failure modes indicated by R_{ds_on}	Exponential function for R_{ds_on}	Covers more than one failure mode	
Data-driven models	Not specific failure modes	Regression-based models	Most commonly used data-driven method	
		Wiener process	Suitable for the bi-directionally developing degradation	Capable to reflect degradation dynamics
		Gamma process	Relatively straightforward calculations with temporal variability	
		MC	Memoryless	
		Artificial intelligence	Relevance vector machines	Representative vector extraction
			Artificial neural networks	Model optimization by combination with maximum likelihood method
			Deep learning algorithms	More accurate lifetime model compared to KF, PF methods
			Genetic algorithms	Valuable principal component selection
			Supervised learning	Voltage, current waveform prediction
Hybrid models	Not specific failure modes	Combination of two or more above models	Capable of leveraging the benefits of different types of models	
			More difficult to represent prognostics uncertainty compared with the other two	

They could leverage the benefits of different types of models. The PoF-based models reflect the real physical mechanisms with the model parameters estimated by the measured data. The challenge in this group of models is that it is more difficult to represent the prognostics uncertainty compared with the other two models [186].

Table IV presents a summary of all the aforementioned three component-level lifetime models.

C. Cycle Counting and Fatigue Damage Accumulation

To efficiently count the random thermal cycles, many counting algorithms have been proposed, such as level-crossing counting, peak counting, simple-range counting, and rainflow counting [187]. Among them, the rainflow counting algorithm is the most well-known [10], [188]. It has been applied to reduce the stress spectrum into simple values for the cyclic accumulated bond wire damage when the amplitude and frequency of the thermal cycles are not repetitive [92]. The extreme points are counted to extract the amplitude [189], [190], mean value [191], and cycling period [192]. Traditional rainflow methods output half-cycles that are difficult to be integrated into reliability algorithms. Counting small cycles within larger ones helps this integration [10]. Besides, to overcome inefficient data storage, real-time minimum or maximum temperature could be counted by stack-based recursive programming [193].

Once the component-level RUL estimation model is created, the fatigue damage accumulation is conducted by either linear or nonlinear approaches. Thus, the stress accumulation with the mission profile characteristics could be reflected.

The linear damage accumulation method based on the Palmgren–Miner's law [194] is mostly accepted in damage evaluations. However, it is independent of the loading levels [195], which reduces the lifetime prediction accuracy. Besides, it assumes a constant damage accumulation rate during the lifetime. However, more damage would lead to increased stresses, and thus causes additional physical mechanisms. This would result in a different damage accumulation rate. For example, as the crack propagates, $R_{\mathrm{th_jc}}$ increases due to more power loss, which accelerates the damage accumulation rate in the bond wires and solder layers. Therefore, lifetime predicted by linear methods is impractically longer.

The nonlinear damage accumulation approach reflects the accumulation rate change in different stress levels. For instance, the method based on the double linear damage law [196] allows each phase of the loading to be analyzed by the Palmgren–Miner linear damage rule. But it ignores the mutual interaction among different stresses. Manson–Halford model [197] considers both stress sequences and interaction by modifying the exponent parameter in double linear damage model. Besides, nonlinear approaches consider the damage accumulation rate change by putting proper weights onto the affected physical parameters. To determine these weights, detailed experimental data are needed, which makes these methods not generally applied.

IV. System-Level Offline Lifetime Modeling

The lifetime models based on the ALT approaches are static because no dynamic real-time RUL estimation is conducted to update initial models. Statistically, most system-level lifetime have been modeled by the Weibull probability distribution functions. It has been adopted in the system-level lifetime prediction for a fuel cell dc–dc power stage [6], an LED source and capacitor system [198], and an onboard dc–dc converter for more electric aircraft [199]. For the systems with an irregular cumulative distribution function (cdf), the maximum entropy probability distribution has been presented to be more suitable compared with the Weibull distribution [200].

In this section, five static system-level lifetime modeling methods will be reviewed, including the combinatorial reliability techniques, such as RBD, FTA, GO-FLOW, and BNs, as well as the state-based modeling techniques, such as MC. In this section, the state-of-the-art system-level lifetime prediction techniques are first summarized. Then, a discussion regarding their applicability in SiC power converters is presented.

A. State-of-the-Art System-Level Lifetime Prediction Techniques

1) Reliability Block Diagram (RBD): RBD system lifetime modeling technique can be applied in the distributions with either constant or inconstant failure rates [7], [9], [197], [201]. It allows us to evaluate concepts in the early design period. This is useful to implement the design for reliability. It is a success-oriented system analysis method [202]. Both in-series and in-parallel systems could adopt it. One issue with RBD is that some big systems have to be modeled with complex series or parallel combinations [203]. Table V compares the typical reliability indexes including system reliability, failure rate, and mean time to failure (MTTF) for in-series and in-parallel systems. Here, a constant failure rate is assumed. In the table, λ_i is the failure rate of individual components. $\lambda_{\max}$ is the maximum failure rate among all the in-series components. RBD cannot model the time-dependent failures, the sequences among failures, or system dynamics. Dynamic RBD (DRBD) has been proposed to resolve these issues. But more complexity is introduced.

TABLE V
Comparison Among Typical Reliability Indexes Between In-Parallel and In-Series System Structures

Reliability Index	In-parallel System	In-series System
System reliability ***R(t)*** [10], [198], [204]	$e^{-\sum_{i=1}^{n}\lambda_i t}$	$1-\left(1-e^{-\lambda_{\max} t}\right)^n$
System failure rate ***Λ*** [9], [197], [204], [205]	$\sum_{i=1}^{n}\lambda_i$	$\lambda_{\max}$
System ***MTTF*** ($\int_0^\infty R(t)dt$) [7], [206]	$1\Big/\sum_{i=1}^{n}\lambda_i$	$\frac{1}{\lambda_{\max}}\sum_{i=1}^{n}\frac{1}{i}$

1) A paralleled inverter lifetime has been modeled by the RBD approach, considering the constant failure rate [10]. A dynamic power distribution control has been adopted to optimize both the reliability and the cost on the system level.
2) A multilevel converter lifetime has also been estimated with RBD, considering the constant failure rate [207].
3) This method could also be applied in the systems with inconstant failure rates. A fuel cell dc–dc converter lifetime has been modeled by RBD with time-dependent failure rate [204].

2) Fault Tree Analysis (FTA): Developed by Bell Telephone Laboratories in 1962, FTA is a deductive, top-down method conducted in failure space to analyze the effect of initial faults on a complex system [197], [206], [208]. FTA only focuses on the failure combination. First, this approach has been applied to analyze the lifetime models following the distribution with constant failure rate such as in the fuel cell lifetime modeling application [206]. Second, FTA has also been used in the circumstances with the inconstant failure rate. In [208], an electric vehicle drive system lifetime has been modeled with the time-dependent failure rate.

However, there are some issues with the FTA approach. First, both the dependences among different degradations and the fault sequences [206], [209] have not been modeled in this method. Second, it could be used to evaluate complex systems by analyzing the probabilities of combined failures [203]. But it must model the relationship among all individual failures [202]. Thus, the failure mechanisms of each component are required. So, with this method, the computational burden is heavy for

complex systems [210]. To solve the abovementioned problems, the extended FTA techniques for dynamic and complex systems are necessary. Below are summarized three typical extended FTA methods.

1) Dynamic FTA (DFTA) defines specific gates to represent failure dependence, redundancy, and sequence relationships [211]. To solve the fault trees, it is conventionally translated into MCs. But Markov model becomes complicated for large systems. A hybrid BN inference algorithm has been used instead to solve the fault trees [212]. Neither numerical integration nor conditional probability table is needed. So, this approach is suitable for the complex systems.
2) Pandora temporal fault trees introduce temporal gates to describe event sequences and allow qualitative analysis of temporal fault trees [213]. This method applies BNs to solve fault trees to analyze dynamic dependability.
3) Repairable fault trees further extend system lifetime by applying different repair strategies into the model [214].

3) GO-FLOW: This system analysis technique is success-oriented [215]. It is an alternative to FTA method and is effective to estimate the lifetime of complex time-dependent systems with multiple states [216]. But it is hard to model the dynamic behavior characteristics. To overcome this, an extended GO integrated with DBN has been used to model the system dynamics [216].

4) Bayesian network (BN): The BN technique could be regarded as a general version of FTA. Dependence among failures could be represented with this method [217]. It is relatively suitable for the complex system lifetime modeling because it performs the factorization of joint probability distribution for conditionally dependent variables [218]. It could be used to represent interdependency among components and include uncertainty in modeling [219]. The derivatives of BN are summarized below.

1) Dynamic BN (DBN) models the temporal sequence of the variables. It is a generalization of the hidden Markov models and KFs [220], [221].
2) By integrating the genetic algorithm into DBN, the system reliability has been regarded as a parameter in design stages to promote the design for reliability [222].
3) Both the standard and DBN methods repeat the random variable probability distribution calculation at every time interval and increase the model complexity. To address this issue, a discrete-time BN (DTBN) method assumes that each event happens at most once [223]. This is especially applicable for the nonrepairable systems.
4) The continuous-time BN (CTBN) generalizes the DTBN framework [224]. The main advantage of a CTBN over a DTBN is that it provides a closed-form solution for the system lifetime. Besides, CTBN also saves memory because the probabilities are described in terms of parametric functions rather than multidimensional tables in DTBN.

5) Markov chain (MC): The MC approach is a random process with the next state depending only on the present state [206]. It is time independent and focuses on either successful or failed combination. It saves the computational effort in the lifetime calculation of systems with fault sequence [202]. MC and its derivatives are suitable to solve dynamic systems with component interactions [225]. However, the Markov model expands its state space exponentially with the number of components. Thus, it is difficult to apply MC into large, complex systems. Besides, MC is not suitable in systems with time-dependent failure rates [202], [209]. Some applications of the MC methods into the power converter area are listed as follows.

1) An interleaved dc–dc boost converter lifetime has been modeled by applying this MC method, considering the constant component failure rates [8].
2) An induction motor drive lifetime modeling has also been conducted with the MC analysis [226].
3) A proton-exchange membrane fuel cell power plant lifetime has been estimated by the MC technique as well, with the continuous state transitions [33].

B. Discussion of the Applicability in SiC Power Converters

Table VI summarizes the aforementioned system-level lifetime models and their derivatives. First, overall speaking, based on the six evaluated indexes, DRBD and DBN could achieve a relatively wide application range. Second, the component failures such as gate oxide breakdown, body diode degradation, bond wire fracture, and liftoff as well as solder-fatigue are all time-dependent. Since the classical RBD, FTA, and MC cannot model the time-dependent failures, they are not applicable in the SiC power converter lifetime prediction. Third, if one failure mechanism occurs after the other one, RBD, FTA are not suitable for this sequence order modeling in the SiC converter lifetime prediction. Fourth, for the components with inconstant failure rate, MC is not a promising option to predict the SiC converter system lifetime. Fifth, regarding the dynamic behavior modeling, such as component interdependence in SiC MOSFET failure mechanisms, redundancy modeling in the multilevel converters, and load sharing modeling in the paralleled devices, RBD, FTA, and GO-FLOW are not applicable. Although DFTA has improved the dynamic capability, it is still hard compared with the DRBD, extended GO-FLOW, and BN techniques. This is decided by the adopted inference algorithm. Sixth, for the complex systems consisting of various components such as the three-port SiC converter consisting of an interleaved boost converter, an interleaved bidirectional flyback converter, and a three-phase voltage source inverter [227], it takes considerable computational resources to utilize the RBD, FTA, and MC techniques in the converter lifetime prediction.

The system lifetime modeling has been conducted in the Si IGBT based inverters following exponential distribution with constant failure rate [9], [10]. SiC MOSFET-based power converter lifetime models following the Weibull distribution with inconstant failure rate could be investigated. Furthermore, system RUL estimation could be based on multiple indicators using techniques such as principal component analysis [43].

V. SiC Converter Lifetime Modeling Software

Both the academia and industry have developed component-level and system-level simulation tools to analyze and predict

TABLE VI
SUMMARY OF SYSTEM-LEVEL LIFETIME MODELS

Modeling methods	Time dependent failure modeling	Event sequence modeling	Applicable to the fixed / variable failure rate	Dynamic behavior modeling			Complex system lifetime modeling	Success- / failure-oriented
				Component interdependency modeling	Customizable redundancy modeling	Load sharing modeling		
RBD	No	No	Either	No			Difficult	Success
DRBD	Yes	Yes	Either	Yes			Yes	Success
FTA	No	No	Either	No			Difficult	Failure
DFTA	Yes	Yes	Either	Hard / Impossible			Yes	Failure
GO-FLOW	Yes	Yes	N/A	No			Yes	Success
Extended GO-FLOW	Yes	Yes	N/A	Yes			Yes	Success
BN	No	Yes	Either	Yes			Suitable	N/A
DBN	Yes	Yes	Either	Yes			Suitable	N/A
MC	No	Yes	Fixed	N/A			Difficult	Either

the lifetime of the SiC converters. These software use different random number generation methods and lifetime modeling strategies to derive the component or system lifetime in the form of statistical probability distributions.

A. Component-Level Lifetime Modeling Software

1) Finite-element analysis software by the ANSYS. It has been used to simulate solder layer lifetime with energy-based and creep-strain-based methods [228].
2) Finite-element analysis software by the COMSOL Multiphysics. The lifetime of the die-attach solder layer has been modeled with thermomechanical physical analysis [91].

B. System-Level Lifetime Modeling Software

Both the academic and commercial system-level lifetime modeling softwares have been developed by using different modeling categories mentioned in Section IV.

1) Academic:

1) Galileo tool [229] by the University of Virginia: It is specifically designed to model and analyze the dynamic fault trees. It can be edited in a web-based graphical environment.
2) Symbolic hierarchical automated, reliability, and performance evaluator [230] by Duke University: It could model the system-level lifetime by integrating the information from each component time-dependent degradation and the system structure. It supports RBD, FTA, and MC modeling methods. It generates lifetime results statistically in the form of a probability distribution function.
3) DFTCalc [231] by the University of Twente: It translates each top-level failure event into an input–output interactive MC. The failure probability of a dynamic fault tree is calculated by composing these chains one by one. It could be used to output the system MTTF.

2) Commercial:

1) Isograph [232] provides two tools to model the SiC converter system-level lifetime in a graphical format, including the Reliability Workbench tool and the Availability Workbench tool. Both of them offer RBD and FTA modeling approaches. The former tool is useful when there is need to refer to the standards such as MIL-STD 1629 and IEC 61508.
2) RAM Commander [233] could utilize the RBD, FTA, and MC techniques to model the system-level lifetime.
3) ReliaSoft [234] offers four tools to model the system lifetime.
   a) BlockSim tool provides RBD and FTA to model the system-level lifetime for both repairable and nonrepairable systems in a graphical interface.
   b) Weibull++ tool is used to analyze lifetime data using Weibull distribution.
   c) ALTA tool could analyze the quantitative lifetime data from accelerated tests.
   d) Lambda Predict tool could estimate the system lifetime based on the standards such as MIL-HDBK-217F.
4) Windchill RBD (formerly Relex OpSim) [235] supports series, parallel, and hybrid RBD configurations. It can be used to calculate the expected number of failures, the failure rate, MTTF for nonrepairable systems, and mean time between failures (MTBF) for repairable systems.
5) Fault Tree Analyzer [236] is an open-source tool. It could do static FTA in a web-based graphical environment.
6) ITEM ToolKit [237] could be utilized to analyze the RBD, FTA, and MC modeling techniques in lifetime prediction.
7) AGENARISK [238] could be used to predict the SiC power converter lifetime with the up-to-date techniques from Bayesian artificial intelligence and probabilistic reasoning. It integrates the real-time degradation data with the knowledge about component causal relationship and interdependence.

VI. SiC Power Converter Condition Monitoring

To update the static system lifetime model based on the results of ALTs, the summary of the component-level lifetime models, and the extrapolation of statistical lifetime modeling in Section III, the identified degradation indicators are further measured in real time. Condition monitoring is a passive method

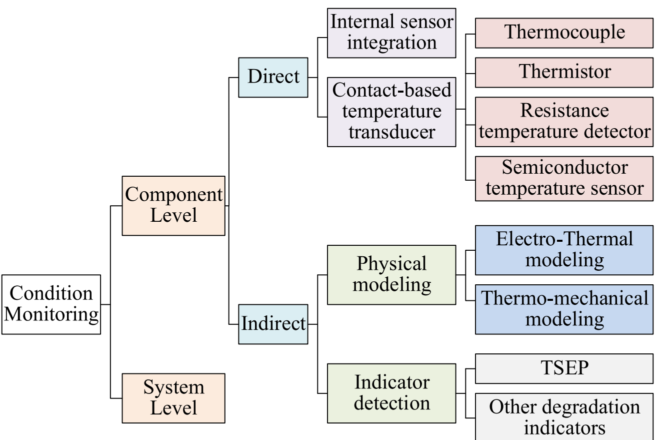


Fig. 7. Condition monitoring method classification.

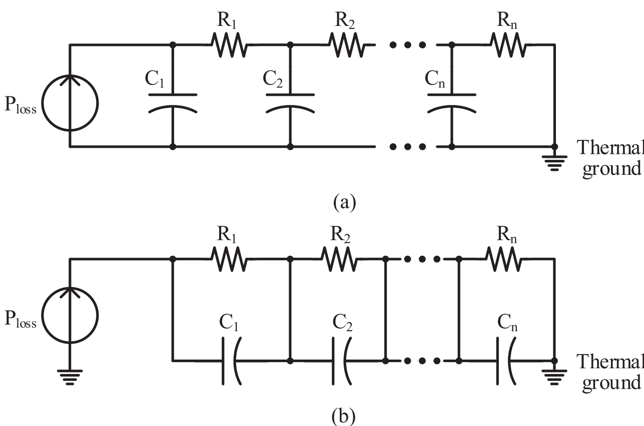


Fig. 8. Two types of *RC* thermal networks. (a) Cauer thermal network. (b) Foster thermal network.

to online indicate the degradation of power devices [107], [239], [240], capacitors [32], [241], and overall systems [107]. Fig. 7 classifies condition monitoring into component and system levels. Component-level condition monitoring includes direct and indirect methods. Since thermally induced failure takes a significant percentage of 55% among all sources of failures [242], most of power electronic condition monitoring has been focused on temperature-related failure.

1) *Direct condition monitoring*: Direct condition monitoring is realized by using internal sensors and contact-based temperature transducers. Device packaging and internal design are essential in the internal sensor integration method. Based on the thermistor principle, a temperature sensor is integrated into the SiC power MOSFETs to measure T_j [243]. More common direct condition monitoring is conducted by applying contact-based temperature transducers such as thermocouples, thermistors, resistance temperature detectors, and semiconductor temperature sensors [244]. However, high-bandwidth temperature sensors are not cost-effective. Another extensively employed contact-based temperature sensors have focused on the negative thermal coefficient (NTC) thermistor. The thermal impedance between the SiC die and the integrated NTC thermistor has been modeled in a Foster thermal network to estimate T_j [245].
2) *Indirect condition monitoring*: Indirect condition monitoring is carried out by either physical modeling or detecting parameters indicating internal degradation. Physical modeling can be further classified into electrothermal modeling and thermomechanical modeling. The indicator detection includes the monitoring of the TSEPs and other degradation indicators reflecting the degradation of the gate oxide, the body diode, bond wires, and solder layers.
3) *System condition monitoring*: System-level condition monitoring has not been explored enough compared with component-level counterpart. It is commonly performed by comparing the responses in real time and under normal operations [107]. The difference between the two responses is used to evaluate system-health condition.

A. Electrothermal Modeling of SiC Power Devices

Electrothermal modeling is normally concerned with the SiC device model, power loss model, and thermal model. Temperature swing [246] and average junction temperature [151] are targeted by electrothermal simulation including power loss calculation. Compared with other temperature estimation methods, electrothermal modeling is more cost-effective. However, it is difficult to model the electrothermal system accurately. One challenge is to consider uneven temperature distribution among the chips, layers, and different points on the chip inside the power module due to thermal coupling. Another challenge is to model mission profiles and thermal dynamics, which are closely related to device lifetime.

Two electrothermal modeling methods have been studied, i.e., 1-D and 3-D thermal networks. Both approaches can be realized by either Cauer or Foster thermal networks [247], as shown in Fig. 8. Cauer grounded-capacitor ladder thermal network is based on heat physics. It is more accurate but computation extensive. Foster nongrounded-capacitor ladder thermal network is not physically based and, thus, mathematically more convenient [248].

1-D lumped *RC* thermal networks are based on manufacturer datasheets [249], [250]. They are convenient to be realized in circuit simulation [249], and thus, fast. They are suitable for a rough estimation of junction temperature. But they basically estimate the average junction temperature of the chip area and intrinsically disregard thermal coupling among chips or different layers beneath chips [251]. Most of the 1-D *RC* thermal modeling is conducted in the time domain and fails to consider the boundary conditions including nonlinear heating and cooling systems [252]. To fix this issue, an electrothermal cosimulation is conducted based on 1-D time-domain *RC* thermal network by including boundary conditions [253]. Also, a frequency-domain 1-D thermal network [254] considers the impact of boundary conditions of nonlinear cooling system on thermal impedance. A low-pass filter has been adopted to model the loss behavior of thermal grease and heat sink so that the junction temperature can be estimated more accurately.

TABLE VII
SUMMARY OF SiC MOSFET ELECTROTHERMAL AND THERMOMECHANICAL MODELING METHODS

Model Categories	Descriptions	Features
Electro-thermal modeling	1-D thermal networks	Convenient to be realized in circuit simulations quickly
		Suitable for a rough estimation of T_j
		Disregards thermal coupling among chips or various layers beneath chips
	3-D thermal networks	More accurate by thermal coupling consideration
		Time-consuming calculation
		Not efficient to analyze long-term mission profiles
Thermo-mechanical modeling	Stress and strain response to thermal loading	N/A

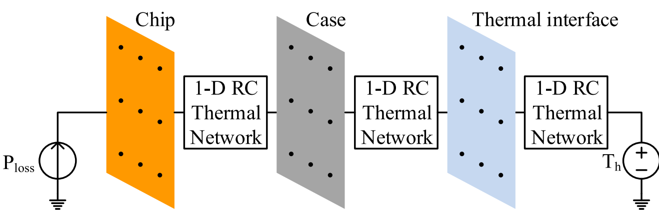


Fig. 9. Typical 3-D thermal network.

Another electrothermal modeling method is based on 3-D lumped *RC* thermal network, as shown in Fig. 9. It is more accurate than 1-D network due to the consideration of thermal coupling and dynamics. Differential thermal analytical equations using finite-difference method [251] and finite-element method [255] have been used to derive both the steady-state and transient temperature profiles (junction temperature swing ΔT_j and maximum junction temperature $T_{j_\max}$). But they are limited with time-consuming calculation [256]. Thus, owing to both the high cost and possible divergence, they are not efficient to analyze long-term mission profiles. To improve the execution speed, the thermal boundary conditions can be transformed from the finite-element method to circuit simulation [257].

B. Thermomechanical Modeling of SiC Power Devices

Thermomechanical modeling is derived from the thermomechanical stress at the bond wires and solder layers. It can be used to diagnose the health condition of these package-level locations. The IGBT module bond wire 3-D thermomechanical degradation modeling has been studied in [258]. The thermomechanical creep behavior of solder layers has been analyzed in [259]. Since the package-level failure mechanisms between SiC MOSFETs and Si IGBTs are similar based on the review in Section II, these thermomechanical modeling methods have also been applied to the SiC MOSFETs [162]. For example, in the SiC power modules, the stress and strain response to thermal loading has been modeled and simulated [158]. The difference between Si and SiC devices regarding this thermomechanical modeling is a potential domain to be further investigated.

A summary of SiC MOSFET electrothermal and thermomechanical modeling techniques has been shown in Table VII.

TABLE VIII
SUMMARY OF TSEPs OF SiC MOSFETs

TSEPs of SiC MOSFETS	Positive/negative temperature relevance
Turn-on current rate dI_d/dt [132], [267]	Positive
Turn-off current rate dI_d/dt [267]	Negative
Turn-on gate current plateau [132]	Positive
Turn-on voltage rate dV_{ds}/dt [271]	Negative
The discharge time of Miller capacitance during turn-off [132], [272]	Positive
Turn-off delay time [269]	Positive
Integral of gate drive turn-on output current over turn-on time [270]	Positive
Gate drive turn-on peak output current [270]	Positive
On-state resistance R_{ds_on} [266]	Positive
Shoot-through current magnitude [133]	Positive

C. TSEP Comparison

Case temperature and junction temperature have been measured for component-level thermal condition monitoring. The relationship has been investigated between the case temperature and the degradation of substrate–baseplate solder as well as bond wire [260]. TSEPs have been widely reviewed for the T_j monitoring of power devices [261]–[264]. ON-state resistance [265], [266], turn-ON current I_d rate [132], [267], turn-ON gate current plateau [132], turn-ON voltage $V_{\rm ds}$ rate [268], turn-OFF discharge time of Miller capacitance [132], turn-OFF delay time [269], integral of the turn-ON gate current over turn-ON time [270], turn-ON peak output current [270], shoot-through current magnitude [133], and drain current for a low gate voltage [136] have been used as the TSEPs of SiC MOSFETs. Table VIII presents a brief summary of these parameters.

1) Current rate dI_d/dt and turn-ON gate current plateau $I_{\rm gp}$: Current rate dI_d/dt has been identified as the SiC MOSFET TSEP [132], [267] because it increases with temperature during turn-ON and decreases with temperature during turn-OFF [273].

   Negative temperature coefficient of the $V_{\rm th}$ is the reason behind the positive temperature coefficient of both dI_d/dt and $I_{\rm gp}$ during SiC MOSFET turn-ON. Both of the

two TSEPs can be integrated with gate drive. There is also a tradeoff between switching loss and temperature-sensitivity for both dI_d/dt and $I_{\rm gp}$ during turn-ON. They are not suitable for fast switching due to the obvious interference of the parasitic inductance. Their temperature dependence is sensitive to die-size and gate resistance. Decoupling is needed since turn-ON $I_{\rm gp}$ would also be affected by the nonthermal parameters such as load current.

2) Turn-ON voltage rate $dV_{\rm ds}/dt$: The turn-ON voltage rate $dV_{\rm ds}/dt$ has a negative temperature dependence for SiC MOSFETs [271]. This is mainly caused by the negative temperature coefficient of the threshold voltage, which is caused by the positive temperature relevance of the intrinsic carrier concentration.
3) Miller capacitance $C_{\rm gd}$ discharge time: The discharge time of Miller capacitance during turn-OFF is another TSEP for SiC MOSFETs [132]. It is less temperature-sensitive for SiC MOSFETs compared with Si IGBTs.
4) Turn-OFF delay time: This TSEP is integrable with gate drive with adjustable gate resistance [269]. But its temperature dependence is sensitive to the dc-link voltage, load current, and gate resistance.
5) The integral of the gate drive turn-ON output current: The gate drive turn-ON output current could be detected in a relatively simple gate drive setup [270]. But its temperature dependence is sensitive to both the dc-link voltage and the load.
6) Gate drive turn-ON peak output current: To detect the gate drive turn-ON peak output current, the gate drive setup is relatively complex [270].
7) Drain–source ON-state resistance $R_{\rm ds_on}$: $R_{\rm ds_on}$ has been shown as the SiC MOSFET TSEP [266]. However, the SiC MOSFET $R_{\rm ds_on}$ is less temperature-dependent compared with that of Si MOSFETs [131]. Besides, SiC MOSFET $R_{\rm ds_on}$ is highly dependent on $V_{\rm gs}$ [274].
8) Shoot-through current magnitude: The amplitude of the shoot-through current caused by the crosstalk is less temperature-sensitive for SiC MOSFETs than Si IGBTs. This is mainly attributed to the relatively smaller Miller capacitance in SiC MOSFETs. This TSEP is based on the crosstalk and thus is intrusive to the normal operation [133].

Following are some discussions about the aforementioned TSEPs.

1) Some of the aforementioned TSEPs are not suitable for SiC MOSFETs. As discussed in Section III-A, $R_{\rm ds_on}$ is less temperature-dependent in SiC MOSFETs compared with Si devices. So, $R_{\rm ds_on}$ is not a promising TSEP here. In addition, the turn-OFF discharge time of the Miller capacitor is not so manifest compared with Si devices due to smaller die-size.
2) Due to higher interface state traps and fixed oxide traps in SiC MOSFETs, the bias temperature instability results in more significant $V_{\rm th}$ drift [275]. This would reduce the T_j estimation accuracy, based on $R_{\rm ds_on}$, body diode forward voltage V_F, turn-ON switching rates dI_d/dt and $dV_{\rm ds}/dt$ [276].
3) Both the statistic and dynamic SiC MOSFET TSEPs have been verified to be affected by the ageing effect in dc PC tests [277]. Thus, to make the T_j estimation more precise, an improved measurement should be developed.
4) In some cases, more than one TSEP could be combined with each other to make the estimation more precise. For instance, both the square root of the device saturation current and the threshold voltage have been integrated into the junction temperature estimation [278].

D. Other Degradation Indicators

Other than the temperature related indicators, there is another group of nonthermal parameters that are dedicated to reflecting the ageing effect corresponding to different failure mechanisms of SiC MOSFETs. Following are the summarized health indicators that have been identified for specific failure modes. They could quantify the degradation extent, and further be used to derive corresponding offline lifetime models through ALTs.

1) ON-state drain–source voltage $V_{\rm ds_on}$ and body diode forward voltage V_F have been used as the indicators of bond wire liftoff failure through PC tests [99].
2) Junction-case thermal impedance $R_{\rm th_jc}$ has been utilized as the indicator of solder-fatigue through TC tests or TS tests [99].
3) Threshold voltage $V_{\rm th}$ [44], [69], [70], [114], [115], [279]–[281], gate leakage current $I_{\rm gss}$ [99], [282], [283], drain leakage current $I_{\rm dss}$ [114], [116], and Miller plateau voltage $V_{\rm gs_mp}$ [41], [61], [62] have been adopted as the indicators of gate oxide failure through HTGB tests.
4) Gate leakage current $I_{\rm gss}$ [284] and forward voltage V_F [57], [58], [82] have been applied as the indicators of body diode failure through HTRB tests.
5) The turn-ON time has been analyzed as an ageing indicator for SiC MOSFETs in [285]. But no specific package or chip failure has been clarified regarding this indicator.
6) The gate–source impedance has been verified as an ageing indicator in [286]. A spread-spectrum time-domain reflectometry hardware has been added to sense this impedance change. So, the degradation could be indirectly detected. But this work does not specify which failure mode it is related to.

Besides, for the dc-link capacitors, the ESR and capacitance [32] have been applied as the indicators of capacitor degradation through floating or cycling aging tests [287], [288].

E. Review of Challenging Online Measurement Techniques

For SiC MOSFETs, the measurement of some parameters is sensitive and requires special implementation techniques. Therefore, a detailed review of these measurement methods is essential for the practical testing regarding the health indicators.

The indicator measurement of SiC MOSFETs generally features the following challenges. The signal amplitude is small, which is hard to detect. The parameter resolution is required to be high enough to fit the fast switching speed. Also, they are susceptible to high-frequency noise. Besides, the inference

from other parameters could generate false alarms. In the result analysis, the propagation delay of extra circuits needs to be considered. Furthermore, the interdependence among different physical mechanisms needs to be decoupled to analyze individual physical mechanism. Finally, the implementation complexity should be evaluated to select a proper indicator.

To address these challenges, seven approaches have been generally employed. They will be summarized ahead in detail.

1) Signal Amplifying: To make the small signal more detectable, most techniques have used the operational amplifiers. In the drain leakage current measurement, $I_{\rm dss}$ is microampere-level at nominal blocking voltage [67]. Due to aging, $I_{\rm dss}$ could reach to milliampere-level [289]. To make $I_{\rm dss}$ more detectable, it could be measured at a higher $V_{\rm ds}$ than the nominal blocking voltage [67]. In the gate leakage current measurement, $I_{\rm gss}$ is negligible in normal condition. But the milliampere-level gate current could occur in aged devices [289]. A difference amplifier with an enough bandwidth at designed switching frequency range has been utilized to measure $I_{\rm gss}$ by detecting turn-ON gate resistance voltage drop. This voltage is then compared to a predetermined threshold voltage to monitor the degradation.

2) High-Resolution Consideration: The detection resolution and accuracy need to be high enough due to SiC MOSFET typically high switching frequency. A microcontroller unit high-resolution capture peripheral with resolution of few hundred picoseconds has been used to measure the nanosecond-level turn-ON delay time [285]. In a turn-OFF delay time measurement, the propagation delay mismatch and jitter of the signal isolator and gate drive IC would adversely affect the measured turn-OFF delay resolution [290]. This undesirable effect has been alleviated by increasing the gate resistance. In a drain leakage current measurement, the high-resolution requirement cannot be affected by the nominal switching drain–source current [289]. In the gate leakage current measurement, the measurement accuracy of voltage on the gate resistance has been included into the design [289].

3) Immunity to High-Frequency Noise: The impact of high-frequency $dV_{\rm ds}/dt$ overshoot and ringing noise on the measurement accuracy needs to be minimized [291]. Take the peak gate current measurement as an example. The transient noise could be induced by the high-frequency electromagnetic interference, and the switching transient from the gate drive power supply or the current peak detector [270]. To resolve these unexpected issues, additional circuits such as a filter and an amplifier with high common-mode rejection ratio have been utilized. In the measurement of peak gate current, an output filter has been applied to reduce the high-frequency noises at the outputs of the peak current detector and integrator. In the turn-ON delay time measurement, to alleviate noise interference, an *RC* filter has also been designed. The input impedance has been increased with additional paralleled capacitors, high-bandwidth buffer circuits [285]. In the turn-OFF delay time measurement, a series–parallel *RC* circuit has been included to filter high frequency noise as well [292]. In the gate leakage current measurement, the amplifier with high common-mode rejection ratio at high switching frequency has been applied to counteract the undesirable noise effect [289].

4) False Alarm Avoidance Due to Other Parameters: Since the detected health indicators interact with other parameters with similar electrical properties in the circuit, it is essential to prevent them from being contaminated by these signals. Hence, a false alarm should be avoided. In the measurement circuit of $I_{\rm gss}$, the amplifier input bias current rating and input offset voltage rating should be small enough in case that it would contaminate the real $I_{\rm gss}$. It has been suggested that input bias current should be at least one order of magnitude smaller than gate leakage current, and the input offset voltage should be at least one order of magnitude smaller than the minimum ageing threshold voltage [289]. Also, $I_{\rm gss}$ could be mixed with gate charging current during switching transients, or the current flowing through extra gate–source resistor, protection-purpose Zener diode. To address this issue, a Zener diode with a small leakage current at gate voltages could be used. In the peak gate current measurement, the switching transient properties of SiC MOSFETs are sensitive to the gate bias voltage [270], which would also induce false alarm.

5) Propagation Delay Consideration: Almost every reviewed health indicator circuit involves adding extra analog circuits. As a result, the corresponding propagation delay would impact the detected signal itself. Thus, including this delay time into the final indicator judgment should be noticed. In the turn-ON delay time measurement, a propagation delay time of the voltage comparison circuits has been considered in the testing result analysis [285].

6) Decoupling Among Different Physical Mechanisms: Some indicators are dependent on more than one physical mechanism. To individually analyze the impact of a certain effect on a specific parameter, a decoupling strategy is normally required. It could be done by either identifying new indicators or developing new measurement methods.

Both the junction temperature rise and the die ageing could cause the commonly applied TSEPs such as $R_{\rm ds_on}$ to change. Therefore, the real T_j of the chip cannot be reflected. The body diode's voltage drop at low current and negative $V_{\rm gs}$ has been utilized as a novel TSEP to decouple the ageing effect and the practical junction temperature rise [134]. On the other hand, if SiC MOSFET degradation needs to be monitored separately, the T_j effect should be excluded. $R_{\rm ds_on}$ in saturation region has been measured to reflect the device ageing, and a low $V_{\rm gs}$ at startup is applied to decouple the heating effect [293].

The decoupling could also be realized through the improvement of measurement methods. To decouple the self-heating effect at high-current high-voltage region from the real turn-OFF delay time measurement, this health indicator has been derived by online measuring the intrinsic ON-state SiC MOSFET capacitance characteristics extracted from their *S*-parameters [294]. Another example is the decoupling of the package and chip degradation. As mentioned in Section II, both of these two mechanisms could impact $V_{\rm ds_on}$. Through utilizing a Kelvin source and drain to measure the chip voltage drop and detecting the bond wire voltage separately, these two failure modes have been monitored individually [281].

7) Measurement Complexity Evaluation: For some health indicators, the measurement involves more than one parameter.

TABLE IX
SUMMARY OF ACTIVE THERMAL CONTROL STRATEGIES

Groups	Control methods	Devices	Realization details: If	Realization details: Then
Topology	Adaptive gate drive	GaN HEMT [297]	$T_C\uparrow$	V_{gs} first-step duration $\uparrow \rightarrow P_{loss}\uparrow \rightarrow T_j\uparrow \rightarrow \Delta T_j\downarrow$
		Si IGBT [298]	Load current $\downarrow$	$R_g\uparrow \rightarrow P_{sw}\uparrow \rightarrow T_j\uparrow \rightarrow \Delta T_j\downarrow$
		Si MOSFET [296]	$R_{ds_on}\uparrow$	V_{gs} amplitude $\downarrow \rightarrow T_j\downarrow$
Control	Switching frequency control	Si IGBT [246], [299], [300]	Load current $\uparrow$	$f_{sw}\uparrow \rightarrow P_{sw}\uparrow \rightarrow \Delta T_j\downarrow$
	Active cooling control	Si IGBT [301]	$T_j\uparrow$	Open-loop feed-forward control of P_{loss} and ΔT_a
			$\Delta T_j\uparrow$	Close-loop feed-back control of temperature
	PWM control modification	Si IGBT [302]	$P_o\uparrow$	DPWM clamping angle $\uparrow \rightarrow P_{loss}\downarrow \rightarrow T_j\downarrow$
		Si IGBT [11]	$T_j\uparrow$	$V_{dc_link}\downarrow$ / DPWM $\rightarrow P_{sw}\downarrow \rightarrow T_j\downarrow$
		Si IGBT [303]	$T_j\uparrow$	Optimize redundant switching states $\rightarrow P_{loss}\downarrow \rightarrow T_j\downarrow$
		Si MOSFET [304]	Phase current $\uparrow$	Duty cycle $\downarrow \rightarrow P_{cond}\downarrow \rightarrow T_j\downarrow$
		Si IGBT [305]	Device current $\uparrow$	Optimize redundant space voltage vectors $\rightarrow P_{loss}\downarrow \rightarrow T_j\downarrow$
		Si IGBT [306]	$P_o\uparrow$	Duty cycle $\downarrow \rightarrow P_{loss}\downarrow \rightarrow T_j\downarrow$
	Turn-off delay time control	Si IGBT [307]	$\Delta T_j\uparrow$	$R\downarrow$ or $C\downarrow$ in RC snubber circuit $\rightarrow P_{off}\downarrow \rightarrow \Delta T_j\downarrow$
	Hybrid control	Si IGBT [308]	$T_j\uparrow$ or $\Delta T_j\uparrow$	$f_{sw}\downarrow \rightarrow P_{sw}\downarrow$
				Duty cycle $\downarrow \rightarrow P_{cond}\downarrow$
		Si MOSFET [309], [310]	$T_{j_mean}\uparrow$ or $\Delta T_j\uparrow$	$f_{sw}\downarrow$
				Load current $\downarrow$
		Si IGBT [311]	$T_j\uparrow$	$f_{sw}\downarrow$
				Load current $\downarrow$
	System level control	Si IGBT [312]	$\Delta T_j\uparrow$	Reactive power injection $\rightarrow \Delta T_j\downarrow$

V_{th} is such an example. The measurement of V_{th} normally requires a high sensing speed and high resolution for both drain current and gate–source voltage [285]. As a result, from the perspective of realization complexity, this indicator is not preferred as an ageing indicator.

VII. SYSTEM-LEVEL LIFETIME EXTENSION

The degradation indicator information obtained from online condition monitoring can be applied to not only passively update but also actively control the system lifetime.

Table IX summarizes the active thermal control strategies from the perspectives of topological and control improvement. No SiC MOSFETs have been included in this table because most of the literature has been focusing on the Si-based components. The approaches applied to these Si devices could be good references for SiC MOSFET-based converter lifetime extension. Two inherent issues exist in this method. Additional thermal control loops are needed. There is a compromise between thermal reliability and overall performance indices such as efficiency, cost, and volume. Active thermal control is normally conducted separately from the lifetime estimation. It can also be conducted together with system lifetime estimation by integrating lifetime and damage accumulation models into active thermal control algorithm [295]. Basically, the control of instantaneous junction temperature T_j [296], junction temperature swing ΔT_j [297], maximum junction temperature $T_{j_\max}$ [298], average junction temperature T_{j_mean} [151], case temperature T_C [179], [260], and heat sink temperature [179] have been targeted. Controlling T_{j_mean} and ΔT_j together has better lifetime improvement compared with the control of individual parameters [246]. But the hybrid control requires more computational resources. Thus, there exists a tradeoff between the microprocessor capability and control preciseness.

From the perspective of the topological improvement, most lifetime extension strategies have been focused on the adaptive gate drives, which are configured with either analog or digital circuits. In spite of the lower cost, the analog circuits have intrinsic weakness of adjusting control parameters and realizing fast switching [313]. The switching frequency is kept constant in this method. First, case temperature-changing rate has been controlled to adjust the turn-ON transient duration, which is related to switching loss [297]. But there exists delay time between the change of junction and case temperature. Second, the load current has been controlled to adjust the gate resistance [298]. Both $T_{j_\max}$ and ΔT_j have been reduced without T_j measurement. But the impact of parameter variation has not been analyzed. Third, gate resistance has been changed to reduce both $T_{j_\max}$ and ΔT_j [298]. Fourth, V_{gs} amplitude has been adjusted to decrease T_j by tracking $R_{\mathrm{ds_on}}$ change [296]. V_{gs} increase causes smaller $R_{\mathrm{ds_on}}$, compensating $R_{\mathrm{ds_on}}$ increase due to temperature rise. Thus, the efficiency has been improved.

From the perspective of control methods, the switching frequency control, active cooling control, active power control,

PWM control modification, turn-OFF delay time control, hybrid control, and system-level control have been studied.

A. Switching Frequency f_{sw} Control

The switching frequency f_{sw} control has been carried out either separately or with other parameters. It is independent of the load cycles. The switching loss increases with higher f_{sw}, whereas the peak current per switching cycle rises with lower f_{sw} [306]. Thus, there is a tradeoff between the efficiency and the device current stress. First, f_{sw} has been changed through a hysteresis controller [151], [246], [299], [300], [314]. ΔT_j is derived from power loss modeling and used as the input of the controller. Second, f_{sw} has also been controlled together with the load current to adjust T_j [308], [309], [311].

B. Active Cooling Control

This approach has been conducted without estimating junction temperature [301]. Feedforward open-loop power loss and ambient temperature control are carried out to improve the dynamic response. Feedback closed-loop baseplate temperature control is intended to reduce the temperature swing. Although the temperature stress of devices could be decreased, two additional control loops make it relatively complex.

C. Active Power Control

Active power control has been applied to limit the maximum photovoltaic (PV) output power [315]. Thermal loading is reduced by combining active power control and maximum power point tracking. However, PV panel degradation has not been included [316]. Therefore, the long-term overall reliability evaluation is not accurate.

D. PWM Control Modification

Most PWM modification techniques have been conducted in Si IGBTs. They could induce issues such as the distorted output waveforms with high THD. To improve the quality of the output waveform, DPWM is applied with variable dc-link voltage control [11]. However, it suffers from unstable input voltage. Following lists the state-of-the-art literature regarding this PWM control modification method.

1) The clamping angle of DPWM has been controlled to reduce the switching loss and corresponding thermal stresses of power devices in a cascaded H-bridge converter [302]. But it suffers from high output THD at the light load.
2) Different from conventional PWM control, two modulation waveforms have been adopted in the improved DPWM scheme to realize active thermal control [317].
3) DPWM1 method has been implemented in a hysteresis controller to decrease the thermal-cycle amplitude [314].
4) Improved carrier phase-shift algorithm has been used to optimize the gate switching sequence so that both the T_j and ΔT_j thermal stresses of the switches are alleviated [303]. But neither the THD nor the cost has been well designed.
5) Space vector PWM (SVPWM) has been adopted to reduce the loss in multilevel topologies [305]. One issue with this method is that the loss control and neutral-point voltage control cannot be conducted simultaneously.
6) Duty cycle has been used as the control parameter to decrease the power loss of devices in the isolated converter [306]. Although this method has fast response and simple implementation, there is a tradeoff between cost and efficiency.
7) Switching states of submodules in modular multilevel converter have been controlled according to the temperature to achieve the thermal balancing among submodules [318]. The submodule capacitor temperature could also be regulated by controlling the capacitor voltage [319]. But this method suffers from a small thermal adjustment range constrained by the constant total arm voltage requirement.
8) Improved PWM method has been used in Si MOSFETs to adjust the switch thermal stress in dc–dc and dc–ac interleaved converters [304]. Although only one control loop is needed, the cost is increased due to full-scale components.

E. Turn-OFF Delay Time Control

The turn-OFF delay time control has been conducted in Si IGBTs by introducing a turn-OFF trajectory adjustment circuit [307]. Individual thermal control is achieved. The turn-OFF loss is adjusted by the IGBT turn-OFF trajectory so that the ΔT_j is decreased. It is useful in controlling the individual power loss of each device. However, the volume and cost are increased. Overall efficiency is discounted due to the additional circuit.

F. Hybrid Control Methods

The technique combining two or more of the previous control strategies has also been extensively investigated. First, PWM selection between SVPWM and DPWM is done accompanying with the switching frequency modification to decrease the power loss [320]. However, there is a tradeoff between the output current waveform quality and the device lifetime. Second, the control of switching frequency, PWM method, and load current has been conducted at the same time in [308]. Although this method is cost effective, it suffers from complex control. Third, the switching frequency and duty cycle are both controlled in [309] and [310]. But T_j is not strictly adjusted due to parameter drift with temperature. Fourth, the switching frequency and load current are both controlled in [311] to optimize the torque and efficiency at the same time. But the variability of load current is required to achieve this optimization.

G. System-Level Active Thermal Control

The system-level active thermal control has been implemented through the reactive current control in an individual converter or load-sharing control among multiple converters. First, the reactive current control has been conducted to stabilize the device ΔT_j in a three-level neutral-point-clamped inverter [312]. But the reactive current brings in additional thermal imbalance issues. Second, the active power is controlled between

two paralleled three-phase PWM inverters [321]. The average switch thermal stresses have been balanced.

According to the previous summarization, some opportunities could be further explored in the active thermal control domain concerning the SiC MOSFET-based power converters.

1) Most of the active thermal control is based on the Si MOSFETs and Si IGBTs. Since temperature-dependent characteristics of SiC MOSFET electrical parameters are different as analyzed in the previous sections, the active thermal control methods should be further investigated. For example, due to less temperature-dependent ON-state resistance in SiC MOSFETs, adjusting ON-state resistance to compensate for the shift caused by temperature rise could be considered.
2) Qualitative improvement has been extensively analyzed in the state-of-the-art active thermal control literature by observing the temperature decrease. It is necessary to make a quantitative comparison of both the lifetime improvement and the efficiency sacrifice for SiC power converters in the further research concerning lifetime modeling.

VIII. Conclusion

A literature overview of the lifetime prediction and extension for SiC MOSFET-based power converters is presented. SiC MOSFET chip-level, package-level failure modes, and mechanisms are summarized. Based on the individual failure indicators, the ALTs are discussed. Component-level RUL estimation is conducted including PoF lifetime models, data-driven lifetime models and hybrid models. Also, component-level cycle counting algorithms and fatigue damage accumulation approaches are reviewed. System-level lifetime estimation methods are further investigated. The component and system-level lifetime modeling software has been summarized based on the state-of-the-art academic and commercial development. Online monitoring techniques concerning junction temperature-related parameters and other nonthermal degradation indicators are analyzed. Finally, the system-level lifetime extension strategies are compared. By online updating the ALT-based static lifetime model, the overall system lifetime estimation accuracy could be improved. Based on the aforementioned analysis, some recommendations are made for future possible research directions in the SiC power converter lifetime prediction and extension area.

1) The SiC MOSFET failure criteria of some emerging indicators have not been well studied. For instance, the Miller plateau amplitude and time duration for gate oxide breakdown, as well as the drain leakage current and forward voltage for body diode degradation have not been covered regarding the failure thresholds in the existing ALT standards. Besides, the failure criteria of the ON-state voltage and ON-state resistance for bond wire liftoff, as well as the thermal resistance for solder-fatigue are also needed concerning SiC MOSFETs in corresponding standards. These regulations would help institutions and manufacturers conduct the fair reliability comparison among different SiC products.
2) SiC MOSFET ALT designs need to be investigated due to their individual failure indicator shifting mechanisms.
3) Most published PoF lifetime models for SiC MOSFETs are based on Si IGBT power modules. Considering the differences in the failure mechanisms between Si and SiC, the PoF lifetime models including SiC reliability characteristics would lead to more accurate lifetime prediction.
4) Most published power electronic lifetime research has done detailed parameter estimation by using the Monte Carlo statistical extrapolating method. The statistical strategies such as reviewed EKF, PF, and artificial intelligence are to be further studied and compared with the Monte Carlo technique in the SiC MOSFET power converters.
5) Palmgren–Miner's Law has been widely used in fatigue damage accumulation. Rather than sticking with this linear method, the nonlinear damage accumulation methods such as the Manson–Halford model is to be investigated in the SiC MOSFET power converters. The fair comparison among different accumulation approaches is useful to improve the accuracy of lifetime prediction, especially considering the loading-level dependence in SiC MOSFET power converters.
6) Much system lifetime modeling has been conducted in the Si IGBT based inverters by using an RBD or MC. SiC MOSFET-based lifetime models following Weibull distribution with the inconstant failure rate could be studied. Also, the comparison by using different system lifetime models would help optimize the system-level lifetime prediction accuracy in SiC MOSFET power converters.
7) Package-level thermomechanical modeling for the SiC MOSFETs has not been given enough attention to. The thermomechanical modeling difference between SiC MOSFETs and Si devices is necessary to improve the SiC MOSFET lifetime prediction accuracy and further provide design directions to enhance their package-level reliability.
8) How to optimally apply the monitored parameter information to update the initial ALT-based statistical lifetime models would be further investigated for SiC power converters.
9) Although both of the thermal and nonthermal health indicators have been well studied for SiC MOSFETs, they are still in a relatively emerging domain and could be further explored. For example, the Miller plateau duration has only been studied in the Si IGBT degradation. The output voltage harmonics have been used to indicate Si IGBT module solder-fatigue and could be investigated in SiC MOSFETs as well.
10) In the condition monitoring area, seldom literature has explored the system-level condition monitoring of SiC MOSFET-based power converter. This technique plays an essential part in an accurate system-level lifetime prediction and, thus, should be investigated further.
11) Controlled parameters in SiC MOSFET-based power converter active thermal control could unfold other research opportunities, considering the TSEP

temperature-dependent characteristics are different from Si devices.

12) Instead of resting on the qualitative analysis, further quantitative comparison among different active thermal control approaches is necessary to make a reasonable tradeoff among lifetime, efficiency, and power density for the gradually widespread applications of SiC power converters.

References

[1] H. Wang, K. Ma, and F. Blaabjerg, "Design for reliability of power electronic systems," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, 2012, pp. 33–44.

[2] T. Dragicevic, P. Wheeler, and F. Blaabjerg, "Artificial intelligence aided automated design for reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7161–7171, Aug. 2019.

[3] C. Olalla, D. Maksimovic, C. Deline, and L. Martinez-Salamero, "Impact of distributed power electronics on the lifetime and reliability of PV systems," *Prog. Photovolt. Res. Appl.*, vol. 25, no. 10, pp. 821–835, 2017.

[4] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential power processing for increased energy production and reliability of photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, Jun. 2013.

[5] M. Piri, M. Niroomand, and R.-A. Hooshmand, "A comprehensive modeling of grid-connected photovoltaic systems using multiphase converter based on reliability concepts," *J. Sol. Energy Eng.*, vol. 139, no. 5, Aug. 2017, Art. no. 054502.

[6] D. Zhou, H. Wang, F. Blaabjerg, S. K. Kor, and D. Blom-Hansen, "System-level reliability assessment of power stage in fuel cell application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[7] D. Zhou, H. Wang, and F. Blaabjerg, "Mission profile based system-level reliability analysis of DC/DC converters for a backup power application," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8030–8039, Sep. 2018.

[8] A. Khosroshahi, M. Abapour, and M. Sabahi, "Reliability evaluation of conventional and interleaved DC–DC boost converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5821–5828, Oct. 2015.

[9] F. Richardeau and T. T. L. Pham, "Reliability calculation of multilevel converters: Theory and applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4225–4233, Oct. 2013.

[10] D. Hirschmann, D. Tissen, S. Schroder, and R. W. De Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2511–2517, Nov. 2007.

[11] Y. Song and B. Wang, "Evaluation methodology and control strategies for improving reliability of HEV power electronic system," *IEEE Trans. Veh. Technol.*, vol. 63, no. 8, pp. 3661–3676, Oct. 2014.

[12] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[13] R. M. Burkart and J. W. Kolar, "Comparative life cycle cost analysis of Si and SiC PV converter systems based on advanced η-ρ-σ multiobjective optimization techniques," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4344–4358, Jun. 2017.

[14] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 912–921, Mar. 2011.

[15] S. Madhusoodhanan *et al.*, "Solid-state transformer and MV grid tie applications enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs based multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3343–3360, Jul. 2015.

[16] "SiC power devices and modules," ROHM Semicond., Kyoto, Japan, Application Note, 2013.

[17] "SiC power modules: Innovative power devices for a sustainable future," Mitsubishi Elect. Corporation, Tokyo, Japan, Application Note, 2014.

[18] B. J. Baliga, "Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*, 1st ed. New York, NY, USA: Springer, 2008, pp. 279–506.

[19] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989.

[20] J. Wang and X. Jiang, "Review and analysis of SiC MOSFETs' ruggedness and reliability," *IET Power Electron.*, to be published, doi:10.1049/iet-pel.2019.0587.

[21] M. Hologne, "Contribution to condition monitoring of silicon carbide MOSFET based power module," Ph.D. dissertation, Energy Dept., Université de Lyon, Lyon, France, 2018.

[22] B. J. Baliga, "Planar power MOSFETs," in *Silicon Carbide Power Devices*. Singapore: World Scientific, 2005, ch. 9, p. 242.

[23] R. Singh, "Reliability and performance limitations in SiC power devices," *Microelectron. Rel.*, vol. 46, no. 5/6, pp. 713–730, 2006.

[24] L. Yu, K. P. Cheung, J. Campbell, J. S. Suehle, and K. Sheng, "Oxide reliability of SiC MOS devices," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep.*, 2008, pp. 141–144.

[25] S. K. Gupta, J. Singh, and J. Akhtar, "Materials and processing for gate dielectrics on silicon carbide (SiC) surface," in *Physics and Technology of Silicon Carbide Devices*. Rijeka, Croatia: IntechOpen, 2012, ch. 8, pp. 207–234.

[26] I. Yonenaga, "Hardness of bulk single-crystal GaN and AlN," *MRS Internet J. Nitride Semicond. Res.*, vol. 7, p. 4, Jun. 2002.

[27] M. Biglarbegian, S. Mostafavi, S. Hauer, S. J. Nibir, and N. Kim, "On condition monitoring of high frequency power GaN converters with adaptive prognostics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1272–1279.

[28] S. Dusmez, H. Duran, and B. Akin, "Remaining useful lifetime estimation for thermally stressed power MOSFETs based on on-state resistance variation," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2554–2563, May/Jun. 2016.

[29] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules—Various factors influencing lifetime," in *Proc. 5th Int. Conf. on Integr. Power Syst.*, 2008, no. April, pp. 1–6.

[30] "Load-cycling capability of HiPak IGBT modules," ABB, Zürich, Switzerland, Appl. Note 5SYA 2043-04. pp. 1–7, 2012.

[31] H. Wang, P. D. Reigosa, and F. Blaabjerg, "A humidity-dependent lifetime derating factor for DC film capacitors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 3064–3068.

[32] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[33] M. Tanrioven and M. S. Alam, "Reliability modeling and analysis of stand-alone PEM fuel cell power plants," *Renewable Energy*, vol. 31, no. 7, pp. 915–933, Jun. 2006.

[34] B. Wang, J. Cai, X. Du, and L. Zhou, "Review of power semiconductor device reliability for power converters," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 101–117, Jun. 2017.

[35] A. Hanif, Y. Yu, D. Devoto, and F. H. Khan, "A comprehensive review toward the state-of-the-art in failure and lifetime predictions of power electronic devices," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4729–4746, May 2019.

[36] X.-S. Si, W. Wang, C.-H. Hu, and D.-H. Zhou, "Remaining useful life estimation—A review on the statistical data driven approaches," *Eur. J. Oper. Res.*, vol. 213, no. 1, pp. 1–14, Aug. 2011.

[37] L. Liao and F. Köttig, "Review of hybrid prognostics approaches for remaining useful life prediction of engineered systems, and an application to battery life prediction," *IEEE Trans. Rel.*, vol. 63, no. 1, pp. 191–207, Mar. 2014.

[38] F. Ahmadzadeh and J. Lundberg, "Remaining useful life estimation: Review," *Int. J. Syst. Assurance Eng. Manage.*, vol. 5, no. 4, pp. 461–474, Dec. 2014.

[39] V. Smet, F. Forest, J.-J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of Vce monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2760–2770, Jul. 2013.

[40] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "In situ diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.

[41] S. Pu, F. Yang, E. Ugur, C. Xu, and B. Akin, "SiC MOSFET aging detection based on miller plateau voltage sensing," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2019, pp. 1–6.

[42] H. Soliman, H. Wang, and F. Blaabjerg, "A review of the condition monitoring of capacitors in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4976–4989, Nov./Dec. 2016.

[43] W. Chen, L. Zhang, P. Krishna, A. M. Bazzi, S. Joshi, and E. M. Dede, "Data-driven approach for fault prognosis of SiC MOSFETs," *IEEE Trans. Power Electron.*, to be published, doi:10.1109/TPEL.2019.2936850.

[44] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[45] H. S. Chung *et al.*, "Modelling for the lifetime prediction of power semiconductor modules," in *Reliability of Power Electronic Converter Systems*, 1st ed. London, U.K.: IET, 2015, pp. 104–124.

[46] N. Baker and M. Liserre, "Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 942–948.

[47] M. Andresen, M. Liserre, and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 2014, pp. 1–10.

[48] M. Andresen, G. Buticchi, and M. Liserre, "Study of reliability-efficiency tradeoff of active thermal control for power electronic systems," *Microelectron. Rel.*, vol. 58, pp. 119–125, 2016.

[49] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 765–776, Jan. 2018.

[50] B. J. Nel and S. Perinpanayagam, "A brief overview of SiC MOSFET failure modes and design reliability," in *Proc. 5th Int. Conf. Through-Life Eng. Services*, 2017, vol. 59, pp. 280–285.

[51] J. Wei *et al.*, "Investigations on the degradations of double-trench SiC power MOSFETs under repetitive avalanche stress," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 546–552, Jan. 2019.

[52] R. Nakamura, Y. Nakano, M. Aketa, K. Noriaki, and K. Ino, "1200V 4H-SiC trench devices," in *Proc. PCIM Eur.; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy, Energy Manage.*, 2014, pp. 1–7.

[53] D. Peters *et al.*, "Performance and ruggedness of 1200V SiC Trench MOSFET," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, 2017, pp. 239–242.

[54] R. Singh and A. R. Hefner, "Reliability of SiC MOS devices," *Solid State Electron.*, vol. 48, no. 10/11, pp. 1717–1720, 2004.

[55] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and reliability review of 650V and 900V silicon and SiC devices: MOSFETs, cascode JFETs and IGBTs," *IEEE Trans. Ind. Electron.*, to be published, doi:10.1109/TIE.2019.2945299.

[56] X. Jiang *et al.*, "Failure modes and mechanism analysis of SiC MOSFET under short-circuit conditions," *Microelectron. Rel.*, vol. 88–90, pp. 593–597, Sep. 2018.

[57] A. Agarwal, H. Fatima, S. Haney, and S. H. Ryu, "A new degradation mechanism in high-voltage SiC power MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 587–589, Jul. 2007.

[58] O. Kusumoto *et al.*, "Reliability of diode-integrated SiC power MOSFET(DioMOS)," *Microelectron. Rel.*, vol. 58, pp. 158–163, 2016.

[59] T. Kimoto and J. A. Cooper, "Device processing of silicon carbide," in *Fundamentals of Silicon Carbide Technology—Growth, Characterization, Devices, and Applications*, 1st ed. Hoboken, NJ, USA: Wiley, 2014, p. 241.

[60] C.-T. Yen *et al.*, "Oxide breakdown reliability of SiC MOSFET," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2019, pp. 1–3.

[61] X. Ye, C. Chen, Y. Wang, G. Zhai, and G. J. Vachtsevanos, "Online condition monitoring of power MOSFET gate oxide degradation based on miller platform voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4776–4784, Jun. 2017.

[62] U. Karki and F. Z. Peng, "Effect of gate oxide degradation on electrical parameters of power MOSFETs," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10764–10773, Dec. 2018.

[63] R. Ouaida *et al.*, "Gate oxide degradation of SiC MOSFET in switching conditions," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1284–1286, Dec. 2014.

[64] Z. Ni, Y. Li, X. Lyu, O. P. Yadav, and D. Cao, "Miller plateau as an indicator of SiC MOSFET gate oxide degradation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1280–1287.

[65] B. Van Zeghbroeck, "MOS field-effect-transistors, Section 7.7.5. Field dependent mobility," in *Principles of Semiconductor Devices*. Boulder, CO, USA: Univ. Colorado Boulder, 2006, ch. 7, p. 342.

[66] D. Dang, S. Guichard, M. Urbain, and S. Raël, "Characterization and modeling of 1200V 100A N-channel 4H-SiC MOSFET," in *Proc. Symp. Genie Electrique*, 2016, no. June, pp. 1–7.

[67] E. Ugur, F. Yang, S. Pu, S. Zhao, and B. Akin, "Degradation assessment and precursor identification for SiC MOSFETs under high temp cycling," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2858–2867, May/Jun. 2019.

[68] A. Ortiz-Conde *et al.*, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 42, no. 4/5, pp. 583–596, 2002.

[69] A. J. Lelis *et al.*, "Time dependence of bias-stress-induced SiC MOSFET threshold-voltage instability measurements," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1835–1840, Aug. 2008.

[70] A. J. Lelis, R. Green, D. Habersat, and N. Goldsman, "Effect of threshold-voltage instability on SiC DMOSFET reliability," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep.*, 2008, pp. 72–76.

[71] D. B. Habersat, R. Green, and A. J. Lelis, "Temperature-dependent threshold stability of COTS SiC MOSFETs during gate switching," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2017, pp. WB-4.1–WB-4.4.

[72] D. Sadik, "On reliability of SiC power devices in power electronics," Ph.D. dissertation, Dept Elect. Power Energy Syst., KTH Roy. Inst. Technol., Stockholm, Sweden, 2017.

[73] A. J. Lelis, R. Green, and D. B. Habersat, "SiC MOSFET threshold-stability issues," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 32–37, May 2018.

[74] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs high-voltage device reliability focusing on threshold voltage instability," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4604–4616, Nov. 2019.

[75] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.

[76] Z. Pavlovic *et al.*, "Influence of gate oxide charge density on VDMOS transistor ON-resistance," in *Proc. Int. Conf. Microelectron.*, 1999, vol. 2, pp. 663–666.

[77] C. Chen, X. Ye, Y. Wang, J. Xu, and G. Zhai, "PHM application of power converters using health precursor of power MOSFETs," in *Proc. Prognostics Syst. Health Manage. Conf.*, 2015, pp. 1–5.

[78] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Appl. Phys. Rev.*, vol. 2, no. 2, 2015, Art. no. 021307.

[79] R. Fujita, K. Tani, K. Konishi, and A. Shima, "Failure of switching operation of SiC-MOSFETs and effects of stacking faults on safe operation area," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4448–4454, Oct. 2018.

[80] R. Green, A. Lelis, and F. Nouketcha, "Comparison of SiC MOSFET characteristics following body-diode forward-current stress," *Mater. Sci. Forum*, vol. 963, pp. 583–587, Jul. 2019.

[81] R. Bonyadi, O. Alatise, S. Jahdi, J. Hu, L. Evans, and P. A. Mawby, "Investigating the reliability of SiC MOSFET body diodes using Fourier series modelling," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 443–448.

[82] A. Fayyaz, G. Romano, and A. Castellazzi, "Body diode reliability investigation of SiC power MOSFETs," *Microelectron. Rel.*, vol. 64, no. September, pp. 530–534, 2016.

[83] "Date sheet of 3 IGBT and SiC diode hybrid power module," Infineon Technol. AG, Neubiberg, Germany, DF200R12W1H3F_B11, pp. 1–11, 2017.

[84] "Date sheet of 1.2 kV silicon carbide six-pack power module," Cree, Durham, NC, USA, CCS020M12CM2, pp. 1–10, 2015.

[85] "Date sheet of 1.2 kV all-silicon carbide half-bridge module," Cree, Durham, NC, USA, CAS325M12HM2, pp. 1–8, 2017.

[86] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, "Short-circuit tests on SiC power MOSFETs," in *Proc. Int. Conf. Power Electron. Drive Syst.*, 2013, pp. 1297–1300.

[87] H. Luo, F. Iannuzzo, N. Baker, F. Blaabjerg, W. Li, and X. He, "Study of current density influence on bond wire degradation rate in SiC MOSFET modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi:10.1109/JESTPE.2019.2920715.

[88] K. Li, G. Y. Tian, L. Cheng, A. Yin, W. Cao, and S. Crichton, "State detection of bond wires in IGBT modules using eddy current pulsed thermography," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5000–5009, Sep. 2014.

[89] C. M. Tan, G. Zhang, and Z. Gan, "Dynamic study of the physical processes in the intrinsic line electromigration of deep-submicron copper and aluminum interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 3, pp. 450–456, Sep. 2004.

[90] F. T. B. W. Göthner, "Experimental investigation of operational reliability of silicon carbide MOSFETs," M.S. thesis, Dept. Electric Power Eng., Norwegian Univ. Sci. Technol., Trondheim, Norway, 2017.

[91] B. Hu *et al.*, "Failure and reliability analysis of a SiC power module based on stress comparison to a Si device," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 727–737, Dec. 2017.
[92] A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "Mission-profile-based stress analysis of bond-wires in SiC power modules," *Microelectron. Rel.*, vol. 64, pp. 419–424, 2016.
[93] M. Horio, Y. Iizuka, and Y. Ikeda, "Packaging technologies for SiC power modules," *Fuji Elect. Rev.*, vol. 58, no. 2, p. 75–80, 2012.
[94] Y. Wang, X. Dai, G. Liu, Y. Wu, D. Li, and S. Jones, "Status and trend of SiC power semiconductor packaging," in *Proc. 16th Int. Conf. Electron. Packag. Technol.*, 2015, pp. 396–402.
[95] V. Mulpuri, "Failure analysis and high temperature characterization of silicon carbide power MOSFETs," M.S. thesis, Dept. Elect. Comput. Eng., Univ. Akron, Akron, OH, USA, 2017.
[96] M. Held *et al.*, "Fast power cycling test of IGBT modules in traction application," in *Proc. 2nd Int. Conf. Power Electron. Drive Syst.*, 1997, vol. 1, pp. 425–430.
[97] J. McPherson, "Time-to-failure models for selected failure mechanisms," in *Reliable Physics and Engineering: Time-to-Failure Modeling*. 2nd ed., Basel, Switzerland: Springer, 2013, p. 159.
[98] S. Ramminger, N. Seliger, and G. Wachutka, "Reliability model for Al wire bonds subjected to heel crack failures," *Microelectron. Rel.*, vol. 40, no. 8–10, pp. 1521–1525, Aug. 2000.
[99] A. Volke and M. Hornkamp, "Type tests and routine tests," in *IGBT Modules—Technologies, Driver and Application*. Neubiberg, Germany:Infineon Technol., 2012, p. 509.
[100] H. Medjahed, P. E. Vidal, and B. Nogarede, "Thermo-mechanical stress of bonded wires used in high power modules with alternating and direct current modes," *Microelectron. Rel.*, vol. 52, no. 6, pp. 1099–1104, 2012.
[101] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Rel.*, vol. 42, no. 4/5, pp. 653–667, 2002.
[102] A. Hamidi, N. Beck, K. Thomas, and E. Herr, "Reliability and lifetime evaluation of different wire bonding technologies for high power IGBT modules," *Microelectron. Rel.*, vol. 39, no. 6/7, pp. 1153–1158, 1999.
[103] P. Nayak, S. K. Pramanick, and K. Rajashekara, "A high-temperature gate driver for silicon carbide MOSFET," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 1955–1964, Mar. 2018.
[104] N. Baker *et al.*, "Test setup for long term reliability investigation of silicon carbide MOSFETs," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–9.
[105] N. Baker, H. Luo, and F. Iannuzzo, "Simultaneous on-state voltage and bond-wire resistance monitoring of silicon carbide MOSFETs," *Energies*, vol. 10, no. 3, Mar. 2017, Art. no. 384.
[106] H. Luo, F. Iannuzzo, and F. Blaabjerg, "Solder layer degradation measurement for SiC-MOSFET modules under accelerated power cycling conditions," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*, 2018, pp. 1–5.
[107] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.
[108] M. Ciappa and A. Castellazzi, "Reliability of high-power IGBT modules for traction applications," in *Proc. IEEE 45th Annu. Int. Rel. Phys. Symp.*, 2007, pp. 480–485.
[109] D. C. Katsis and J. D. V. Wyk, "Void-induced thermal impedance in power semiconductor modules: Some transient temperature effects," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1239–1246, Sep. 2003.
[110] D. C. Katsis and J. D. V. Wyk, "A thermal, mechanical, and electrical study of voiding in the solder die-attach of power MOSFETs," *IEEE Trans. Compon. Packag. Technol.*, vol. 29, no. 1, pp. 127–136, Mar. 2006.
[111] W. Lai *et al.*, "Experimental investigation on the effects of narrow junction temperature cycles on die-attach solder layer in an IGBT module," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1431–1441, Feb. 2017.
[112] T. Kim and T. Funaki, "Thermal measurement and analysis of packaged SiC MOSFETs," *Thermochim. Acta*, vol. 633, pp. 31–36, 2016.
[113] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power modules: A survey," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 1, pp. 80–97, Mar. 2016.
[114] P. Losee *et al.*, "1.2 kV class SiC MOSFETs with improved performance over wide operating temperature," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2014, pp. 297–300.
[115] T. Santini *et al.*, "Accelerated degradation data of SiC MOSFETs for lifetime and remaining useful life assessment," *Microelectron. Rel.*, vol. 54, no. 9/10, pp. 1718–1723, Sep. 2014.
[116] R. Green, A. Lelis, and D. Habersat, "Application of reliability test standards to SiC Power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2011, pp. 756–764.
[117] S. A. Ikpe *et al.*, "Silicon-carbide power MOSFET performance in high efficiency boost power processing unit for extreme environments," in *Proc. Int. Conf. High Temp. Electron.*, 2016, pp. 184–189.
[118] L. Yang and A. Castellazzi, "High temperature gate-bias and reverse-bias tests on SiC MOSFETs," *Microelectron. Rel.*, vol. 53, no. 9–11, pp. 1771–1773, 2013.
[119] D. N. Dalal and N. Christensen, "Power cycle test bench for accelerated life testing of 10 kV SiC MOSFETs," Group Master's thesis, Dept. Energy Technol., Aalborg Univ., Aalborg, Denmark, 2016.
[120] H. Luo, F. Iannuzzo, F. Blaabjerg, M. Turnaturi, and E. Mattiuzzo, "Aging precursors and degradation effects of SiC-MOSFET modules under highly accelerated power cycling conditions," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2506–2511.
[121] J. P. Kozak, K. D. T. Ngo, D. DeVoto, and J. Major, "Impact of accelerated stress-tests on SiC MOSFET precursor parameters," in *Proc. Int. Symp. 3D Power Electron. Integration Manuf.*, 2018, pp. 1–5.
[122] *Temperature, Bias, and Operating Life*, JEDEC Standard JESD22-A108D, JEDEC Solid State Technology Association, no. November, pp. 1–7, 2010.
[123] "Reliability and quality for IGBTs," On Semiconductor, Phoenix, AZ, USA, Application Note AND9058/D, pp. 1–7, 2016.
[124] S. A. Ikpe *et al.*, "Long-term reliability of a hard-switched boost power processing unit utilizing SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2016, vol. 2016, pp. ES11–ES18.
[125] J. A. O. Gonzalez and O. Alatise, "A novel non-intrusive technique for BTI characterization in SiC MOSFETS," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5737–5747, Jun. 2019.
[126] L. R.G. Reddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.
[127] "Failure mechanism based stress test qualification for discrete semiconductors in automotive applications," Automot. Electron. Council, New York, NY, USA, AEC-Q101-Rev-D1, 2013.
[128] S. L. Rumyantsev *et al.*, "Channel mobility and on-resistance of vertical double implanted 4H-SiC MOSFETs at elevated temperatures," *Semicond. Sci. Technol.*, vol. 24, no. 7, 2009, Art. no. 075011.
[129] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.
[130] C. M. Dimarino, "High temperature characterization and analysis of silicon carbide (SiC) power semiconductor transistors," M.S. thesis, Dept. Elect. Comput. Eng., Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2014.
[131] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kV, 20 A SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 1480–1487.
[132] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. Mawby, "Temperature sensitive electrical parameters for condition monitoring in SiC power MOSFETs," in *Proc. 8th IET Int. Conf. Power Electron., Mach., Drives*, 2016, pp. 1–6.
[133] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Feb. 2016.
[134] F. Yang, E. Ugur, B. Akin, and G. Wang, "Design methodology of DC power cycling test setup for SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi:10.1109/JESTPE.2019.2914419.
[135] T. Ziemann, U. Grossner, and J. Neuenschwander, "Power cycling of commercial SiC MOSFETs," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 24–31.
[136] H. Malorie, B. Pascal, A. Bruno, C. Guy, and R. Hubert, "Test bench and data analysis towards an on-line Health Monitoring for emerging power modules," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, 2018, pp. 1531–1536.
[137] International Electrotechnical Commission (IEC), "Bias-temperature stability test for metal-oxide-semiconductor field-effect transistors (MOSFET)," 2006. [Online]. Available: https://webstore.iec.ch/publication/6938
[138] *Test Method Standard: Test Methods for Semiconductor Devices*, MIL-STD-750F, Department of Defense of the USA, pp. 1–19, 2012.

[139] JEDEC Committee, "JC-70 wide bandgap power electronic conversion semiconductors," 2018. [Online]. Available: https://www.jedec.org/committees/jc-70

[140] L. A. Escobar and W. Q. Meeker, "A review of accelerated test models," *Statistical Sci.*, vol. 21, no. 4, pp. 552–577, 2006.

[141] H. A. Schafft, "Testing and fabrication of wire-bond electrical connections : A comprehensive survey," Nat. Bur. Standards, Gaithersburg, MD, USA, Tech. Note 726, 1972.

[142] R. Ouaida, M. Berthou, P. Brosselard, S. Oge, P. Bevilacqua, and C. Joubert, "Investigation of using SiC MOSFET for high temperature applications," *Eur. Power Electron. Drives J.*, vol. 25, no. 2, pp. 5–11, Jun. 2015.

[143] D. J. Lichtenwalner *et al.*, "Reliability studies of SiC vertical power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2018, vol. 2018, pp. 2B.21–2B.26.

[144] I. F. Kovacevic and J. W. Kolar, "Modelling for the lifetime prediction of power semiconductor modules," in *Reliability of Power Electronic Converter Systems*, 1st ed., H. S. Chung, H. Wang, F. Blaabjerg, and M. Pecht, Eds., UK: IET, 2015, pp. 103–140.

[145] T. Hunger and R. Bayerer, "Extended reliability of substrate solder joints in power modules," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–8.

[146] I. F. Kovacevic, U. Drofenik, and J. W. Kolar, "New physical model for lifetime estimation of power modules," in *Proc. Int. Power Electron. Conf. ECCE Asia*, 2010, pp. 2106–2114.

[147] W. Lai, M. Chen, L. Ran, O. Alatise, S. Xu, and P. Mawby, "Low ΔTj stress cycle effect in IGBT power module die-attach lifetime modeling," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6575–6585, Sep. 2016.

[148] Z. Qiu, J. Zhang, P. Ning, and X. Wen, "Reliability modeling and analysis of SiC MOSFET power modules," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 1459–1463.

[149] M. Bakowski, "Status and prospects of SiC power devices, section 4.8.5 power cycling," in *Advancing Silicon Carbide Electronics Technology I: Metal Contacts to Silicon Carbide: Physics, Technology, Applications*. Millersville, PA, USA: Mater. Res. Forum LLC, 2018, ch. 4, p. 225.

[150] L. Yang, P. A. Agyakwa, and C. M. Johnson, "Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules," *IEEE Trans. Device Mater. Rel.*, vol. 13, no. 1, pp. 9–17, Mar. 2013.

[151] M. Weckert and J. Roth-Stielow, "Lifetime as a control variable in power electronic systems," in *Proc. Emobility—Elect. Power Train*, 2010, pp. 1–6.

[152] R. Have, B. Vermulst, and J. van Duivenbode, "An approach to lifetime estimation of SiC MOSFETs subjected to thermal stress," in *Proc. PCIM Eur.*, 2015, pp. 19–21.

[153] W. W. Lee, L. T. Nguyen, and G. S. Selvaduray, "Solder joint fatigue models: Review and applicability to chip scale packages," *Microelectron. Rel.*, vol. 40, no. 2, pp. 231–244, 2000.

[154] H. Lu, T. Tilford, C. Bailey, and D. R. Newcombe, "Lifetime prediction for power electronics module substrate mount-down solder interconnect," in *Proc. Int. Symp. High Density Packag. Microsyst. Integration*, 2007, pp. 1–10.

[155] O. Salmela, "Acceleration factors for lead-free solder materials," *IEEE Trans. Compon. Packag. Technol.*, vol. 30, no. 4, pp. 700–707, Dec. 2007.

[156] J. Mi, Y. F. Li, Y. J. Yang, W. Peng, and H. Z. Huang, "Thermal cycling life prediction of Sn-3.0Ag-0.5Cu solder joint using type-I censored data," *Sci. World J.*, vol. 2014, pp. 1–11, 2014.

[157] L. Ceccarelli, R. M. Kotecha, A. S. Bahman, F. Iannuzzo, and H. A. Mantooth, "Mission-profile-based lifetime prediction for a SiC MOSFET power module using a multi-step condition-mapping simulation strategy," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9698–9708, Oct. 2019.

[158] K. Brinkfeldt *et al.*, "Thermo-mechanical simulations of SiC power modules with single and double sided cooling," in *Proc. 16th Int. Conf. Thermal, Mech. Multi-Phys. Simul. Exp. Microelectron. Microsyst.*, 2015, pp. 1–7.

[159] Y. Shen, E. Liivik, F. Blaabjerg, D. Vinnikov, H. Wang, and A. Chub, "Reliability evaluation of an impedance-source PV microconverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1104–1108.

[160] J. R. Celaya *et al.*, "Prognostics of power MOSFETs under thermal stress accelerated aging using data-driven and model-based methodologies," in *Proc. Annu. Conf. Prognostics Health Manage. Soc.*, 2011, vol. 2, pp. 1–10.

[161] J. R. Celaya, A. Saxena, C. S. Kulkarni, S. Saha, and K. Goebel, "Prognostics approach for power MOSFET under thermal-stress aging," in *Proc. Annu. Rel. Maintainability Symp.*, 2012, pp. 1–6.

[162] A. Sokolov, C. Liu, and F. Mohn, "Reliability assessment of SiC power module stack based on thermo-structural analysis," in *Proc. 19th Int. Conf. Thermal, Mech. Multi-Phys. Simul. Exp. Microelectron. Microsyst., EuroSimE*, 2018, pp. 1–4.

[163] A. Vulli, "Accelerated ageing and prognostics of silicon carbide power MOSFET," Master's thesis, Dept. Elect. Eng. Automat., Aalto Univ., Helsinki, Finland, p. 69, 2018.

[164] E. Zio and G. Peloni, "Particle filtering prognostic estimation of the remaining useful life of nonlinear components," *Rel. Eng. Syst. Saf.*, vol. 96, no. 3, pp. 403–409, 2011.

[165] Y. Lei, N. Li, S. Gontarz, J. Lin, S. Radkowski, and J. Dybala, "A model-based method for remaining useful life prediction of machinery," *IEEE Trans. Rel.*, vol. 65, no. 3, pp. 1314–1326, Sep. 2016.

[166] M. Heydarzadeh, S. Dusmez, M. Nourani, and B. Akin, "Bayesian remaining useful lifetime prediction of thermally aged power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2718–2722.

[167] B. Saha, K. Goebel, and J. Christophersen, "Comparison of prognostic algorithms for estimating remaining useful life of batteries," *Trans. Inst. Meas. Control*, vol. 31, no. 3/4, pp. 293–308, 2009.

[168] R. Razavi-Far *et al.*, "Information fusion and semi-supervised deep learning scheme for diagnosing gear faults in induction machine systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6331–6342, Aug. 2019.

[169] A. Alghassi, S. Perinpanayagam, and M. Samie, "Stochastic RUL calculation enhanced with TDNN-based IGBT failure modeling," *IEEE Trans. Rel.*, vol. 65, no. 2, pp. 558–573, Jun. 2016.

[170] H.-Z. Huang, H.-K. Wang, Y.-F. Li, L. Zhang, and Z. Liu, "Support vector machine based estimation of remaining useful life: Current research status and future trends," *J. Mech. Sci. Technol.*, vol. 29, no. 1, pp. 151–163, Jan. 2015.

[171] S. Khomfoi and L. M. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using AI-based techniques," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2954–2968, Dec. 2007.

[172] K. L. Son, M. Fouladirad, and A. Barros, "Remaining useful life estimation on the non-homogenous gamma with noise deterioration based on Gibbs filtering: A case study," in *Proc. IEEE Int. Conf. Prognostics Health Manage.: Enhancing Saf., Efficiency, Availability, Effectiveness Syst. Through PHM Technol. Appl., Conf. Program*, 2012, pp. 1–6.

[173] Y. Zheng, L. Wu, X. Li, and C. Yin, "A relevance vector machine-based approach for remaining useful life prediction of power MOSFETs," in *Proc. Prognostics Syst. Health Manage. Conf.*, 2014, pp. 642–646.

[174] M. Baharani, M. Biglarbegian, B. Parkhideh, and H. Tabkhi, "Real-time deep learning at the edge for scalable reliability modeling of Si-MOSFET power electronics converters," *IEEE Internet Things J.*, vol. 6, no. 5, pp. 7375–7385, Oct. 2019.

[175] L. Liao, W. Jin, and R. Pavel, "Enhanced restricted Boltzmann machine with prognosability regularization for prognostics and health assessment," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7076–7083, Nov. 2016.

[176] S. H. Ali, M. Heydarzadeh, S. Dusmez, X. Li, A. S. Kamath, and B. Akin, "Lifetime estimation of discrete IGBT devices based on Gaussian process," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 395–403, Jan. 2018.

[177] S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran, and B. Akin, "Aging precursor identification and lifetime estimation for thermally aged discrete package silicon power switches," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 251–260, Jan./Feb. 2017.

[178] S. Dusmez and B. Akin, "Remaining useful lifetime estimation for degraded power MOSFETs under cyclic thermal stress," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 3846–3851.

[179] X. Han and M. Saeedifard, "Junction temperature estimation of SiC MOSFETs based on extended Kalman filtering," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1687–1694.

[180] S. Dusmez, M. Heydarzadeh, M. Nourani, and B. Akin, "Remaining useful lifetime estimation for power MOSFETs under thermal stress with RANSAC outlier removal," *IEEE Trans. Ind. Informat.*, vol. 13, no. 3, pp. 1271–1279, Jun. 2017.

[181] M. Bossy *et al.*, "Monte Carlo methods for linear and non-linear Poisson-Boltzmann equation," *ESAIM Proc. Surv.*, vol. 48, pp. 420–446, 2015.

[182] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of IGBTs in a PV inverter under a long-term operation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7171–7182, Oct. 2016.

[183] F. Chiacchio, L. Compagno, D. D'Urso, G. Manno, and N. Trapani, "An open-source application to model and solve dynamic fault tree of real industrial systems," in *Proc. 5th Int. Conf. Softw., Knowl. Inf., Ind. Manage. Appl.*, 2011, pp. 1–8.

[184] M. A. Miner, "Cumulative damage in fatigue," *J. Appl. Mech.*, vol. 3, pp. A159–A164, 1945.

[185] A. Fatemi and L. Yang, "Cumulative fatigue damage and life prediction theories: A survey of the state-of-the-art for homogeneous materials," *Int. J. Fatigue*, vol. 20, no. 1, pp. 9–34, 1998.

[186] S. S. Manson *et al.*, "Application of a double linear damage rule to cumulative fatigue," NASA, Cleveland, OH, USA, Tech. Note NASA TN D-3839, 1967.

[187] *Standard Practices for Cycle Counting in Fatigue Analysis*, ASTM E1049-85, pp. 1–10, 2011.

[188] K. Mainka, M. Thoben, and O. Schilling, "Lifetime calculation for power modules, application and theory of models and counting methods," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–8.

[189] S. D. Downing and D. F. Socie, "Simple rainflow counting algorithms," *Int. J. Fatigue*, vol. 4, no. 1, pp. 31–40, Jan. 1982.

[190] I. Rychlik, "A new definition of the rainflow cycle counting method," *Int. J. Fatigue*, vol. 9, no. 2, pp. 119–121, 1987.

[191] L. R. GopiReddy, L. M. Tolbert, B. Ozpineci, and J. O. P. Pinto, "Rainflow algorithm-based lifetime estimation of power semiconductors in utility applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3368–3375, Jul./Aug. 2015.

[192] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 590–602, Feb. 2015.

[193] M. Musallam and C. M. Johnson, "An efficient implementation of the rainflow counting algorithm for life consumption estimation," *IEEE Trans. Rel.*, vol. 61, no. 4, pp. 978–986, Dec. 2012.

[194] H. Gao, H. Z. Huang, S. P. Zhu, Y. F. Li, and R. Yuan, "A modified nonlinear damage accumulation model for fatigue life prediction considering load interaction effects," *Sci. World J.*, vol. 2014, pp. 1–7, 2014.

[195] H. Huang, "Lifetime prediction for power converters," Ph.D. dissertation, Sch. Eng., Univ. Warwick, Coventry, U.K., p. 147, 2012.

[196] N. Sintamarean, F. Blaabjerg, H. Wang, F. Iannuzzo, and P. D. P. Rimmen, "Reliability oriented design tool for the new generation of grid connected PV-inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2635–2644, May 2015.

[197] Reliasoft, "System analysis reference: Reliability, availability and optimization," p. 281, 2015. [Online]. Available: http://reliawiki.org/index.php/System_Analysis_Reference

[198] X. Qu, Q. Liu, H. Wang, and F. Blaabjerg, "System-level lifetime prediction for LED lighting applications considering thermal coupling between LED sources and drivers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1860–1870, Dec. 2018.

[199] V. Raveendran, M. Andresen, and M. Liserre, "Improving onboard converter reliability for more electric aircraft with lifetime-based control," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5787–5796, Jul. 2019.

[200] H. Li, D. Wen, Z. Lu, Y. Wang, and F. Deng, "Identifying the probability distribution of fatigue life using the maximum entropy principle," *Entropy*, vol. 18, no. 4, Apr. 2016, Art. no. 111.

[201] X. Yu and A. M. Khambadkone, "Reliability analysis and cost optimization of parallel-inverter system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3881–3889, Oct. 2012.

[202] W. Ahmed, O. Hasan, U. Pervez, and J. Qadir, "Reliability modeling and analysis of communication networks," *J. Netw. Comput. Appl.*, vol. 78, pp. 191–215, Jan. 2017.

[203] B. E. Goldberg, K. Everhart, R. Stevens, N. Babbitt, III, P. Clemens, and L. Stout, "System engineering 'toolbox' for design-oriented engineers," NASA Marshall Space Flight Center, Huntsville, AL, USA, 1994.

[204] M. S. Nasrin, F. H. Khan, and M. K. Alam, "Quantifying device degradation in live power converters using SSTDR assisted impedance matrix," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3116–3131, Jun. 2014.

[205] M. K. Alam and F. H. Khan, "Reliability analysis and performance degradation of a boost converter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3986–3994, Nov. 2014.

[206] L. Placca and R. Kouta, "Fault tree analysis for PEM fuel cell degradation process modelling," *Int. J. Hydrogen Energy*, vol. 36, no. 19, pp. 12393–12405, Sep. 2011.

[207] *Reliability Prediction of Electronic Equipment*, MIL-HDBK-217F, Department of Defense of the USA, pp. 1–205, 1991.

[208] W. Ying, K. Jinsong, Z. Ye, J. Shiyi, and H. Dabing, "Study of reliability and accelerated life test of electric drive system," in *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, 2009, pp. 1060–1064.

[209] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013.

[210] P. O. Chelson, "Reliability computation using fault tree analysis," NASA Jet Propulsion Lab., California Inst. Technol., Pasadena, CA, USA, Tech. Rep. 32-1542, 1971.

[211] J. B. Dugan, S. J. Bavuso, and M. A. Boyd, "Dynamic fault-tree models for fault-tolerant computer systems," *IEEE Trans. Rel.*, vol. 41, no. 3, pp. 363–377, Sep. 1992.

[212] D. Marquez, M. Neil, and N. Fenton, "Solving dynamic fault trees using a new hybrid Bayesian network inference algorithm," in *Proc. Mediterranean Conf. Control Autom. Conf.*, 2008, pp. 609–614.

[213] S. Kabir, M. Walker, and Y. Papadopoulos, "Reliability analysis of dynamic systems by translating temporal fault trees into Bayesian networks," in *Proc. 4th Int. Symp.*, 2014, pp. 96–109.

[214] E. Ruijters and M. Stoelinga, "Fault tree analysis: A survey of the state-of-the-art in modeling, analysis and tools," *Comput. Sci. Rev.*, vol. 15, pp. 29–62, 2015.

[215] T. Matsuoka and M. Kobayashi, "GO-FLOW: A new reliability analysis methodology," *Nucl. Sci. Eng.*, vol. 98, no. 1, pp. 64–78, 1988.

[216] Y. Ren *et al.*, "System dynamic behavior modeling based on extended GO methodology," *IEEE Access*, vol. 6, pp. 22513–22523, 2018.

[217] J. G. T. Toledano and L. E. S. Succar, "Bayesian networks for reliability analysis of complex systems," in *Proc. Prog. Artif. Intell.*, 1998, pp. 195–206.

[218] P. Weber, G. Medina-Oliva, C. Simon, and B. Iung, "Overview on Bayesian networks applications for dependability, risk analysis and maintenance areas," *Eng. Appl. Artif. Intell.*, vol. 25, no. 4, pp. 671–682, 2012.

[219] A. Bobbio, L. Portinale, M. Minichino, and E. Ciancamerla, "Improving the analysis of dependable systems by mapping fault trees into Bayesian networks," *Rel. Eng. Syst. Saf.*, vol. 71, no. 3, pp. 249–260, 2001.

[220] S. Russell and P. Norvig, "Probabilistic reasoning over time, section 15.5 dynamic Bayesian network," in *Artificial Intelligence: A Modern Approach*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2009, ch. 15, p. 566.

[221] U. N. Lerner, "Hybrid Bayesian networks for reasoning about complex systems," Ph.D. dissertation, Dept. Comput. Sci., , Stanford Univ., Stanford, CA, USA, pp. 173–175, 2002.

[222] D. Cao, S. Kan, and Y. Sun, "Design of reliable system based on dynamic Bayesian networks and genetic algorithm," in *Proc. Annu. Rel. Maintainability Symp.*, 2012, pp. 1–6.

[223] H. Boudali and J. B. Dugan, "A discrete-time Bayesian network reliability modeling and analysis framework," *Rel. Eng. Syst. Saf.*, vol. 87, no. 3, pp. 337–349, Mar. 2005.

[224] H. Boudali and J. B. Dugan, "A continuous-time Bayesian network reliability modeling, and analysis framework," *IEEE Trans. Rel.*, vol. 55, no. 1, pp. 86–97, Mar. 2006.

[225] H. Boudali and J. B. Dugan, "A new Bayesian network approach to solve dynamic fault trees," in *Proc. Annu. Rel. Maintainability Symp.*, 2005, pp. 451–456.

[226] A. M. Bazzi, A. Dominguez-Garcia, and P. T. Krein, "Markov reliability modeling for induction motor drives under field-oriented control," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 534–546, Feb. 2012.

[227] G. R. Chandra Mouli, J. Schijffelen, M. Van Den Heuvel, M. Kardolus, and P. Bauer, "A 10 kW solar-powered bidirectional EV charger compatible with Chademo and COMBO," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1082–1098, Feb. 2019.

[228] Y. Liu, Y. Xu, and Y. Liu, "Reliability modeling analysis of a power module," in *Proc. 14th Int. Conf. Thermal, Mech. Multi-Phys. Simul. Experiments Microelectron. Microsyst., EuroSimE*, 2013, pp. 1–11.

[229] K. J. Sullivan, J. B. Dugan, and D. Coppit, "The Galileo fault tree analysis tool," in *Proc. 29th Annu. Int. Symp. Fault-Tolerant Comput.*, 2003, pp. 232–235.

[230] R. A. Sahner, K. S. Trivedi, and A. Puliafito, "Part II: Modeling examples," in *Performance and Reliability Analysis of Computer Systems: An Example-Based Approach Using the SHARPE Software Package*, 1st ed., New York, NY, USA: Springer, 1996, p. 152.

[231] F. Arnold, A. F. E. Belinfante, F. I. Van der Berg, D. Guck, and M. I. A. Stoelinga, "DFTCalc: A tool for efficient fault tree analysis," in *Proc. 32nd Int. Conf. Comput. Saf., Rel. Secur.*, 2013.

[232] Isograph, "Isograph reliability and availability software." 1986. [Online]. Available: https://www.isograph.com/software/

[233] Reliass, "RAM commander." 2015. [Online]. Available: http://www.reliability-safety-software.com/products/ram-commander/

[234] HBM Prenscia Inc., "ReliaSoft reliability analysis software." 2020. [Online]. Available: https://www.reliasoft.com/products/reliability-analysis

[235] Crimson Quality LLC, "Windchill RBD (formerly Relex OpSim) Software." 2020. [Online]. Available: http://www.crimsonquality.com/products/rbd/

[236] ALD (Advanced Logistics Development) Reliability Engineering, Ltd., "ALD fault tree analyzer." 1984. [Online]. Available: https://www.fault-tree-analysis-software.com/

[237] ITEM Software, "ITEM ToolKit (A reliability analysis software)." 2000. [Online]. Available: https://www.itemsoft.com/item_toolkit.html

[238] N. Fenton and M. Neil, "Decision analysis, decision trees, value of information analysis, and sensitivity analysis," in *Risk Assessment and Decision Analysis with Bayesian Networks*, 2nd ed., Boca Raton, FL, USA: Chapman and Hall/CRC, 2018, ch. 11, pp. 347–369.

[239] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, May 2015.

[240] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, "Condition monitoring: A decade of proposed techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 4, pp. 22–36, Dec. 2015.

[241] A. M. Imam, "Condition monitoring of electrolytic capacitors for power electronics applications," Ph.D. dissertation, Sch. Elect. Comput. Eng., Georgia Inst. Technol., Atlanta, GA, USA,2007.

[242] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.

[243] M. Berthou, P. Godignon, and J. Millan, "Monolithically integrated temperature sensor in silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4970–4977, Sep. 2014.

[244] W. Kester, J. Bryant, and W. Jung, "Section 7: Temperature sensors," in *Practical Design Techniques for Sensor Signal Conditioning*. Norwood, MA, USA: Analog Devices. 1999, pp. 1–39.

[245] F. Stella, G. Pellegrino, E. Armando, and D. Dapra, "On-line junction temperature estimation of SiC power MOSFETs through on-state voltage mapping," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3453–3462, Jul./Aug. 2018.

[246] L. Wei, J. McGuire, and R. A. Lukaszewski, "Analysis of PWM frequency control to improve the lifetime of PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 922–929, Mar./Apr. 2011.

[247] R. P. Stout, "Thermal RC ladder networks—Packaging technology development," On Semiconductor, Phoenix, AZ, USA, Application Note AND8221/D, pp. 1–4, 2006.

[248] L. Ceccarelli, A. S. Bahman, and F. Iannuzzo, "Impact of device aging in the compact electro-thermal modeling of SiC power MOSFETs," *Microelectron. Rel*, vol. 100–101, Sep. 2019, Art. no. 113336.

[249] R. Wu, H. Wang, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 2901–2908.

[250] S. Lineykin and S. Ben-yaakov, "Modeling and analysis of thermo-electric modules," *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 505–512, Mar./Apr. 2007.

[251] C. H. van der Broeck, R. D. Lorenz, and R. W. De Doncker, "Methods for monitoring 3-D temperature distributions in power electronic modules," in *Proc. Appl. Power Electron. Conf. Expo.*, 2018, pp. 3022–3030.

[252] A. S. Bahman, K. Ma, and F. Blaabjerg, "General 3D lumped thermal model with various boundary conditions for high power IGBT modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 261–268.

[253] L. Ceccarelli, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "A fast electro-thermal co-simulation modeling approach for SiC power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 966–973.

[254] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7183–7193, Oct. 2016.

[255] T. Kojima, Y. Yamada, Y. Nishibe, and K. Torii, "Novel RC compact thermal model of HV inverter module for electro-thermal coupling simulation," in *Proc. 4th Power Convers. Conf.*, 2007, pp. 1025–1029.

[256] A. S. Bahman, K. Ma, and F. Blaabjerg, "A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018.

[257] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A 3-D-lumped thermal network model for long-term load profiles analysis in high-power IGBT modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1050–1063, Sep. 2016.

[258] K. B. Pedersen and K. Pedersen, "Dynamic modeling method of electro-thermo-mechanical degradation in IGBT modules," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 975–986, Feb. 2016.

[259] M. Ciappa, F. Carbognani, and W. Fichtner, "Lifetime modeling of thermomechanics-related failure mechanisms in high power IGBT modules for traction applications," in *Proc. IEEE 15th Int. Symp. Power Semicond. Devices ICs*, 2003, pp. 295–298.

[260] Z. Wang, B. Tian, W. Qiao, and L. Qu, "Real-time aging monitoring for IGBT modules using case temperature," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 1168–1178, Feb. 2016.

[261] D. L. Blackburn, "Temperature measurements of semiconductor devices—A review," in *Proc. 20th Annu. IEEE Semicond. Thermal Meas. Manage. Symp.*, 2004, pp. 70–80.

[262] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[263] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 17–27, Sep. 2014.

[264] H. Niu and R. D. Lorenz, "Evaluating different implementations of online junction temperature sensing for switching power semiconductors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 5696–5703.

[265] F. Gonzalez-Hernando, J. San-Sebastian, M. Arias, A. Rujas, and F. Iannuzzo, "Discontinuous PWM for online condition monitoring of SiC power modules," *IEEE J. Emerg. Sel. Top. Power Electron.*, to be published, doi:10.1109/JESTPE.2019.2950405.

[266] Y. Zhang and Y. C. Liang, "A simple approach on junction temperature estimation for SiC MOSFET dynamic operations within safe operating area," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 5704–5707.

[267] S. Jahdi, O. Alatise, P. Alexakis, L. Ran, and P. Mawby, "The impact of temperature and switching rate on the dynamic characteristics of silicon carbide Schottky barrier diodes and MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 163–171, Jan. 2015.

[268] S. Ji, S. Zheng, Z. Zhang, F. Wang, and L. M. Tolbert, "Protection and temperature-dependent switching characterization of latest generation 10 kV SiC MOSFETs," in *Proc. Conf. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 783–788.

[269] Z. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, and B. J. Blalock, "Online junction temperature monitoring using turn-off delay time for silicon carbide power devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7.

[270] H. Niu and R. D. Lorenz, "Real-time junction temperature sensing for silicon carbide MOSFET with different gate drive topologies and different operating conditions," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3424–3440, Apr. 2018.

[271] H. Li, X. Liao, Y. Hu, Z. Huang, and K. Wang, "Analysis of voltage variation in silicon carbide MOSFETs during turn-on and turn-off," *Energies*, vol. 10, no. 10, pp. 1–19, Sep. 2017.

[272] V. K. Sundaramoorthy *et al.*, "A study on IGBT junction temperature (Tj) online estimation using gate-emitter voltage (Vge) at turn-off," *Microelectron. Rel.*, vol. 54, no. 11, pp. 2423–2431, 2014.

[273] X. Liao, H. Li, Y. Hu, Z. Huang, E. Song, and H. Xiao, "Analysis of SiC MOSFET dI/dt and its temperature dependence," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 864–869.

[274] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1478–1483.

[275] J. O. Gonzalez, "Impact of the gate oxide reliability of SiC MOSFETs on the junction temperature estimation using temperature sensitive electrical parameters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 837–844.

[276] J. O. Gonzalez and O. Alatise, “Challenges of junction temperature sensing in SiC power MOSFETs,” in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 891–898.

[277] F. Yang, E. Ugur, and B. Akin, “Evaluation of aging's effect on temperature sensitive electrical parameters in SiC MOSFETs,” *IEEE Trans. Power Electron.*, to be published, doi:10.1109/TPEL.2019.2950311.

[278] H. C. Yang, R. Simanjorang, and K. Y. See, “A method for junction temperature estimation utilizing turn-on saturation current for SiC MOSFET,” in *Proc. Int. Power Electron. Conf.*, 2018, pp. 2296–2300.

[279] N. Stojadinović *et al.*, “Impact of negative bias temperature instabilities on lifetime in p-channel power VDMOSFETs,” in *Proc. 8th Int. Conf. Telecommun. Modern Satellite, Cable, Broadcasting Services*, 2007, pp. 275–282.

[280] “Stress test qualification for automotive grade discrete semiconductors,” Automot. Electron. Council, New York, NY, USA, AEC-Q101-Rev-C, 2005.

[281] H. Luo, F. Iannuzzo, and M. Turnaturi, “Role of threshold voltage shift in highly accelerated power cycling tests for SiC MOSFET modules,” *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi:10.1109/JESTPE.2019.2894717.

[282] F. Richardeau, F. Boige, and S. Lefebvre, “Gate leakage-current, damaged gate and open-circuit failure-mode of recent SiC power MOSFET : Overview and analysis of unique properties for converter protection and possible future safety management,” in *Proc. IEEE Int. Conf. Elect. Syst. Aircraft, Railway, Ship Propulsion Road Veh. Int. Transp. Electrific. Conf.*, 2018, pp. 1–6.

[283] Y. Zhou, T. Yang, H. Liu, and B. Wang, “Failure models and comparison on short-circuit performances for SiC JFET and SiC MOSFET,” in *Proc. 1st Workshop Wide Bandgap Power Devices Appl. Asia*, 2018, pp. 123–129.

[284] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, “The impact of gate-induced drain leakage current on MOSFET scaling,” in *Proc. Int. Electron Devices Meeting*, 1987, pp. 718–721.

[285] S. Pu, E. Ugur, F. Yang, G. Wang, and B. Akin, “In-situ degradation monitoring of SiC MOSFET based on switching transient measurement,” *IEEE Trans. Ind. Electron.*, to be published, doi:10.1109/TIE.2019.2924600.

[286] A. Hanif and F. Khan, “Degradation detection of thermally aged SiC and Si power MOSFETs using spread spectrum time domain reflectometry (SSTDR),” in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 18–23.

[287] R. German, P. Venet, A. Sari, O. Briat, and J. M. Vinassa, “Improved supercapacitor floating ageing interpretation through multipore impedance model parameters evolution,” *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3669–3678, Jul. 2014.

[288] M. Makdessi, A. Sari, and P. Venet, “Health monitoring of DC link capacitors,” *Chem. Eng. Trans.*, vol. 33, pp. 1105–1110, 2013.

[289] F. Erturk, E. Ugur, J. Olson, and B. Akin, “Real-time aging detection of SiC MOSFETs,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 600–609, Jan./Feb. 2019.

[290] Z. Zhang *et al.*, “Online junction temperature monitoring using intelligent gate drive for SiC power devices,” *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7922–7932, Aug. 2019.

[291] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, “Temperature-dependent characterization, modeling and switching speed limitation analysis of latest generation 10 kV SiC MOSFET,” *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4317–4327, May 2018.

[292] J. H. Dyer, “Online switching time monitoring of SiC devices using intelligent gate driver for converter performance improvement,” Master of Science thesis, Dept. Elect. Eng. Comput. Sci., Univ. Tennessee, Knoxville, TN, USA, p. 46, 2018.

[293] S. Pu, F. Yang, E. Ugur, B. T. Vankayalapati, C. Xu, and B. Akin, “Onboard SiC MOSFET degradation monitoring through readily available inverter current/voltage sensors,” in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2019, pp. 1–5.

[294] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, “Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges,” *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018.

[295] J. Falck, G. Buticchi, and M. Liserre, “Thermal stress based model predictive control of electric drives,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1513–1522, Mar. 2017.

[296] L. Wu and A. Castellazzi, “Temperature adaptive driving of power semiconductor devices,” in *Proc. IEEE Int. Symp. Ind. Electron.*, 2010, pp. 1110–1114.

[297] P. K. Prasobhu, V. Raveendran, G. Buticchi, and M. Liserre, “Active thermal control of a DC / DC GaN-based converter,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1146–1152.

[298] H. Luo, F. Iannuzzo, K. Ma, F. Blaabjerg, W. Li, and X. He, “Active gate driving method for reliability improvement of IGBTs via junction temperature swing reduction,” in *Proc. IEEE 7th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2016, pp. 1–7.

[299] J. Falck, M. Andresen, and M. Liserre, “Active thermal control of IGBT power electronic converters,” in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc.*, 2015, pp. 1–6.

[300] M. Andresen, G. Buticchi, J. Falck, and M. Liserre, “Active thermal management for a single-phase H-bridge inverter employing switching frequency control,” in *Proc. PCIM Eur.; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy, Energy Manage.*, 2015, pp. 1–8.

[301] A. Castellazzi, M. Onifade, X. Wang, and P. Zanchetta, “State-space modeling of power assemblies for advanced thermal management solutions,” in *Proc. IEEE 13th Workshop Control Model. Power Electron.*, 2012, pp. 1–8.

[302] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, “Thermally compensated discontinuous modulation strategy for cascaded H-bridge converters,” *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2704–2713, Mar. 2018.

[303] M. Aly, E. M. Ahmed, and M. Shoyama, “Thermal stresses relief carrier-based PWM strategy for single phase multilevel inverters,” *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9376–9388, Dec. 2017.

[304] S. Dusmez and B. Akin, “An active life extension strategy for thermally aged power switches based on the pulse-width adjustment method in interleaved converters,” *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5149–5160, Jul. 2016.

[305] T. M. Phan, N. Oikonomou, G. J. Riedel, and M. Pacas, “PWM for active thermal protection in three level neutral point clamped inverters,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 3710–3716.

[306] M. Andresen, G. Buticchi, and M. Liserre, “Active thermal control of isolated soft switching DC / DC converters,” in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 6818–6823.

[307] B. Wang, L. Zhou, Y. Zhang, K. Wang, X. Du, and P. Sun, “Active junction temperature control of IGBT based on adjusting the turn-off trajectory,” *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5811–5823, Jul. 2018.

[308] V. Blasko, R. Lukaszewski, and R. Sladky, “On line thermal model and thermal management strategy of a three phase voltage source inverter,” in *Proc. Ind. Appl. Conf. 34th IAS Annu. Meet. Conf. Rec. IEEE*, 1999, vol. 2, pp. 1423–1431.

[309] D. A. Murdock, J. E. R. Torres, J. J. Connors, and R. D. Lorenz, “Active thermal control of power electronic modules,” *Ind. Appl. IEEE Trans.*, vol. 42, no. 2, pp. 552–558, Mar./Apr. 2006.

[310] T. A. Polom, B. Wang, and R. D. Lorenz, “Control of junction temperature and its rate of change at thermal boundaries via precise loss manipulation,” *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4796–4806, Sep. 2017.

[311] J. Lemmens, P. Vanassche, and J. Driesen, “Optimal control of traction motor drives under electrothermal constraints,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 2, pp. 249–263, Jun. 2014.

[312] K. Ma, M. Liserre, and F. Blaabjerg, “Reactive power influence on the thermal cycling of multi-MW wind power inverter,” *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 922–930, Mar./Apr. 2013.

[313] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, “Active gate control in half-bridge inverters using programmable gate driver ICs to improve both surge voltage and switching loss,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1153–1159.

[314] I. Vernica, F. Blaabjerg, and K. Ma, “Modelling and design of active thermal controls for power electronics of motor drive applications,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2902–2909.

[315] Y. Yang, E. Koutroulis, A. Sangwongwanich, and F. Blaabjerg, “Minimizing the levelized cost of energy in single-phase photovoltaic systems with an absolute active power control,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 28–34.

[316] A. Sangwongwanich, Y. Yang, D. Sera, and F. Blaabjerg, “Lifetime evaluation of grid-connected PV inverters considering panel degradation rates and installation sites,” *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1125–1236, Feb. 2018.

[317] Y. Ko, M. Andresen, G. Buticchi, J. Lee, and M. Liserre, "Modulation strategy for highly reliable cascade H-bridge inverter based on discontinuous PWM," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 3241–3246.

[318] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal analysis and balancing for modular multilevel converters in HVDC applications," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1985–1996, Mar. 2018.

[319] J. Gon, "Thermal regulation and balancing in modular multilevel converters," Ph.D. dissertation, Sch. Eng., Cardiff Univ., Cardiff, U.K., p. 121, 2018.

[320] S. Dusmez, E. Ugur, and B. Akin, "Power switch lifetime extension strategies for three-phase converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1176–1182.

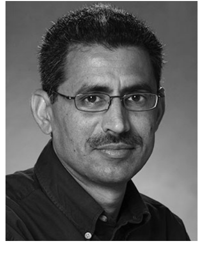
[321] M. N. Marwali, J.-W. Jung, and A. Keyhani, "Control of distributed generation systems—Part II: Load sharing control," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1551–1561, Nov. 2004.

Ze Ni (Student Member, IEEE) received the B.S. degree in electrical engineering from the Hubei University of Technology, Wuhan, China, in 2010, and the M.S. degree in electrical engineering from the Harbin Institute of Technology, Shenzhen, China, in 2013. He is currently working toward the Ph.D. degree with North Dakota State University, Fargo, ND, USA.

From 2013 to 2015, he worked on 10-kV static synchronous compensator in Shenzhen. He is currently with Oak Ridge National Laboratory, Oak Ridge, TN, USA, as a Research Intern. His research interests include wide-bandgap device reliability and applications, switched-capacitor resonant converter and multilevel inverters.

Xiaofeng Lyu (Member, IEEE) received the B.S. degree from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2010, the M.S. degree in power electronics from Zhejiang University, Hangzhou, China, in 2013, and the Ph.D. degree from North Dakota State University, Fargo, ND, USA, in 2017.

He was with General Electric Shanghai, Joulwatt Hangzhou, and John Deere Electronic Solutions, Fargo. He is currently a Staff Applications Engineer with Navitas Semiconductor, Inc., Los Angeles, CA, USA. His research interests include SiC high-density inverters, grid-tied control, LED drivers, multilevel converters, data center switched tank converters, and GaN-based chargers.



Om Prakash Yadav received the B.S. degree in mechanical engineering from the Malaviya National Institute of Technology, Jaipur, India, the M.S. degree in industrial engineering from the National Institute of Industrial Engineering, Mumbai, India, and the Ph.D. degree in industrial engineering from Wayne State University, Detroit, MI, USA, in 1987, 1992, and 2002, respectively.

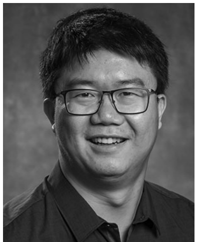
He is currently a Professor and a Duin Endowed Fellow with the Department of Industrial and Manufacturing Engineering, North Dakota State University, Fargo, ND, USA. The research work of his group has been published in *Reliability Engineering and Systems Safety*, *Journal of Risk and Reliability*, *Quality and Reliability Engineering International*, *International Journal of Production Research*, *Engineering Management Journal*, and IEEE TRANSACTION OF SYSTEMS, MAN, AND CYBERNETICS: SYSTEMS. He has authored/coauthored more than 120 research papers in the area of reliability, risk assessment, design optimization, and operations management. His research interests include reliability modeling and analysis, risk assessment, design optimization and robust design, and manufacturing systems analysis.

Dr. Yadav is currently an Associate Editor for the *International Journal of Reliability and Safety* and on the Editorial Board of several international journals. He is a recipient of the IISE William A.J. Golomski Best Paper Awards in 2015 and 2018. He is currently a member of IISE, ASQ, SRE, and INFORMS.

Brij N. Singh (Senior Member, IEEE) received the B.E. degree in electrical engineering from the Madan Mohan Malviya University of Technology, Gorakhpur, India, in 1989, the M.E. degree in electrical engineering from the Indian Institute of Technology, Roorkee, India, in 1991, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, New Delhi, India, in 1996.

He is currently a Senior Staff Engineer with John Deere, Inc., Moline, IL, USA, and leading the US Department of Energy—PowerAmerica (DOE-PowerAmerica) funded project to develop a 200-kW SiC inverter for heavy-duty vehicle applications. In 1996, he joined the École de Technologie Supérieure, Université du Québec, Montreal, QC, Canada, as a Postdoctoral Fellow. In 1999, he joined Concordia University, Montreal, as a Research Fellow. In 2000, he joined the Department of Electrical Engineering and Computer Science, Tulane University, New Orleans, LA, USA, as an Assistant Professor. In 2007, he joined John Deere, Inc., Fargo, ND, as a Power Electronics Staff Engineer. He published over 90 research papers in various Journals including IEEE Transactions and IET Journals. He also holds 26 U.S. patents, one trade secret, and numerous pending patents.

Dr. Brij is a recipient of the numerous teaching awards for outstanding instructions in electrical engineering in Tulane, and for product and technology innovations and team collaboration activities in John Deere.



Sheng Zheng (Senior Member, IEEE) was born in Hangzhou, China, in 1985. He received the B.E. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2007 and 2013, respectively.

From 2013 to 2017, he was a Postdoctoral Research Associate with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN, USA. In 2017, he joined the Power Electronics and Electric Machine Group, Oak Ridge National Laboratory, Oak Ridge, TN, USA. He is currently the R&D Staff Member with Electric Energy Systems Integration Group, Oak Ridge National Laboratory. His current research interests include high-voltage widebandgap semiconductors and its application, gate driver technology and design, high-power interfacing converters for FACT devices, renewable generation systems and microgrids, and hardware-in-the-loop real-time tests.

Dong Cao (Member, IEEE) received the B.S. degree from Zhejiang University, Hangzhou China, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Michigan State University, East Lansing, MI, USA, in 2010 and 2012, respectively.

He was with Ford Motor Company as a Core Power Electronics Engineer for hybrid electric vehicle electrified driveline hardware development from 2012 to 2014. He was an Assistant Professor with North Dakota State University from 2014 to 2019. He joined the University of Dayton, where he has been a GE EPISCenter Professor and Associate Professor since August 2019. His research interests include high power or high-frequency wide bandgap devices i.e., SiC or GaN smart gate drive and their applications; high density and high efficiency power conversion for data center, LED driving, electric grid, solar farm, electric vehicle, and electrified airplane applications; health monitoring; and lifetime prediction of power converters using artificial intelligence.

Dr. Cao is a recipient of Early Career Researcher of the Year Award from North Dakota State University in 2019. He was also the recipient of three prize paper awards from IEEE and a couple of presentation and poster awards from IEEE conferences. He is an Associate Editor and Guest Editor for several IEEE journals and transactions.