Modeling and Validation of Common-Mode Emissions in Wide Bandgap-Based Converter Structures

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***Abstract*—Modern power converters designed with wide bandgap (WBG) semiconductors are known to generate substantial conducted electromagnetic interference (EMI) as a side effect of high-edge-rate and high-frequency switching. This article provides a consolidated treatment of an approach to the derivation of common-mode equivalent models that are useful for analyzing this increased EMI signature. Also included is a step-by-step demonstration of this approach applied to a prototype converter that exemplifies many practical power electronic applications. For empirical validation of the developed model, this converter is operated within a custom-designed EMI characterization testbed that is similar to the setup specified by MIL-STD-461 CE-102. Good agreement is achieved between analytical predictions and empirical results in both the time domain and the frequency domain. Spectral comparisons are shown to be especially accurate in the frequency range between 10 kHz and 30 MHz, which is the principal range of interest for controlling conducted emissions in WBG-based systems. In order to achieve the demonstrated model agreement, a set of parasitic parameter values were obtained through impedance characterization of the system under study. Identification of the critical parasitic elements that must be quantified to achieve good predictive capability for the presented model represents one of the specific contributions of this article.**

***Index Terms*—Electromagnetic interference (EMI), equivalent circuits, power semiconductor devices, packaging, power electronics.**

I. Introduction

CONTINUED progress in the maturation of wide bandgap (WBG) semiconductors presents new opportunities for improving the efficiency and power density of power electronic systems. However, such systems are known to generate increased electromagnetic interference (EMI) compared to traditional silicon-based systems [1]–[3]. It can be shown that this increased EMI signature is linked to three contemporary trends in power electronics, as illustrated in Fig. 1. This plot represents the spectral envelope of the common-mode (CM) voltage generated by a notional single-phase inverter as a function of bus voltage ($V_{\rm dc}$), switching frequency ($f_{\rm sw}$), and switching transition rates ($\mathrm{d}v/\mathrm{d}t$). Increasing the dc bus voltage applies a magnitude scaling factor to the CM voltage envelope; increasing the operating frequency and switching transition rates expand the spectral envelope by increasing the break frequencies of the 20 dB/decade and 40 dB/decade envelope asymptotes, respectively. Collectively, these trends exacerbate the burden on the EMI management components in WBG-based systems compared to silicon-based systems.

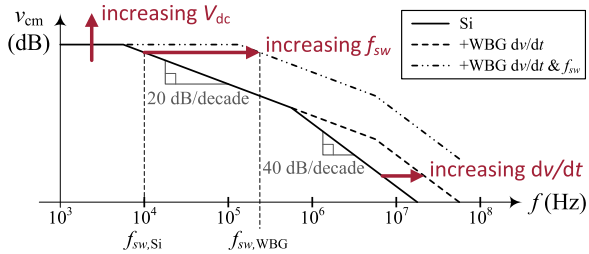

Fig. 1. Impact of trends in power electronics on CM-source spectral envelopes.

In light of the emphasis on power density that is driving much of the contemporary WBG technology adoption, the trends shown in Fig. 1 are practical rather than theoretical. Designers are pursuing WBG system configurations that require aggressive switching frequencies along with commensurate switching transition rates to achieve density targets while maintaining acceptable efficiency. In this type of WBG system design, conducted emissions are of primary concern, particularly in the spectral range above $f_{\rm sw,WBG}$ in Fig. 1, which includes switching frequency content as well as the "extended dynamics" introduced by aggressively switching WBG semiconductors [4]. Both categories of spectral content fall within the conducted emission band, which may broadly be defined as 10 kHz–30 MHz. This band, therefore, defines the target range for modeling efforts seeking to provide predictive capabilities of conducted emissions for WBG-based systems.

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The system-level effects of this elevated EMI signature are not comprehensively understood at present, in spite of significant research efforts. The power-electronics literature contains numerous descriptions of models developed to aid in the understanding and prediction of conducted EMI. In general, these studies fall into one of two main categories. The first category is marked by the development of a detailed mixed-mode (MM) model for the converter topology in question [5]–[12], often with extensive characterization of parasitics in the semiconductor packaging, load, and ancillary structures. The resulting model is typically exercised in the time domain using circuit simulation software, and EMI performance metrics such as CM current magnitude or heat sink voltage are extracted and analyzed. The second category is characterized by the development of simplified or equivalent models of power electronic systems or filter components [13]–[20]. Some examples in this category treat the converter as a black box [13], [14]; others produce simplified MM models [15]–[17] or CM equivalent models (CEMs) [18]–[20] based on a detailed knowledge of the system configuration and dominant parasitics. Empirical validation or application of these modeling approaches usually includes the estimation of model parameter values using frequency-domain techniques.

One unifying theme that can be traced through both categories is the sensitivity of system EMI to the parasitics of discrete semiconductors and multichip power modules (MCPMs). MCPM parasitics are of particular interest herein. Much prior work has been done to characterize the impact of parasitic elements within MCPMs. Most of this research has focused on the presence of parasitic interconnect inductances within the module structure [21]–[24]. However, the baseplate capacitance (BPC) is also widely recognized as a parameter of sensitivity that affects system EMI and CM behavior in particular [11], [25], [26]. This insight has led to various recommendations for both module and application designers, such as reducing the overall BPC [6], [27]; minimizing the capacitive coupling of the output node in the phase leg [5], [28], [29]; balancing the capacitive coupling of the dc module terminals [5], [28], [29]; and ensuring symmetry of all dc-side impedances [30]. A detailed analysis and demonstration of the impact of the distribution of the BPC among the terminals of an MCPM is presented in [31] and [32].

An ongoing effort by the authors is the development of theoretical and empirical tools necessary for the evaluation and characterization of conducted emissions in converter systems based on WBG semiconductors [4], [33]. A key component in this tool set is a dedicated empirical test platform for full-scale power electronic systems. The testbed, shown in Fig. 2, is similar to the metrology setup called for by MIL-STD-461 CE-102 [4], [34]. This testbed employs line impedance stabilization networks (LISNs) on the input of the equipment under test (EUT). The output terminations in this system were chosen to mirror the impedance of the LISNs on the input. It is noted that these output terminations are not intended to serve as metrology elements. Rather, the terminations simply provide a reference impedance to the ground plane without excessive filtering of switching transients, as called for by [34]. The testbed provides a means to demonstrate and validate the rigorous development of CM models and ascertain which parasitic elements are most critical to CM emissions. As an example, the present article models and analyzes this testbed when configured with a single-phase ungrounded inverter as the EUT.

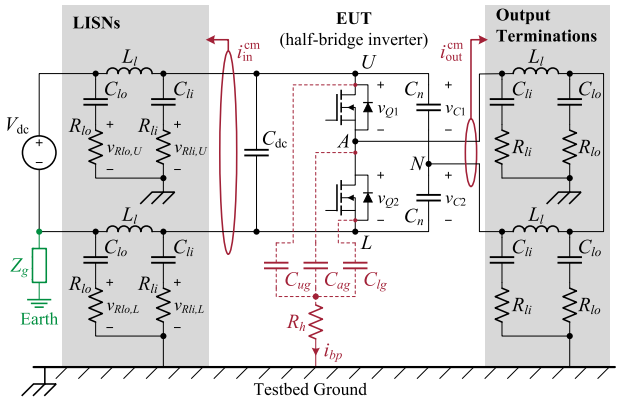

Fig. 2. EMI characterization testbed with half-bridge EUT.

The contributions of this work are as follows. First, this article provides a consolidated treatment of a rigorous approach to the derivation of CEMs, elements of which have been reported in [31] and [33]. Second, it provides a step-by-step demonstration of this approach applied to the analysis of a prototype converter that exemplifies many practical power electronic applications. Third, it provides a detailed characterization of the parasitic elements of the example system and identifies the subset of parasitics to which the CM emissions are most sensitive. Fourth, it provides a thorough empirical validation of the developed model in multiple configurations of the EUT, thereby increasing confidence in the modeling approach as well as delineating its challenges. In total, this article presents a self-contained demonstration and validation of the authors' technique for modeling and predicting conducted emissions in power electronic applications. This technique is based on straightforward circuit analysis methods, and can be effectively implemented with characterization data obtained from a commonly available impedance analyzer. The combined simplicity and accuracy of the proposed approach make it a useful tool for practicing engineers in the reduction of CM emissions during early-stage design of power electronic systems.

The outline of the article is as follows. In Section II, definitions and background on DM and CM decomposition are provided followed by details of the derivation and simulation of the CEM for the EMI characterization testbed. Section III provides details of the testbed's design, construction, and characterization. Section IV describes the procedure for accurate extraction of the BPC elements. In Section V, the developments of the prior sections are brought together to empirically validate the CEM of the testbed.

II. CM Modeling and Analysis

A. Background and Definitions

A systematic CM modeling approach was developed in [19] and [33] wherein CM voltage is defined with respect to an

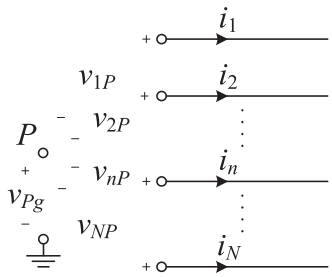

Fig. 3. Diagram for DM and CM definitions.

arbitrary reference that is distinct from ground. The floating reference facilitates the piecemeal transformation of MM system components into their respective CM equivalent representations. These can be subsequently assembled to form CEMs of arbitrarily large and complicated power electronic systems. Specifically, the definitions for CM voltage with respect to the arbitrary reference P and CM current for the set of N lines in Fig. 3 are

$$v_{\rm cm} \triangleq \frac{1}{N}\sum_{n=1}^{N} v_{nP} \tag{1}$$

$$i_{\rm cm} \triangleq \sum_{n=1}^{N} i_n. \tag{2}$$

DM voltage and current for any pair of the N lines in Fig. 3 are defined in a dual sense as

$$v_{mn} \triangleq v_{mP} - v_{nP} \tag{3}$$

$$i_{mn} \triangleq \tfrac{1}{2}(i_m - i_n). \tag{4}$$

The DM definitions play an important role in analyzing CM behavior in the presence of coupling between differential and common modes arising from parametric imbalances [7], [17], [30], [35], [36], also known as mode conversion. These definitions can be expressed generally as linear transformations from N MM quantities to $N-M$ differential modes and M common modes [33]

$$\mathbf{v}^{\rm dcm}_{1\ldots N} \triangleq \mathbf{T}^{v}_{N}\mathbf{v}_{nP} \tag{5}$$

$$\mathbf{i}^{\rm dcm}_{1\ldots N} \triangleq \mathbf{T}^{i}_{N}\mathbf{i}_{n} \tag{6}$$

where $\mathbf{v}_{nP}$ is the vector of MM line voltages, and $\mathbf{v}^{\rm dcm}_{1\ldots N}$ is the vector of DM and CM voltages and likewise for the current vectors. In the present article, decomposition of the differential and common modes will require only the 2×2 transforms, $\mathbf{T}^{v}_{2}$ and $\mathbf{T}^{i}_{2}$

$$\mathbf{T}^{v}_{2} = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{7}$$

$$\mathbf{T}^{i}_{2} = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 \end{bmatrix}. \tag{8}$$

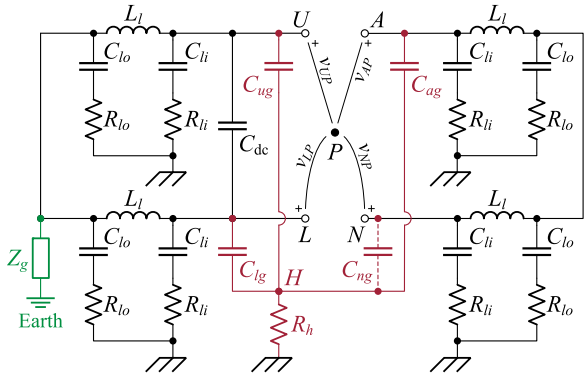

Fig. 4. Partitioning of MM model for equivalent circuit derivation.

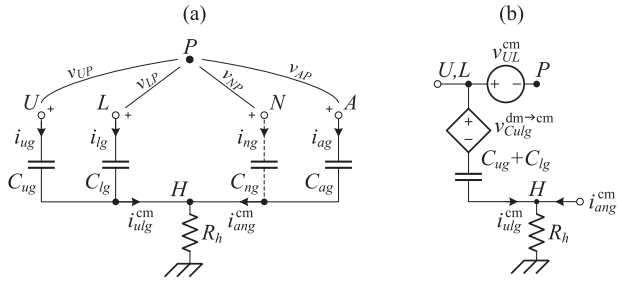

Fig. 5. (a) Module parasitics segregated to dc and ac sides of the converter, and (b) CM equivalent circuit of the dc-side parasitic capacitors.

B. Deriving the Nominal CEM of the EMI Testbed

The CEM of the EMI testbed in Fig. 2 may be determined in four steps, summarized as follows:

1) separating the system into ac and dc sections, as shown in Fig. 4;
2) expressing the line-to-ground voltages in terms of an arbitrary reference;
3) decomposing the voltage equations using (5) and (6); and
4) connecting the CEM components by specifying the reference P to be a convenient physical point.

In the nominal testbed of Fig. 2, the LISNs and output terminations are balanced, and therefore, the CM equivalent circuits of their respective sections can be determined by inspection through standard parallel combination rules as detailed in [33]. In contrast, the parasitic BPC is typically distributed unequally across the module terminals. Therefore, these elements require formal decomposition as detailed in the following paragraphs.

First, the system is separated into two sections, and the parasitic capacitors are segregated by virtue of their location on the ac or dc side of the converter. Specifically, C_{ug} and C_{lg} are shifted to the dc-side whereas C_{ag} is associated with the ac-side, as shown in Fig. 4. Therein, an additional fictitious capacitor C_{ng} is shown connecting the neutral point N to the module baseplate in order to reuse dc-side results for the ac-side parasitics. This capacitor will be set to zero after forming the CEM.

Second, the line-to-ground voltage equations of the dc-side capacitor branches shown isolated from the larger system in Fig. 5(a) are expressed with respect to the arbitrary reference

point P as

$$\begin{bmatrix} v_{UP} \\ v_{LP} \end{bmatrix} + \begin{bmatrix} v_{Pg} \\ v_{Pg} \end{bmatrix} = \begin{bmatrix} v_{Cug} \\ v_{Clg} \end{bmatrix} + R_h \begin{bmatrix} i_{ug} + i_{lg} + i_{ag} + i_{ng} \\ i_{ug} + i_{lg} + i_{ag} + i_{ng} \end{bmatrix}. \quad (9)$$

Henceforth, vector notation will be employed to express such equations more compactly, e.g.

$$\mathbf{v}_{ULP} + v_{Pg} \begin{bmatrix} 1 \\ 1 \end{bmatrix} = \mathbf{v}_{Culg} + \mathbf{R}_h(\mathbf{i}_{ulg} + \mathbf{i}_{ang}) \quad (10)$$

where $\mathbf{R}_h$ is the heat-sink resistance matrix given by

$$\mathbf{R}_h = R_h \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}. \quad (11)$$

It is noted that the heat sink could be represented as a more complex RLC network, but it is assumed to be purely resistive in the present derivation for simplicity without loss of generality. The capacitor voltages in (10) are in accordance with the constitutive equation

$$\mathbf{i}_{ulg} = \mathrm{p} \begin{bmatrix} C_{ug} & 0 \\ 0 & C_{lg} \end{bmatrix} \mathbf{v}_{Culg} \quad (12)$$

where p is the Heaviside operator $\mathrm{p} \triangleq \frac{\mathrm{d}}{\mathrm{dt}}$.

Third, one obtains the decomposed set of voltage equations by left-multiplying (10) by $\mathbf{T}_2^v$ and employing the substitutions $\mathbf{i}_{ulg} = (\mathbf{T}_2^i)^{-1}\mathbf{i}_{ulg}^{\mathrm{dcm}}$ and $\mathbf{i}_{ang} = (\mathbf{T}_2^i)^{-1}\mathbf{i}_{ang}^{\mathrm{dcm}}$

$$\mathbf{v}_{UL}^{\mathrm{dcm}} + \begin{bmatrix} 0 \\ v_{Pg} \end{bmatrix} = \mathbf{v}_{Culg}^{\mathrm{dcm}} + \mathbf{R}_h'(\mathbf{i}_{ulg}^{\mathrm{dcm}} + \mathbf{i}_{ang}^{\mathrm{dcm}}) \quad (13)$$

in which

$$\mathbf{R}_h' = \mathbf{T}_2^v \mathbf{R}_h (\mathbf{T}_2^i)^{-1} = R_h \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}. \quad (14)$$

It is observed in (13) and (14) that the CM-reference-to-ground voltage and heat-sink resistance appear only in the CM equation after decomposition.

In the interest of forming the CM model of the system of Fig. 2, the CM equation may be extracted from (13) and expressed in a scalar form as

$$v_{UL}^{\mathrm{cm}} + v_{Pg} = v_{Culg}^{\mathrm{cm}} + R_h \left(i_{ulg}^{\mathrm{cm}} + i_{ang}^{\mathrm{cm}}\right). \quad (15)$$

Of course, it remains to establish the CM voltage drop across the parasitic capacitors C_{ug} and C_{lg}. The voltage v_{Culg}^{cm} may be determined by decomposing the constitutive equation in (12) separately. Since (12) is a current equation, it is decomposed by left-multiplying by $\mathbf{T}_2^i$ and employing the substitutions $\mathbf{v}_{ulg} = (\mathbf{T}_2^v)^{-1}\mathbf{v}_{ulg}^{\mathrm{dcm}}$ yielding

$$\mathbf{i}_{ulg}^{\mathrm{dcm}} = \mathrm{p} \begin{bmatrix} \frac{C_{ug} + C_{lg}}{4} & \frac{C_{ug} - C_{lg}}{2} \\ \frac{C_{ug} - C_{lg}}{2} & C_{ug} + C_{lg} \end{bmatrix} \mathbf{v}_{Culg}^{\mathrm{dcm}}. \quad (16)$$

Equation (16) may be inverted to solve for v_{Culg}^{cm} (and v_{Culg}^{dm}) in terms of the DM and CM currents, i_{ulg}^{dm} and i_{ulg}^{cm}. However, it is often more insightful to express the CM voltage drop in terms of CM *current* and DM *voltage*. Therefore, the CM equation is simply extracted from (16) and solved for v_{Culg}^{cm}

$$v_{Culg}^{\mathrm{cm}} = -\frac{C_{ug} - C_{lg}}{C_{ug} + C_{lg}} \frac{v_{Culg}^{\mathrm{dm}}}{2} + \frac{1}{\mathrm{p}(C_{ug} + C_{lg})} i_{ulg}^{\mathrm{cm}}. \quad (17)$$

Two interesting features may be noted from the expression for the CM voltage across the dc-side parasitic capacitors in (17). First, the first term to the right of the equal sign indicates mode conversion from DM to CM proportional to the difference between C_{ug} and C_{lg}. It can be shown that this term is precisely equivalent to the mean of the series DM voltage drops across the two capacitors between the U and L nodes as determined by voltage division. Second, the last term in (17) indicates a CM capacitance that is the parallel combination of the two dc-side parasitic capacitors—i.e., $C_{ug} + C_{lg}$—in keeping with the balanced-parameter case. The developed approach, therefore, aligns with the intuition that CM current sees the two paths as a simple parallel combination regardless of symmetry.

The CM model for the dc-side parasitics is completed by substituting (17) into (15), yielding

$$v_{UL}^{\mathrm{cm}} + v_{Pg} = -\frac{C_{ug} - C_{lg}}{C_{ug} + C_{lg}} \frac{v_{Culg}^{\mathrm{dm}}}{2} + \frac{1}{\mathrm{p}(C_{ug} + C_{lg})} i_{ulg}^{\mathrm{cm}} + R_h(i_{ulg}^{\mathrm{cm}} + i_{ang}^{\mathrm{cm}}). \quad (18)$$

The equivalent circuit indicated by (18) is depicted in Fig. 5(b). Recall that in (18), v_{UL}^{cm} is determined by definition from (1) as

$$v_{UL}^{\mathrm{cm}} \triangleq \frac{1}{2}(v_{UP} + v_{LP}). \quad (19)$$

This voltage source will be fully specified upon selecting a convenient point for the CM reference P. Any other portion of the system connected in parallel with the parasitic capacitors at U and L (viz., the LISNs) will share an identical CM voltage definition, and, therefore, will connect to the parasitic capacitor CM equivalent circuit at the point designated U, L in Fig. 5(b).

The CM model for the ac-side parasitic capacitors is obtained using the same approach as demonstrated for the dc-side capacitors by replacing C_{ug} and C_{lg} with C_{ag} and C_{ng}, respectively. For the half-bridge inverter considered herein $C_{ng} = 0$. Therefore, the CM equation for the ac-side parasitics is given by

$$v_{AN}^{\mathrm{cm}} + v_{Pg} = -\frac{1}{2} v_{ang}^{\mathrm{dm}} + \frac{1}{\mathrm{p}C_{ag}} i_{ang}^{\mathrm{cm}} + R_h \left(i_{ulg}^{\mathrm{cm}} + i_{ang}^{\mathrm{cm}}\right). \quad (20)$$

Finally, the CM equivalent circuits of the LISNs, output terminations, and module parasitics on the ac and dc sides of the inverter implied by (18) and (20) are connected to produce the CEM of Fig. 6. Their connection is accomplished by specifying the CM reference P to be a convenient point with respect to both ac and dc sides of the inverter. For the half-bridge inverter, the phase terminal A is a suitable choice. For this designation, the

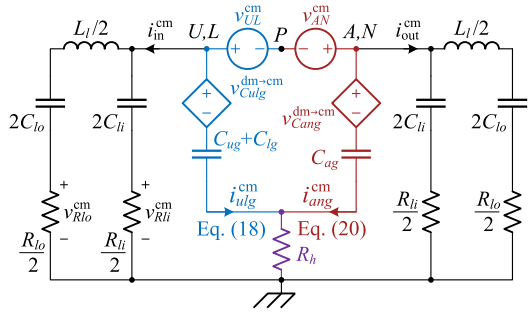

Fig. 6. Initial CEM of the EMI characterization testbed with half-bridge inverter EUT.

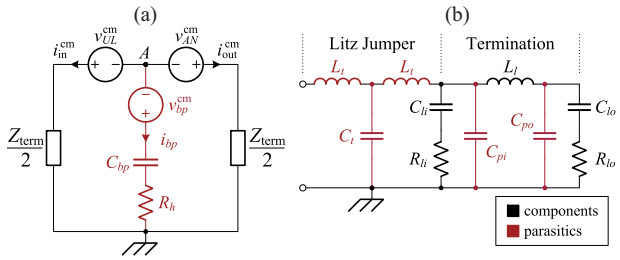

Fig. 7. (a) Final CEM employed for CM simulations, and (b) LISN model with interconnect parasitics included.

CM voltage sources in (18) and (20) are determined by definition from (1)

$$v_{UL}^{\text{cm}} \triangleq \frac{1}{2}(v_{UA} + v_{LA}) = \frac{1}{2}(v_{Q1} - v_{Q2}) \tag{21}$$

$$v_{AN}^{\text{cm}} \triangleq \frac{1}{2}(v_{AA} + v_{NA}) = -\frac{1}{2}v_{AN}. \tag{22}$$

Fortunately for analysis, v_{UL}^{cm} is solely a function of the switch voltages. The expression for v_{AN}^{cm}, however, includes the load voltage v_{AN} due to the neutral-forming capacitor bridge although this too is readily expressed in terms of switch voltages. Specifically, from inspection of Fig. 2, the voltage from A to N can be determined by

$$\begin{aligned} v_{AN} &= -v_{Q1} + v_{C1} \\ &= v_{Q2} - v_{C2} \\ &= -\frac{1}{2}(v_{Q1} - v_{Q2} - v_{C1} + v_{C2}). \end{aligned} \tag{23}$$

If the neutral-forming capacitor voltages are relatively constant, which is desirable in a half-bridge inverter, then v_{C1} and v_{C2} have little impact on leakage current through the baseplate and may be neglected. Substituting (23) into (22) and employing this approximation, the ac-side CM voltage source is given by

$$v_{AN}^{\text{cm}} \approx \frac{1}{4}(v_{Q1} - v_{Q2}). \tag{24}$$

The mode-conversion sources in the module parasitic branches in Fig. 6—resulting from the unequal capacitors forming leakage paths on both the dc and ac sides of the converter—are provided by (18) and (20). Since the dc- and ac-side parasitic capacitors span the dc bus and load, respectively, v_{Culg}^{dm} and v_{Cang}^{dm} in (18) and (20) are equivalent to the dc bus and load voltages, respectively. Therefore, the mode-conversion sources in Fig. 6 may be approximated as

$$v_{Culg}^{\text{dm}\to\text{cm}} \approx -\frac{C_{ug} - C_{lg}}{C_{ug} + C_{lg}}\frac{V_{\text{dc}}}{2} \tag{25}$$

$$v_{Cang}^{\text{dm}\to\text{cm}} \approx \frac{1}{4}(v_{Q1} - v_{Q2}). \tag{26}$$

C. Simulation Approach and Model Refinement

The CEM, shown in Fig. 6, may be simulated to predict CM current flows in the given system assuming that the source terms in (21) and (24)–(26) can be suitably determined. Indeed, it will be shown in Section V that the dc input voltage, switching frequency, duty cycle, and device slew rates suffice as source parameters to accurately predict CM emissions in the system analytically. In this article, said source parameters are employed to generate a Fourier series representation of the term

$$v_Q \triangleq v_{Q1} - v_{Q2} \tag{27}$$

which appears in all ac CM voltage source definitions. Specifically, the dc bus voltage is assumed constant, and ideal, zero-bias, symmetric trapezoidal waves are employed to approximate the switch voltages. With these approximations, the Fourier series representation of v_Q is given by

$$v_Q = 4\,dV_{\text{dc}} \sum_{n=1}^{\infty} \text{Re}\left\{\text{sinc}(\pi nd)\,\text{sinc}(\pi n\tau_{rf} f_{\text{sw}})e^{j2\pi n f_{\text{sw}} t}\right\} \tag{28}$$

where V_{dc}, f_{sw}, d, and τ_{rf} are the dc-bus voltage, switching frequency, duty cycle, and average switch-voltage rise/fall time, respectively [37]. Using the sources' Fourier series coefficients, the sinusoidal steady-state solutions of $i_{\text{in}}^{\text{cm}}$ and $i_{\text{out}}^{\text{cm}}$, shown in Fig. 6, are computed at the switching frequency and every integer harmonic up to 30 MHz using phasor analysis. Moreover, to simplify the phasor analysis, the CEM is manipulated via standard circuit analysis into the form shown in Fig. 7(a). Therein, the CM parasitic capacitance is $C_{bp} = C_{ag} + C_{ug} + C_{lg}$, and the CM voltage source in the parasitic branch is given by

$$v_{bp}^{\text{cm}} = \frac{C_{ug} + C_{lg}}{C_{bp}}\frac{v_Q}{2}. \tag{29}$$

It is noted that the particular form of v_{bp}^{cm} in (29) is obtained by neglecting the source term $v_{Culg}^{\text{dm}\to\text{cm}}$ since it is virtually constant, as indicated in (25).

For validation purposes, the inboard and outboard LISN resistor currents are obtained from $i_{\text{in}}^{\text{cm}}$ using current division and multiplied by $R_{li}/2$ and $R_{lo}/2$, respectively, to obtain the inboard and outboard CM LISN voltages v_{Rli}^{cm} and v_{Rlo}^{cm}, as depicted in Fig. 6. The CM LISN voltages are the average of the physical MM LISN voltages depicted in Fig. 2

$$v_{Rli}^{\text{cm}} \triangleq \frac{1}{2}(v_{Rli,U} + v_{Rli,L}) \tag{30}$$

$$v_{Rlo}^{\text{cm}} \triangleq \frac{1}{2}(v_{Rlo,U} + v_{Rlo,L}). \tag{31}$$

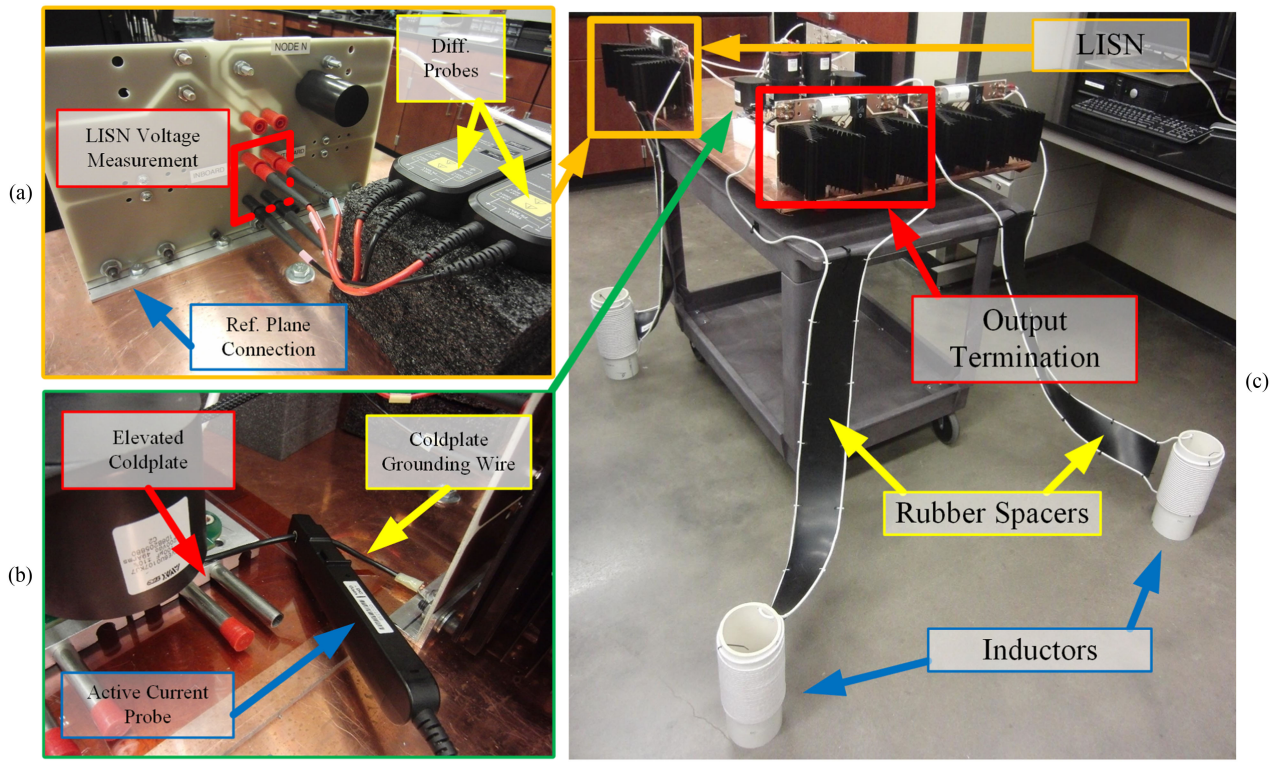

Fig. 8. CM/EMI characterization testbed: (a) LISN metrology and attachment to reference plane, (b) metrology setup used for direct measurement of displacement current through module baseplate, and (c) complete testbed assembly.

As an additional quantity for validation, the module baseplate current, as shown in Fig. 2 and equivalently in Fig. 7(a), is determined by

$$i_{bp} = -(i_{\text{in}}^{\text{cm}} + i_{\text{out}}^{\text{cm}}). \tag{32}$$

The LISNs and output terminations are shown in Fig. 7(a) as identical lumped impedances Z_{term}; the detailed impedance model of a single termination is shown in Fig. 7(b). In Fig. 7(b), the nominal components of the LISN model specified by MIL-STD-461 CE-102 [34] are depicted in black. To achieve a satisfactory match between analytical prediction and measured CM behavior, additional parasitic components (shown in red) are included in the Z_{term} model. First, a T-equivalent transmission line model is included to represent the interconnection between the inboard terminal and the EUT. Second, the parasitic coupling between L_l and the testbed reference plane is modeled as a pair of lumped capacitances, C_{pi} and C_{po}, at the inboard and outboard terminals of the inductor, respectively. Further explanation of these parasitic parameters and the determination of associated values are included in Section III-C. Provided that the parasitics are balanced for each pair of terminations ($\{U, L\}$ and $\{A, N\}$) in the testbed of Fig. 2, they may be introduced into Z_{term} without requiring any further modifications to the CEM shown in Fig. 7(a).

III. EMI Characterization Testbed

The notional EMI testbed, shown in Fig. 2, was reduced to practice during the efforts described in this article. The hardware realization that resulted from this process is shown in Fig. 8. Although the hardware setup of Fig. 8 was designed and built from scratch for the effort reported in this article, this design incorporates many features of an earlier EMI characterization testbed, which was designed and implemented by the authors as detailed in [4]. For the sake of brevity, only the most significant changes made to the design since the description in [4] will be reported here.

A. LISN and Output Termination Design Updates

The first major update to the hardware setup of [4] is associated with the design of the LISNs and output terminations. For both the new testbed and its predecessor, the termination design is based on MIL-STD-461, CE-102 [34]. However, the outboard resistors R_{lo} in the previous design were not thermally stable under certain EUT operating conditions. To improve the thermal performance of the system in the new design, the power rating of R_{lo} was increased from 120 to 240 W, and a large aluminum heat-sink with a thermal impedance in still air of 0.5 °C/W was fitted to these components. In addition, the updated termination printed circuit board (PCB) incorporates high-voltage connectors that enable direct attachment of differential voltage probes to the LISN ports, as illustrated in Fig. 8(a). This direct attachment technique eliminates the long clip-leads, which were required for measuring LISN voltages in [4], and minimizes the risk of coupling stray fields into the loop formed by the probe leads.

Improvements were also made to the implementation of the termination inductors in the new testbed design. In the previous

design, the inductor coils were attached to the testbed with Litz wire leads of approximately 1.5 m. During the impedance characterization of the testbed, it was found that the orientation of the leads contributed to measurable variation in the value of these inductors. To address this source of inconsistency, a semirigid strip of nonconductive rubber was fixed between the inductor leads in the new design. This change, which is shown in Fig. 8(c), helps to ensure a consistent and repeatable impedance profile for each termination within the testbed.

B. Testbed Metrology Updates

The second major update to the hardware setup of [4] is associated with the metrology practices employed. In the previous testbed design, the input and output CM currents were measured using a cascaded combination of current transformers. The displacement current through the module baseplate and attached heat sink was calculated from these two measured currents as in (32). While this method of measurement was useful for exploring general baseplate-current trends observed in simulation, some discrepancies remained between the simulated baseplate-current waveforms and those obtained through experiment due to the inherent numerical difficulties associated with seeking a small signal as the difference of two much larger signals. Thus, for validating the theoretical model presented in this article, a more accurate method for baseplate current measurement is used in the new testbed design. This technique involves the use of a 120 MHz active current probe to measure the current in a wire jumper connecting the module baseplate to the testbed ground plane, as shown in Fig. 8(b). This technique also requires the physical separation of the module baseplate and attached coldplate from the testbed ground plane, which was accomplished in the new testbed design with a spacer comprised of $1/4''$ polycarbonate sheet stock overlaid with a thin film of polyimide (Kapton).

In addition to the baseplate current measurement, the LISN voltages are also instrumented in the new testbed design. There are four attachment points of the LISN filters to the reference plane: each LISN has a single "inboard" attachment (across R_{li}, toward the EUT), and a single "outboard" attachment (across R_{lo}, opposite the EUT). In a typical qualification laboratory setup, only the inboard attachments would be instrumented and used to evaluate compliance to a given standard such as MIL-STD-461, CE-102. However, capturing all four LISN voltages provides additional insight into the system's CM/EMI behavior as well as additional data that can be used for detailed validation of the CM model presented in Section II. In the experiments reported here, all four LISN voltages are simultaneously measured using differential voltage probes rated at 1.5 kV and 200 MHz attached to an eight-channel oscilloscope with a bandwidth of 2 GHz (Tektronix MSO58).

C. Testbed Impedance Characterization

One important contribution of the current effort compared to the authors' previous work [4] is that the new EMI testbed has been extensively characterized. This characterization was originally undertaken in order to help identify a suspected missing parameter in the CEM outlined in Section II. While this aim was ultimately accomplished, this characterization effort also served another purpose. During the course of this analysis, many of the component parasitic parameters were found to have very little influence on the accuracy of the CEM predictions. Thus, through detailing the parasitic parameters of the EMI testbed, it was found through process of elimination that comparatively few parameters exert significant influence on the overall CM behavior of the system.

TABLE I
CHARACTERIZED LISN COMPONENT AND LEAD PARASITIC VALUES

Parameter		Value				Units
		L	*U*	*A*	*N*	
Components	L_l	52.12	51.25	51.35	52.95	μH
	C_{li}	0.2173	0.2166	0.2170	0.2166	μF
	C_{lo}	8.1563	8.1936	8.2126	8.1748	μF
	R_{li}	0.9899	1.0297	0.9901	0.9904	kΩ
	R_{lo}	4.9266	4.9333	4.9377	4.9445	Ω
Parasitics	L_t	307.0	362.0	339.0	203.5	nH
	C_t	16.67	15.00	13.57	14.59	pF
	C_{pi}	52.77	47.50	42.96	46.19	pF
	C_{po}	15.56	14.00	20.16	21.12	pF

1) LISN and Output Termination Component Measurement: The first major elements within the EMI testbed to be characterized were the individual components of the LISNs and output terminations. Each of the capacitors and inductors was disconnected from the testbed and measured with a Keysight E4990 A precision impedance analyzer across a frequency range from 20 Hz to 120 MHz. The resulting complex frequency data were imported into MATLAB and curve-fit to a single equivalent value using the technique outlined in [24]. Each of the resistors was also disconnected from the testbed and measured with a GW-INSTEK GOM-804 micro-ohm meter configured for a dc stimulus. All of these measurements were performed at room temperature in a laboratory environment.

The detailed results from this characterization step are presented in Table I. Additional analysis was performed on the measured characterization data reported here. For example, a value for the equivalent series resistance and equivalent series inductance was computed for each of the capacitors. The equivalent parallel capacitance for each resistor was also computed, along with the frequency-dependent resistance of the inductors. However, the model proved to be insensitive to these parameter values, and they were, therefore, not included in the model presented in Section II.

2) LISN and Output Termination Parasitic Measurement: During the investigations reported here, it was found that the CM behavior of the testbed was more nuanced than could be explained by the inclusion of the parasitic properties of the individual components described in Section III-C1. This led to a deeper exploration of the parasitic characteristics of the testbed. Ultimately, two different factors were found to play an important role in determining the CM behavior of the system under study. The first factor is the characteristic impedance of the litz wire jumpers between the EUT and the inboard ports of the LISNs and output terminations. Initially, the influence of

these jumpers was assumed to be negligible, because their length is short (0.5 m) compared to the length of litz wire used in the inductors (13.5 m) and they are spaced as far as possible from the testbed reference plane (200 mm). For these reasons, it was assumed that the series impedance and reference-plane-coupling of these jumpers would not be important. However, neglecting these parasitic contributions caused a significant error in the CM resonant frequency predicted by the model. This finding led to the introduction of a T-equivalent transmission line model to represent these jumpers, as shown in Fig. 7(b).

The second factor is the presence of a parasitic capacitive coupling between the testbed reference plane and various structures within the LISNs and output terminations. An extensive set of impedance analyzer experiments was conducted in an effort to determine the exact location of this coupling. However, it was found that this coupling is distributed broadly across all terminating components, interconnects, and the PCBs used to attach these components to the testbed. This finding led to the introduction of two additional parasitic capacitors within the Z_{term} model, one on either side of the inductor, as shown in Fig. 7(b).

The characterization process used for measuring the collective contribution of these parasitic parameters was as follows. First, each of the litz wire jumpers was disconnected from the testbed at the EUT end. Next, the free ends of the two input jumpers were connected together, and an impedance measurement was performed between this node and the testbed reference plane at the location of the MCPM baseplate. This process produced a measurement of the input CM impedance of the LISNs, inclusive of the litz jumper wires but exclusive of the 50 Ω terminations typically provided by the EMI receiver in a compliance setup. The results of this process for the LISNs are represented by the "measured" trace in Fig. 9. Also shown in Fig. 9 is the predicted CM impedance of the nominal LISN model without the contribution of the additional parasitic parameters described in this section. It should be noted that this model prediction diverges significantly from the measured behavior of the testbed at frequencies greater than 3 MHz. However, by including the additional parasitic parameters described in this section, the agreement shown in Fig. 9 is achieved. The complete set of parasitic parameter values that resulted from this process are tabulated in Table I.

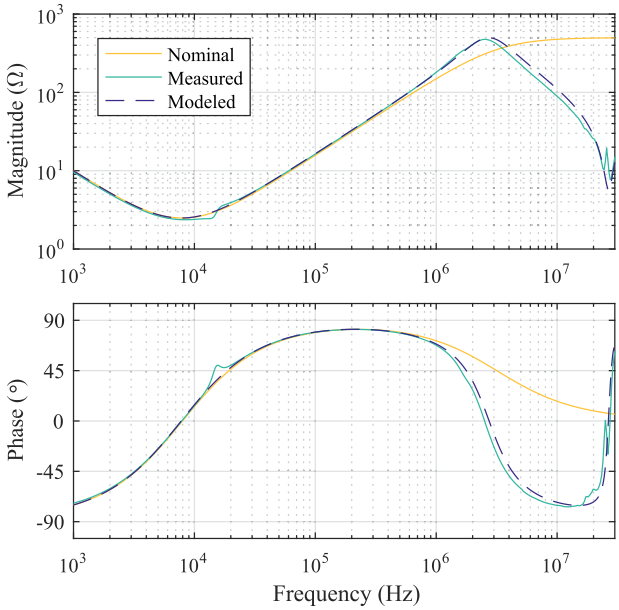

Fig. 9. Comparison of CM impedance of LISNs as measured from the EUT with Z_{term} model without parasitics (nominal) and with parasitics (modeled); note that all results exclude the 50 Ω terminations.

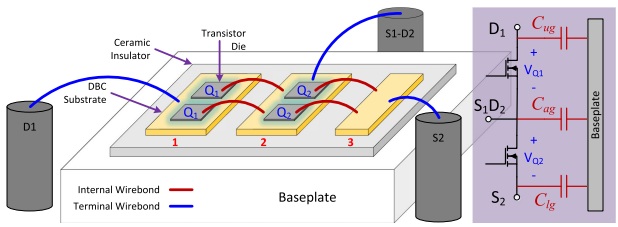

Fig. 10. Geometry diagram of a notional half-bridge MCPM.

IV. MCPM Parasitic Characterization

One parasitic that must be accurately determined in order to predict the conducted emissions of WBG-based converters is the BPC of the MCPMs used in such systems. A diagram of a notional half-bridge MCPM is presented in Fig. 10 to elucidate the origin of the module BPC. This simplified diagram shows a typical module configuration including the baseplate, ceramic insulator, conductive direct-bond-copper (DBC) substrate regions, and wire-bonds. Power semiconductor structures such as the DMOSFET present the drain terminal on the back of the die and the source and gate terminals on the top of the die. Wire-bonds are employed to connect the drain of Q_1 to external terminal D_1 via DBC region 1; the source of Q_1 and the drain of Q_2 to external terminal S_1D_2 via DBC region 2; and the source of Q_2 to external terminal S_2 via intermediate DBC region 3. Multiple parallel wire-bonds are generally used to meet ampacity requirements in high-current modules; however, only a single wire-bond per connection is shown here for simplicity. It is noted that the metallic baseplate, ceramic insulator layer, and DBC substrate regions form three unintentional parallel-plate capacitors between the MCPM terminals and the baseplate, which is usually mounted to a grounded heat sink. These three capacitances comprise the BPC.

A critical detail in the structure shown in Fig. 10 is that two of the three primary DBC regions shown are used to attach semiconductor die to the module substrate—viz., regions 1 and 2. Region 3 serves mainly as a current distribution mechanism and a means to reduce interconnect inductance (reduce wire-bond length) and, therefore, is usually smaller than the other regions. As a result, it is expected that the capacitive coupling between DBC region 1 and the baseplate is likely to be similar to the capacitive coupling between DBC region 2 and the baseplate. Conversely, the coupling between region 3 and the baseplate is expected to be somewhat smaller, since substrate area is not reserved for die mounting. Specific MCPM examples, which

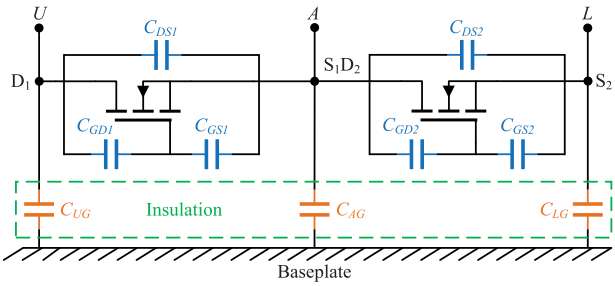

Fig. 11. Internal parasitic capacitances of a notional half-bridge MCPM.

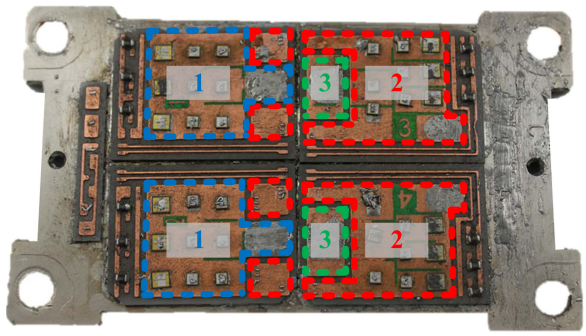

Fig. 12. Deconstructed MCPM with labeled substrate regions; region 1 constitutes C_{ug}; region 2 constitutes C_{ag}; and region 3 constitutes C_{lg}.

demonstrate the occurrence of this geometric convention in actual practice are reported in [6], [27], [38], and [39]. It has been shown in the authors' previous work that the magnitude of this imbalance has significant consequences for the interaction of CM and DM behavior and the overall leakage current through the module baseplate [31], [32], [40].

In order to populate the parameters of the model under consideration, it is necessary to estimate the BPC of the specific MCPM employed in the testbed of Fig. 8. This module is a commercially available SiC MOSFET half-bridge module from Cree, part number CAS120M12BM2. Techniques for empirically extracting estimates of MCPM interconnect inductance are well documented in the literature [24], [41], [42], but terminal-to-BPC is not considered by these procedures. Unfortunately, empirical techniques that extract inductances from terminal impedance measurements cannot be directly applied to extract these capacitances. This is due to the internal connections within the module that attach the semiconductor die to the substrate areas and the module terminals, as shown in Fig. 11. When the impedance between one of the terminals and the baseplate is measured for a fully assembled module, the resulting capacitance value represents a combination of series and parallel parasitic capacitances rather than the desired individual BPC component.

In order to accurately measure the individual BPC elements for the MCPM employed in the testbed of Fig. 8, a sample of the module utilized in the validation study (CAS120M12BM2) was deconstructed. The outer case of the module was removed along with the dielectric potting material to expose the substrate regions. In addition, each of the wire-bond connections represented in Fig. 10 was cut to isolate the individual substrate regions and allow independent measurement of each parasitic BPC element. The deconstructed module with the isolated substrate regions is shown in Fig. 12. Before the terminals were removed from the module, a Keysight E4990 A precision impedance analyzer was used to characterize the impedance between each terminal and the baseplate. The measured impedance data were subsequently imported into MATLAB and curve-fit with a series–RLC circuit using the technique in [24]. For each terminal, the measurement and curve-fit procedures were independently performed three times, and the extracted capacitor values from the independent runs were averaged for each terminal to minimize measurement error. The averaged curve-fit values that resulted from this process are shown in Table II.

TABLE II
AVERAGED BPC OF CREE CAS120 MCPM

Parameter	Description	Value	Units
C_{ug}	U-to-baseplate capacitance	191	pF
C_{ag}	A-to-baseplate capacitance	255.7	pF
C_{lg}	L-to-baseplate capacitance	102.6	pF
C_{bp}	total BPC	549.3	pF

V. EXPERIMENTAL VALIDATION

One goal of this article is to leverage the EMI testbed described in Section III to quantitatively demonstrate the predictive capabilities of a CEM rigorously derived as shown in Section II. To this end, both time-domain and frequency-domain comparisons of model predictions and empirical measurements are provided in this section. Although it is a common practice in the EMI/electromagnetic compatibility literature to provide model validation solely through comparison of spectral envelopes, this approach complicates quantitative error analysis and has a tendency to obscure model mismatches since such comparisons are plotted in decibels (i.e., a logarithmic scale). In order to address these shortcomings while maintaining relevance to qualification procedures, this article provides time-domain validation in addition to traditional spectral comparisons. Obtaining a high-fidelity model match in the time domain is a challenging endeavor and represents one of the distinguishing contributions of this article.

To generate time-domain waveforms for validation of the CEM, the EMI testbed described in Section III was exercised with a half-bridge EUT constructed from the commercially available silicon-carbide half-bridge module described in Section IV. The design and configuration of the single-phase inverter serving as the EUT in this setup is very similar to that described in [4]; therefore, only the differences from the previously reported configuration will be detailed here.

A. EUT Design Updates

The primary update to the EUT within the hardware setup of [4] concerns the custom gate-drive circuitry within this inverter. In the previous EUT design, pulsewidth modulation (PWM) signals were generated by a digital signal processor

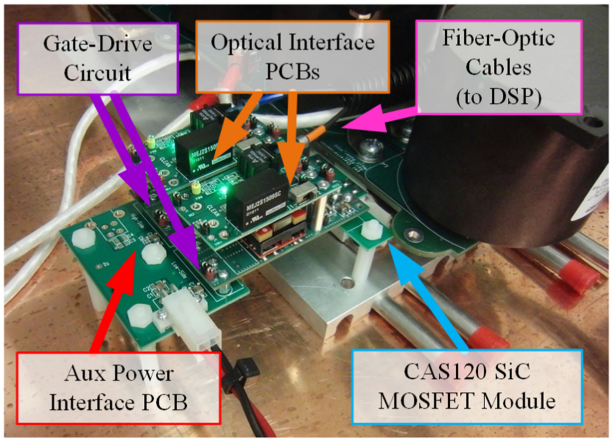

Fig. 13. Redesigned gate-drive circuit used in half-bridge inverter serving as EUT.

(DSP) and routed through a ribbon cable between the DSP board and the gate-drive circuitry attached to the power module. Galvanic isolation for the signaling path was provided within the gate-drive circuit itself by means of a digital isolator with a minimum common-mode transient immunity rating of 75 V/ns. This circuit was designed with the objective of ensuring sufficient galvanic isolation and high CM impedance. However, the unquantified coupling across this isolation barrier raised concerns that CM currents flowing through the gate-drive circuit could complicate the validation of the CEM. To address this potential CM leakage path, the new testbed design incorporates a fiber-optic cable interface between the DSP and the gate-drive circuitry attached to the power module. This change required a redesign of the gate-drive circuit, with the result shown in Fig. 13. The use of the fiber-optic interface not only reduces CM leakage currents through this path, but also reduces the likelihood that stray fields coupling into this path could cause uncommanded switching events. In addition, during this redesign process, the current amplifier used in the gate-drive circuit was upgraded to a new component capable of 30 A peak drive current, compared to 14 A peak drive current in the previous design. A 2-Ω externally applied gate resistor was used in the gate-drive circuit of both switch positions for all experiments reported here.

B. EUT Operating Conditions and Load Configuration

The EUT was operated continuously during multiple experiments that involved a range of operating conditions. In each experiment, the inverter was operated for a time period sufficient to reach thermal steady-state before measurements were performed. Achievement of thermal steady-state was verified by monitoring the inverter with a thermal camera during the initial few minutes of each test. All experiments were performed with a dc-bus voltage of approximately 600 V for consistency with previous efforts and to provide generous voltage headroom for the EUT, which is based on semiconductors rated at 1.2 kV. In all experiments, the inverter was operated open-loop with gate timing provided by a DSP running custom-developed, user-configurable firmware. For the particular experiments

TABLE III
TESTBED AND SIMULATION PARAMETERS

	Parameter	Value Case 1	Case 2	Case 3	Units
	EUT				
$V_{\rm dc}$	dc voltage	600	"	"	V
dv/dt	slew rate	3.42	2.13	2.13	V/ns
τ_{rf}	avg. rise/fall time	176	282	282	ns
$f_{\rm sw}$	switching frequency	100	"	"	kHz
d	duty cycle	50.09	"	"	%
t_{dt}	dead time	300	400	400	ns
$C_{\rm dc}$	DC-link capacitor	400	"	"	μF
C_n	neutral-forming cap.	100	"	"	μF
R_h	heat sink resistance	0	"	"	Ω
	LISNs				
L_l	input inductor	51.68	"	"	μH
C_{li}	inboard capacitor	0.22	"	"	μF
C_{lo}	outboard capacitor	8	"	"	μF
R_{li}	inboard resistor	1000	1000	50	Ω
R_{lo}	outboard resistor	5	"	"	Ω
L_t	jumper inductance	332.2	"	"	nH
C_t	jumper capacitance	15.84	"	"	pF
C_{pi}	inboard parasitic	50.13	"	"	pF
C_{po}	outboard parasitic	14.78	"	"	pF
	Output Terminations				
L_l	output inductor	52.14	"	"	μH
C_{li}	inboard capacitor	0.22	0	0	μF
C_{lo}	outboard capacitor	8	0	0	μF
R_{li}	inboard resistor	1000	∞	∞	Ω
R_{lo}	outboard resistor	5	∞	∞	Ω
L_t	jumper inductance	254.3	"	"	nH
C_t	jumper capacitance	14.08	"	"	pF
C_{pi}	inboard parasitic	44.58	"	"	pF
C_{po}	outboard parasitic	20.64	"	"	pF

reported here, the DSP was configured to operate the inverter in fixed-duty PWM at a switching frequency of 100 kHz. All salient parameters of the experiments reported in this article are detailed in Table III.

For the sake of brevity, this article provides detailed results for only three of the experiments performed. However, the included results are representative of the larger body of results, some of which are presented in [31]. The three experiments reported here are distinguished by the load applied to the inverter during operation and the configuration of the LISNs. For the first experiment (Case 1), the inverter was loaded with the output terminations connected in series as shown in Fig. 2. The LISNs were configured with high-impedance (1-kΩ) terminations on the inboard legs where qualification measurements are traditionally taken. This configuration evaluates the EUT with a known, reference impedance to the ground plane without excessive damping and filtering of switching transients. For the second experiment (Case 2), the output terminations were modified by physically removing R_{li} and R_{lo}, resulting in a nominally inductive load with an effective value of approximately 100 μH. Case 2 represents a configuration one step closer to the standard setup employed for qualification to MIL-STD-461 CE-102 [34], wherein the EUT load is floating with respect to the reference plane. Finally, for the third experiment (Case 3), the Case-2 configuration was modified by terminating the inboard legs of the LISNs with 50-Ω resistors to conform with a standard conducted emissions qualification setup. Additionally, the coldplate was mounted directly to the testbed ground plane and the ground

strap was removed. Comparison of these three experimental cases provides a first-order estimation of the impact of the metrology and load coupling on the CM behavior of the EUT.

C. Model Predictions Versus Experimental Results

Simulation studies were performed to compare the predictions of the model derived in Section II with the experimentally observed behavior of the testbed. To this end, the steady-state CM emissions of the testbed were computed via Fourier series and phasor analysis of the model in Fig. 7, as described in Section II, using the parameters summarized in Tables II and III. The sole inputs provided to the CEM were the CM voltage expressions given by (21) and (24)–(26). It is noted that nominal values of many testbed components were used in the populated CEM, even though characterized values were available as detailed in Section III-C. In these cases, CM behavior was found to be insensitive to the parameters in question, so nominal values were utilized to demonstrate the minimal complement of characterized values necessary to accurately predict the system's CM emissions.

For all of the experiments presented, graphical comparisons are provided between the CEM prediction and the measured behavior of the EUT in terms of three metrics: the outboard CM voltage at the LISN v_{Rlo}^{cm}, the inboard CM voltage at the LISN v_{Rli}^{cm}, and the displacement current through the module baseplate i_{bp}. It should be noted that no filtering or smoothing was applied to any of the experimental data presented in this section. For v_{Rli}^{cm} and i_{bp}, spectral comparisons are provided in addition to the transient waveform overlays. A quantitative assessment of the agreement between the CEM and the measured behavior of the system is also provided for all three transient metrics. The normalized rms error between simulated and measured results is used for this purpose. This value is computed as follows:

$$\mathrm{Error}_{x,\mathrm{nrms}} = \frac{\sqrt{\frac{1}{N}\sum_{n=1}^{N}(x_{\mathrm{meas},n} - x_{\mathrm{sim},n})^2}}{\max_n \left|x_{\mathrm{meas},n}\right|} \times 100\%. \tag{33}$$

1) Case 1: The simulated CM LISN voltages and MCPM baseplate current for Case 1 are compared to measured waveforms in Fig. 14. The transient comparisons of the CM outboard and CM inboard LISN voltages shown in Fig. 14(a) and (b), respectively, demonstrate good agreement. This verifies the accuracy of the CEM in predicting the transient behavior of the CM current at the input of the EUT, which is a critical component of the conducted emissions for this type of system. The transient plots of the measured baseplate current in Fig. 14(d) and (e) also demonstrate good agreement with the CEM predictions. This is another important predictive capability of the CEM, as the baseplate current is known to contribute to CM emission challenges in high-power converters.

The spectral comparisons of the CM inboard LISN voltage and the baseplate current in Fig. 14(c) and (f), respectively, also demonstrate good agreement for Case 1. Specifically, both the odd and even switching harmonics are accurately predicted by the CEM up to at least 5 MHz, and reasonable agreement is achieved up to 30 MHz, the upper limit of the commercial conducted emissions standards. Overall, the values presented in Table IV confirm that the CEM is able to predict the CM behavior of this system for Case 1 with a high degree of fidelity, as all waveforms are predicted with a normalized root-mean-square (rms) error value below 4%.

TABLE IV
NORMALIZED RMS ERROR BETWEEN MEASURED AND SIMULATED CM EMISSIONS

Measurement	Label	NRMS Error		
		Case 1	Case 2	Case 3
Outboard LISN Voltage	v_{Rlo}^{cm}	0.91%	7.22%	16.99%
Inboard LISN Voltage	v_{Rli}^{cm}	2.81%	9.83%	6.64%
MCPM Baseplate Current	i_{bp}	3.50%	4.86%	6.14%

2) Case 2: The simulated CM input LISN voltages and MCPM baseplate current for Case 2 are compared to measured waveforms in Fig. 15. The transient comparisons of the CM outboard and CM inboard LISN voltages shown in Fig. 15(a) and (b), respectively, demonstrate good agreement, which is corroborated by quantitative error metrics in Table IV. It is noted that the large triangle wave present in the CM outboard LISN voltage for Case 1 is not present for Case 2. This is the expected behavior, as the low-impedance outboard path in the termination loop formed by the output terminations is not present for Case 2. The spectral comparison of the CM inboard LISN voltage in Fig. 15(c) also demonstrates reasonable agreement for Case 2. Similar to Case 1, both the odd and even switching harmonics are accurately predicted by the CEM up to at least 4 MHz, and reasonable agreement is achieved up to 30 MHz. Above 4 MHz, the observed spectral roll-off is faster than what is predicted by the model. This discrepancy is attributable to the noise source approximation employed in the simulation—i.e., v_Q was assumed to be an ideal trapezoidal wave as given by (28), which results in an overestimate of the high-frequency band.

Good agreement between model predictions and measured results is also achieved for the baseplate current in Fig. 15(d)–(f) although there is a modest discrepancy between simulation and measurement around 20 MHz. As shown therein, there is a resonant peak near 20 MHz not captured by the model. This peak is due to parasitic inductance introduced by the coldplate grounding wire shown in Fig. 8(b), which is used to obtain a high-resolution measurement of the baseplate current. Thus, the resonance can be moved to a higher frequency by shortening the ground strap as will be shown in Case 3.

Nevertheless, the most significant characteristics of the baseplate current are accurately predicted by the CEM for Case 2. For example, the peak value of the baseplate current (less the high-frequency ringing) is increased from 400 mA in Case 1 to 700 mA in Case 2. This change, which is accurately predicted by the CEM, is due to the elimination of a cancellation effect that is created by the termination loop as detailed in [31] and [32]. Thus, the dynamics at the primary CM resonance of 1.5 MHz, which would drive CM filtering requirements in the given system, are accurately predicted. Overall, the values presented in Table IV confirm that the CEM is able to predict the CM behavior of this

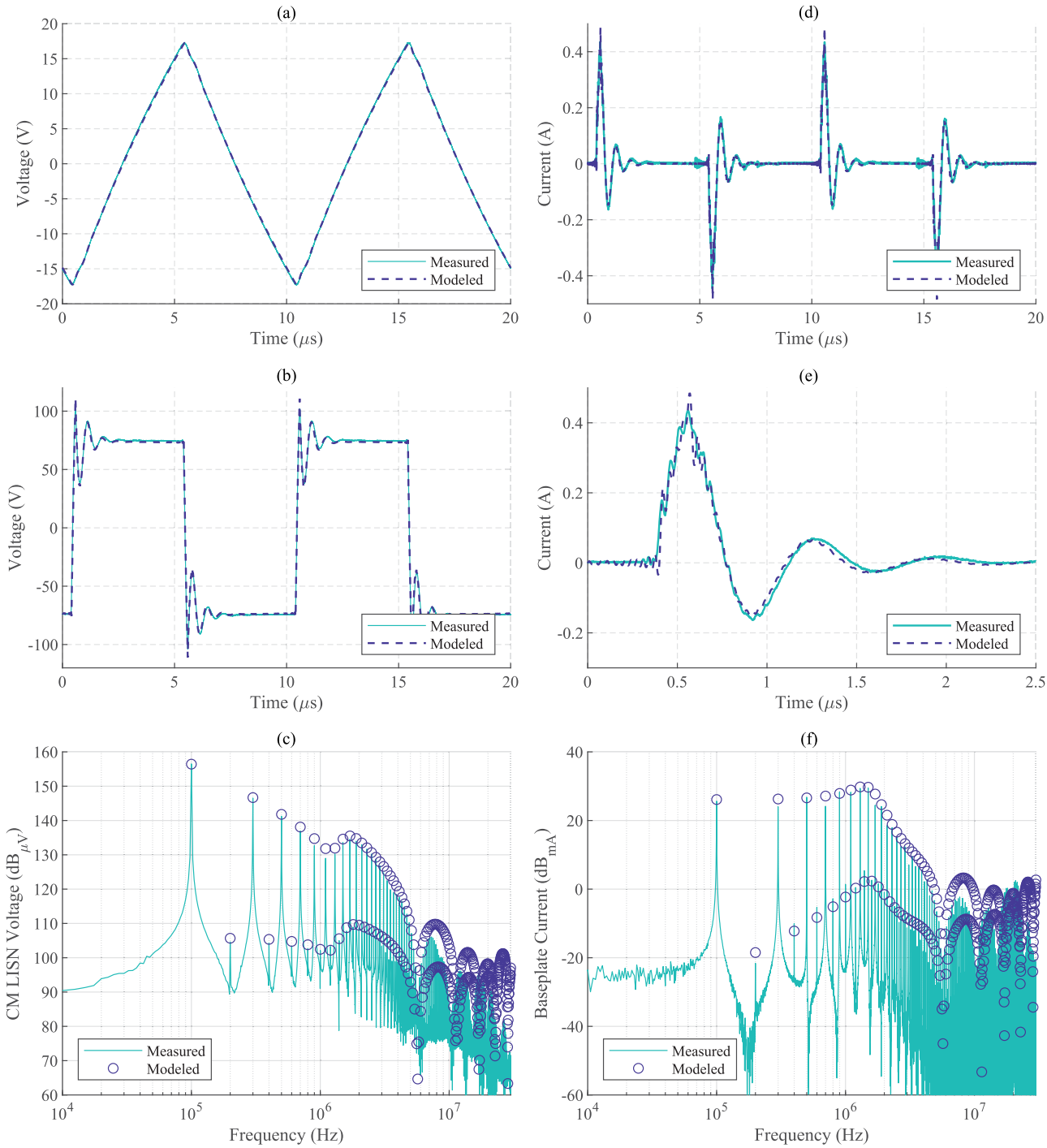

Fig. 14. Comparison of measured and modeled CM voltages and currents in EMI testbed for Case 1: (a) outboard CM voltage at the LISN v_{Rlo}^{cm}; (b) time-domain and (c) frequency-domain inboard CM voltage at the LISN v_{Rli}^{cm}; (d) time-domain, (e) zoomed-view time-domain, and (f) frequency-domain leakage current through the MCPM baseplate i_{bp}.

system for Case 2 with high fidelity, as the normalized rms errors are all below 10%.

3) Case 3: The simulated CM LISN voltages and MCPM baseplate current for Case 3 are compared to measured waveforms in Fig. 16. It is noted that in Case 3, the coldplate grounding wire was removed, and the coldplate was mounted directly to the testbed ground plane to reduce the partial inductance of this path. Therefore, the baseplate current plotted in Fig. 16 is calculated as the sum of all currents flowing through all of the LISN resistors, unlike the direct measurements shown in Cases 1 and 2.

The transient comparisons of the CM inboard LISN voltage and baseplate current shown in Fig. 16(b) and (d), respectively, demonstrate good agreement once again. The accuracy of the CM outboard LISN voltage prediction shown in Fig. 16(a) appears to be reduced in this case. However, this is a result of

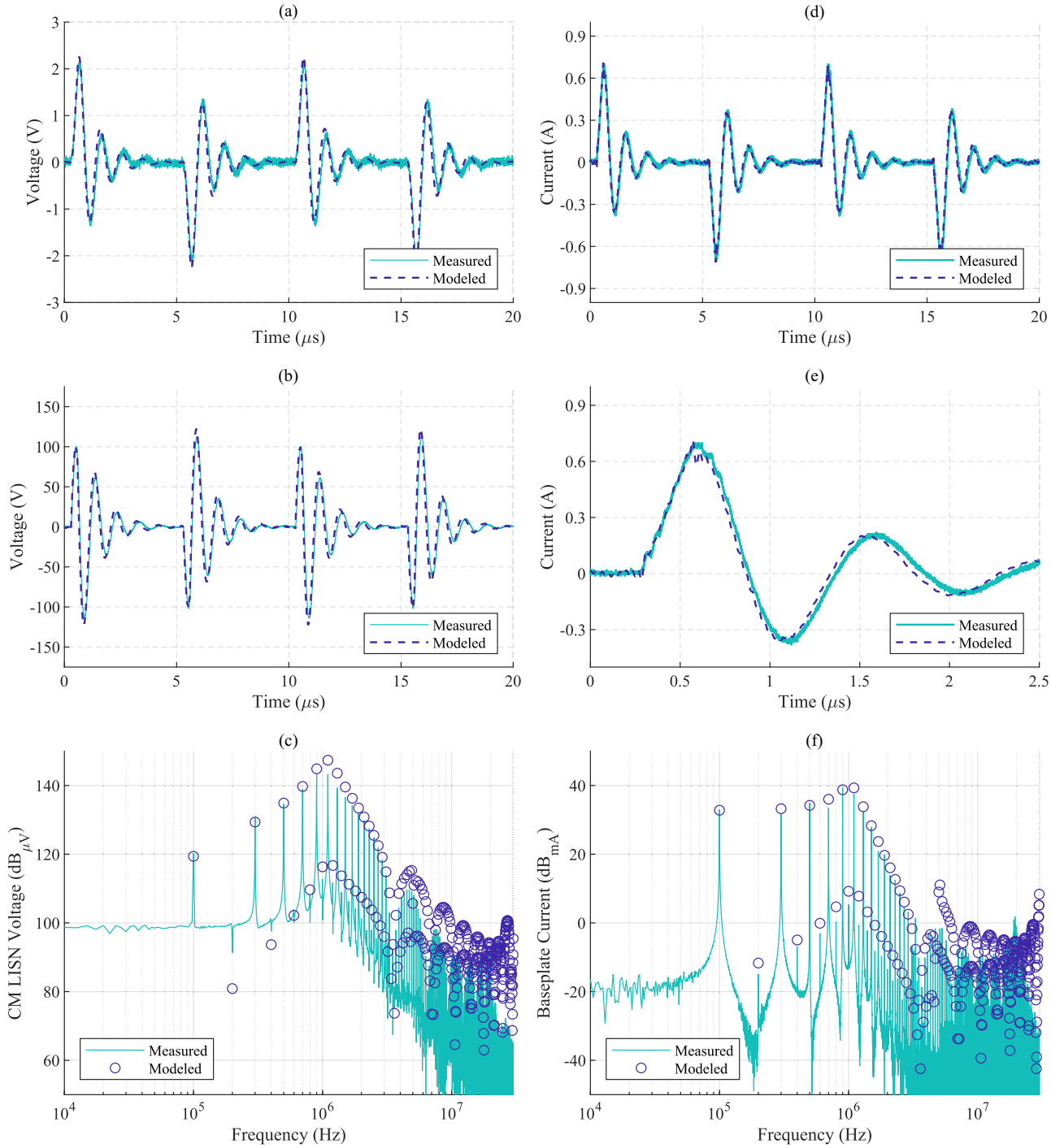

Fig. 15. Comparison of measured and modeled CM voltages and currents in EMI testbed for Case 2: (a) outboard CM voltage at the LISN v_{Rlo}^{cm}; (b) time-domain and (c) frequency-domain inboard CM voltage at the LISN v_{Rli}^{cm}; (d) time-domain, (e) zoomed-view time-domain, and (f) frequency-domain leakage current through the MCPM baseplate i_{bp}.

a drastic reduction in emissions generated by the EUT flowing through the outboard legs due to the low-impedance 50-Ω terminations on the inboard legs. Thus, a relatively large component of the noise conducted through the outboard legs originates from the dc supply, which is not modeled herein. This is also the reason for the substantially larger error reported for v_{Rlo}^{cm} for Case 3 in Table IV.

In any case, the plots in Fig. 16 and the quantitative results in Table IV indicate a strong match between measurements and model predictions for Case 3 as with Cases 1 and 2. Comparing all three experiments, it is observed that there is significant resonant behavior in the baseplate current appearing between 1 and 2 MHz in Cases 1 and 2 that is notably absent in Case 3. The 50-Ω terminations associated with standard qualification

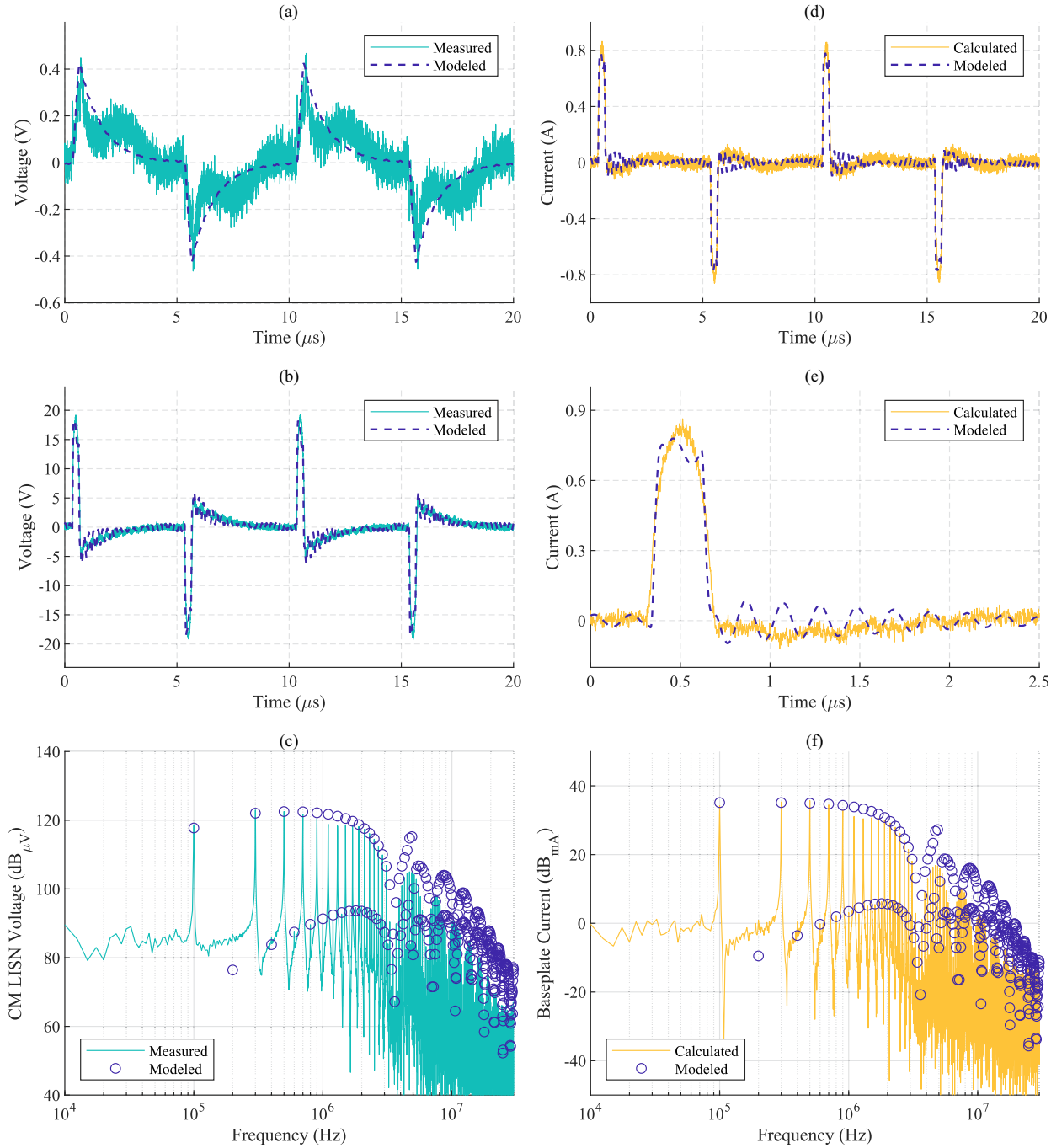

Fig. 16. Comparison of measured and modeled CM voltages and currents in EMI testbed for Case 3: (a) outboard CM voltage at the LISN v_{Rlo}^{cm}; (b) time-domain and (c) frequency-domain inboard CM voltage at the LISN v_{Rli}^{cm}; (d) time-domain, (e) zoomed-view time-domain, and (f) frequency-domain leakage current through the MCPM baseplate i_{bp}.

metrology appear to significantly damp the conducted emissions of the example inverter system. Thus, depending on the coupling to ground present in the final application, the qualification setup may significantly underestimate the emissions in the fielded system.

VI. Conclusion

This article has outlined a formalized approach for developing CEMs of power electronic applications that is especially useful for evaluating parametric sensitivities within such systems. This procedure is utilized to derive a detailed CEM for an example system, which is a single-phase inverter within a custom hardware testbed designed by the authors specifically for EMI characterization of WBG-based power electronics. The resulting model is demonstrated to accurately predict the measured CM behavior of the example system, when populated with a modest set of parasitic parameter values obtained through impedance characterization of the hardware testbed. The predictions of the CEM in both the time domain and the frequency domain are

shown to closely agree with the measured behavior of the testbed in all considered configurations of the EUT.

It is further shown that the predictive capability of the developed CEM is strongest in the frequency range between 10 kHz and 30 MHz, which is the principal range of interest for controlling conducted emissions in WBG-based systems. Thus, the modeling approach demonstrated here is expected to be particularly useful to application designers seeking to understand the impact of CM behavior in WBG-based designs, which are known to produce elevated emissions in this frequency range. One additional contribution of this article is the identification of the specific set of parasitic elements that must be considered within the CEM in order to obtain appreciable agreement to the measured behavior of the system under consideration. While a large number of characterization experiments were performed in support of this effort, it was found that the primary sensitivity of the system is the subset of parasitics, which involve coupling to the reference plane within the testbed.

In total, this article presents a self-contained demonstration and validation of the authors' technique for modeling and predicting conducted emissions in power electronic applications. This technique is based on straightforward circuit analysis methods, and can be effectively implemented with characterization data obtained from a commonly available impedance analyzer. The combined simplicity and accuracy of the proposed approach make it a useful tool for practicing engineers in the reduction of CM emissions during early-stage design of power electronic systems.

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