Modeling and Mitigation of Multiloops Related Device Overvoltage in Three-Level Active Neutral Point Clamped Converter

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***Abstract*—This article establishes an analytical model for the device drain–source overvoltage related to the two loops in three-level active neutral point clamped (3L-ANPC) converters. Taking into account the nonlinear device output capacitance, two common modulation methods are investigated in detail. The results show that the line switching frequency device usually has higher overvoltage, and the switching speed of the high switching frequency device is not strongly influenced by the multiple loops. By keeping the nonactive clamping switch OFF, the effect of the nonlinear device output capacitance can be significantly mitigated, which helps reduce the overvoltage. Moreover, the loop inductance can be reduced with vertical loop layout and magnetic cancellation in the printed circuit board and busbar design. A 500-kVA 3L-ANPC converter using silicon carbide MOSFETs was built and tested. The experimental results validate the overvoltage model of the two modulation methods as well as the busbar design. With the nonactive clamping switch OFF, the overvoltage of both the high and line switching frequency devices is significantly reduced, which helps achieve higher switching speed.**

***Index Terms*—Model, overvoltage, 3L-ANPC converter, SiC MOSFET, layout.**

I. Introduction

COMPARED to conventional two-level (2L) converters, three-level (3L) converters have the merits of lower device voltage rating, better output harmonic spectrum, lower electromagnetic interference (EMI) noise, higher switching speed capability, and better dynamic response [1], [2]. Among 3L converter topologies, the neutral point clamped (NPC) converter is a popular candidate for medium voltage and high-power applications such as grid-tied solar inverters, motor drives, and electric transportation systems. In applications requiring high efficiency or flexible power flow control, the active neutral point clamped (ANPC) converter is proposed by replacing the diodes in the NPC converter with active switches like MOSFETs or IGBTs [3]–[5]. The topology of a 3L-ANPC converter is shown in Fig. 1.

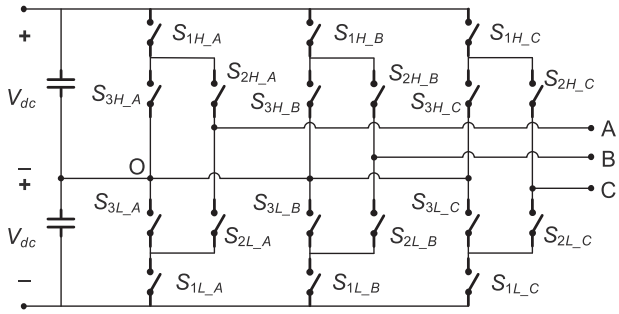

Fig. 1. Topology of 3L-ANPC converter.

Conventionally, Si IGBTs are the main power switches used in high power 3L-ANPC converters. Recently, with the development of wide bandgap (WBG) technology, silicon carbide (SiC) MOSFETs have been attracting more and more attention. Compared with Si IGBTs, SiC MOSFETs exhibit higher switching speed and can achieve lower switching loss with the same switching frequency [6], [7]. However, the higher di/dt and dv/dt during the switching transient also introduces worse resonance and voltage/current spikes because of the parasitics in the power loop. These resonances and spikes not only deteriorate electromagnetic compatibility, but also can cause device failure when they exceed the device ratings [8]–[10]. This issue becomes even more severe and complicated in multilevel topologies since they have multiple loops.

Extensive work has been conducted to analyze, model, and minimize device overvoltage [10]–[13] in converters with high-speed switching devices. However, they were mainly based on

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2L configurations and did not consider the multiloop impact. Several studies have focused on switching loops in 3L-ANPC converters [14]–[17]. Two commonly used modulation methods were compared in [14] to evaluate the loss distribution with different switching loops. The multiloop influence on loss, harmonics, and overvoltage was analyzed in [15]. The overvoltage issue in the 3L-ANPC converter and its causes were investigated in [16], while [17] provided a solution for overvoltage mitigation. However, there is still a lack of an analytical model that can explain the coupling effect among different loops and build the relationship between the overvoltage and the parasitics for the 3L-ANPC converter.

Based on the previous review and analysis, this article establishes an analytical overvoltage model for 3L-ANPC converters with two commonly used modulation schemes, and the effect of multiloops and nonlinear device output capacitance are considered. Based on the model, the overvoltage and switching speed relationship between the high and line switching frequency devices caused by the multiloops is investigated in detail. Moreover, a design recommendation is provided for the printed circuit board (PCB) and busbar layout of the 3L-ANPC converter to reduce the parasitic inductance.

This article is organized as follows. Section II presents the comparison of multiple loops under different modulations. Sections III and IV build the analytical model for the two modulations with different nonactive switch states. Section V provides the design considerations in PCB and busbar layouts to reduce the parasitic inductance. Section VI demonstrates the experimental results of the overvoltage comparison with different modulations, and Section VII gives the conclusion.

II. Modulation Schemes and Loop Analysis of 3L-ANPC Converter

According to the switch states transitions, there are two main types of fundamental modulation schemes for a 3L-ANPC converter single phase leg. For the modulation 1 in Fig. 2(a), during a half-line period, the outer switch (S_{1L}) and the clamping switch (S_{3L}) operate complementarily at high switching frequency. The inner switches (S_{2H} and S_{2L}) also operate complementarily but at line switching frequency [14], [18]–[22]. As a result, the high switching speed commutation occurs between the outer and clamping switches (S_{3L} and S_{1L}), and the commutation loop only includes these two switches. Compared with the other modulation scheme, it involves fewer switches and has a shorter loop length. Therefore, the loop in modulation 1 is called the short loop. Note that in the other half phase leg, the clamping switch (S_{3H} in Fig. 2) can be kept either in ON state (modulation 1-A), or in OFF state (modulation 1-B). For modulation 1-B, special attention should be paid to the transition between positive and negative half-line cycles. The control in [20] can be adopted to guarantee a smooth transition.

The other modulation scheme (modulation 2) is drawn in Fig. 2(b). In contrast with modulation 1, the inner switches continuously operate at high switching frequency, while the outer and clamping switches operate at line frequency [3], [23]–[25]. The commutation loop contains four switches [S_{3H}, S_{2H}, S_{2L}, and S_{1L} in Fig. 2(b)], and is called the long loop. There are also

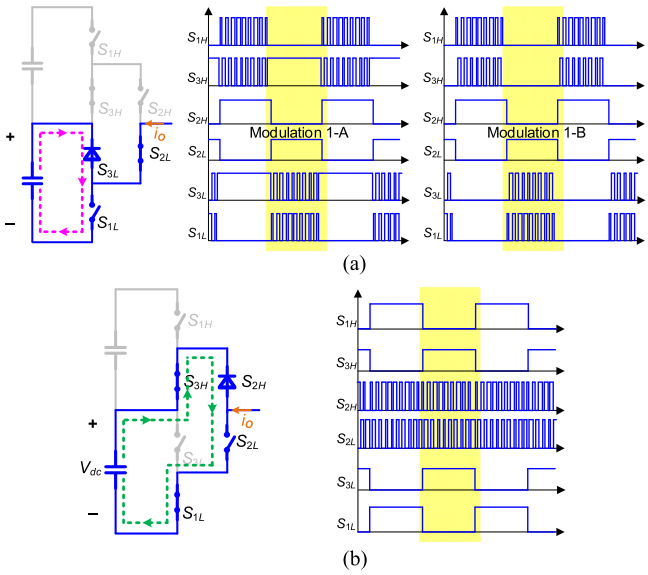

Fig. 2. Modulation schemes for 3L-ANPC converter single phase leg. (a) Modulation 1-A and 1-B. (b) Modulation 2.

some hybrid modulations that combine these two basic schemes together but with higher complexity [26], [27].

Conventionally, modulation 2 has wider implementation as only two switches operate at high switching frequency. However, with the increase of switching speed by SiC MOSFETs, modulation 1 is adopted more and more frequently because of the following reasons.

1) Modulation 2 has longer commutation loop, which introduces more parasitic inductance. At the same switching speed, more inductance results in higher overvoltage across the switch. To avoid damaging the power device and reduce EMI, the switching speed has to be reduced, leading to higher loss. Decoupling capacitors can be added across the half-bridge S_{2H} and S_{2L} to reduce the overvoltage. However, the resonance between the parasitics introduce extra energy loss especially at high switching frequencies [25].
2) In high-power applications, power modules with half bridge structure are popular for bridge-type topologies. With modulation 1, it is easier to achieve loss balance among three modules if S_{1H} and S_{3H}, S_{1L} and S_{3L}, and S_{2H} and S_{2L} are paired. On the contrary, it is difficult to achieve such balance in modulation 2 because S_{2H} and S_{2L} always operate at high switching frequency and these devices bear most of the switching loss.

III. Modeling of Device Overvoltage With Modulation 1-A

As shown in the analysis previously, modulation 1 is more suitable for high switching frequency applications due to the shorter commutation loop and better loss balancing. With the nonactive clamping switch ON, modulation 1-A can provide stable potential for the nonactive outer and inner switches. However, as has been pointed out in [15]–[17], there is a multiloop issue in 3L-ANPC converters.

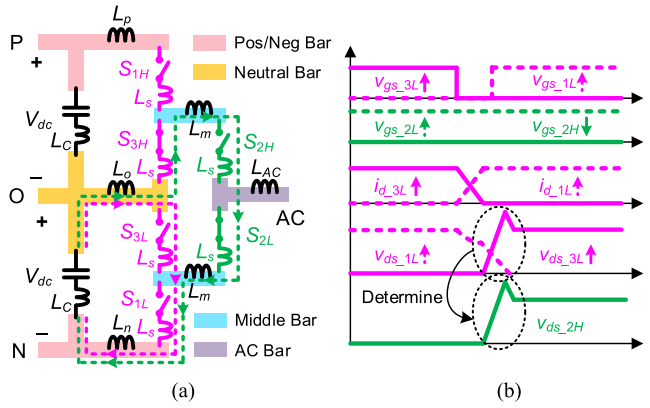

Fig. 3. 3L-ANPC converter single phase. (a) Topology considering layout and parasitics. (b) Ideal switching waveforms when S_{1L} is the active switch.

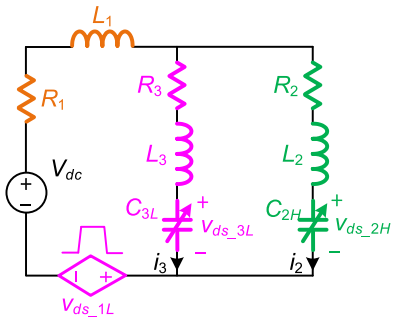

Fig. 4. Equivalent circuit of single phase leg during half-line cycle with modulation 1-A.

A. Loop Analysis

The equivalent circuit of a phase leg in the 3L-ANPC converter is illustrated in Fig. 3(a). Different busbar parts and parasitic inductances are highlighted. Since S_{2L} and S_{3H} are on, S_{2H} is equivalently paralleled with S_{3L}. The detailed switching waveform is plotted in Fig. 3(b). Note that S_{2H} is a nonactive switch during a half-line cycle. When the active switch S_{3L} commutates with S_{1L}, the drain–source voltage of S_{2H} follows that of S_{3L}. The parasitic inductance resonates with the output capacitance of S_{2H}. So the resonance of v_{ds_2H} is excited by the operation of S_{3L}, which differs from modulation 2, where S_{2H} is an active switch and the resonance is independent of S_{3L}. Therefore, both the short and long loops exist, and there is coupled influence between S_{3L} and S_{2H}.

Assume each busbar part is independent and is not coupled with other busbar parts, and each switch has the same stray inductance. The two loops share the neutral busbar, positive/negative busbar, the switch S_{1L}, and the dc-link capacitor. The short loop contains the switch S_{3L} while the longer loop includes two pieces of middle busbar as well as the switches S_{3H}, S_{2H}, and S_{2L}. When the load current flows into the phase leg and S_{1L} is the active switch, the equivalent circuit of the phase leg can be drawn in Fig. 4. Generally, the overvoltage during turn-ON is higher than during turn-OFF [28], [29], so here, the turn-ON transient of the active switch S_{1L} is analyzed. L_1 is the shared loop inductance by two loops and equals to the sum of capacitor equivalent series inductance L_C, neutral busbar inductance L_o, negative busbar inductance L_n, and one switch stray inductance L_s. L_2 is the sum of two middle busbar inductances $2L_m$, and three switch stray inductances $3L_s$. L_3 equals to one switch stray inductance L_s. The short-loop inductance L_{st} is L_1+L_3 while the long-loop inductance L_{lg} is L_1+L_2. R_1, R_2 and R_3 are the loop parasitic resistances. C_{3L} and C_{2H} are the output capacitances of S_{3L} and S_{2H}, respectively. i_3 and i_2 are, respectively, the currents through S_{3L} and S_{2H}. S_{1L} is represented as a controlled voltage source.

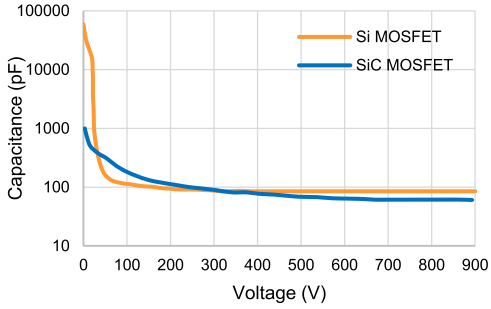

Fig. 5. Nonlinear output capacitance of 900 V Si and SiC MOSFET.

B. Modeling With Nonlinear Device Output Capacitance

For semiconductor power devices like MOSFETs and IGBTs, the output capacitance is nonlinear and is dependent on the drain–source voltage. Based on different semiconductor material and device structure, the output capacitance at low voltage can be 10–500 times higher than that at high voltage as shown in Fig. 5 [30]. According to [17], this nonlinearity of the output capacitance is a large contributor for the overvoltage.

The instantaneous voltage and current relationship in Fig. 4 can be derived based on Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL)

$$\begin{cases} V_{\rm dc} = L_3\frac{di_3}{dt} + v_{ds\_3L} + (R_1+R_3)\,i_3 + R_1 i_2 \\ \qquad +L_1\left(\frac{di_3}{dt}+\frac{di_2}{dt}\right) + v_{ds\_1L} \\ V_{\rm dc} = L_2\frac{di_2}{dt} + v_{ds\_2H} + (R_1+R_2)\,i_2 + R_1 i_3 \\ \qquad +L_1\left(\frac{di_3}{dt}+\frac{di_2}{dt}\right) + v_{ds\_1L} \\ C_{3L}\frac{dv_{ds\_3L}}{dt} = i_3 \\ C_{2H}\frac{dv_{ds\_2H}}{dt} = i_2. \end{cases} \tag{1}$$

Since the output capacitance is nonlinear and voltage dependent, it is difficult to directly derive the voltage response. Here, the state-space analysis is implemented to build the analytical voltage response model in the time domain. The detailed equations and matrices of the model are in Appendix A.

The voltage dependent output capacitance is modeled with the following equation [31]:

$$C\,(v) = C_{hv} + \frac{1}{\frac{1}{C_{0v}} + \frac{v^x}{C_j}} \tag{2}$$

where C_{0v} and C_{hv} are the low-voltage and high-voltage capacitances, respectively, and x and C_j are curve fitting coefficients.

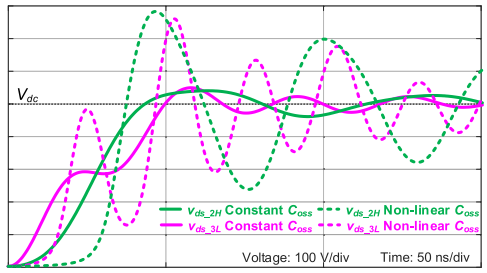

Fig. 6. Voltage transient waveforms with constant and nonlinear capacitance based on established model.

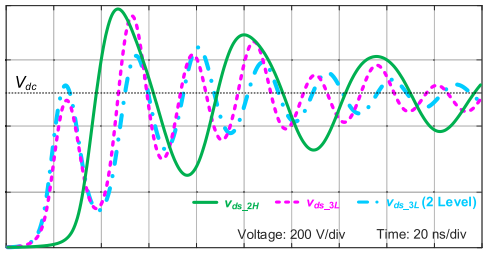

Fig. 7. Voltage transient waveforms with 3L and 2L phase leg based on the proposed model.

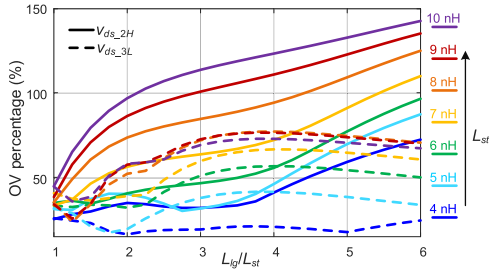

Fig. 8. Overvoltage of high and line switching frequency devices under different L_{st} and L_{lg}/L_{st}.

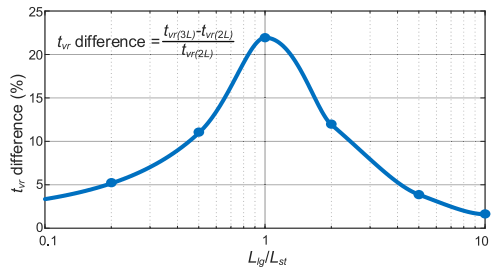

Fig. 9. Voltage rise-time difference of high switching frequency devices between 3L and 2L single phase.

Fig. 6 compares the derived analytical voltage transient waveforms between constant and nonlinear output capacitances. The constant capacitance uses the time related effective value based on the device datasheet. Obviously, the overvoltage with nonlinear capacitance is much higher than the constant capacitance case. To predict the real condition during a switching transient, voltage dependent nonlinear capacitance has to be taken into consideration in the model.

C. Analysis of Overvoltage With Established Model

Based on the analytical model built previously, the overvoltage of both high and line switching frequency switches can be evaluated. Fig. 7 illustrates the transient waveforms of 3L and 2L phase leg. The resonant frequencies of the high and line switching frequency devices are different. For the high switching frequency device, the resonant frequency is close to that in a typical 2L phase leg, and is higher than the line switching frequency device.

The relationship between the loop inductance and the overvoltage of both the high and line switching frequency devices needs to be evaluated. The overvoltage percentage OV(%) is defined to simplify the analysis

$$\mathrm{OV}\,(\%) = \frac{V_{ds\_pk} - V_{\mathrm{dc}}}{V_{\mathrm{dc}}} \times 100\%. \tag{3}$$

Based on the model, the relationship among the short-loop inductance L_{st}, the ratio between long- and short-loop inductances L_{lg}/L_{st}, and OV(%) is shown in Fig. 8. From the plot, the following conclusions can be made.

1) With the same inductance ratio of short and long loops, the increase of inductance value leads to higher overvoltage for both the high and line switching frequency devices.
2) Keeping the same short loop inductance, the larger long-loop inductance results in higher overvoltage across the line switching frequency device. However, the overvoltage of the high switching frequency device reaches its peak when L_{lg}/L_{st} is 3 to 4. Further increasing the long-loop inductance does not cause higher overvoltage. This is because the increased L_{lg} decouples C_{3L} and C_{2H}. The voltage rise on C_{3L} is due to the excitation of the resonance on C_{2H}. Larger L_{lg} prevents v_{ds_2H} from following the trend of v_{ds_3L}, and v_{ds_2H} in turn shows less influence on v_{ds_3L}.
3) When $L_{lg}/L_{st} = 1$, the two devices have the same overvoltage, which is easy to understand. Generally speaking, the line frequency device exhibits higher overvoltage compared to the high switching frequency device especially with large L_{st} and inductance ratio. The only exception is when L_{st} is small (lower than 6 nH) and L_{lg}/L_{st} is between 2.5 to 4. Hence, the overvoltage of the line switching frequency device requires more attention.

In terms of the coupling effect between the high and line frequency devices, it is also important to know the influence of the long loop on the switching speed of the high switching frequency device. Fig. 9 shows the voltage rise-time of the high switching frequency device in 3L and 2L phase legs with different loop inductance ratios. The closer the two loop inductances are, the longer voltage rise-time appears for the high switching frequency device in a 3L phase leg. The two loops have the strongest coupling when they have the same loop inductance value, leading to the largest influence on the rising speed of the voltage across the switch. From Fig. 9, when the loop inductance ratio is larger than 2.2, the voltage rise-time difference between 3L and 2L phase legs is smaller than 10%. Considering the

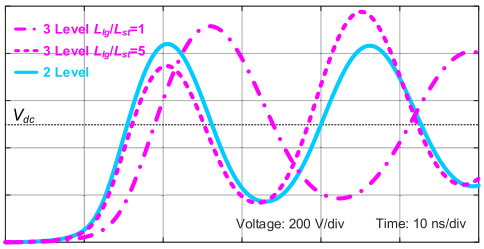

Fig. 10. Voltage transient waveforms with different L_{lg}/L_{st} and same L_{st} based on established model.

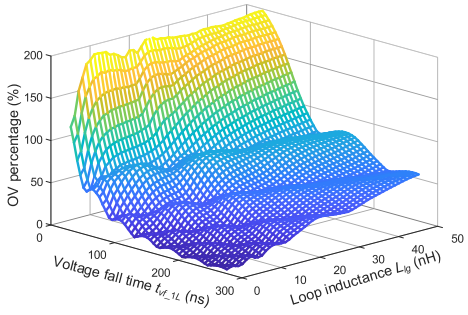

Fig. 11. Overvoltage of line switching frequency device under different L_{lg} and t_{vf_1L}.

3L-ANPC converter, it is common that the long loop has much larger parasitic inductance than the short loop does. Therefore, in most cases, the switching speed of the high switching frequency device in a 3L phase leg is not slowed much compared with a 2L phase leg. A similar conclusion is also drawn in [15].

The detailed analytical transient waveform comparison under the same short-loop inductance is shown in Fig. 10. For a 2L phase leg, the voltage rise-time is 15 ns. In a 3L phase leg, when the two loops have the same inductance, the voltage rise-time is 18.5 ns, which indicates a 23% increase. Meanwhile, when the long-loop inductance is five times higher than the short loop inductance, the voltage rise-time increase is less than 1 ns.

In Figs. 8–10, it can be summarized that the overvoltage on the line frequency device is normally more severe, and the switching speed of the high switching frequency device is not impacted. Thus, the line switching frequency device deserves more analysis.

Fig. 11 shows the relationship between the overvoltage on the line switching frequency device and the voltage fall time of the excitation S_{1L} as well as the long-loop inductance L_{lg}. Although the relationship is not purely monotonic, generally larger L_{lg} and lower t_{vf_1L} result in higher overvoltage.

IV. Modeling of Device Overvoltage With Modulation 1-B

A. Loop Analysis and Modeling

For modulation 1-B, the three nonactive switches ($S_{1H} - S_{3H}$ in Fig. 2) are OFF during the half-line cycle. It makes the analysis more complicated because the voltage distribution on these switches is changing during the commutation between S_{1L} and S_{3L}. Not only the transient overvoltage but also the steady-state voltage within a switching cycle should be evaluated.

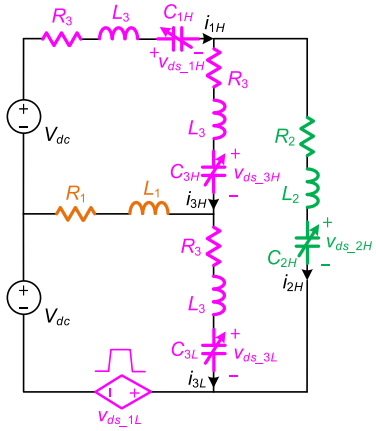

Fig. 12. Equivalent circuit of single phase leg during half-line cycle with modulation 1-B.

The equivalent circuit with modulation 1-B is plotted in Fig. 12. In addition to the nonactive line switching frequency device S_{2H}, both nonactive high switching frequency devices S_{1H} and S_{3H} are involved.

State-space analysis is again adopted to build the analytical voltage response model. The instantaneous voltage and current relationship is derived as

$$\begin{cases} V_{\rm dc} = L_3\frac{di_{1H}}{dt} + v_{ds\_1H} + R_3 i_{1H} + L_3\frac{di_{3H}}{dt} + v_{ds\_3H} \\ \qquad +R_3 i_{3H} + L_1\left(\frac{di_{3H}}{dt} - \frac{di_{3L}}{dt}\right) + R_1\left(i_{3H} - i_{3L}\right) \\ V_{\rm dc} = L_3\frac{di_{3L}}{dt} + v_{ds\_3L} + R_3 i_{3L} + v_{ds\_1L} \\ \qquad +L_1\left(\frac{di_{3L}}{dt} - \frac{di_{3H}}{dt}\right) + R_1\left(i_{3L} - i_{3H}\right) \\ L_3\frac{di_{3L}}{dt} + v_{ds\_3L} + R_3 i_{3L} + L_3\frac{di_{3H}}{dt} + v_{ds\_3H} + R_3 i_{3H} \\ = L_2\left(\frac{di_{1H}}{dt} - \frac{di_{3H}}{dt}\right) + v_{ds\_2H} + R_2\left(i_{1H} - i_{3H}\right) \\ C_{1H}\frac{dv_{ds\_1H}}{dt} = i_{1H} \\ C_{2H}\frac{dv_{ds\_2H}}{dt} = i_{1H} - i_{3H} \\ C_{3H}\frac{dv_{ds\_3H}}{dt} = i_{3H} \\ C_{3L}\frac{dv_{ds\_3L}}{dt} = i_{3L}. \end{cases} \tag{4}$$

The detailed equations and matrices of the model are derived in Appendix B.

B. Analysis of Overvoltage

In Fig. 12, the line switching frequency device S_{2H} is no longer equivalently paralleled with S_{3L}. When S_{3L} is ON, there is initial voltage across the drain source of S_{2H}. For a typical power device, the output capacitance shown in Fig. 5 can be approximately divided into two regions [11]. When the drain–source voltage is low, the capacitance decreases rapidly as the voltage increases, and this is the main nonlinear region. On the other hand, the capacitance does not change much after the voltage reaches a certain threshold (normally less than 1/10 of the voltage rating). Therefore, if the initial voltage on the switch is higher than this threshold, the influence of the capacitance nonlinearity can be significantly mitigated.

The switching transient waveforms based on the established model is illustrated in Fig. 13. The initial voltage on S_{2H} is 120 V. The modulation 1-B reduces the overvoltage of the

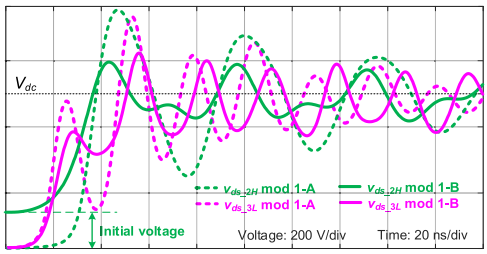

Fig. 13. Voltage transient waveforms with different control based on established model.

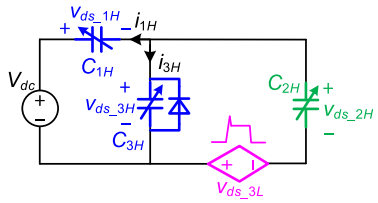

Fig. 14. Equivalent circuit of single phase leg with modulation 1-B for steady-state analysis.

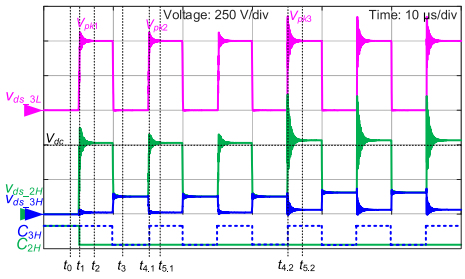

Fig. 15. Waveforms with modulation 1-B based on established model.

high switching frequency device by 124 V compared to the modulation 1-A, and a reduction of 188 V in the line switching frequency device is achieved.

C. Analysis of Steady-State Voltage

Since there is voltage distribution among the nonactive switches, this distribution is worth investigating because the steady-state voltage in different switching states can introduce extra loss and increase the voltage stress. Moreover, the reduction of the transient overvoltage is highly dependent on the initial voltage of the line switching frequency device.

To simplify the analysis, the loop inductances are neglected as they only affect the transient. v_{ds_3L} is modeled as a trapezoidal pulse with overvoltage. The equivalent circuit is shown in Fig. 14.

In addition, the nonlinear output capacitance is simplified as two discrete values [11]

$$C_{\text{oss}} = \begin{cases} nC & 0 \le v_{ds} \le \frac{V_{\text{dc}}}{m} \\ C & v_{ds} > \frac{V_{\text{dc}}}{m} \end{cases} \quad (n, m > 1) \tag{5}$$

where m and n are the coefficients that determine the threshold and the nonlinearity of the capacitance, respectively.

The operating waveforms are shown in Fig. 15. Assume the voltage across S_{3L}, S_{2H}, and S_{3H} is zero at t_0. At t_1, v_{ds_3L} rises from 0 to V_{pk1}, which includes the overvoltage. v_{ds_2H} follows v_{ds_3L} and increases to its peak value while v_{ds_3H} remains zero. At t_1, C_{2H} and C_{3H} equal to C and nC.

From t_1 to t_2, v_{ds_3L} finishes the dynamic resonance and drops back to V_{dc}. The relationship between v_{ds_3H} and v_{ds_2H} can be expressed as

$$\begin{aligned} v_{ds\_3H}(t_2) &= \frac{1}{nC}\int_{t_1}^{t_2} i_{3H}dt = v_{ds\_2H}(t_2) - V_{\text{dc}} \\ &= V_{pk1} - V_{\text{dc}} - \frac{n+1}{nC}\int_{t_1}^{t_2} i_{3H}dt. \end{aligned} \tag{6}$$

Assuming $V_{pk1} = (1+k_1)V_{\text{dc}}$ and $0 < k_1 < 1$, v_{ds_3H} and v_{ds_2H} at t_2 can be calculated by

$$\begin{cases} v_{ds\_3H}(t_2) = \frac{1}{nC}\int_{t_1}^{t_2} i_{3H}dt = \frac{k_1}{n+2}V_{\text{dc}} \\ v_{ds\_2H}(t_2) = v_{ds\_3H}(t_2) + V_{\text{dc}} = \left(1 + \frac{k_1}{n+2}\right)V_{\text{dc}}. \end{cases} \tag{7}$$

At t_3, v_{ds_3L} has decreased to 0. S_{2H} and S_{3H} are in parallel, and $v_{ds\_2H} = v_{ds\_3H}$. Note that during the switching transition, C_{3H} changes from nC to C. v_{ds_3H} and v_{ds_2H} at t_3 is calculated as

$$v_{ds\_3H}(t_3) = v_{ds\_2H}(t_3) = \frac{m(k_1+1) - n + 1}{3m}V_{\text{dc}}. \tag{8}$$

At $t_{4.1}$, v_{ds_3L} and v_{ds_2H} reach the peak in the new switching cycle. Because of the initial voltage of v_{ds_2H}, the overvoltage is lower than the previous switching cycle. Note that C_{3H} changes from C to nC during the switching. Assuming $V_{pk2} = (1+k_2)V_{\text{dc}}$ and $0 < k_2 < k_1 < 1$, v_{ds_3H} and v_{ds_2H} at $t_{4.1}$ are expressed as

$$\begin{cases} v_{ds\_3H}(t_{4.1}) = v_{ds\_3H}(t_3) - \frac{1}{C_{3H}}\int_{t_3}^{t_{4.1}} i_{3H}dt = \frac{k_1-k_2}{n+2}V_{\text{dc}} \\ v_{ds\_2H}(t_{4.1}) = v_{ds\_3H}(t_{4.1}) + V_{pk2} \\ \qquad\qquad = \frac{m(k_1+1)+(n+1)(k_2+1)}{n+2}V_{\text{dc}}. \end{cases} \tag{9}$$

After v_{ds_3L} and v_{ds_2H} recover from the dynamic peak at $t_{5.1}$, v_{ds_3H} and v_{ds_2H} are

$$\begin{cases} v_{ds\_3H}(t_{5.1}) = v_{ds\_3H}(t_{4.1}) + \frac{1}{nC}\int_{t_{4.1}}^{t_{5.1}} i_{3H}dt = \frac{k_1}{n+2}V_{\text{dc}} \\ v_{ds\_2H}(t_{5.1}) = v_{ds\_3H}(t_{5.1}) + V_{\text{dc}} = \left(1 + \frac{k_1}{n+2}\right)V_{\text{dc}}. \end{cases} \tag{10}$$

If the overvoltage of S_{3H} increases due to the change of load, v_{ds_3H} drops to 0 and is clamped by the body diode before v_{ds_3L} and v_{ds_2H} rise to their peak value at $t_{4.2}$. As a result, the condition at $t_{4.2}$ is the same as t_1 except for the voltage peak value. Assuming $V_{pk3} = (1+k_3)V_{\text{dc}}$ and $0 < k_1 < k_3 < 1$, v_{ds_3H} and v_{ds_2H} from $t_{4.2}$ to $t_{5.2}$ follow the same process as from t_1 to t_2

$$\begin{cases} v_{ds\_3H}(t_{5.2}) = \frac{1}{nC}\int_{t_{4.2}}^{t_{5.2}} i_{3H}dt = \frac{k_3}{n+2}V_{\text{dc}} \\ v_{ds\_2H}(t_{5.2}) = v_{ds\_3H}(t_{5.2}) + V_{\text{dc}} = \left(1 + \frac{k_3}{n+2}\right)V_{\text{dc}}. \end{cases} \tag{11}$$

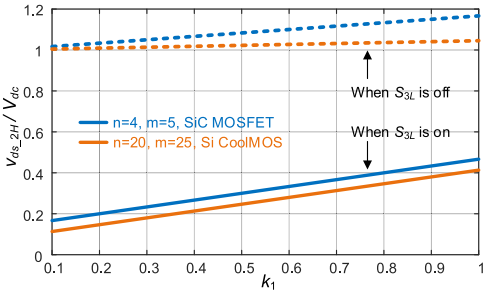

Fig. 16. Relationship between steady-state v_{ds_2H} and k_1 with different devices.

Comparing (7), (10), and (11), it is observed that the steady-state v_{ds_3H} and v_{ds_2H} are only dependent on the highest peak v_{ds_3L} that occurs in the previous pulses.

The relationship between the steady-state v_{ds_2H} and the overvoltage coefficient k_1 for two kinds of devices is calculated based on the model in Appendix B and is plotted in Fig. 16. The initial voltage across S_{2H} when S_{3L} is ON is always higher than $V_{\rm dc}/m$, which indicates that modulation 1-B can keep the device output capacitance out of the nonlinear region and reduce the overvoltage. Moreover, the steady-state v_{ds_2H} when S_{3L} is OFF does not exceed 1.2 times of the dc voltage. Therefore, the steady-state voltage stress on the device is not increased significantly.

V. Loop Layout Design for 3L-ANPC Converter

In addition to the nonlinearity of the device output capacitance, high loop inductance is also a main cause of the overvoltage. To reduce the loop inductance, the layout of the converter requires careful design. There are two main methods to minimize the loop inductance: first, decrease the loop area as the magnetic flux is proportional to the area, and second, decrease the distance between two currents with opposite directions so that the magnetic cancellation effect is better utilized [32].

A. PCB Layout With Discrete Devices

In the design of multilayer PCBs, two main layout structures are usually adopted: The lateral layout and the vertical layout [33], [34]. Fig. 17 presents an example of the two layout methods for a 20-kW SiC MOSFET based 3L-ANPC converter phase leg. In the lateral layout, as shown in Fig. 17(a), the placement of the devices follows the circuit schematic drawing, where two line frequency devices are next to the four high switching frequency devices. This layout is straightforward and can utilize multiple copper layers to conduct current in parallel. However, the penalty is that the whole loop is at one layer and unavoidably results in a large area.

For the vertical layout in Fig. 17(b), all six devices are located in a line and the loops are perpendicular to the PCB layers. The loop inductance can be reduced due to the small section area and the magnetic cancellation between the two PCB layers with opposite currents. Based on the simulation in ANSYS Q3D, the loop inductance of the long loop with the lateral layout is 57 nH, while that in the vertical layout is 12 nH.

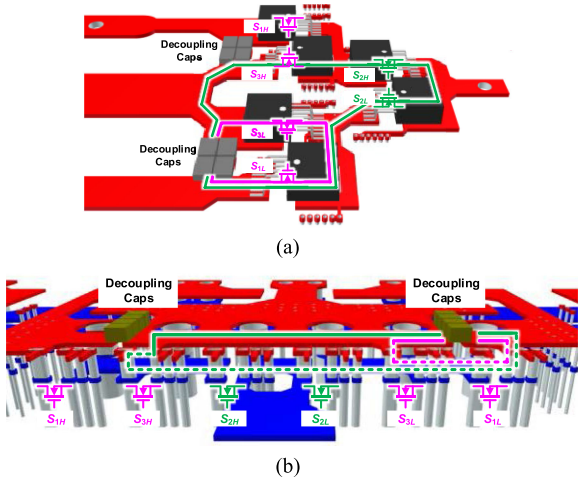

Fig. 17. Examples of PCB design layout. (a) Lateral. (b) Vertical.

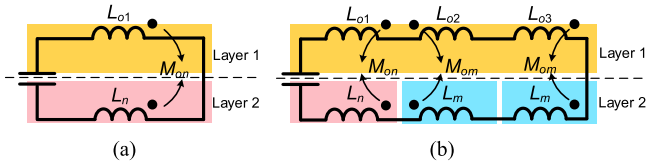

Fig. 18. Equivalent circuits of commutation loops considering mutual inductance. (a) Short loop. (b) Long loop.

B. Busbar Design With Power Modules

In high-power applications, power modules are normally implemented, and busbars are the main connectors between different components. Extensive work has been conducted for the busbar design, and a laminated structure is usually used [35], [36]. To minimize the loop inductance, it is preferred to increase the magnetic cancellation between two adjacent busbar layers. An example of designing a two-layer busbar for a 3L-ANPC converter phase leg is given as follows.

According to Fig. 3, the short loop only includes two busbar parts: the neutral busbar and the negative (or positive) busbar. So, the two parts should be laminated and located in two layers. The long loop consists of four busbar parts: the neutral busbar, negative busbar, and two middle busbars. The middle busbars and the negative busbar are placed in the same layer. The neutral busbar is a whole plate and serves as the return path of the loop.

The equivalent circuits of the loops considering the busbar structure are illustrated in Fig. 18. From the perspective of loop inductance, the magnetic cancellation introduces a negative mutual inductance in the loop in addition to the self-inductance of each busbar part. For the short loop, the negative and neutral busbar are coupled, and the absolute value of the mutual inductance is $M_{\rm on}$. The total short-loop inductance $L_{st} = L_{o1} + L_n - M_{\rm on}$. For the long loop, the negative and middle busbars are coupled with the neutral busbars. The absolute value of the mutual inductance between middle and neutral busbars is M_{om}. The total loop inductance $L_{lg} = L_o + L_n + 2L_m - M_{\rm on} - 2M_{om}$. Note that the effective self-inductance of the neutral busbar in the short loop (L_{o1}) is smaller than that in the long loop

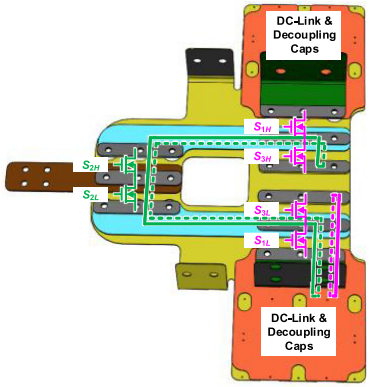

Fig. 19. Laminated busbar design for 3L-ANPC phase leg.

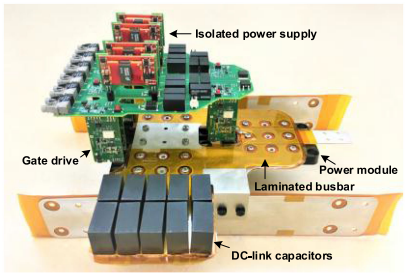

Fig. 20. Prototype of 3L-ANPC converter phase leg.

($L_o = L_{o1} + L_{o2} + L_{o3}$). With this design, the negative mutual inductance can be increased with the current flowing in opposite directions in two adjacent busbar layers, resulting in lower total loop inductance. Fig. 19 shows the finalized laminated busbar design with two loops highlighted. Based on the Q3D simulation, the loop inductances of the short and long loop are 4 and 13 nH excluding the decoupling capacitors and the power modules.

VI. Experimental Results and Discussion

A 500-kVA 3L-ANPC converter based on SiC MOSFETs was built to verify the analytical model. The dc-bus voltage $V_{\rm dc}$ is $\pm$500 V, and the line-to-line output voltage rms value is 600 V. The switching frequency of the SiC MOSFETs is 60 kHz, and the output line frequency is 3 kHz. The 900 V HT-3000 series SiC MOSFET module from Wolfspeed is used for all switches. The laminated busbar shown in Fig. 19 was fabricated and implemented. A phase leg of the converter prototype is shown in Fig. 20.

Five line cycles with full voltage and load are generated to verify the electrical performance of the converter. Modulation 1-A is employed first, and the voltage waveforms of the SiC MOSFETs in one line cycle as well as the zoom in switching transient are illustrated in Fig. 21. The applied gate resistance is 2.5 Ω, with which the *dv/dt* of v_{ds_1L} is 10 V/ns. The peak voltage of S_{3L} is 754 V, while that of S_{2H} is 736 V. Based on the resonant frequency of the voltage, it is calculated that the parasitic inductances of the short and long loop are 6.5 and 17.5 nH, respectively. They are lower than the parasitic inductances found in NPC type converters in existing references

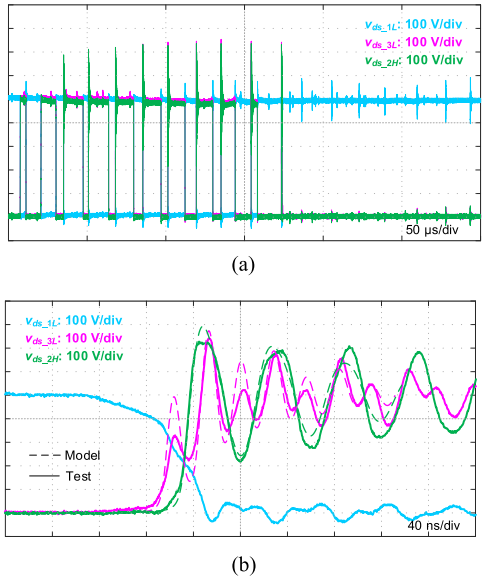

Fig. 21. Tested switching waveforms with modulation 1-A ($R_g = 2.5\,\Omega$). (a) One line cycle. (b) Switching transient.

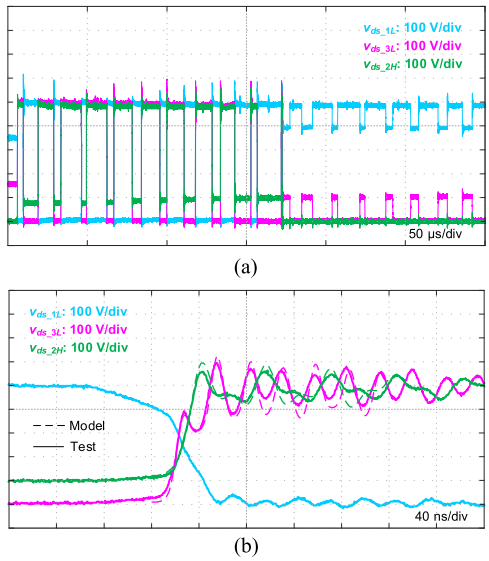

Fig. 22. Tested switching waveforms with modulation 1-B ($R_g = 2.5\,\Omega$). (a) One line cycle. (b) Switching transient.

[14], [25], [37]–[39], which indicates the effectiveness of the evaluation in Section V-B.

Fig. 22 plots the waveforms with modulation 1-B. The peak voltages of S_{3L} and S_{2H} are 592 and 560 V, respectively. The overvoltage is significantly reduced compared with the tested results of modulation 1-A under the same switching speed and parasitic inductances, which validates the attenuation of the nonlinear capacitance influence shown in Section IV-B.

With modulation 1-B, it is possible to increase the switching speed. Fig. 23 shows the tested waveforms when the gate resistance is reduced from 2.5 to 1.3 Ω. The peak voltages of the two devices are 702 and 806 V, which are still lower than the voltage rating (900 V). The envelope of the peak voltage and

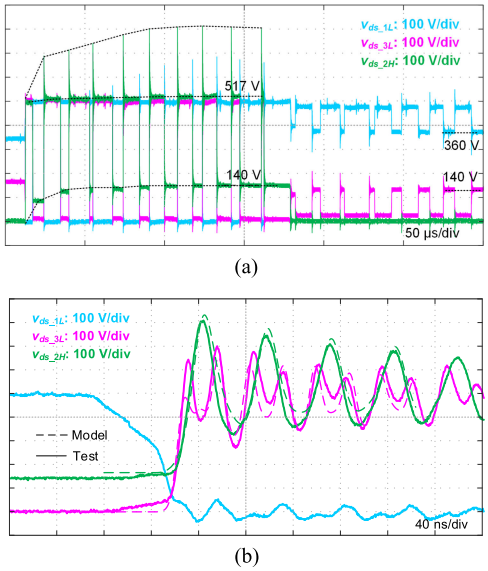

Fig. 23. Tested switching waveforms with modulation 1-B ($R_g = 1.3\,\Omega$). (a) One line cycle. (b) Switching transient.

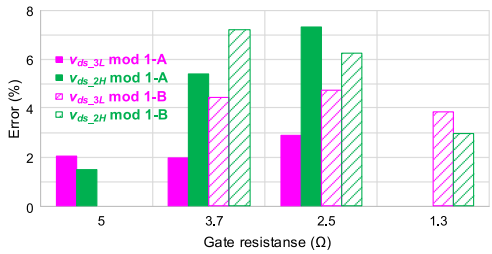

Fig. 24. Error of drain–source peak voltage between model estimation and tested results with different gate resistance.

steady-state voltage of S_{2H} is highlighted in Fig. 23(a). As the peak voltage increases, the steady-state voltage also increases, which matches with the analysis in Section IV-C. The *dv*/*dt* of v_{ds_1L} is 18 V/ns.

In Figs. 21(b), 22(b), and 23(b), the tested waveforms are compared with the analytical model results. The error of device drain–source peak voltage between the model and tested results with different gate resistances is shown in Fig. 24. The error is lower than 8%. The mismatch is mainly caused by the following reasons.

1) The excitation is assumed to have an ideal trapezoidal shape in the model. However, the actual voltage rise and drop is not linear, as shown in v_{ds_1L} of Figs. 21–23.
2) The coupling between different busbar parts is complicated, and it leads to errors when using a single inductance value to represent the inductance of each part.
3) The model of high frequency ac resistance is an estimate, making the prediction of the amplitude after the first peak pulse to not match exactly. Nevertheless, the analytical model is good enough to show the trend of the overvoltage.

Since the two modulations cause different steady-state drain–source voltages on the devices, the output capacitance loss $E_{\rm oss}$ varies. The capacitance energy loss of a device during one

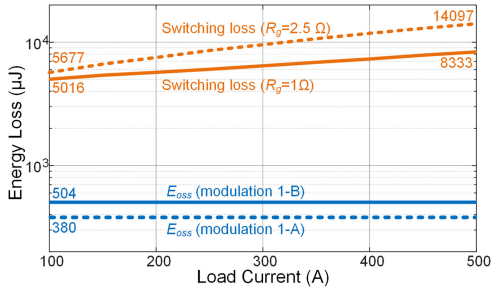

Fig. 25. Comparison of output capacitance loss and switching loss with different modulations.

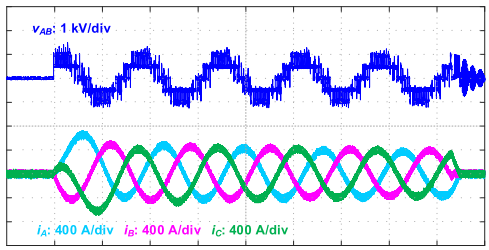

Fig. 26. Tested output waveforms of 3L-ANPC converter.

switching cycle is calculated as

$$E_{\rm oss} = \frac{1}{2}\left|C\left(V_{ds\_h}\right)\cdot V_{ds\_h}^2 - C\left(V_{ds\_l}\right)\cdot V_{ds\_l}^2\right| \qquad (12)$$

where V_{ds_h} and V_{d_l} are, respectively, the high and low steady-state drain–source voltages in one switching cycle.

Fig. 25 compares $E_{\rm oss}$ of the two modulations with the switching loss from the device datasheet. Modulation 1-B introduces 124 μJ more $E_{\rm oss}$ in each switching cycle than modulation 1-A. Therefore, with the same switching speed of the high switching frequency devices, modulation 1-B has higher switching loss. However, the lower overvoltage with modulation 1-B allows a higher switching speed. Compared to the switching loss reduction by increasing the switching speed, as shown in Fig. 25, the increased $E_{\rm oss}$ can be neglected.

Fig. 26 plots the tested output line-to-line voltage and phase currents with five generated line cycles at full voltage and load condition. The dynamic peak phase current reaches 680 A.

VII. Conclusion

This article develops an analytical model for the device overvoltage in 3L-ANPC converters. Two loops exist during the switching transient in the analyzed two modulations, which results in coupling effect between the high and line switching frequency devices. According to the investigation with the model established in this article, several conclusions can be drawn.

1) The nonlinearity of the device output capacitance shows significant influence on the device overvoltage.
2) The line switching frequency device usually has higher overvoltage than the high switching frequency device.
3) The resonant frequency of the line switching frequency device is lower than the high switching frequency device.

4) The switching speed of the high switching frequency device is not impacted by the coupling effect of the line switching frequency device when the long-loop inductance is much larger than the short one.

Comparing the two modulations, turning OFF the nonactive clamping switch can build initial voltage across the line switching frequency device, which helps the device output capacitance avoid the nonlinear region, and the overvoltage is decreased. Design rules on PCB and busbar layout for the 3L-ANPC converters are provided to reduce the loop inductance. Vertical loop layout is preferred and the magnetic cancellation should be fully utilized. Following the busbar design rules, a 500-kVA 3L-ANPC converter with 60 kHz switching frequency based on SiC MOSFETs is built and tested with several line cycle pulses. The overvoltage model of the two modulations and the busbar loop inductance are verified. With the nonactive clamping switch OFF, 162 and 176 V overvoltage reduction is achieved for the high and line switching frequency devices.

APPENDIX A

By applying the state space, (1) in modulation 1-A can be written in the format of

$$\dot{X}(t) = AX(t) + BU(t). \tag{13}$$

$X = [i_3\, i_2\, v_{ds\_3L}\, v_{ds\_2H}]^T$ is the state vector. The analysis begins when v_{ds_1L} starts to drop. At this moment, $i_3 = i_2 = v_{ds\_3L} = v_{ds\_2H} = 0$. So the initial state $X_0 = [0\,0\,0\,0]^T$.

$U = V_{\rm dc} - v_{ds\_1L}$ is the input vector. Here, v_{ds_1L} is assumed to drop linearly during turn-ON

$$v_{ds\_1L}(t) = \begin{cases} V_{ds\_1L\_0}\left(1 - \frac{t}{t_{vf\_1L}}\right) & t \le t_{vf\_1L} \\ 0 & t > t_{vf\_1L} \end{cases} \tag{14}$$

where $V_{ds\_1L\_0}$ is the initial voltage of S_{1L} and is expressed as

$$V_{ds\_1L\_0} = V_{\rm dc} - (L_1 + L_3)\frac{di_{1L}}{dt} \tag{15}$$

where i_{1L} is the current flowing through S_{1L}.

A and *B* are state and input matrices, and they can be derived as (16), shown at the bottom of this page

$$K = 1 + \frac{L_1}{L_2} + \frac{L_1}{L_3}. \tag{17}$$

APPENDIX B

For modulation 1-B, (4) is also unified into (13). $X = [i_{1H}\, i_{3H}\, i_{3L}\, v_{ds\_1H}\, v_{ds\_2H}\, v_{ds\_3H}\, v_{ds\_3L}]^T$ is the state vector. $U = [V_{\rm dc}\, v_{ds\_1L}]^T$ is the input vector. v_{ds_1L} is still assumed to drop linearly during turn-ON as in (14).

The state and input matrixes *A* and *B* are expressed as (18) and (19), shown at the bottom of this page.

$$A = \begin{bmatrix} -\frac{(R_1+R_3)L_2+R_3L_1}{KL_2L_3} & -\frac{R_1L_2-R_2L_1}{KL_2L_3} & -\frac{L_1+L_2}{KL_2L_3} & \frac{L_1}{KL_2L_3} \\ -\frac{R_1L_3-R_3L_1}{KL_2L_3} & -\frac{(R_2+R_3)L_3+R_2L_1}{KL_2L_3} & \frac{L_1}{KL_2L_3} & -\frac{L_1+L_3}{KL_2L_3} \\ \frac{1}{C_{3L}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{2H}} & 0 & 0 \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{KL_3} & \frac{1}{KL_2} & 0 & 0 \end{bmatrix}^T \tag{16}$$

$$A = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & -\frac{2L_1L_3+L_3^2}{M} & -\frac{L_1L_2+L_2L_3}{M} & -\frac{L_1L_2}{M} \\ a_{21} & a_{22} & a_{23} & -\frac{L_1L_2+L_2L_3}{M} & \frac{L_1L_3+L_3^2}{M} & a_{26} & -\frac{L_1L_2+L_1L_3}{M} \\ a_{31} & a_{32} & a_{33} & -\frac{L_1L_2}{M} & \frac{L_1}{M} & -\frac{L_1L_2+L_1L_3}{M} & a_{37} \\ \frac{1}{C_{1H}} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{2H}} & -\frac{1}{C_{2H}} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{3H}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{3L}} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{18}$$

$$B = \begin{bmatrix} \frac{2L_1L_2+4L_1L_3+L_2L_3+2L_3^2}{M} & \frac{2L_1L_2+L_2L_3-L_3^2}{M} & \frac{2L_1L_2+2L_2L_3+L_3^2}{M} & 0 & 0 & 0 & 0 \\ -\frac{L_1L_2+2L_1L_3+L_3^2}{M} & -\frac{L_1L_2-L_3^2}{M} & -\frac{L_1L_2+2L_2L_3+L_3^2}{M} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{19}$$

$$a_{11} = -\frac{R_2(2L_1L_3+L_3^2)+R_3(L_1L_2+2L_1L_3+L_2L_3+L_3^2)}{M} \qquad a_{12} = -\frac{R_1L_2L_3-R_2(2L_1L_3+L_3^2)+R_3(L_1L_2+L_2L_3)}{M}$$

$$a_{13} = \frac{R_1L_2L_3-R_3L_1L_2}{M} \qquad a_{14} = -\frac{L_1L_2+2L_1L_3+L_2L_3+L_3^2}{M}$$

$$a_{21} = -\frac{R_2(L_1L_3+L_3^2)-R_3(L_1L_2+L_2L_3)}{M} \qquad a_{22} = -\frac{R_1(L_2L_3+L_3^2)+R_2(L_1L_3+L_3^2)+R_3(L_1L_2+L_1L_3+L_2L_3+L_3^2)}{M}$$

$$a_{23} = -\frac{R_1(L_2L_3+L_3{}^2)-R_3(L_1L_2+L_1L_3)}{M} \qquad a_{26} = -\frac{L_1L_2+L_1L_3+L_2L_3+L_3^2}{M}$$

$$a_{31} = -\frac{R_2L_1L_3+R_3L_1L_2}{M} \qquad a_{32} = \frac{R_1(2L_2L_3+L_3^2)-R_2L_1L_3-R_3(L_1L_2+L_1L_3)}{M}$$

$$a_{33} = -\frac{R_1(2L_2L_3+L_3^2)+R_3(L_1L_2+L_1L_3+2L_2L_3+L_3^2)}{M} \qquad a_{37} = -\frac{L_1L_2+L_1L_3+2L_2L_3+L_3^2}{M}$$

$$M = L_3(3L_1L_2 + 2L_1L_3 + 2L_2L_3 + L_3^2)$$

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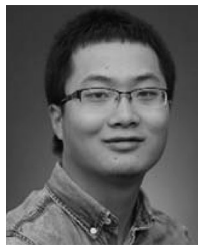

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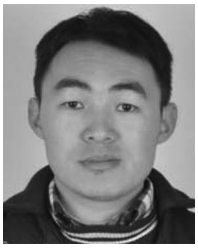

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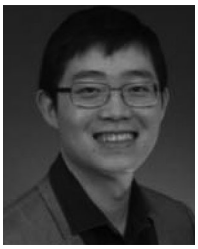

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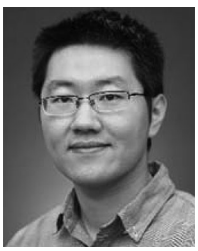

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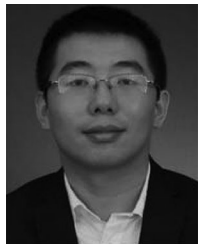

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