Localization and Detection of Bond Wire Faults in Multichip IGBT Power Modules

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***Abstract*—Multichip insulated gate bipolar transistor (mIGBT) power modules (PMs) degrade over power cycling. Bond wire lift–off is one of the major failure modes. This article presents a technique to diagnose bond wire lift-off by analyzing the ON-state voltages across collector and emitter terminals and the voltages across collector and Kelvin emitter terminals. The proposed method can indicate the first lift-off out of 37 bond wires in a mIGBT. The main novelty of the proposed technique is that it can locate the chip that has bond wire lift-off(s). In addition, the temperature dependence of the proposed approach is negligible. The article describes the proposed technique in detail and shows results and discussions based on practical tests which are carried out on two mIGBT PMs with different packages.**

***Index Terms*—Bond wire lift-off, fault diagnosis, multichip insulated gate bipolar transistor (mIGBT).**

I. Introduction

THE insulated gate bipolar transistor (IGBT) is one of the most commonly used semiconductors in power electronics. Today the power capability of a single IGBT power module (PM) has been boosted up to kiloampere [1], [2]. These IGBT PMs are realized through multichip paralleled package to achieve the required high current level. However, the increase in paralleling chips within one package will introduce severe thermal stress on the module and as such affects its lifetime. It is reported that about 21% of the power converter failures are attributed to semiconductors [3]. Solder fatigue and bond wire failures are reported as the most common failures that occur over lifetime [4]–[6]. This article is going to focus on the bond wire failure.

A large number of research papers have been published, proposing different detection methods for bond wire lift-off [7]–[14]. Techniques proposed have been applied either intrusively on opened PMs with direct access to bond wires or non-intrusively on unopened package measuring voltages and currents at available terminals: the collector *C*, the emitter *E*, the gate *G*, and the auxiliary emitter AE, which provides the return path for the gate current, and the Kelvin emitter KE which acts as sensing point if provided.

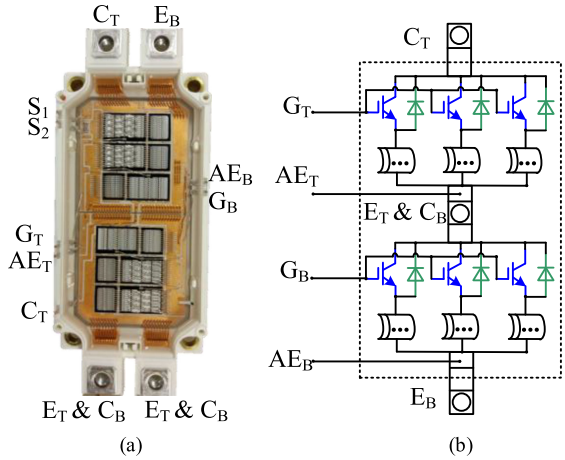

Fig. 1. Infineon 1.7 kV 600 A half-bridge IGBT PM (FF600R17ME4). (a) Interior view. (b) Terminal illustration.

Fig. 1(a) shows the layout of the terminals in a half-bridge IGBT PM, Infineon FF600R17ME4, which has three IGBT chips and three antiparallel diodes in parallel for the top switch and the same design for the bottom switch. In Fig. 1(a), the terminals of the top switch are labeled by the index T and the terminals of the bottom switch are labeled by the index B. As in most standard PMs illustrated in Fig. 1(a), the collector of the top IGBT chips is soldered onto the direct copper bonded (DCB) layer that is connected with the C_T terminal. The collector of the bottom chips is also soldered to the DCB, but connected to C_B. The emitter of the IGBT chips is attached to the DCB through bond wires. The emitter terminals for load current are E_T and E_B for the top and the bottom switch individually. In the half-bridge topology, E_T and C_B share the same terminal. G_T and G_B are the gate terminals for the top and the bottom switch, respectively. AE_T and AE_B terminals are connected via wires with the corresponding emitter tracks for E_T and E_B on the DCB layer. Both terminals provide the current return paths for the gate drives. Fig. 1(b) shows the schematic of the PM along with the terminals.

There are seven signal terminals, as shown in Fig. 1(a), along the edge of the PM frame (G_T, AE_T, C_T, AE_B, G_B, S_1, and S_2)

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TABLE I
COMPARISON OF EXISTING TECHNIQUES FOR BOND WIRE STATE ESTIMATION

Detection type	Involved terminals	Signatures	Number of IGBT chips each switch	Total number of bond wires in one switch	Number of first detected bond wires lift-off – sensitivity
Intrinsic signatures	C-E	$V_{\text{CE(on)}}$ [7]	1	6	First – 20 mV increase
		$V_{\text{CE(on)}}$ at the inflexion point [8]	1	5	Second – 9 mV increase
		$R_{\text{CE(on)}}$ [9]	2	8	Second – 0.1 mΩ increase
		$\Delta V_{\text{CE(turn-off)}}$ [10]	2	24	Fourth – 20 V increase
	G-AE	$V_{\text{G-AE}}$ [11]	2	12	Sixth – detects only if all bond wires are detached from one chip
		I_{G} [12]	2	12	Sixth – detects only if all bond wires are detached from one chip
	KE	Sense point [13]	2	4	First – 700 mV increase
Induced signatures	Open module	Temperature [14]	1	4	First – 0.5 °C increase

in the form of pins, where S_1 and S_2 are two terminals of the DCB temperature sensor. The position of these terminals is subject to manufacturer preferences and DCB layout.

In literatures [7]–[14], all of the five terminals (C, E, G, AE, and KE) have been used for bond wire degradation detection either by directly monitoring an electrical signal (intrinsic signature) that will change with bond wire lift-off or by stimulating and monitoring a responding signal (induced signature) where the responding signal correlates with bond wire lift-off. Table I summaries recent contributions in detecting bond wire lift-off.

A. Intrinsic Signatures

Intrinsic signatures are obtained by direct measurement of either the voltage across two of the five terminals or the current through any terminal.

*1) Signatures from Collector (*C*) and Emitter (*E*):* The ON-state voltage $V_{CE(\text{on})}$ measured across the terminals *C* and *E* has been widely exploited to monitor the bond wire state [15], [16]. However, $V_{CE(\text{on})}$ has also been popularized as a thermosensitive electrical parameter because of its linear relationship with temperature variation. Therefore, the bond wire state diagnosis based on $V_{CE(\text{on})}$ is influenced by the temperature of the chips. This dependency has been studied extensively.

For instance, authors in [7] proposed to measure $V_{CE(\text{on})}$ under sensing current (100 mA) as well as loading current (50 A) to decouple the influence of the virtual junction temperature T_{vj} and bond wire lift-off. This method has now been well established [5], [6], [17]. In [8], [18] and [19], the influence of T_{vj} is eliminated by taking advantage of the inflexion point at which the temperature dependence of $V_{CE(\text{on})}$ is negligible.

ON-state resistance $R_{CE(\text{on})}$ is the combination of $V_{CE(\text{on})}$ and I_C and has also been investigated as bond wire lift-off indicator [9], [20]. Advanced algorithms such as the recursive least square algorithm is used to exclude the impact from T_{vj}.

In online operation, the overshoot of V_{CE} during the turn-OFF transient, denoted as $\Delta V_{CE(\text{turn}-\text{off})}$ in Table I, has also been reported for bond wire lift-off prediction [10].

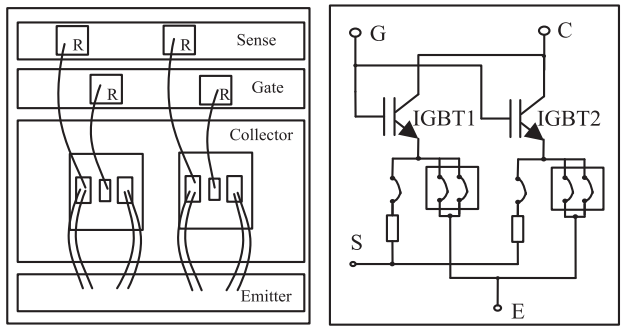

Fig. 2. Implementation of the sensing bond wires by redesign of the DCB layer (left) and its equivalent circuit diagram (right) [13].

2) Signatures From Gate and Auxiliary Emitter: In [11], [12], [21]–[23], voltage V_{G-AE} and gate peak current I_G during the turn-ON transient were proposed. These methods can only detect a complete chip failure meaning all bond wires have been lifted from one IGBT chip.

3) Signatures From Kelvin Emitter: In [13], sensing bond wires were introduced which were bonded across the DCB. As such additional tracks were formed on the DCB to connect the sensing bond wires with corresponding KE terminals. The implementation of the approach is depicted in Fig. 2. The DCB layer of the PM is redesigned to introduce the sensing terminal via the additional copper track, the additional sensing resistor, and the additional bond wires. The bond wires are used to connect the emitter side of the IGBT chip to the sensing point via the sensing resistor. The equivalent circuit is shown in Fig. 2. In the case a bond wire in one of the IGBT chip is lifted, the voltages measured via the sensing bond wire will shift. However, in order to include sensing bond wires, the DCB of the PM has to be redesigned. In addition, large resistive sense resistors are required to reduce the power loss caused by the measurement.

B. Induced Signatures

In order to detect induced signatures, voltage or current signals must be injected first. The response from these signals can then be measured.

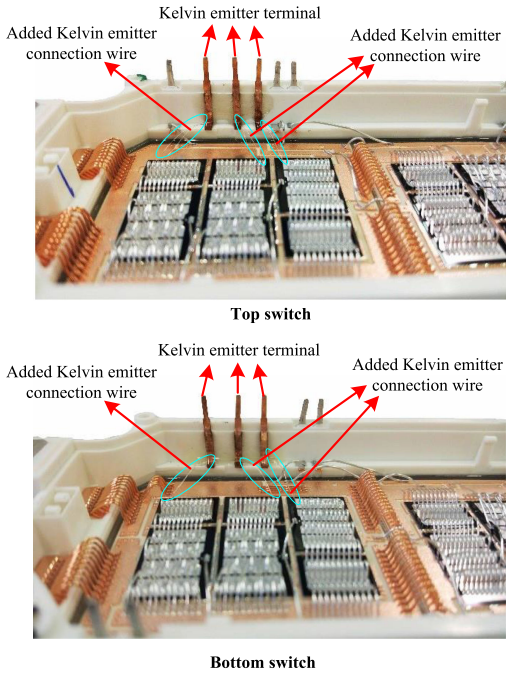

Fig. 3. Half bridge IGBT module with added pins for Kelvin emitter connection.

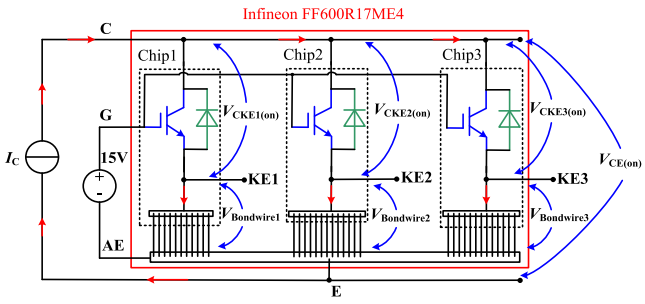

Fig. 4. Schematic of ON-state voltage measurement for FF600R17ME4.

Li *et al.* [14] proposed applying electromagnetic induction thermography to open PMs. In this method, the pulsed electromagnetic field produces eddy currents. The temperature distribution, as the response of the eddy current, changes when there is bond wire lift-off. This is used to detect bond wire states.

C. Research Gap

In principal, each technique described in Table I is able to detect bond wire lift-off. However, for most of them, the ratio of the earliest detection of failure to the total bond wire number is between two out of five to one out of six. Therefore, they are not suitable for detecting early bond wire lift-offs for mIGBT PMs with large number of bond wires. In addition, locating the bond wire lift-off has not been reported in any of these methods.

D. Contribution and Structure of this Article

This article proposes a method to detect and locate the early lifted bond wires in mIGBT PMs. The method makes use of the well-known ON-state voltage measurement across *C* and *E*. Meanwhile, voltages across terminals *C* and KE are measured. All measurement results are processed to identify the number of lifted bond wires and locate these lifted wires.

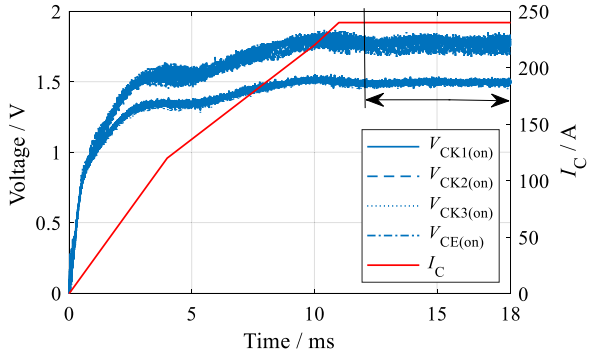

Fig. 5. Collector current and ON-state voltage waveforms upon current injection at $T_{vj} = 46$ °C.

This article is organized as follows. The proposed technique is described in Section II. The experimental set-up is presented in Section III including practical results on an Infineon IGBT module with three IGBT chips for each switch. The fault diagnosis regarding bond wire lift-off detection and location is presented in Section IV. A repeat of the test is carried out on a Dynex mIGBT PM and results are described in Section V to demonstrate that the method is applicable to PMs with different layouts. Section VI concludes this article.

II. Methodology of Proposed Technique

The proposed technique is demonstrated on the Infineon PM FF600R17ME4 using its bottom switch.

A. Modification for Kelvin Emitter Connection

The Kelvin connection is realized by introducing additional terminals as shown in Fig. 3. Thin copper wires, 50 μm in diameter, are used to connect the emitter side of the IGBT chip with the added Kelvin pins which are glued against the frame of the IGBT module. In this prototype, two wires are used for each IGBT chip. The Kelvin pins are copper. Compared with the technique in [13], the technique proposed in this article does not need any modification to the DCB layer. The extra Kelvin connection can be constructed with only limited modification to the mIGBT module.

B. Schematic for Experiment Setup

Fig. 4 illustrates the experimental setup for testing the bottom switch of FF600R17ME4 by showing the exact number of bond wires per chip. Three KE terminals (KE1, KE2, and KE3) are also introduced in addition to the existing four terminals *C*, AE, *E* , and *G*. Introduction of three additional terminals allows the measurement of seven voltages, three voltages across the three chips: $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$; three voltages across the bond wires connected to each IGBT chip:

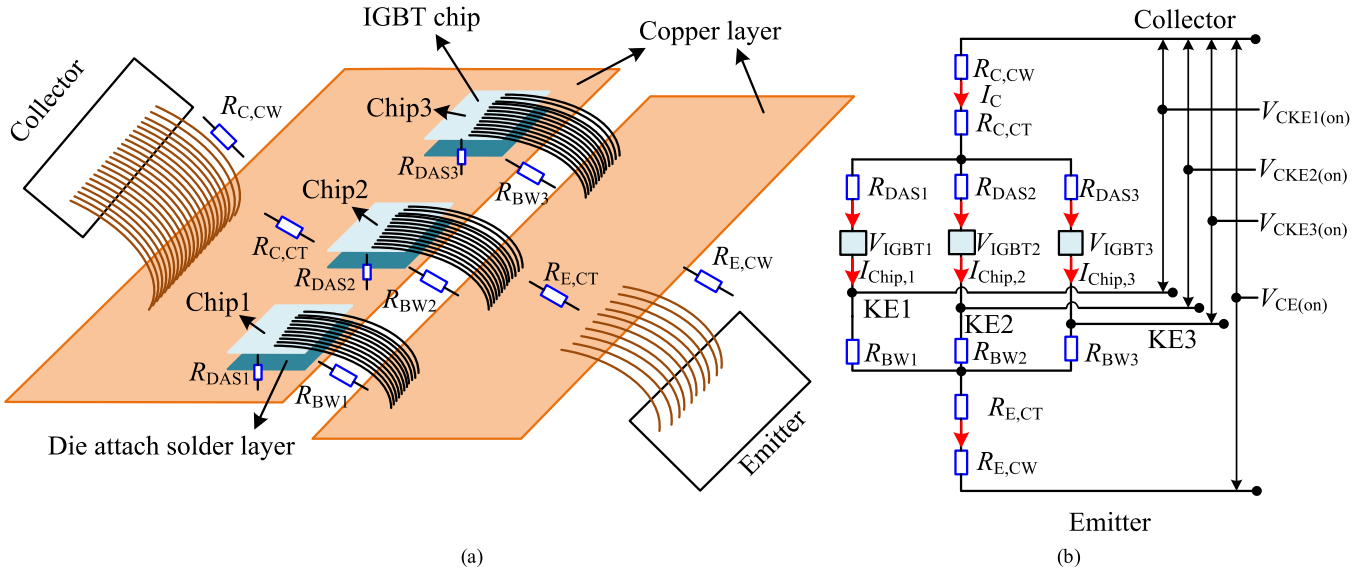

Fig. 6. (a) Illustration about components in the *C*–*E* and *C*–KE path. (b) Equivalent circuitry between *C*–*E*.

$V_{\mathrm{Bondwire1}}$, $V_{\mathrm{Bondwire2}}$, $V_{\mathrm{Bondwire3}}$; and the voltage across *C* and *E*: $V_{CE(\mathrm{on})}$.

The KE terminals KE1, KE2, and KE3 are directly bonded with the corresponding emitters of the IGBT chips as shown in Fig. 3. The voltages $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, and $V_{\mathrm{CKE3(on)}}$ are measured across C and KE1, KE2, and KE3, respectively, representing the ON-state voltages of the corresponding chips.

Fig. 5 is an example of the measurement at $T_{vj} = 46$ °C. The collector current is controlled by the TopCon power source. The current rises to 240 A in a step by step approach to compromise with the limitation of the TopCon device and to avoid overshot during the injection. Fig. 5 shows also the ON-state voltages $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$.

In these tests, each measurement is repeated twice. The rms values of voltage measurement in the region highlighted with arrow are the ON-state voltage for each measurement. The average value of the two measurements are used as the final voltage measurements. The final voltage measurements are used in the plot like Fig. 9.

C. $V_{CKE(\mathrm{on})}$ and $V_{CE(\mathrm{on})}$

The *C*–*E* circuitry of the bottom switch in Fig. 3 is exhibited in Fig. 6(a). All the influential parts are displayed. The collector terminal is linked to the copper layer via the copper wires. The collector copper wire are denoted as $R_{C,CW}$. The collector copper track is represented by $R_{C,CT}$. IGBT chips are soldered onto the copper layer. This solder layer is considered as pure resistance and the corresponding resistors are represented as R_{DAS1}, R_{DAS2}, and R_{DAS3} for chip 1, chip 2, and chip 3, respectively. The voltages across the IGBT chip collector pad and emitter pad are denoted as V_{IGBT1}, V_{IGBT2}, and V_{IGBT3} for the three IGBT chips. The emitter pad of the IGBT chip is connected to the emitter copper layer via bond wires. Then,

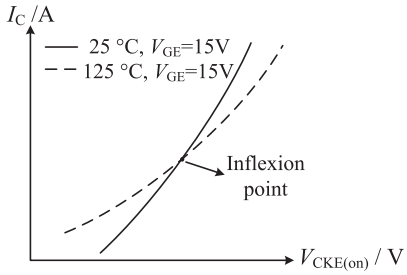

Fig. 7. Forward characteristic of an IGBT chip.

copper wires are used to connect the emitter copper track with the emitter terminal. The resistors of the bond wires are presented by R_{BW1}, R_{BW2}, and R_{BW3} for the three chips. The emitter copper track and emitter copper wires are pure resistance and denoted as $R_{E,CT}$ and $R_{E,CW}$ respectively.

Fig. 6(b) depicts the equivalent diagram of the *C*–*E* circuitry. $V_{\mathrm{CKE(on)}}$ and $V_{CE(\mathrm{on})}$ can be derived as below. It can be noted that the difference between $V_{\mathrm{CKE(on)}}$ and $V_{CE(\mathrm{on})}$ is the voltage across the bond wires, emitter copper track, and emitter copper wires

$$V_{\mathrm{CKE},i(\mathrm{on})} = I_C R_{C,CW} + I_C R_{C,CT} + I_{\mathrm{Chip},i} R_{\mathrm{DAS},i} + V_{\mathrm{IGBT},i} \quad (1)$$

where $i = 1, 2, 3$

$$V_{CE(\mathrm{on})} = I_C R_{C,CW} + I_C R_{C,CT} + I_{\mathrm{Chip},i} R_{\mathrm{DAS},i} + V_{\mathrm{IGBT},i} + I_{\mathrm{Chip},i} R_{BW} + I_C R_{E,CW} + I_C R_{E,CT}. \quad (2)$$

Note, as $R_{\mathrm{DAS},i}$, $V_{\mathrm{IGBT},i}$, and $R_{BW,i}$ are in parallel in (2), *i* is either only 1 or only 2 or only 3.

Fig. 7 shows the forward characteristic of an IGBT chip at constant gate emitter voltage V_{GE}. The figure shows that

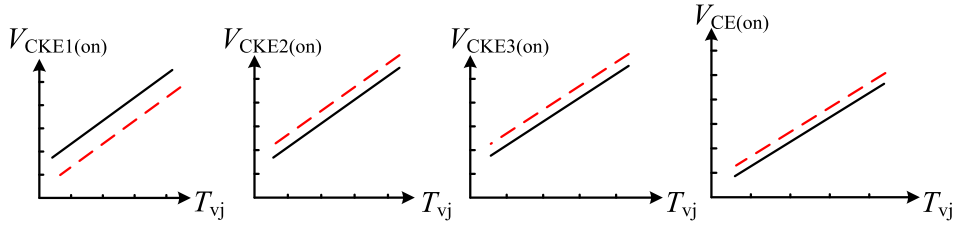

Fig. 8. ON-state voltage variation in the case of bond wire lift-off in chip 1. Solid line: healthy. Dashed line: lift-off in chip 1.

$V_{\mathrm{CKE(on)}}$ is nonlinear and influenced by the collector current I_C and T_{vj}. Above the inflexion point, $V_{\mathrm{CKE(on)}}$ at a particular current level rises at rising T_{vj} and below the inflexion point $V_{\mathrm{CKE(on)}}$ declines at rising T_{vj}.

Since the three IGBT chips are not exactly the same, each has its own ON-state forward characteristic, therefore: $V_{\mathrm{CKE1(on)}} \neq V_{\mathrm{CKE2(on)}} \neq V_{\mathrm{CKE3(on)}}$.

Parallel connected bond wires attached to an IGBT chip can be described with an equivalent resistance $R_{0,i}$ at T_0 and its temperature coefficient is β_i, where i is the chip number (i = 1, 2, 3). Thus, the voltage across the bond wires of chip i is

$$V_{BW,i} = R_{BW} I_{\mathrm{Chip},i} = (R_{0,i} + \beta_i (T_{vj} - T_0)) I_{\mathrm{Chip},i}. \quad (3)$$

The ON-state voltage $V_{CE(\mathrm{on})}$ can be described as given

$$V_{CE(\mathrm{on})} = V_{\mathrm{CKE1(on)}} + I_C R_{E,CW} + I_C R_{E,CT} + V_{BW1} \quad (4)$$

$$V_{CE(\mathrm{on})} = V_{\mathrm{CKE2(on)}} + I_C R_{E,CW} + I_C R_{E,CT} + V_{BW2} \quad (5)$$

$$V_{CE(\mathrm{on})} = V_{\mathrm{CKE3(on)}} + I_C R_{E,CW} + I_C R_{E,CT} + V_{BW3}. \quad (6)$$

Since I_C, $R_{E,CT}$, and $R_{E,CW}$ does not change upon bond wire lift-off, it is clear that if the bond wire voltage of chip i decreases the corresponding ON-state voltage of chip i must increase and vice-versa. This relationship can be used to determine bond wire conditions.

D. $V_{CKE(\mathrm{on})}$ and $V_{CE(\mathrm{on})}$ Change in the Case of Bond Wire Lift-Off

In order to illustrate the above on an example, it is assumed that one bond wire has lifted from chip 1 in Fig. 4. The IGBT switch is in ON-state by applying +15 V. The collector current is controlled by the dc current source. In this case one bond wire is lifted from chip 1, the equivalent resistance of the bond wires connecting to chip 1 will increase. Consequently, the collector current $I_{\mathrm{Chip\ 1}}$ flowing through chip 1 will decrease. In order to maintain the same current level from the dc current source, collector currents $I_{\mathrm{Chip\ 2}}$ and $I_{\mathrm{Chip\ 3}}$ flowing through the other two chips will increase respectively. As a result, $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, and $V_{\mathrm{CKE3(on)}}$ will change in different ways as indicated in

$$V_{\mathrm{CKE1(on)}} \downarrow, V_{\mathrm{CKE2(on)}} \uparrow, V_{\mathrm{CKE3(on)}} \uparrow. \quad (7)$$

TABLE II
VOLTAGE VARIATION IN THE CASE OF ONE BOND WIRE LIFT-OFF IN CHIP1

Chip	$V_{\mathrm{CKE(on)}}$	$V_{\mathrm{CE(on)}}$
Chip1	$V_{\mathrm{CKE1(on)}} \downarrow$	$\uparrow$
Chip2	$V_{\mathrm{CKE2(on)}} \uparrow$	$\uparrow$
Chip3	$V_{\mathrm{CKE3(on)}} \uparrow$	$\uparrow$

Accordingly, the bond wire voltages vary as

$$V_{BW1} \uparrow, V_{BW2} \uparrow, V_{BW3} \uparrow. \quad (8)$$

Despite individual voltage variations, the voltage $V_{CE(\mathrm{on})}$, summation of $V_{BW,i}$ and $V_{\mathrm{CKE},i(\mathrm{on})}$, always goes up when there is bond wire lift-off. The alterations of these voltages are given in Table II.

$V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ are estimated and visualized in Fig. 8 where each voltage is shown as a function of T_{vj}. It should be pointed out that the collector current following through the IGBT switch is constant. With the help of Fig. 8, the following general statements can be concluded.

1) $V_{\mathrm{CKE(on)}}$ decreases when the corresponding chip has lost a bond wire and $V_{\mathrm{CKE(on)}}$ increases for the remaining chips.
2) $V_{CE(\mathrm{on})}$ will always increase as bond wire lift-off.

These statements form the base of the new proposed bond wire detection and location technique.

E. Fault Detection and Location Without the Knowledge of T_{vj}

So far the knowledge of T_{vj} is required for the proposed technique. The following section illustrates how bond wire states can be predicted without the knowledge of T_{vj}.

Fig. 9 shows the voltage-temperature characteristics ($V_{\mathrm{CKE}i(\mathrm{on})}$ and $V_{CE(\mathrm{on})}$) of FF600R17ME4 PM measured at I_C = 240 A and V_{GE} = 15 V. Fig. 9 is extracted from Fig. 12 and all four characteristics represent the baselines for a healthy PM.

Scenario 1: Healthy condition

At healthy condition, for example as shown in Fig. 9, each measured voltages $V_{\mathrm{CKE1(on)}}$ = 1.525 V, $V_{\mathrm{CKE2(on)}}$ = 1.527 V, $V_{\mathrm{CKE3(on)}}$ = 1.511 V, and $V_{CE(\mathrm{on})}$ = 1.701 V will estimate the same temperature of 60 °C. T_{vj} is commonly treated as the global temperature [24]–[26] and as such it can be described as

$$T_{\mathrm{est}(V_{\mathrm{CKE1}})} = T_{\mathrm{est}(V_{\mathrm{CKE2}})} = T_{\mathrm{est}(V_{\mathrm{CKE3}})} = T_{\mathrm{est}(V_{CE})} = T_{vj} \quad (9)$$

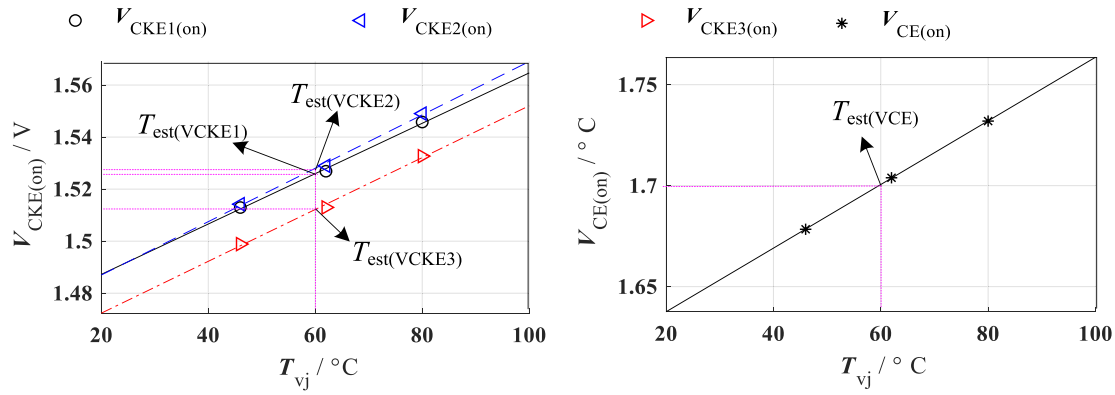

Fig. 9. $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ baselines at $I_C = 240$ A and $V_{GE} = 15$ V representing a healthy PM.

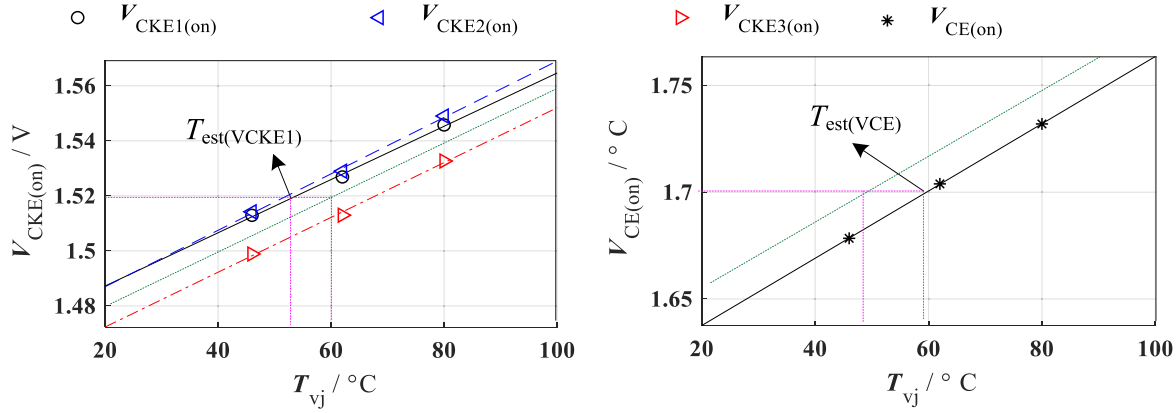

Fig. 10. Prediction change in the case of bond wire lift-off in chip 1 at $I_C = 240$ A. Dotted line in the left diagram: variation of $V_{\mathrm{CKE1(on)}}$ at bond wire lift-off. Dotted line in the right diagram: variation of $V_{CE(\mathrm{on})}$ at bond wire lift-off.

where $T_{\mathrm{est(VCKE1)}}$, $T_{\mathrm{est(VCKE2)}}$, $T_{\mathrm{est(VCKE3)}}$, and $T_{\mathrm{est(VCE)}}$ are the estimated temperatures from the measured voltages $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$, respectively.

Scenario 2: Bond wire lift-off at chip 1

If a bond wire has lifted, the base line shifts away from the healthy baseline. This is shown in Fig. 10 where a new line is added for chip 1 but shifted under the healthy baseline. The new line results that $T_{est(VCKE1)} \neq T_{vj}$. In fact, T_{vj} becomes larger than $T_{\mathrm{est(VCKE1)}}$

$$T_{\mathrm{est}(V_{\mathrm{CKE1}})} < T_{vj}. \tag{10}$$

From the previous findings, we know that the baselines for $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ shift upward. As such it can be derived as (11). The shift for $V_{CE(\mathrm{on})}$ is shown in Fig. 10. The ON-state voltage of chip 2 and chip 3 follow the same tendency

$$\begin{aligned} T_{\mathrm{est}(V_{\mathrm{CKE2}})} &> T_{vj} \\ T_{\mathrm{est}(V_{\mathrm{CKE3}})} &> T_{vj} \\ T_{\mathrm{est}(V_{CE})} &> T_{vj}. \end{aligned} \tag{11}$$

Equation (12) shows the difference between the estimated temperature of each chip and the estimated temperature based on $V_{CE(\mathrm{on})}$. The estimated temperature differences are deployed to determine the number of bond wire lift-off and the location of the lift-off

$$\begin{aligned} \Delta T_{\mathrm{est1}} &= \left| T_{\mathrm{est}(V_{\mathrm{CKE1}})} - T_{\mathrm{est}(V_{CE})} \right| \\ \Delta T_{\mathrm{est2}} &= \left| T_{\mathrm{est}(V_{\mathrm{CKE2}})} - T_{\mathrm{est}(V_{CE})} \right| \\ \Delta T_{\mathrm{est3}} &= \left| T_{\mathrm{est}(V_{\mathrm{CKE3}})} - T_{\mathrm{est}(V_{CE})} \right|. \end{aligned} \tag{12}$$

F. Influence of the Solder Layer, Copper Track, and Copper Wire

This section discusses the influence of the solder layer, copper track, and copper wire on the estimation of bond wire lift-off. To describe the linear relationship between $V_{CE(\mathrm{on})}$, $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$ and the temperature, the reference curves for $V_{CE(\mathrm{on})}$, $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, and $V_{\mathrm{CKE3(on)}}$ are described as

$$V_{CE(\mathrm{on})} = k_{CE}T + b_{CE} \tag{13}$$

$$V_{\mathrm{CKE1(on)}} = k_{\mathrm{CKE1}}T + b_{\mathrm{CKE1}} \tag{14}$$

$$V_{\mathrm{CKE2(on)}} = k_{\mathrm{CKE2}}T + b_{\mathrm{CKE2}} \tag{15}$$

$$V_{\mathrm{CKE3(on)}} = k_{\mathrm{CKE3}}T + b_{\mathrm{CKE3}} \tag{16}$$

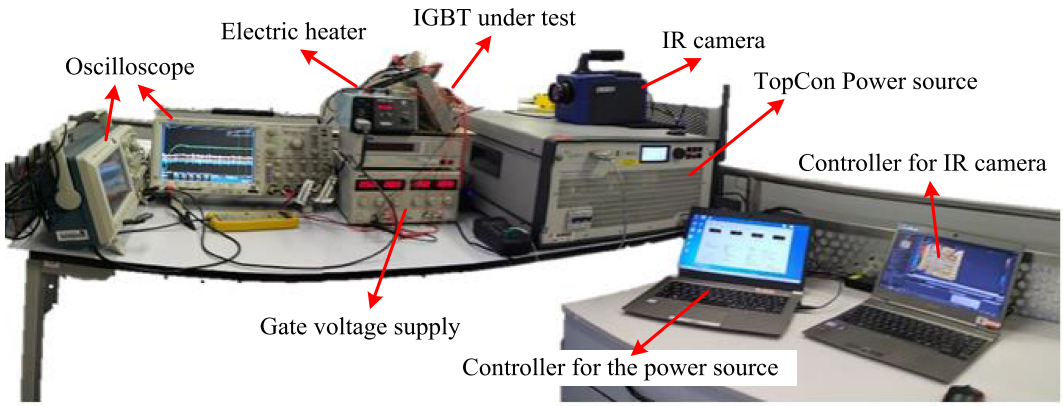

Fig. 11. Test rig set up.

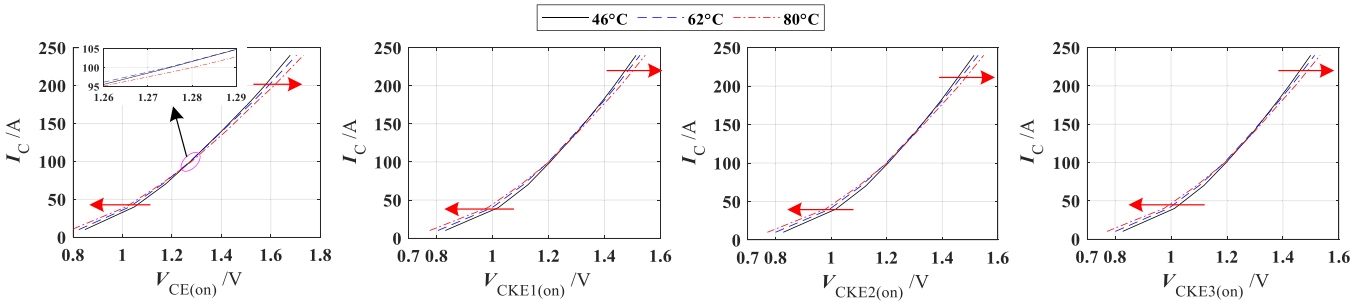

Fig. 12. Forward characteristics of the bottom IGBT switch of FF600R17ME4 at three temperatures. $V_{GE} = 15$ V.

where k_{CE}, k_{KE1}, k_{KE2}, k_{KE3}, b_{CE}, b_{KE1}, b_{KE2}, and b_{KE3} are the constants to describe the linear relationship between $V_{CE(\mathrm{on})}$, $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, and $V_{\mathrm{CKE3(on)}}$ and temperature.

Therefore, the estimated temperature can be derived as

$$T_{\mathrm{est}(V_{CE})} = (V_{CE(\mathrm{on})} - b_{CE})/k_{CE} \tag{17}$$

$$T_{\mathrm{est}(V_{\mathrm{CKE1}})} = (V_{\mathrm{CKE1(on)}} - b_{\mathrm{CKE1}})/k_{\mathrm{CKE1}} \tag{18}$$

$$T_{\mathrm{est}(V_{\mathrm{CKE2}})} = (V_{\mathrm{CKE2(on)}} - b_{\mathrm{CKE2}})/k_{\mathrm{CKE2}} \tag{19}$$

$$T_{\mathrm{est}(V_{\mathrm{CKE3}})} = (V_{\mathrm{CKE3(on)}} - b_{\mathrm{CKE3}})/k_{\mathrm{CKE3}}. \tag{20}$$

For example, in the case, there is bond wire lift-off in Chip 1. The estimation drift by $V_{\mathrm{CKE1(on)}}$ is derived as

$$\Delta T_{\mathrm{est1}} = \left| \frac{V_{\mathrm{CKE1(on)}}(k_{\mathrm{CKE1}} - k_{CE}) + a \times k_{CE} - b}{k_{CE} k_{\mathrm{CKE1}}} \right| \tag{21}$$

where $a = I_{Chip1} R_{BW1} + I_C R_{E,CT} + I_C R_{E,\mathrm{CW}}$, $b = -b_{CE} k_{CKE1} + b_{CKE1} k_{CE}$.

It can be noted that $|k_{CKE1} - k_{CE}| < |k_{CE}|$ and $|k_{CKE1} - k_{CE}| < |k_{CKE1}|$. Therefore, the temperature impact caused by the die attach solder is small. Also the emitter copper wire and copper track have the same coefficient of thermal expansion and are exposed to the same temperature swing. Thus, their resistances rarely changes which means that $I_C R_{E,CT} + I_C R_{E,CW}$ can be assumed as constant in the case of bond wire failure. In summary, the impact of die attach solder is small. The emitter copper track and emitter copper wires do not influence the estimation. ΔT_{est1} mainly varies with the bond wire part $|I_{\mathrm{Chip\ 1}} R_{\mathrm{BW1}}/k_{\mathrm{CKE1}}|$.

TABLE III
NUMBER OF LIFTED BOND WIRES IN IGBT CHIPS IN EACH TEST

Test	1	2	3	4	5	6	7	8	9	10
Chip1	0	1	2	3	4	4	4	4	4	4
Chip2	0	0	0	0	0	2	4	4	4	5
Chip3	0	0	0	0	0	0	0	2	4	6

III. Experimental Set-Up

A. Test Bench

Experimental tests were conducted to verify the method described in Section II. The test rig is shown in Fig. 11. It is constructed according to the schematic in Fig. 4. The IGBT under test is mounted on a heat plate. The junction temperature is varied by the electric heater. First, the IGBT is switched on by the voltage source. Then, a current pulse is injected into the IGBT by the TopCon power source, which is controlled by the computer shown on the bottom left. The thermal characteristics

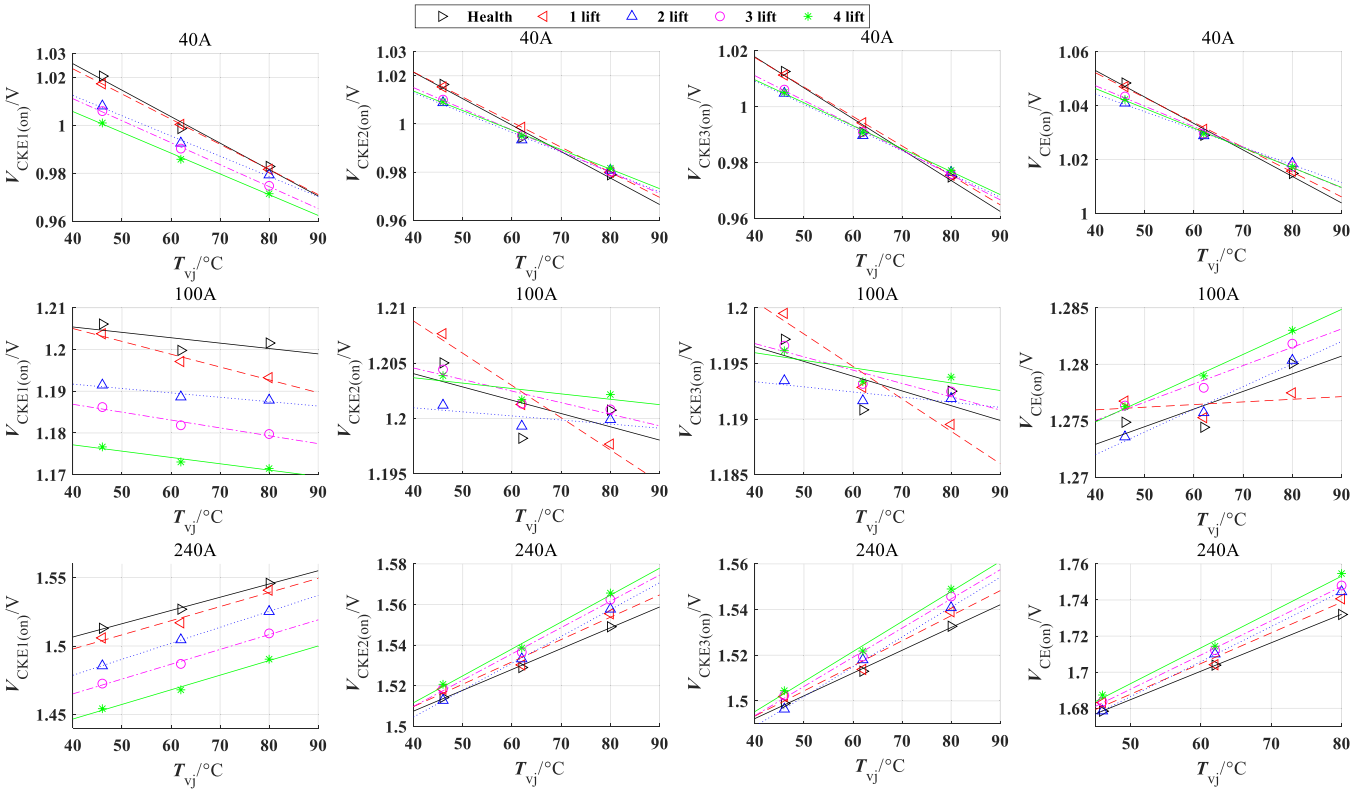

Fig. 13. $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ against T_{vj} and bond wire cuts in Chip 1 only. $V_{GE} = 15$ V.

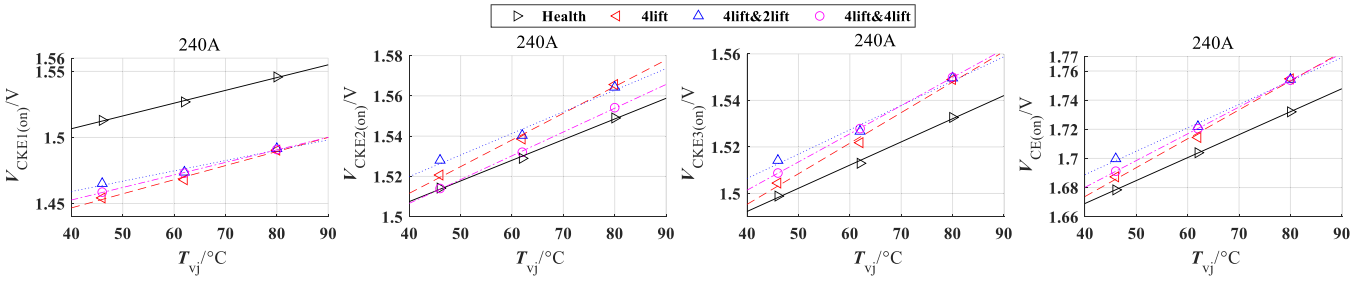

Fig. 14. $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ at various T_{vj} and bond wire cuts in chip 1 and chip 2. (4lift: four lift-off in chip 1; 4lift and 2lift: four lift-off in chip 1 and two lift-off in chip 2; 4lift and 4lift: four lift-off in chip 1 and four lift-off in chip 2.)

are recorded by the IR camera, which is controlled by the computer shown on the bottom right. Two oscilloscopes are used to capture electrical parameters. The IR camera starts to record temperature measurements when the IGBT module has been heated for about 20 min and the IGBT has reached thermal equilibrium. The IR camera is preferred since it can record the thermal information of each pixel in the picture quickly and accurately. In addition, the IR camera is only used to acquire T_{vj} of the module.

B. Test Conditions

In this article, ten ON-state voltage tests were carried out in succession to measure $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ at different bond wire states. Bond wires are cut to imitate the lift-off failure. Table III shows the lift-off conditions of all tests.

IV. Bond Wire Lift-Off Diagnosis

A. Characterization for $V_{CE(\mathrm{on})}$ and $V_{CKE(on)}$

The proposed $V_{CE(\mathrm{on})}$ and $V_{\mathrm{CKE(on)}}$ approach is tested on the FF600R17ME4 module. Fig. 12 is the forward characteristics $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ at three different temperatures. It provides the reference of the IGBT at healthy condition.

The inflexion point of $V_{CE(\mathrm{on})}$ is around $I_C = 100$ A. It is important to emphasize that $I_C - V_{CE(\mathrm{on})}$ curves at different temperatures do not cross each other at the same point. This means inflexion point is not strictly temperature

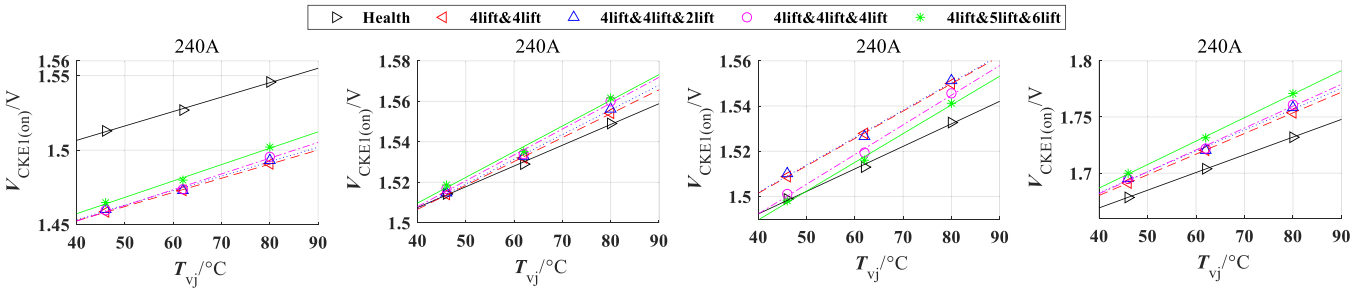

Fig. 15. $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ at various T_{vj} and bond wire cuts in chip 1, chip 2, and chip 3. (4lift and 4lift and 2lift: four lift-off in both chip 1 and chip 2 and two lift-off in chip 3; 4lift and 4lift and 4lift: four lift-off in chip 1, chip 2, and chip 3; 4lift and 5lift and 6lift: four lift-off in chip 1, five lift-off in chip 2, and six lift-off in chip 3.

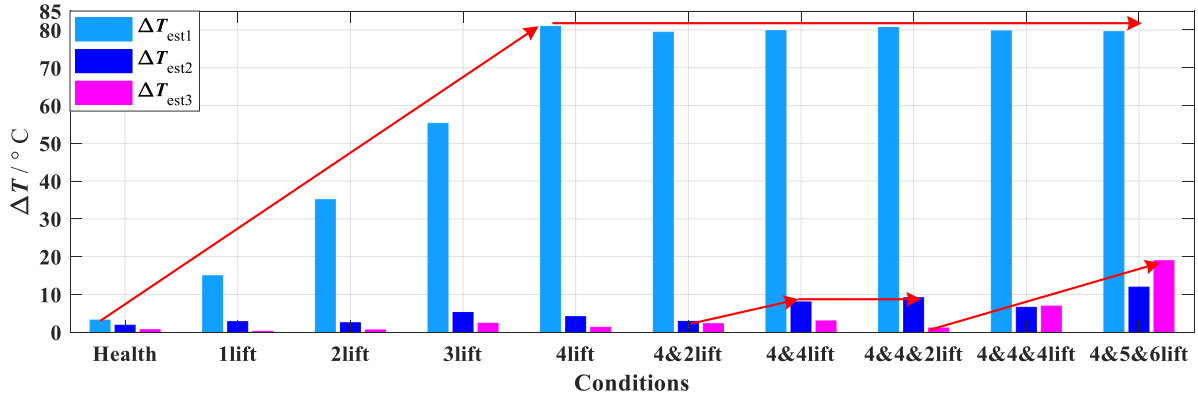

Fig. 16. Estimated temperature error for different bond wire lift-offs at $I_C = 240$ A.

TABLE IV
LINEARITY OF THE ON-STATE VOLTAGE VERSUS TEMPERATURE

I_C	V_{CKE1}	V_{CKE2}	V_{CKE3}	V_{CE}
40 A	0.9949	0.9940	0.9951	0.9939
100 A	0.8358	0.6172	0.6969	0.7531
240 A	0.9897	0.9914	0.9900	0.9957

independent but the temperature dependency is small and thus negligible.

B. Voltage Shift Upon Bond Wire Lift-Offs

Fig. 13 depicts the variation of $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ upon bond wire lift-offs in chip 1 at 40, 100, and 240 A. These current values were chosen to represent the behavior of the voltage variations at the collector current levels of below, around, and above the inflexion point.

Table IV describes the linearity of the ON-state voltage versus temperature. The linearity is derived from the measurement in Fig. 13. Each value is the average linearity of all the measurements at different bond wire failure condition. It can be noted that there is no clear linearity at $I_C = 100$ A (around inflexion point) where the temperature dependency is negligible. The variation upon the first bond wire failure is too small for $I_C = 40$ A (below inflexion point). As such this current level cannot be chosen for practical applications. When $I_C = 240$ A is applied,

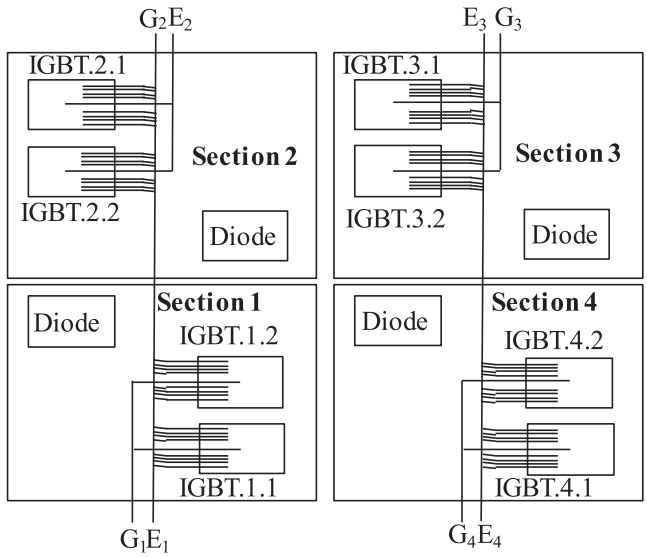

Fig. 17. Layout of the DIM400NSM33-F000 IGBT module.

all voltages show good linearity with temperature. $V_{\mathrm{CKE1(on)}}$ declines about 7 mV upon the first bond wire lift-off, whereas $V_{\mathrm{CKE2(on)}}$, $V_{\mathrm{CKE3(on)}}$, and $V_{CE(\mathrm{on})}$ rises about 3 mV.

Bond wires were also cut for chip 2 and chip 3 as detailed in Table III. Figs. 14 and 15 show results for these scenarios

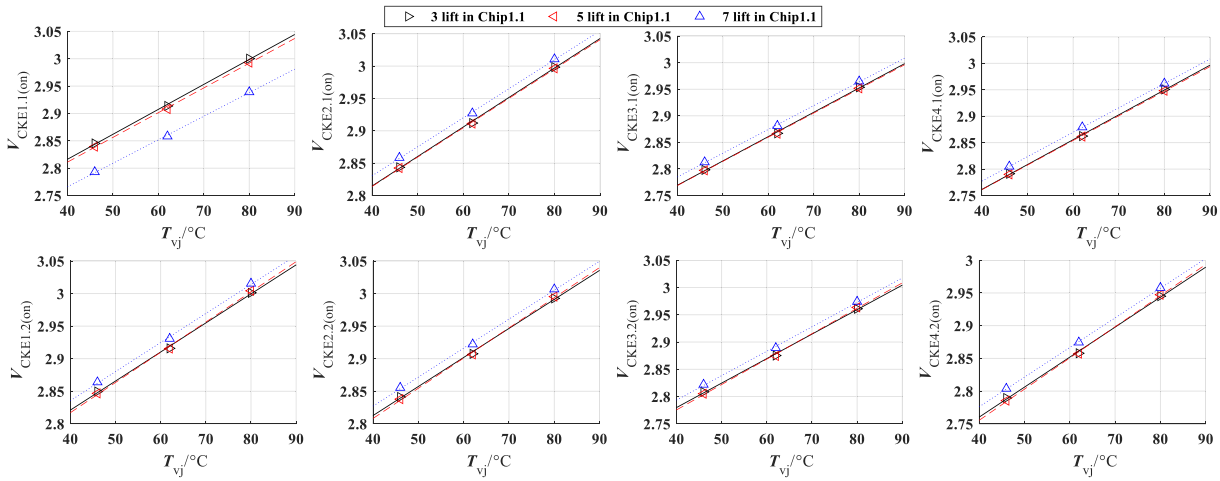

Fig. 18. Experimental results: ON-state voltage change upon bond wire lift-off in chip 1.1 at $I_C = 360$ A.

at $I_C = 240$ A. Both figures show that $V_{\mathrm{CKE(on)}}$ drops for those chips with lifted bond wires and $V_{\mathrm{CKE(on)}}$ rises for the remaining chips. For example, Fig. 13 shows clearly the changes in $V_{\mathrm{CKE1(on)}}$, $V_{\mathrm{CKE2(on)}}$ and $V_{\mathrm{CKE3(on)}}$ between a healthy module denoted as "health" and a module where chip 1 lost four bond wires denoted as "4lift." Cutting two additional bond wires at chip 2 is represented by "4lift and 2lift" as shown in Fig. 14, which shows that $V_{\mathrm{CKE2(on)}}$ starts to decrease (as two bond wires were cut) and $V_{\mathrm{CKE1(on)}}$ and $V_{\mathrm{CKE3(on)}}$ rise slightly compared to results "4lift." The tendency of the results shown in Fig. 15 is similar with that in Fig. 13. When there is bond wire failure in chip 3, $V_{\mathrm{CKE3(on)}}$ goes down, however, $V_{\mathrm{CKE1(on)}}$ and $V_{\mathrm{CKE2(on)}}$ goes up.

It is of interest to observe that every time a bond wire lifts-off $V_{CE(\mathrm{on})}$ increases. This has been reported in other literature [7] and [8] too. The rise is due to the total equivalent resistance increases upon bond wire cut. However, from 4lift and 2lift to 4lift and 4lift, only two bond wires are cut which means there is only slight variance between the two measurements. Thus, the measurement of 4lift and 2lift is higher than 4lift and 4lift at lower temperature and overlaps with 4lift and 4lift at high temperature.

Overall, test results confirm that the variations in $V_{CE(\mathrm{on})}$ and $V_{\mathrm{CKE(on)}}$ can detect and locate the bond wire lift-off failures.

C. Analysis for Fault Detection and Location

Fig. 16 describes the estimated temperature difference $\Delta T_{\mathrm{est},i}$ $(i = 1, 2, 3)$ for different bond wire lift-off conditions at $I_{\mathrm{C}} = 240$ A. The arrows denote the trend of $\Delta T_{\mathrm{est},i}$ for each IGBT chip. On the condition of lift-off in chip 1, ΔT_{est1} shoots up with every additional cut. ΔT_{est2} and ΔT_{est3} keep unchanged around almost zero. In the case of lift-off in chip 2, ΔT_{est2} goes up. When there is bond wire lift-off in chip 3, ΔT_{est3} starts to rise. This phenomenon locates the faulty chip and the level of ΔT_{est} can determine the number of bond wire lift-off.

It can be noticed that the temperature drift of chip 2 and chip 3 are smaller than that of chip 1. This is linked to the specified bond wire cut sequence and the current redistribution among these IGBT chips upon the bond wire lift-off. The bond wire lift-off is carried out on IGBT chips one by one to capture as more failure condition as possible. For example, if bond wires are lifted in chip 2 and chip 3 in the first test, the failure scenarios of lift-offs only in chip 1 are lost.

Due to the lift-off in chip 1, the increment of bond wire resistance in chip 1 circuit causes the decline of $I_{\mathrm{Chip\ 1}}$. As the total current I_C does not change, the extra current is shared between chip 2 and chip 3. This means the variation in $I_{\mathrm{Chip\ 1}}$ is larger than that in $I_{\mathrm{Chip\ 2}}$ and $I_{\mathrm{Chip\ 3}}$. As illustrate in previous section, ΔT_{est1} varies with the bond wire part $|I_{\mathrm{Chip\ 1}} R_{\mathrm{BW1}}/k_{\mathrm{CKE1}}|$. The influence of the resistance is amplified by multiply $I_{\mathrm{Chip\ 1}}$ causing the drift in chip 1 to be the largest.

V. Tests on PM With Different Package

In order to verify the feasibility of the proposed technique on PMs with a different package, repeated tests were carried out on the Dynex DIM400NSM33-F000 PM. The layout of DIM400NSM33-F000 is shown in Fig. 17. This is a 3.3 kV 400 A single switch IGBT module with eight IGBT chips and each IGBT chip has eight bond wires. Each IGBT chip is denoted by the numbers as shown in Fig. 17.

The test rig is constructed according to Fig. 4. Fig. 18 shows the experimental results for the bond wire lift-off in the IGBT chip 1.1, denoted as IGBT.1.1, where 3, 5, and 7 bond wires have been cut. All tests are carried out on the same opened IGBT module without gel. For each test, the gate drive voltage is kept at 15 V. The collector current I_C is maintained at 360 A.

The first three lifted bond wires cause a 6 mV decrease in $V_{\mathrm{CKE1.1(on)}}$ and about 1 mV increment in the ON-state voltage of the other chips. More cuts lead to further decreases of $V_{\mathrm{CKE1.1(on)}}$, whereas all the other ON-state voltages of the IGBT chips increase. The experimental results on the Dynex module are consistent with the results from the Infineon module. It confirms that the proposed method can be applied to PMs with different packages.

As it is known that the ON-state voltage under load current is not only influenced by bond wire failure, but also the virtual junction temperature T_{vj}. The technique proposed in this article can estimate the bond wire lift-off as well as locate the lift-off. Furthermore, since the temperature differece is dervied by feeding the voltage measurement to the references at health condition, the influence of temperature on the estimation is negligible. Compared to work presented in the past, like [13], the proposed method does not rely on the knowledge of T_{vj} to determine bond wire lift-off. In addition, since the Kelvin Emitter terminal is only a measurement point in the proposed technique, there is no current flowing through, the power loss caused by the bond wire is eliminated.

VI. Conclusion

The article describes for the first time a technique that is able to detect and locate the bond wire lift-off in multichip IGBT PMs. The proposed technique is based on the ON-state voltage measurements of $V_{\mathrm{CKE}}(\mathrm{on})$ across the collector and the Kelvin emitter and the voltage $V_{CE(\mathrm{on})}$ across the collector and the emitter. Compared with the traditional $V_{CE(\mathrm{on})}$ approach, the proposed technique can detect early bond wire lift-offs in mIGBT PMs and the accuracy of the detection is independent of junction temperature.

It is shown that $V_{\mathrm{CKE(on)}}$ decreases for the chip where the bond wire is lifted and increases for the remaining chips. $V_{CE(\mathrm{on})}$ always increases.

Tests conducted on the Infineon module show that the technique is able to detect the first lifted bond wire out of 37. The resolution is 7 mV for detecting the first bond wire lift-off. A second test was conducted on a 64-bond wire PM from Dynex of different package. The proposed system can detect the third bond wire lift-off. As such the proposed technique can be applied to various packaged PMs.

The proposed technique requires a small set of additional Kelvin terminals embedded in the frame of the PM where terminals are commonly placed. The additional Kelvin emitters are directly bonded with the emitter of the chips and no DCB layout change is required.

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