Investigation and Failure Mode of Asymmetric and Double Trench SiC MOSFETs Under Avalanche Conditions

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***Abstract*—In this article, commercially 1200-V asymmetric and double trench silicon carbide (SiC) metal–oxide–semiconductor-field-effect transistors (MOSFETs) from two manufacturers are investigated by experiment and finite-element simulation under single-pulse unclamped inductive switching (UIS) stress. The variation in avalanche time with MOSFET avalanche energy and temperatures dependence of critical avalanche energy and maximum power dissipation are evaluated. It is found that two failure mechanisms are identified, i.e., thermal runaway and gate oxide rupture. For asymmetric trench SiC MOSFETs, the failure mode are all thermal runaway at various temperatures. However, the failure mode of double trench SiC MOSFETs is thermal runaway or gate oxide rupture, which indicates an instable avalanche robustness under UIS stress. The variations of dc parameters are recorded to evaluate external features of device failure. Furthermore, finite-element simulation is used to reveal the electro-thermal stress inside the device during avalanche. Finally, failed devices are decapsulated to verify the location of failure point from the perspective of the semiconductor die.**

***Index Terms*—Failure mechanisms, gate oxide rupture, thermal runaway, trench silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs), unclamped inductive switching (UIS).**

I. Introduction

DUE to the superior material properties, silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs) is considered as a promising competitor in high power electronics fields [1]–[3]. SiC MOSFETs typically have lower conduction loss and switching loss, which can increase the efficiency and power density of power systems [4]–[6].

With the development of SiC material and device fabrication technology, SiC MOSFETs are becoming more and more mature. Nowadays, a variety of commercial SiC MOSFETs with planar gate and trench gate structure from different manufacturers are available [7]–[9]. Compared with planar gate structure, trench gate structure has a higher power density and a lower ON-resistance, which significantly improves the performance of SiC MOSFETs [10]–[12].

Unfortunately, the trench gate SiC devices are suffering from gate oxide reliability problems [13]–[15]. First, the critical electric field strength of SiC devices is about ten times stronger than that of Si-based devices, which makes it easy for gate oxide layer of SiC MOSFETs to reach its reliability limit (>3 MV/cm) based on the Gauss Law [16], [17]. Furthermore, the poor quality of SiC/SiO_2 interface leads to instability of electrical parameters of trench SiC MOSFETs [18], [19]. Finally, the inhomogeneity of SiC oxidation process results in a thinner oxide layer thickness at the bottom in comparison with that at the sidewalls of the trench, which could deteriorate gate oxide reliability of trench SiC MOSFETs [20]. Therefore, an asymmetric and double trench structure are employed to relieve the gate oxide electric field crowding at the corner of the trench bottom [21], [22].

As trench SiC MOSFETs is operated in avalanche conditions, the degradation and even the failure of the devices may occur due to the parasitic inductance or inductive load in the circuit for the automotive traction inverter and converters application [23]–[25]. Up to now, the investigation into the avalanche breakdown robustness for planar gate SiC MOSFETs have been reported [26]–[28]. However, only a few reports on the reliability of trench SiC MOSFETs under single-pulse avalanche stress are available. Under avalanche conditions, the high electrothermal stress in the SiC devices, especially in trench gate SiC devices, leads to a marked impact on the gate oxide reliability. Therefore, it is necessary to investigate the avalanche robustness of trench SiC MOSFETs and determine its failure mechanism.

In this article, the robustness of two 1200-V trench SiC MOSFETs with different gate-oxide shield structures (asymmetric and double trench) under single-pulse avalanche stress is investigated by experiment and two-dimensional numerical simulation.

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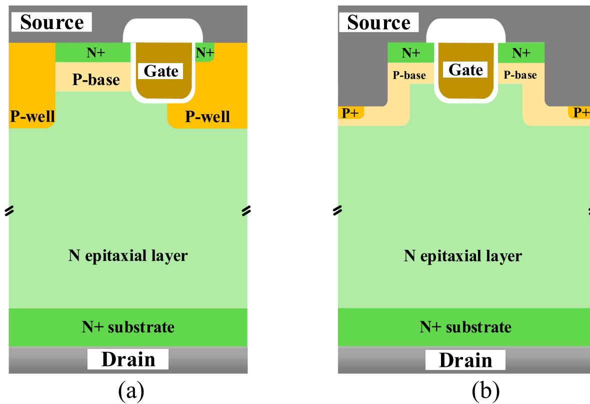


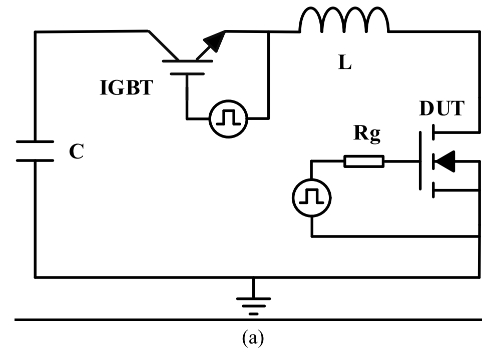
Fig. 1. Schematic cross section of (a) asymmetric trench SiC MOSFETs and (b) Double trench SiC MOSFETs. For asymmetric trench SiC MOSFETs, deep p-wells are used to limit the electric field in the gate oxide. For double trench SiC MOSFETs, p-implant source trench is applied to limit the electric field in the gate oxide.

Temperatures dependence of the avalanche withstand capability is evaluated for asymmetric and double trench SiC MOSFETs. In order to verify the experimental results, the variations of dc parameters are recorded, and finite-element simulation is used to reveal the electrothermal stress inside the device during the avalanche. Additionally, failed devices are decapsulated to examine the failure sites on semiconductor die.

A. Device Structure and Stress Experimental Setup

Fig. 1 shows the schematic cross sections of 1200-V trench SiC MOSFETs with asymmetric trench structure and double trench structure. The breakdown voltage and threshold voltage (V_{th}) of the asymmetric trench MOSFETs are 1350 V (with a drain current (I_d) of 1 μA) and 4.2 V at room temperature. The corresponding values for the double trench MOSFETs are 1650 V (I_d of 1 μA) and 4.5 V. The specific ON-resistance ($R_{ON} \times A$) of asymmetric trench SiC MOSFETs and double trench SiC MOSFETs are 4.2 and 4.1 mΩ·cm^2, respectively [29], [30].

Fig. 2 shows the circuit diagram and image of experimental setup to generate the single-pulse unclamped inductive switching (UIS) stress. Two parallel-connected 470 μF/1100 V capacitors are coupled with a high voltage supply to provide adequate energy for test. A 1700-V Si IGBT module is used to decouple the test circuit from the capacitors. The load inductors L is selected to be 3.6 mH. IGBT module and DUT are normally OFF. The capacitors are charged to test voltage before test begins. When the DUT and IGBT are turned ON, the inductor is charged to a peak current I_{av}. Subsequently, DUT is turned OFF, the energy stored in the inductor flows into the DUT, forcing the DUT into avalanche mode. The avalanche mode will last until the energy stored in the inductive load is consumed. If the energy exceeds the critical value, the DUT will eventually fail [31], [32]. In this circuit, IGBT module turns OFF after the energy stored in the inductive load is consumed through DUT, and ensures the safety of the platform in off-state, especially after the avalanche failure of DUT, it isolates DUT from dc bus. The gate voltages (V_{gs}) are set from 0 to +18 V for double trench MOSFETs and



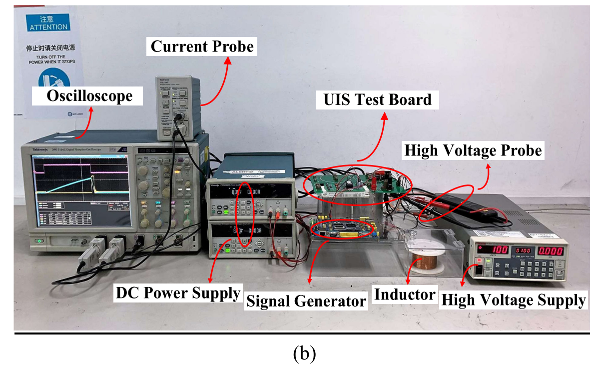


Fig. 2. (a) Schematic of UIS test equivalent circuit and (b) Image of UIS test hardware.

from –3.5 to +15 V for asymmetric trench SiC MOSFETs. The external gate resistor is 20 Ω for both devices. During the test, case temperature ranges from 25 to 175 °C.

II. Avalanche Robustness at Various Temperatures

A. Asymmetric Trench SiC MOSFET

The typical experimental waveforms of asymmetric trench SiC MOSFET are shown in Fig. 3. The case temperature is 25 °C and load inductance is 3.6 mH. Fig. 3(a) illustrates the waveform of the last test before failure, and Fig. 3(b) presents the waveform of failure.

The peak avalanche current is increased gradually by increasing the pulse width until the device reach its failure point. As can be seen from Fig. 3(a), the peak drain current and the voltage across the drain to source are 25.4 A and 1560 V during avalanche, respectively. The avalanche regime time (t_{av}) lasts for 64.7 μs, and the avalanche energy (E_{av}) is measured to be 1.22 J. Fig. 3(b) plots the typical failure waveform with a peak avalanche current of 26.8 A and a drain–source voltage of 1560 V. The device collapses suddenly after avalanche time lasts for 33 μs. The measured waveforms indicate complete device failure due to formation of a conductive path between drain and source.

Fig. 4 depicts the avalanche time (t_{AV}) dependence of avalanche capability (E_{av}) of asymmetric trench SiC MOSFET with different temperatures in the UIS event. It is found that the temperatures have only a small impact on t_{AV} of SiC MOSFETs under the inductance load of 3.6 mH. Those measured results are obtained without failure and can be used as a reference

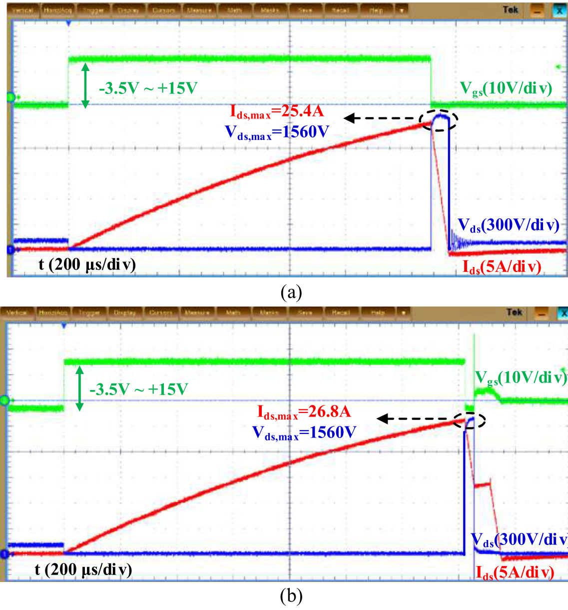


Fig. 3. Measured typical UIS waveforms for asymmetric trench SiC MOSFETs: (a) the last test before failure, and (b) failure.

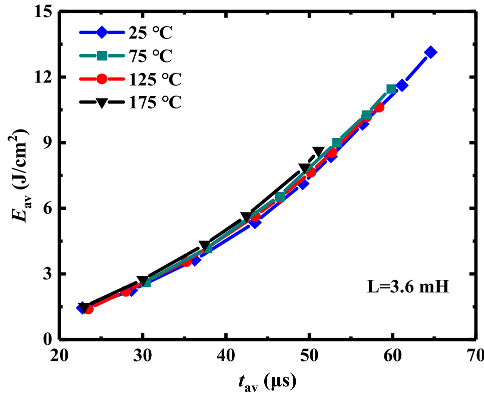


Fig. 4. E_{AV} dependence on t_{AV} for asymmetric trench SiC MOSFETs with different temperatures.

for preventing failure of avalanche in the power electronics applications.

Fig. 5 shows the relationship between the critical avalanche energy density and maximum power dissipation ($P_{\max}$, multiplying V_{DS} and I_{DS} waveforms) with various case temperature. The maximum avalanche tolerance decreases with the increase of temperature. The critical avalanche energy density is 13.1 J/cm^2 at 25 °C, and the value decreases by about 34% as the temperature rises to 175 °C. It is also found that temperature dependence of maximum power dissipation of asymmetric trench SiC MOSFETs shows a similar trend with the critical avalanche energy.

B. Double Trench SiC mosfet

Fig. 6 shows the typical experimental waveforms of double trench MOSFETs under 3.6 mH inductance load at room temperature. Fig. 6(a) shows the waveform of the last test before failure. The peak drain current of 14.0 A and drain to source

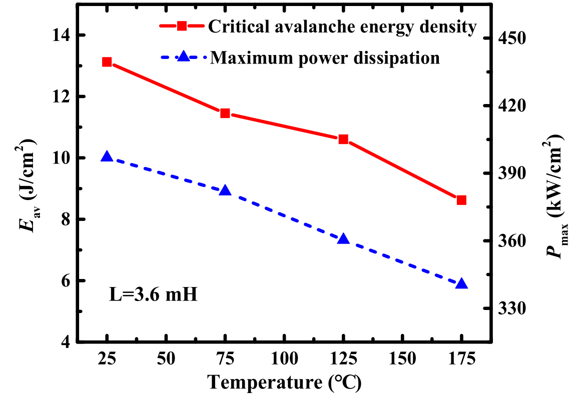


Fig. 5. Comparison of temperature-dependent critical avalanche energy and maximum power dissipation.

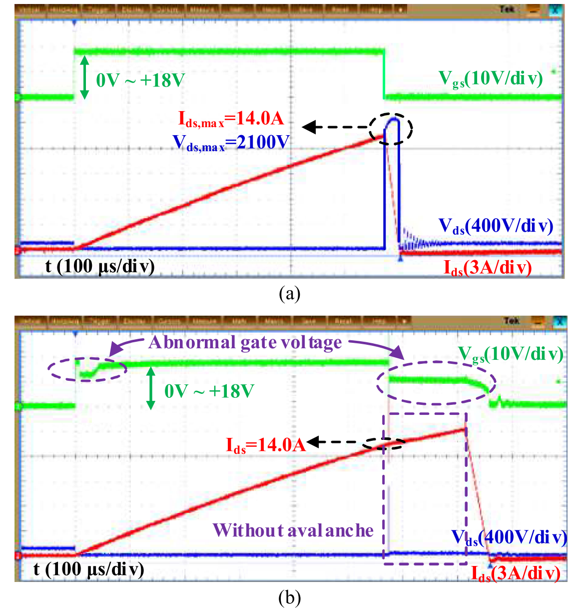


Fig. 6. Measured typical UIS waveforms (gate oxide damage mode) for double trench SiC MOSFETs: (a) the last test before failure, and (b) failure.

voltage of 2100 V are observed during avalanche. The avalanche regime time last for 26.3 μs, and the measured avalanche energy is 0.34 J. The typical failure for double trench MOSFETs is shown in Fig. 6(b). Unlike the avalanche failure of asymmetric trench SiC MOSFETs, double trench MOSFETs collapses without avalanche when the device turns OFF. It is should be noted that the waveforms of gate voltage and drain current are obviously different from those of asymmetric trench SiC MOSFETs [33]. The abnormal gate voltage waveform indicates that failure mechanism is a gate oxide damage.

Fig. 7 shows the waveforms of the last test before failure and failure of double trench MOSFET under 3.6 mH inductance load at 175 °C. It is clear that the waveforms of gate voltage and drain current at failure are similar to those of asymmetric trench SiC MOSFETs, which indicate a thermal runaway failure mode.

Fig. 8 presents the dependence of t_{AV} on E_{AV} for double trench SiC MOSFETs with different temperatures in the UIS

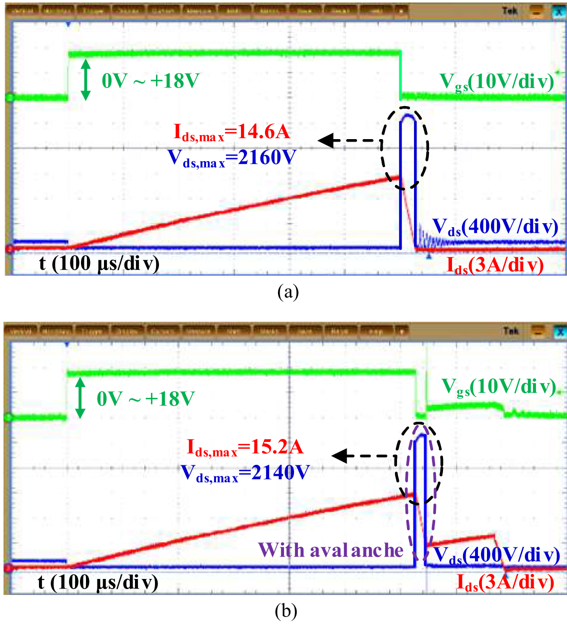


Fig. 7. Measured typical UIS waveforms (thermal runaway failure mode) for double trench SiC MOSFETs: (a) the last test before failure, and (b) failure.

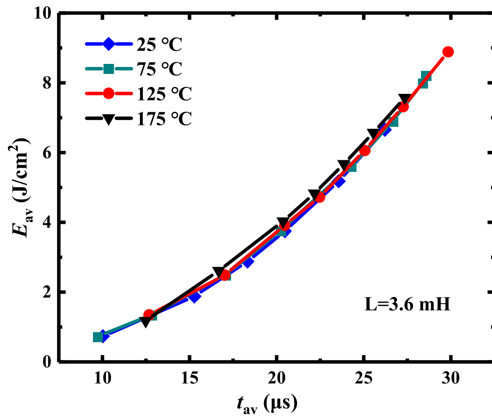


Fig. 8. Influence of tA_V on E_{AV} with varied temperature.

conditions. There is no significant temperature correlation for the critical avalanche energy in the whole temperature range.

Fig. 9 compares the measured critical avalanche energy density and maximum power dissipation of double trench SiC MOSFETs at different temperatures. The critical avalanche energy increases from 25 to 125 °C, and decreases at 175 °C. The critical avalanche energy density is 6.2, 8.3, 8.9, and 7.6 J/cm^2.

It is found that there are two failure modes, i.e., gate oxide rupture at 25 °C, and thermal runaway at 75, 125, and 175 °C, which could be observed for double trench SiC MOSFETs under single-pulse UIS stress. For gate oxide damage, as shown in Fig. 6, the abnormal gate voltage waveform indicates that the gate oxide of the device has been destroyed. For thermal runaway, as shown in Fig. 7, the device collapses suddenly after avalanche mode last for some time indicates that complete device failure due to the critical junction temperature has been reached inside the device.

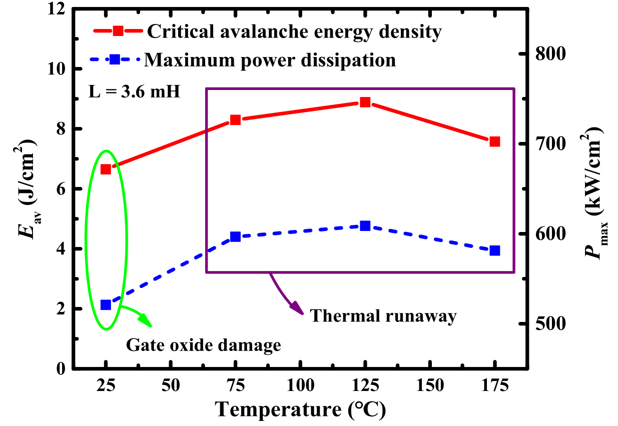


Fig. 9. Comparison of temperature-dependent critical avalanche energy and maximum power dissipation.

Given stochastic process of the etched trench and implanted p-type shielding structures, the location of avalanche can localize near the trench gate. The gate oxide can be catastrophically ruptured by high electric fields. In single pulse UIS destructive test, a large number of electron–hole pairs are generated by impact ionization because of the higher critical avalanche energy and the faster spread of heat generation and accumulation inside the device. Therefore, the combination of large electrothermal stresses in the device can easily damage the gate oxide.

Nowadays, many researchers have reported the poor reliability of gate oxide for trench gate SiC MOSFET due to the trapped charge in the SiO_2/SiC interface [19], [34]. Some defects with the appropriate energy level and spatial location will locally enhance leakage current via trap-assisted tunneling during high-field stress. The increased leakage current will lead to an increase in oxide wear-out rate and, therefore, a shorter lifetime [35]. However, the charge in interface states, which depends on the position of the Fermi level. At room temperature, the Fermi level is closer to the conduction band edge, which moves toward the midgap at elevated temperatures. As the temperature rises and Fermi level moves closer to the midgap, the charge in interface states decreases [36], [37]. There are fewer filled interface traps at high temperatures, i.e., the high temperature measurements could provide adequate activation energy to help the trapped charge release, resulting in an improvement of gate oxide reliability. Therefore, the failure mode of double trench SiC MOSFETs under avalanche conditions will change from gate oxide rupture to thermal runaway as the case temperature rises.

III. Failure Mechanisms

During the UIS test, a significant variation in device performance would indicate damage to the device due to avalanche induced energy dissipation. Before device failure, the initial characterization (i.e., $V_{\rm th}$, $I_{\rm gss}$) was repeated for all test devices between each UIS measurement. The $V_{\rm th}$ and $I_{\rm gss}$ are used to monitor the reliability of the gate oxide before failures. Additionally, the impedance between the three terminals of the device is used to monitor the characteristics of the device after failures.

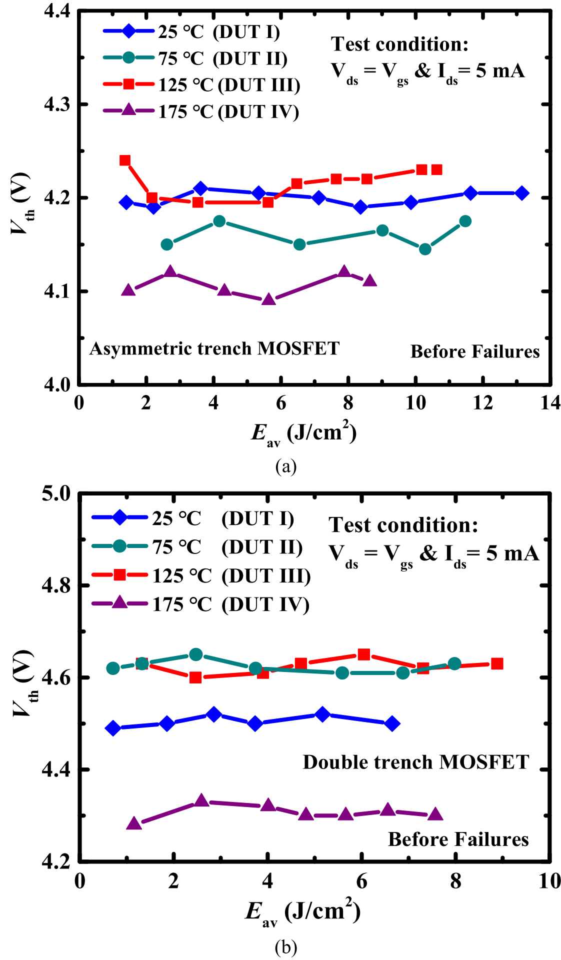


Fig. 10. Measured threshold voltage at incrementally higher energy levels before failures: (a) asymmetric trench SiC MOSFETs, and (b) double trench SiC MOSFETs.

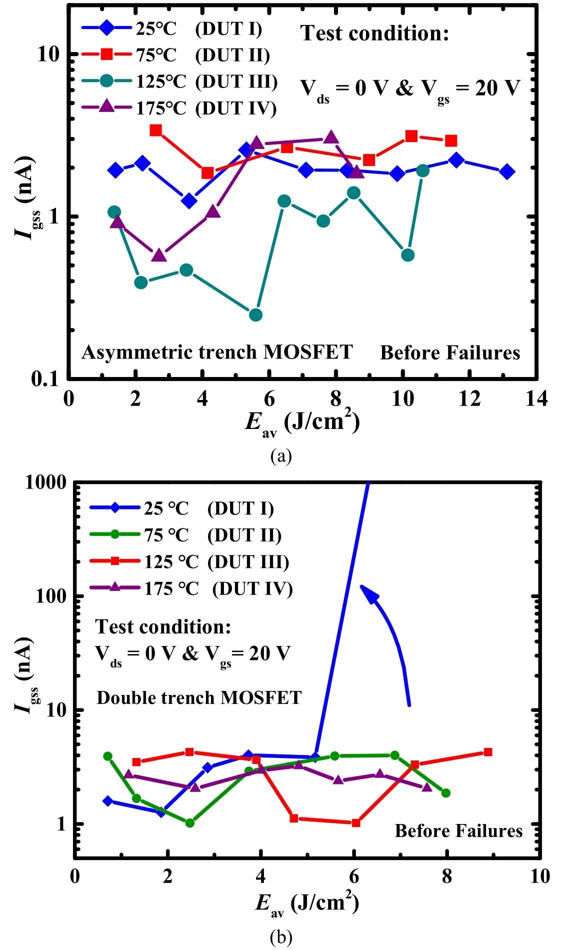


Fig. 11. Measured gate leakage current at incrementally higher energy levels before failures: (a) asymmetric trench SiC MOSFETs, and (b) double trench SiC MOSFETs.

A. DC Electrical Parameters

In this article, the V_{th} is measured at $V_{\text{ds}} = V_{\text{gs}}$ and $I_{\text{DS}} = 5$ mA using a Keithley 4200 curve tracer. The variations in threshold voltage of SiC MOSFETs with E_{AV} at 3.6 mH load are shown in Fig. 10. It is clear that the threshold voltage remained effectively stable for both asymmetric and double trench SiC MOSFETs, proving that the channel and the oxide above channel of the devices does not suffer evident damage.

The gate oxide of trench MOSFETs has been suffered from electrothermal stress at each avalanche hits. In order to investigate the degradation of gate oxide, the gate leakage current (I_{gss}) is monitored. In this work, I_{gss} of SiC MOSFET is measured at $V_{\text{gs}} = 20$ V and $V_{\text{ds}} = 0$ V using a Keithley 4200 curve tracer. Fig. 11 shows the variations in I_{gss} with E_{AV} under 3.6 mH load at different temperatures. With variations below normal measurement errors, the gate leakage current of asymmetric trench SiC MOSFETs keeps constant, showing the gate oxide at the trench does not suffer from damage during shocks. The stability of gate leakage current proves that deep p-wells are effectively shaped in the field in the gate oxide at the bottom, the corners, and the sidewalls of the trench. However, an evident gate leakage current appears for double trench SiC MOSFETs before failure, which indicates that a gate oxide damage has been occurred under the combination of electric and thermal stresses. This is because the double trench structure could not effectively protect the gate oxide layer at the trench bottom.

TABLE I
IMPEDANCE BETWEEN THREE TERMINALS OF ASYMMETRIC TRENCH SiC MOSFETS AFTER FAILURES

test conditions		R_{gs} (Ω)	R_{gd} (Ω)	R_{ds} (Ω)
3.6 mH	25 °C	7.9	18	20
	75 °C	32.2	51.1	20.1
	125 °C	20.7	41.7	36.6
	175 °C	24.6	65	52

The measured impedance between the three terminals of asymmetric trench SiC MOSFETs and double trench SiC MOSFETs is summarized in Tables I and II after the destructive avalanche tests.

For devices without failure, the impedance between the three terminals is immeasurable. As can be observed from Table I,

TABLE II
IMPEDANCE BETWEEN THREE TERMINALS OF DOUBLE TRENCH SiC MOSFETs AFTER FAILURES

test conditions		R_{gs} (Ω)	R_{gd} (Ω)	R_{ds} (Ω)	Failure Mode
3.6 mH	25 °C	334.8 k	749	330.8 k	gate oxide damage
	75 °C	242.3	249.5	9.4	thermal runaway
	125 °C	1.4	8.5	8.1	
	175 °C	925	515	1253	

all three terminals of asymmetric trench SiC MOSFETs are nearly short connected at various test conditions. The extremely low resistances between the three terminals indicate that the device has been completely damaged, and the failure mode is thermal runaway. For double trench SiC MOSFETs, the impedance between the three terminals is extremely low under thermal runaway. However, in gate oxide damage failure mode, the impedance between gate and drain is extremely low, while the blocking characteristics indicate that the device failure is due to the gate oxide damage. The abnormal impedance characteristics of the double trench SiC MOSFETs in both failure modes indicate that the device has been failed.

B. Finite Element Simulation

In order to investigate the electrothermal stress and get insight failure mechanisms of SiC MOSFETs during an avalanche, Sentaurus TCAD software is used to evaluate its internal electrical and thermal variations at room temperature (300 K) under 3.6 mH load.

For asymmetric trench SiC MOSFETs, the doping concentration and thickness of the epitaxial layer are 1×10^{16}cm^{-3} and 11 μm. The doping of the deep p-well and the thickness of the gate oxide are set to 5×10^{19} cm^{-3} and 75 nm, respectively. For the double trench SiC MOSFETs, the thickness of the epitaxial layer is 12 μm, and the doping concentration is 8×10^{15} cm^{-3}. The doping of the p-implant source trench is set at 7.5×10^{17} cm^{-3}. The thickness of the gate oxide at sidewall and bottom are 50 and 100 nm, respectively. The channel length is 0.5 μm in both devices. Thermodynamic model and Okuto–Crowell impact ionization model are included to reveal the temperature and electric field variations in the device.

Referring to the literature data and design criteria to define the doping and dimension parameters is to make the static characteristics of this simulated device more reasonable. Meanwhile, the appropriate physical models ensure that the same UIS stress is applied to the device in a mix-mode simulation. It should be noted that the calibrated structure is not exactly consistent with the actual device in the experiments, it can be taken as a more general case study in this article.

The temperature distribution along the vertical axis from the surface to the bottom (when peak junction temperature is occurred) in asymmetric and double trench MOSFETs is shown in Fig. 12. The case temperature is 300 K. The maximum junction temperature for both SiC MOSFETs is located at the surface of the

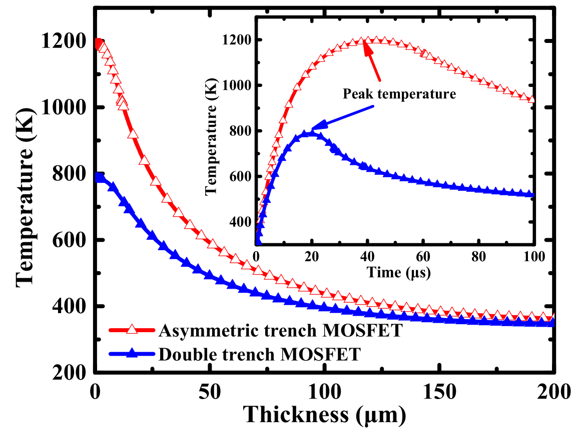


Fig. 12. Temperature distribution along vertical axis from the surface to the bottom (when peak junction temperature is occurred) in asymmetric trench SiC MOSFETs and double trench SiC MOSFETs.

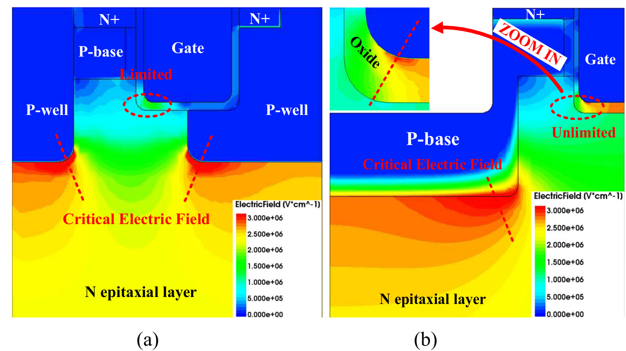


Fig. 13. Electric field distribution in the device (when peak junction temperature is occurred): (a) asymmetric trench SiC MOSFETs, and (b) double trench SiC MOSFETs.

device due to the highest electric field at the depletion region. It is also found that the surface temperature of asymmetric trench MOSFETs is higher than that of double trench MOSFETs. This is due to the fact that gate oxide damage is occurred for double trench MOSFETs and a thermal runaway failure is occurred for asymmetric trench MOSFETs. The gate oxide failure mode of double trench SiC MOSFETs results in a smaller critical avalanche energy. Therefore, the temperature inside the double trench MOSFET rises more slowly and a lower peak junction temperature can be found.

As can be seen in the inset of Fig. 12, the peak junction temperature of asymmetric trench SiC MOSFETs could exceed 1200 K during avalanche. However, the peak junction temperature in double trench SiC MOSFETs is not more than 800 K, which proves that device failure is more like an electrical stress induced failure rather than a thermal induced failure. If the initial case temperature is high enough, the junction temperature inside the device will easily exceed 930 K (the melting point of aluminum electrode) of a critical temperature for failure [9].

Fig. 13 presents the electric field distribution in asymmetric and double trench MOSFETs during the UIS test when peak junction temperature is happened.

For asymmetric trench SiC MOSFETs, the peak electric field in the oxide layer is less than 3 MV/cm although the maximum

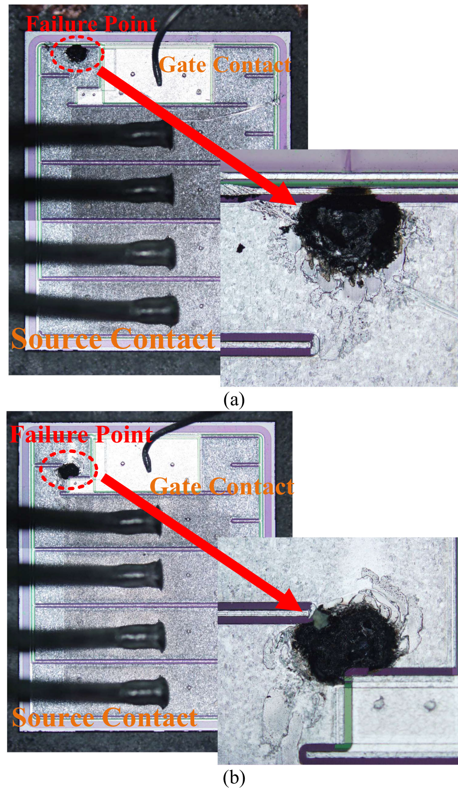


Fig. 14. Images of devices failing during avalanche conditions using a 3.6 mH load inductor at (a) 25 °C and (b) 125 °C.

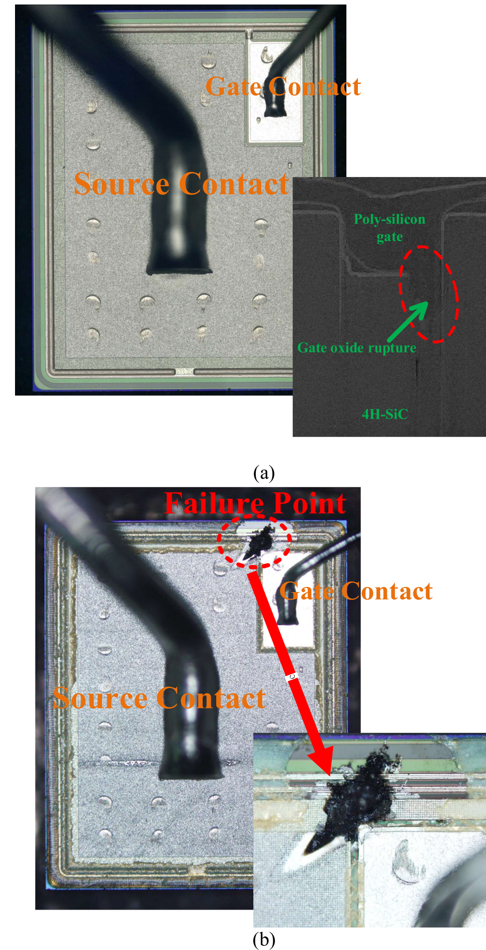


Fig. 15. Images of devices failing during avalanche conditions using a 3.6 mH load inductor at (a) 25 °C (b) 125 °C.

junction temperature is more than 1200 K. This indicated that deep p-wells in asymmetric trench structure could effectively limit the electric field crowding in the gate oxide at the trench bottom and prevent the gate oxide breakdown. However, double trench SiC MOSFETs appear the opposite phenomenon. The peak junction temperature in device is less than 800 K, while the electric field at the trench bottom is over 3 MV/cm, leading to gate oxide breakdown.

C. Device Damage Region Determination

Fig. 14 shows the postdecapsulation of failed asymmetric trench SiC MOSFETs using a 3.6 mH load inductor at 25 °C and 125 °C. In both cases, failures are occurred highly localized in the vicinity of the source/gate metallization within the device, indicating that critical temperature have been reached. It is also found that the failure points are random for both devices. Although failure locations are shown to vary, it is concluded that the mechanism of failure is equivalent for all cases due to the formation of mesoplasma, and mesoplasma would likely damage a smaller region of the device due to thermal runaway [9]. These observations also indicate that the deep p-wells in an asymmetric trench structure could prevent the rupture of the gate oxide caused by higher electric fields or degrade the gate oxide through hot carrier injection.

The failed double trench SiC MOSFETs, under 3.6 mH inductor at 25 °C and at 125 °C, are shown in Fig. 15. There is no obvious damage point on the surface of the die. It is clearly seen that a catastrophically ruptured gate oxide on the right of trench bottom is observed using scanning electron microscope (SEM), as shown in Fig. 15(a), which is found by using a focused ion beam cut based on an emission microscope analysis. Cross-sectional SEM image of the damaged trench gate indicates that a significant amount of poly-silicon has migrated into the 4H-SiC epitaxial layer, thus causing device failure. In a thermal runaway failure mode, as shown in Fig. 15(b), highly localized metallization occurs at the periphery of the source pad. The decapsulation and SEM image of the failed devices reveal two different failure mechanisms in UIS conditions. Given stochastic process of the etched trench and implanted p-type shielding structures, the location of avalanche can localize near the trench gate. The gate oxide at the trench bottom is catastrophically ruptured by high electric fields during avalanche.

IV. Conclusion

The avalanche withstand capability of 1200-V trench SiC MOSFETs with asymmetric and double trench shield structures is investigated using experimental and finite-element methods. Two failure mechanisms, i.e., thermal runaway and gate oxide rupture, are confirmed. Asymmetric trench SiC MOSFETs show

the thermal runaway under 3.6 mH inductors at temperatures ranging from 25 °C to 175 °C. Gate oxide degradation is not observed during the test since asymmetric trench structure effectively limits the electric field in the oxide layer during an avalanche. These experimental results indicate a stability failure mode under an avalanche for asymmetric trench SiC MOSFETs. However, two failure modes are identified for double trench SiC MOSFETs. Gate oxide rupture and a higher gate leakage current are observed when the devices is under 3.6 mH load at room temperature. With the increase of the case temperature, double trench SiC MOSFETs show a thermal runaway failure instead of gate oxide damage. The failed devices are also decapsulated to examine the location of failure point from the perspective of the semiconductor die.

References

[1] W. Zhou, X. Zhong, and K. Sheng, "High temperature stability and the performance degradation of SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2329–2337, May 2014.

[2] S. Hazra *et al.*, "High switching performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[3] X. Deng *et al.*, "A multiple-ring-modulated JTE technique for 4H-SiC power device with improved JTE-Dose window," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5042–5047, Dec. 2017.

[4] X. She, A. Q. Huang, O. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[5] X. Li *et al.*, "A SiC power MOSFET loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron*, vol. 64, no. 10, pp. 8268–8276, Oct. 2017.

[6] K. Wada and M. Ando, "Switching loss analysis of SiC-MOSFET based on stray inductance scaling," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 1919–1924.

[7] D. Peters *et al.*, "Performance and ruggedness of 1200V SiC Trench MOSFET," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, 2017, pp. 239–242.

[8] J. W. Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. 26th Int. Symp. Power Semicond. Devices IC's*, 2014, pp. 79–82.

[9] M. D. Kelley, B. N. Pushpakaran, and S. B. Bayne, "Single-pulse avalanche mode robustness of commercial 1200 V/80 mΩ SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6405–6415, Aug. 2017.

[10] J. Wei, Y. Wang, M. Zhang, H. Jiang, and K. J. Chen, "High-speed power MOSFET with low reverse transfer capacitance using a trench/planar gate architecture," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's*, 2017, pp. 331–334.

[11] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET: Part I—History, technology, and prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 674–691, Mar. 2017.

[12] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017.

[13] S. Harada *et al.*, "3.3-kV-class 4H-SiC MeV-implanted UMOSFET with reduced gate oxide field," *IEEE Electron Devices Lett.*, vol. 37, no. 3, pp. 314–316, Mar. 2016.

[14] Y. Wang, Y. Ma, Y. Hao, Y. Hu, G. Wang, and F. Cao, "Simulation study of 4H-SiC UMOSFET structure with p+−polySi/SiC shielded region," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3719–3724, Sep. 2017.

[15] X. Li *et al.*, "SiC trench MOSFET with integrated self-assembled three-level protection Schottky barrier diode," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 347–351, Jan. 2018.

[16] T. Nguyen, A. Ahmed, T. V. Thang, and J. Park, "Gate Oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.

[17] C. Kuan Yew, S. Dimitrijev, and H. Jisheng, "Investigation of ultralow leakage in MOS capacitors on 4H SiC," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1361–1365, Sep. 2004.

[18] M. A. Anders, P. M. Lenahan, C. J. Cochrane, and A. J. Lelis, "Relationship between the 4H-SiC/SiO_2 interface structure and electronic properties explored by electrically detected magnetic resonance," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 301–308, Feb. 2015.

[19] M. Sagawa, H. Miki, Y. Mori, H. Shimizu, and A. Shima, "Evaluation of gate oxide reliability in 3.3 kV 4H-SiC DMOSFET with J-Ramp TDDB methods," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs*, 2018, pp. 363–366.

[20] A. Agarwal, K. Han, and B. J. Baliga, "Analysis of 1.2 kV 4H-SiC trench-gate MOSFETs with thick trench bottom oxide," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 125–129.

[21] T. Nakamura *et al.*, "High performance SiC trench devices with ultra-low ron," in *Proc. Int. Electron Devices Meeting*, 2011, pp. 26.5.1–26.5.3.

[22] R. Siemieniec *et al.*, "A SiC Trench MOSFET concept offering improved channel mobility and high reliability," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.13.

[23] W. Chou, A. Kempitiya, and O. Vodyakho, "Reduction of power losses of SiC MOSFET based power modules in automotive traction inverter applications," in *Proc. IEEE Transport. Electrific. Conf. Expo*, 2018, pp. 1035–1038.

[24] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Evaluation of switching performance of SiC devices in PWM inverter-fed induction motor drives," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5701–5711, Oct. 2015.

[25] Z. Tong, L. Gu, Z. Ye, K. Surakitbovorn, and J. M. R. Davila, "On the techniques to utilize SiC power devices in high- and very high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12181–12192, Dec. 2019.

[26] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun, and A. Q. Huang, "Repetitive unclamped-inductive-switching-induced electrical parameters degradations and simulation optimizations for 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4331–4338, Nov. 2016.

[27] J. Hu, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran, and P. A. Mawby, "The effect of electrothermal nonuniformities on parallel connected SiC power devices under unclamped and clamped inductive switching," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4526–4535, June 2016.

[28] X. Zhou *et al.*, "A deep insight into the degradation of 1.2-kV 4H-SiC MOSFETS under repetitive unclamped inductive switching stresses," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5251–5261, Jun. 2018.

[29] J. Wei, S. Liu, S. Li, J. Fang, T. Li, and W. Sun, "Comprehensive investigations on degradations of dynamic characteristics for SiC power MOSFETs under repetitive avalanche shocks," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2748–2757, Mar. 2019.

[30] D. Peters *et al.*, "The new CoolSiC$^{\mathrm{TM}}$ trench MOSFET technology for low gate oxide stress and high performance," in *Proc. Int. Exhib. Conf. Power Electron., Intell.. Motion, Renew. Energy Energy Manag.*, 2017, pp. 1–7.

[31] B. Kakarla, T. Ziemann, S. Nida, E. Doenni, and U. Grossner, "Planar to trench: Short circuit capability analysis of 1.2 kV SiC MOSFETs," *Mater. Sci. Forum*, vol. 924, pp. 782–785, 2018.

[32] A. Kumar, S. Parashar, J. Baliga, and S. Bhattacharya, "Single shot avalanche energy characterization of 10kV, 10A 4H-SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2737–2742.

[33] N. Ren, H. Hu, K. L. Wang, Z. Zuo, R. Li, and K. Sheng, "Investigation on single pulse avalanche failure of 900V SiC MOSFETs," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs*, 2018, pp. 431–434.

[34] A. Fayyaz *et al.*, "UIS failure mechanism of SiC power MOSFETs," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, 2016, pp. 118–122.

[35] J. Berens, F. Rasinger, T. Aichinger, M. Heuken, M. Krieger, and G. Pobegen, "Detection and cryogenic characterization of defects at the SiO_2/4H-SiC interface in trench MOSFET," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1213–1217, Mar. 2019.

[36] Y. N.-Cohen, J. Shappir, and D. F.-Bentchkowsky, "Trap generation and occupation dynamics in SiO2 under charge injection stress," *J. Appl. Phys.*, vol. 60, no. 6, pp. 2024–2035, Jun. 1986.

[37] M. S. Chinthavali, B. Ozpineci, and L. M. Tolbert, "High-temperature and high-frequency performance evaluation of 4H-SiC unipolar power devices," in *Proc. Twentieth Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2005, pp. 322–328.

[38] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*. Singapore: Wiley, 2014.