Hybrid Model Predictive Control of ANPC Converters With Decoupled Low-Frequency and High-Frequency Cells

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***Abstract*—Active-neutral-point-clamped (ANPC) converters can be decomposed into a low-frequency cell (LFC) and a high-frequency cell (HFC), and fundamental-frequency operation of the LFC is becoming popular. However, balancing the dc-link voltage and three flying capacitor voltages while maintaining very fast control of the output current is always a challenging task, especially when the flying capacitor is small. This article proposes a hybrid model predictive control (MPC) to guarantee the fundamental-frequency operation of the LFC and achieve the fixed-switching frequency operation of the HFC. In the hybrid MPC, the classical MPC regulates the LFC, whereas the duty-cycle-optimized MPC regulates the HFC. The capacitor voltage balance is achieved by adjusting the duty cycles to avoid the weighting factor tuning process. The proposed MPC features a fixed switching frequency and improves the steady-state performance while guaranteeing the fundamental-frequency operation of the LFC. Simulation and experimental results on a five-level ANPC are presented to validate the advantages of the proposed hybrid MPC method over the classical MPC.**

***Index Terms*—Active-neutral-point-clamped (ANPC) converter, capacitor voltage balance, model predictive control (MPC), phase-shifted pulsewidth modulation.**

I. Introduction

MULTILEVEL converters have been widely applied in medium-voltage motor drive systems [1], grid-tied inverters [2], energy storage systems [3], and so on [4]. The most attractive features of the multilevel converter are as follows:

1) they can operate at a higher equivalent switching frequency and better output voltage quality with reduced requirements on filters;
2) they can operate at higher ac voltage levels and minimize or even eliminate the interface transformer; and
3) they reduce switching losses.

Among the existing multilevel converters, neutral-point-clamped (NPC) [5], [6], flying capacitor (FC) [7], and cascaded H-bridge [8] multilevel converters are classical multilevel topologies that are most widely used in the industry for various applications.

In the recent decade, a number of new topologies have been proposed, for example, the hybrid clamped-multilevel converter [9], [10] and active NPC (ANPC) converters [11]–[13]. Compared to other topologies, the ANPC converters featuring advantages, such as reasonable component utilization and simple control and modulation, have been widely accepted in industrial or commercial products. A key feature of the ANPC-type topologies is that the topology can be decomposed into a low-frequency cell (LFC) and a high-frequency cell (HFC). Owing to this feature, different types of device implementations can be selected according to the application circumstances, offering opportunities to enhance the efficiency, reliability, and cost-effectiveness of the system. For example, in medium-voltage applications, the LFC of a five-level ANPC (5L-ANPC) converter can be built by two series-connected devices. In low-voltage applications, silicon insulated-gate bipolar transistors (IGBT) can be used in the LFC, whereas the emerging wide bandgap (WBG) devices can be applied in the HFC [11], [13].

With the help of WBG devices, the 5L-ANPC converter can operate at a high switching frequency for minimization of the distortion of the output voltage and of output current. However, its control and modulation problem is significantly more complex than that of two- and three-level converters. Balancing the dc-link voltage and three-phase FC voltages while maintaining very fast control of the output current is a challenging task, especially when the FC is small [14].

To achieve high-performance control of the 5L-ANPC converter, a number of control and modulation strategies have been proposed. Generally, these approaches divide the control and modulation problem into two hierarchical layers. The upper layer controls the output current by regulating the three-phase converter voltages [15], [16], and the lower layer maps the converter voltage of the upper layer into the gate signals by modulation techniques [17]–[20]. To ensure proper operation of the ANPC converters, the capacitor voltage and the neutral-point voltage should be balanced simultaneously together with the output current control. The multiple proportional-integral (PI) or proportional-resonance (PR) loops with pulsewidth modulation (PWM) based controller are an alternative solution. Other than two PI or three PR loops for the output current control, PI loops for capacitor voltage balancing are also needed [20]–[22].

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However, multiple PI loops lead to tedious tuning works, and the post-error-based PI/PR loops lead to poor dynamic performance [23], [24].

Model predictive control (MPC) appears to be an ideal control scheme for this type of converter due to its ability to handle a complex multiobjective problem, its fast dynamic response, and its ability to provide very low switching frequencies and losses [15], [16], [25]–[28]. In particular, MPC allows one to address the output current control problem as well as the balancing of the internal converter voltages in a combined manner. All the control goals are expressed as a cost function, and its minimization is used as a criterion to choose the best switching state, which would be applied to the converter during the next sampling interval [29]. As a result, all the control objectives can be met simultaneously.

However, the classical MPC of the ANPC converters suffers from variable switching frequency, which affects the design of the power filters and heat sinks [30], [31]. Moreover, non-interleaved switching manner in the classical MPC leads to the limited current control performance. More importantly, the fundamental-frequency operation of the LFC, FC balance and, dc-link capacitor voltage balance should be achieved simultaneously in addition to output current control in the ANPC converter. Substantial weighting factors, which are cumbersome to tune, are required to achieve all the control objectives simultaneously [32].

The duty-cycle-optimized MPC approach can achieve improved performance at a constant switching frequency while retaining all the advantages of the classical MPC methods. Therefore, the duty-cycle-optimized MPC approach has been extensively studied in a 2L-converter [33]–[36]. In these methods, vectors in each sector were selected, and the optimal duty cycles for each vector were calculated by tracking error minimization. However, as there are 96 sectors in a 5L-ANPC converter, selecting one sector out of 96 sectors results in heavy computation burden. Considering the massive computation required to select the desired sectors and determine the dwell time calculation for each vector, the duty-cycle-optimized MPC design for the 5L-ANPC becomes quite difficult. Therefore, no literature, to our best knowledge, is reported using the duty-cycle-optimized MPC for an ANPC converter.

This article proposes a hybrid MPC to guarantee the fundamental-frequency operation of the LFC and achieve fixed-switching frequency operation of the HFC. In the proposed hybrid MPC, classical MPC is utilized for the LFC control, whereas duty-cycle-optimized MPC is applied to the HFC control. The optimal duty cycle of the proposed MPC is calculated by the virtual switching state and applied by the phase-shifted PWM (PS-PWM). Thanks to the interleaved switching manner of PS-PWM, the proposed hybrid MPC presents better output waveforms. The capacitor voltage balance is achieved by adjusting the duty cycles to avoid the weighting factor tuning process. The proposed MPC features a fixed switching frequency and enhanced steady-state performance while retaining the benefits of the classical MPC. Simulation and experimental results on a 5L-ANPC converter are presented to validate the advantages of the proposed hybrid MPC method over the classical MPC.

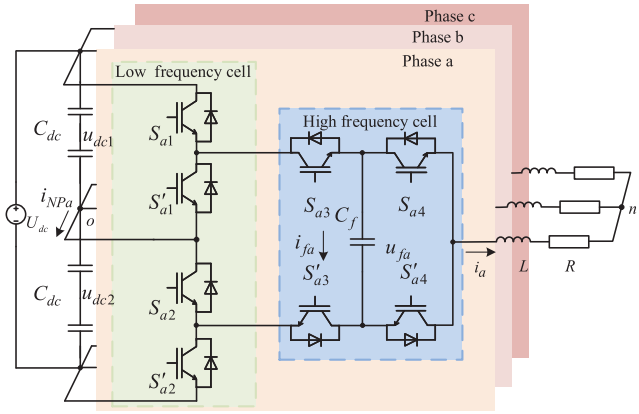

Fig. 1. Structure of a 5L-ANPC converter.

TABLE I
SWITCHING STATE OF A 5L-ANPC CONVERTER

	S_{x1}/S_{x2}	S_{x3}	S_{x4}	u_{xo}	v_x	i_{NPx}	i_{fx}
$V0$	0	0	0	$-U_{dc}/2$	-2	0	0
$V1$	0	0	1	$-U_{dc}/4$	-1	0	$-i_x$
$V2$	0	1	0	$-U_{dc}/4$	-1	i_x	i_x
$V3$	0	1	1	-0	0	i_x	0
$V4$	1	0	0	+0	0	i_x	0
$V5$	1	0	1	$U_{dc}/4$	+1	i_x	$-i_x$
$V6$	1	1	0	$U_{dc}/4$	+1	0	i_x
$V7$	1	1	1	$U_{dc}/2$	+2	0	0

II. MATHEMATICAL MODEL OF A 5L-ANPC CONVERTER

The 5L-ANPC converter is utilized as a case study to illustrate the concept of the proposed hybrid MPC scheme. The three-phase 5L-ANPC topology, as shown in Fig. 1, is a combination of an ANPC and an FC topology. Each phase of the 5L-ANPC converter consists of eight switches and an FC.

S_{x1}, S'_{x1}, S_{x2}, and S'_{x2} require two switches connected in series or high-voltage switches to bear a higher voltage, which is the double of S_{x3}, S'_{x3}, S_{x4}, and S'_{x4}, where x represents phase (a, b, or c). i_{NPx} and i_{fx} are the corresponding NP current and FC current. i_x and u_{xo} are the phase current and voltage. (S_{x1}, S'_{x1}), (S_{x2}, S'_{x2}), (S_{x3}, S'_{x3}), and (S_{x4}, S'_{x4}) are complementary switch pairs. S_{x1} and S_{x2} require the same switching signal. The voltage across the FC is assumed constant and equal to $u_f = U_{\mathrm{dc}}/4$, and the voltages across the dc-link capacitor are u_{dc1} and u_{dc2}. The total dc-link voltage is U_{dc}. The output voltage level and current direction corresponding to the switching state are summarized in Table I.

From Table I, it can be seen that S_{x1} and S_{x2} are turned OFF when the output voltage is negative and turned ON when the output voltage is positive. Therefore, the high-voltage switch pairs (S_{x1}, S'_{x1}) and (S_{x2}, S'_{x2}) can be operated at the fundamental frequency to reduce the switching loss.

The output phase voltage of the 5L-ANPC u_{xo} can be represented as follows:

$$u_{xo} = \left(S_{x1} + \frac{S_{x3}}{2} + \frac{S_{x4}}{2} - 1\right)\frac{U_{\mathrm{dc}}}{2}. \tag{1}$$

It is straightforward to design a classical MPC strategy for a 5L-ANPC converter, which evaluates all the possible switching states and selecting the one minimizes the cost function. As shown in Table I, the 5L-ANPC converter only generates five different output voltages (0, $\pm U_{\rm dc}/4$, $\pm U_{\rm dc}/2$) assuming FC voltage and the dc-link voltage constant. Five corresponding changes in the output current dynamics are possible in each phase. The output current dynamics of each phase can be expressed as

$$u_{xo} = i_x R + L\frac{di_x}{dt} \tag{2}$$

where L and R are the load inductance and resistance, respectively.

The instantaneous NP current $i_{\rm NPx}$ can be written as

$$i_{\rm NPx} = \begin{cases} (1 - S_{x3})i_x, & S_{x1} = 1 \\ S_{x3} i_x, & S_{x1} = 0 \end{cases}. \tag{3}$$

Applying Kirchhoff's current law, the dynamic equation for dc-link capacitor voltage can be denoted by

$$C_{\rm dc}\frac{du_{\rm dc1}}{dt} - C_{\rm dc}\frac{du_{\rm dc2}}{dt} = \sum i_{\rm NPx} \tag{4}$$

where $\sum i_{\rm NPx}$ is the sum of three-phase NP current.

The instantaneous FC current i_{fx} can be expressed as

$$i_{fx} = (S_{x3} - S_{x4})i_x. \tag{5}$$

III. Classical MPC

The classical MPC considers the power converter as a finite set of linear models, each representing a physical switching state. A prediction of the controlled variables for each switching combination is calculated, evaluated in a cost function. The switching combination that minimizes the cost function is selected and directly applied to the converter during the entire sampling period. All the control objectives are directly regulated by the switching combination selection [37].

A. Implementation of the Classical MPC

To clarify the advantage of the proposed hybrid MPC scheme, the classical MPC, which can guarantee the fundamental-frequency operation of the LFC, is also developed for comparison in this section.

The output current dynamics can then be expressed in the discrete-time domain as follows:

$$i_x(k+1) = i_x(k) + \frac{T_s}{L}\left(u_{xo}(k) - i_x(k)R\right). \tag{6}$$

The dc-link capacitor voltage and the FC voltage dynamics can be written in the discrete-time domain as follows:

$$\Delta u_{\rm dc}(k+1) = \Delta u_{\rm dc}(k) + \sum \frac{T_s}{C_{\rm dc}} i_{\rm NPx}(k) \tag{7}$$

$$u_{fx}(k+1) = u_{fx}(k) + \frac{T_s}{C_f} i_{fx}(k) \tag{8}$$

where $\Delta u_{\rm dc} = u_{\rm dc1} - u_{\rm dc2}$ at each sampling period.

In the classical MPC method, the future output current, dc-link capacitor voltage, and FC voltage are predicted on the basis of the dynamics provided by (6)–(8), respectively. By evaluating eight predicted values from the standpoint of the errors at every sampling instant, one optimal switching state among eight obtainable switching states is selected to minimize errors between the one-step future references and predicted values. The cost function can be defined as

$$\begin{aligned} J = {} & (i_x^*(k+1) - i_x(k+1))^2 + \mu_1 (u_{fx}^* - u_{fx}(k+1))^2 \\ & + \mu_2 (\Delta u_{dc}^* - \Delta u_{dc}(k+1))^2 \\ & + \mu_3 (S_{x1}(k+1) - S_{x1}(k))^2 \end{aligned} \tag{9}$$

where $i_x^*(k+1)$ is the extrapolation output current reference at the $(k+1)$th instant, which will be illustrated in (10). $\Delta u_{\rm dc}^*$ is the difference value of the two dc-link capacitor voltage references, which is always set to zero. u_{fx}^* is the FC voltage reference, which is set to $U_{\rm dc}/4$. $S_{x1}(k)$ is the switching state applied in the present control period. μ_1, μ_2, and μ_3 are the weighting factors that determine the importance of different objectives when selecting the optimal switching combination. With a proper selection of the weighting factors, the fundamental-frequency operation of the LFC can be guaranteed.

Since the cost function performs the comparison at the $(k+1)$th instant, the references should be extrapolated to future state. The following fourth-order Lagrange extrapolation [38] is used here:

$$i_x^*(k+1) = 4i_x^*(k) - 6i_x^*(k-1) + 4i_x^*(k-2) - i_x^*(k-3). \tag{10}$$

Finally, the switching state with the minimum cost function value will be applied at the next sampling instant. The classical MPC method evaluates the switching states at only fixed sampling instants and applies one optimal switching state during the entire sampling period. The control diagram of the classical MPC is depicted in Fig. 2.

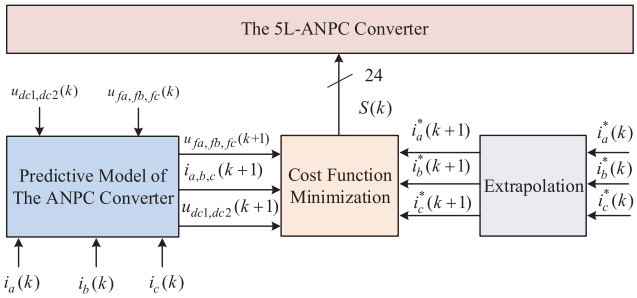

Fig. 2. Control diagram of the classical MPC.

B. Limitation of Classical MPC

There are several inherent limitations within the classical MPC when applied to the ANPC converter.

1) Variable Switching Frequency: In the classical MPC, the optimal switching state is applied during the entire sampling period to force the actual output to approach the reference at the next step. The resulting switching frequency is variable with a maximum value not exceeding the half of the sampling frequency. In order to achieve satisfactory control performance for

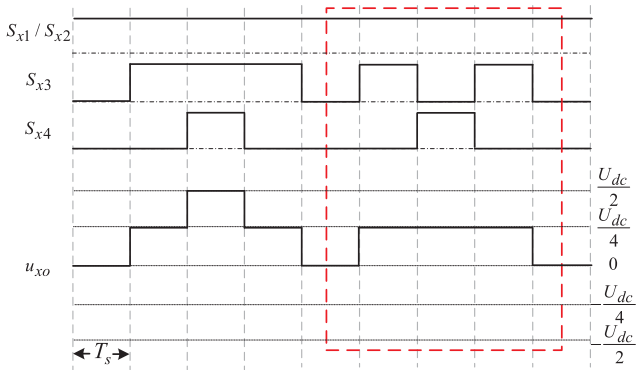

Fig. 3. Depiction of the switching pulses generated by a classical MPC controller for a 5L-ANPC converter. From top to bottom are switching pulses of $S_{x1}/S_{x2}, S_{x3}, S_{x4}$, and output voltage level.

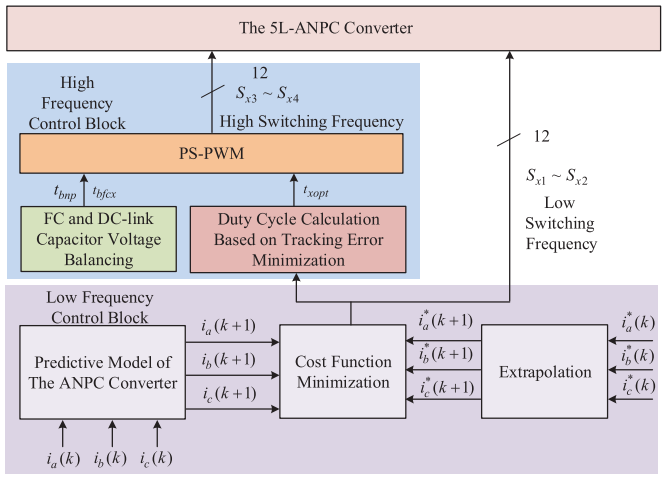

Fig. 4. Control diagram of the proposed MPC.

reference tracking, the control algorithm has to be evaluated at a higher rate than the switching frequency. When it comes to the case of the ANPC converter, this situation is not alleviated since the switching manner of the classical MPC is noninterleaved. It leads to that the maximum equivalent switching frequency at the output terminal does not exceed the half of the sampling frequency, as shown in Fig. 3. Moreover, in some extreme conditions, the internal switching time is much higher than the equivalent switching time in the output terminal, as shown in the dashed box in Fig. 3, where the total switching time of the two switches is three, whereas only one switching time exists in the terminal. The extra switching time is caused by internal dynamics such as FC voltage balance.

2) Weighting Factor Tuning: All the control objectives are regulated by the switching combination selections in the classical MPC. When the number of the control objectives is over two, which is exactly the case in the ANPC converter, as shown in (9), substantial weighting factors are introduced. Up to now, there is no formal way to get the optimal value of the weighting factors. They are always determined in an empirical trial-and-error way [32]. Therefore, it is sometimes challenging to fine-tune those weighting factors.

IV. Proposed Hybrid MPC

The ANPC converters can be decomposed into an LFC and an HFC. It is, therefore, very suitable to decouple the MPC scheme into two parts, i.e., the classical MPC for the LFC control and the duty-cycle-optimized MPC for the HFC control. The control diagram of the proposed MPC for the ANPC is depicted in Fig. 4. Each part is clarified as follows.

A. LFC Control

The series-connected or high-voltage switches S_{x1} and S_{x2} are ON when the output phase voltage is positive, whereas S'_{x1} and S'_{x2} are ON when the output phase voltage is negative. Therefore, the switching state of LFC can be selected by evaluating the cost function through substituting (6) and (10) into the following equation:

$$J_h = \left(i_x^*(k+1) - i_x(k+1)\right)^2. \tag{11}$$

TABLE II
Virtual Switching States Table

S_{x1}/S_{x2}	S_{vx}	Output Voltage value
0	0	$-U_{dc}/2$
0	1	-0
1	0	0
1	1	$U_{dc}/2$

As there are two switching states in the LFC, voltages with the same magnitude and opposite signs ($U_{\rm dc}/2$, $-U_{\rm dc}/2$) are substituted into $u_{xo}(k)$ to select the proper switching state of LFC for output current tracking. If $U_{\rm dc}/2$ has a smaller cost function value, $S_{x1} = 1$ will be selected, and S_{x1} and S_{x2} will be ON. Otherwise, if $-U_{\rm dc}/2$ has a smaller cost function value, S'_{x1} and S'_{x2} will be ON.

To ensure the fundamental-frequency operation of the LFC, a hysteresis technique is included. That is, the switching state of the LFC changes only when its switching state is different from that of the previous control period for consecutive two control periods. Otherwise, the switching state of the LFC stays unchanged.

B. HFC Control

As shown in (1), the switching pairs in the HFC can be considered as functionally identical parts, where the switching action of each switching pair only leads to $U_{\rm dc}/4$ change in the output terminal. In order to simplify the duty cycle calculation process, the two functionality-equivalent switching pairs are considered as a whole during the duty cycle calculation. For simplicity, the two switching pairs are considered as a virtual single switching pair, whose switching state is denoted by S_{vx}. The virtual switching state $S_{vx} = 1$ when $S_{x3} = 1$ and $S_{x4} = 1$, and the virtual switching state $S_{vx} = 0$ when $S_{x3} = 0$ and $S_{x4} = 0$. The virtual switching state and their output voltages are listed in Table II.

The optimal duty cycle is obtained based on the tracking error minimization. The implementation process of the proposed scheme, when $S_{x1}/S_{x2} = 1$ is selected, is presented. The case,

when $S_{x1}/S_{x2} = 0$ is selected, can be calculated in the same way. The slopes of the output current when applying virtual switching state S_v can be denoted by the following:

$$s_{x1} = \frac{1}{L}\left(\frac{U_{\rm dc}}{2}S_{vx} - i_x(k)R\right)\Big|_{S_{vx}=1} \tag{12}$$

$$s_{x0} = \frac{1}{L}\left(\frac{U_{\rm dc}}{2}S_{vx} - i_x(k)R\right)\Big|_{S_{vx}=0}. \tag{13}$$

The predicted output current at the end of the control period can be expressed by

$$i_x(k+1) = i_x(k) + s_{x1}t_{\rm xopt} + s_{x0}(T_s - t_{\rm xopt}) \tag{14}$$

where $t_{\rm xopt}$ is the optimal duty cycle for virtual switching state $S_{vx} = 1$ and $(T_s - t_{\rm xopt})$ is the duty cycle for virtual switching state $S_{vx} = 0$.

To obtain the minimized output current tracking error, the optimal values of $t_{\rm xopt}$ should satisfy the minimum value condition

$$\frac{\partial J_h}{\partial t_{\rm xopt}} = 0. \tag{15}$$

The solution of (15) is given by

$$t_{\rm xopt} = \frac{i_x^*(k+1) - i_x(k) - s_{x0}T_s}{s_{x1} - s_{x0}}. \tag{16}$$

In the proposed MPC, the optimal duty cycle for the output current control is calculated by the MPC using the virtual switching state and applied by PS-PWM. Taking $S_{x1}/S_{x2} = 1$ for example, the output voltage is equal to $NU_{\rm dc}/4$ if $S_{vx} = 1$ or 0 if $S_{vx} = 0$. N is number of the cascaded cells, and N=2 in the 5L-ANPC converter. The duty cycle for $S_{vx} = 1$ is $t_{\rm xopt} \in [0, T_s]$. The calculated output voltage–second at each sampling point is

$$\zeta_c = N\frac{U_{\rm dc}}{4}t_{\rm xopt}. \tag{17}$$

In PS-PWM, the voltage across the cascaded part is $U_{\rm dc}/4$, and the duty cycles for S_{x3} and S_{x4} are $t_{x3} \in [0, NT_s]$ and $t_{x4} \in [0, NT_s]$. The total output voltage–second generated by the PS-PWM is

$$\zeta_a = \frac{U_{\rm dc}}{4}(t_{x3} + t_{x4}). \tag{18}$$

Obviously, if $Nt_{\rm xopt} = t_{x3} + t_{x4}$ is guaranteed, the calculated voltage–second value ζ_c is equal to the applied voltage–second value ζ_a. As shown in Fig. 5, the proposed hybrid MPC scheme meets the voltage–second balance rule.

Hence, the optimal duty cycle for each cell can be calculated as follows:

$$t_{\rm opt} = \frac{N(U_{\rm dc}/4)t_{\rm xopt}}{U_{\rm dc}/4} = Nt_{\rm xopt}. \tag{19}$$

The equivalence of the duty cycle calculation and implementation is presented in Fig. 5. The duty cycle is updated at the peak/valley point of carriers. For each cell, the applied duty cycle $t_{\rm opt} \in [0, NT_s]$ and the update frequency is $\frac{1}{NT_s}$.

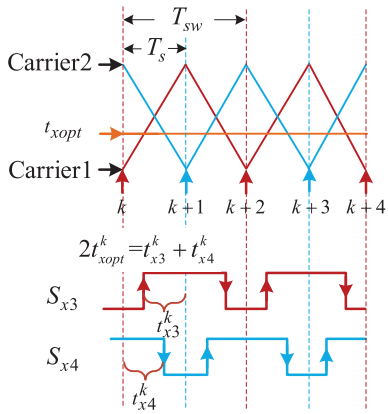

Fig. 5. Depiction of the PWM pulse trains for two phase-shifted triangular carriers.

C. FC Voltage Balance

FC voltage control is necessary in the 5L-ANPC [19]. The FC voltage can be written as

$$i_{fx} = (S_{x3} - S_{x4})i_x. \tag{20}$$

The average FC current in a carrier period is

$$i_{fx} = (t_{x3} - t_{x4})i_x \tag{21}$$

where t_{x3} and t_{x4} are the duty cycles of S_{x3} and S_{x4} in a carrier period, respectively.

As S_{x3} and S_{x4} are cascaded cells, the balance of FC voltage can be achieved by adjusting the duty cycles of S_{x3} and S_{x4}. As long as the sum of the duty cycles of S_{x3} and S_{x4} remains unchanged, the output voltage will not be affected. The duty cycle applied for FC voltage balance can be denoted by

$$t_{\rm bfcx} = k_{\rm bfc}{\rm sgn}(i_x)(u_f^* - u_{fx}) \tag{22}$$

where u_f^* is the reference for FC voltage, ${\rm sgn}(*)$ is a sign function that extracts the sign of a real number, and $k_{\rm bfc}$ is a positive constant for the FC voltage balancing.

Taking (21) into consideration, the FC voltage balance can be achieved by adjusting the duty cycles of S_{x3} and S_{x4} as follows:

$$t_{x3} = Nt_{\rm xopt} + t_{\rm bfcx} \tag{23}$$

$$t_{x4} = Nt_{\rm xopt} - t_{\rm bfcx}. \tag{24}$$

As shown in (23) and (24), the sum of the duty cycles of S_{x3} and S_{x4} remains unchanged, and the output voltage will not be affected for the FC voltage balance.

D. DC-Link Voltage Balance

$\sum i_{\rm NPx}$ can be represented by the sum of its dc component $\sum \bar{i}_{\rm NPx}$ and ac component $\sum \tilde{i}_{\rm NPx}$, and the analytical solution of (4) is deduced to the following:

$$u_{\rm dc1}(t) - u_{\rm dc2}(t) = \sum \frac{1}{C_{\rm dc}}\int (\tilde{i}_{\rm NPx} + \bar{i}_{\rm NPx})dt + u_{\rm dc1}(0) - u_{\rm dc2}(0). \tag{25}$$

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Simulation	Experiment
DC bus voltage: U_{dc}	1500 V	240 V
Load inductance: L	10 mH	3 mH
DC bus capacitance:C_{dc}	1000 μF	1500 μF
Load resistance: R	30 Ω	10 Ω
Output frequency: f_0	60 Hz	60 Hz
Flying capacitance: C_f	50 μF	50 μF
Dead time	NA	1.5 μs

The integral of the ac component in a period is equal to zero, which means that the ac component do not affect the balance of the dc-link capacitor voltage. However, a small dc-component $\sum \bar{i}_{\text{NPx}}$ will give rise to the deviation of the dc-link capacitor voltages. When $\sum \bar{i}_{\text{NPx}}$ is positive, the voltage of the upper capacitor deviates to a higher value, whereas that of the lower one deviates to a lower value and vice versa.

The dc-link capacitor voltages are measured in real time, which consist of both ac and dc components. In order to suppress the capacitor voltage deviation effectively, the dc component difference of the capacitor voltages is extracted by a low-pass filter (LPF). The control of the dc-link capacitor voltage balance can be achieved by injecting a small amount of $\sum \bar{i}_{\text{NPx}}$. In the three-phase system, zero-sequence voltage does not influence the output line voltage and current. However, it will result to different NP current [39]. This feature can be utilized to balance the dc-link capacitor voltages

$$t_{\text{bnp}} = k_{\text{bnp}}(\Delta u^*_{\text{dc}} - \Delta \bar{u}_{\text{dc}}) \tag{26}$$

where $\Delta \bar{u}_{\text{dc}} = \bar{u}_{\text{dc1}} - \bar{u}_{\text{dc2}}$, $\bar{u}_{\text{dc1}}$ and $\bar{u}_{\text{dc2}}$ are the filtered upper and lower capacitor voltages, respectively. k_{bnp} is a proportional control parameter to adjust the balance of the dc-link capacitor voltage.

Taking the dc-link capacitor voltage and FC voltage balancing into consideration, the duty cycle for the ANPC at each sampling point can be represented as

$$d_{x3} = Nt_{\text{xopt}} + t_{\text{bnp}} + t_{\text{bfcx}} \tag{27}$$

$$d_{x4} = Nt_{\text{xopt}} + t_{\text{bnp}} - t_{\text{bfcx}}. \tag{28}$$

In the hybrid MPC, the interleaved switching manner in each phase is achieved by the employment of the PS-PWM, as shown in Fig. 5. In this regard, the steady-state output waveform can be improved in comparison with that of the classical MPC. Furthermore, due to the flexibility provided by the duty cycle, the dc-link voltage and FC voltage balance can be achieved without using weighting factors.

V. SIMULATION RESULTS

In order to validate the effectiveness of the proposed MPC for the 5L-ANPC converter, simulation studies have been carried out in the MATLAB/Simulink environment. The parameters of the simulation and experimental test are presented in Table III.

A. Steady-State Performance Analysis

The switching states diagram of the three MPC schemes is presented in Fig. 6. As shown, the fundamental switching frequency of S_{x1}/S_{x2} is achieved by the hybrid MPC. The fundamental switching frequency of the LFC is also achieved in the classical MPC by properly tuning the weighting factor μ_3. For the proposed hybrid MPC, the switching state of each phase are interleaved due to the phase shift modulator, whereas for the classical MPC, the switching manner of the classical MPC is noninterleaved, which leads to fewer pulses at the total arm output voltage as shown in Fig. 6. Fewer pulses simply mean that it generates higher current ripples, and this explains why the proposed hybrid MPC has better steady-state performance than that of the classical ones.

The fundamental switching frequency of the LFC in all the three control methods is guaranteed. Therefore, the switching frequency of S_{x1}/S_{x2} is 60 Hz. As well known, the switching frequency of S_{x3}/S_{x4} in the classical MPC is variable. The effect of load variations on the switching frequency is investigated by changing the load within the range from 20 to 100% of their nominal values where five points are selected for the test. The tested results are presented in Fig. 7. Due to the employment of PS-PWM, the switching frequency of S_{x3}/S_{x4} in the proposed MPC is constant, and equal to the carrier frequency (5 kHz). As shown in Fig. 7, the average frequency of S_{x3}/S_{x4} of the classical MPC presents a higher switching frequency under the medium-load profile. The reason is that the redundant switching state exists at output voltage level $\pm\frac{U_{\text{dc}}}{4}$ if the switching state S_{x1}/S_{x2} is determined, as shown in Table I. On the other hand, the classical MPC at a sampling frequency of 20 kHz, which presents an average switching frequency from 4.5 to 6.6 kHz, can be regarded as the benchmark for comparison with the proposed MPC under the same average switching frequency.

In the classical MPC, all the control objectives are controlled by selecting the switching states. Therefore, a certain number of switching times are required to guarantee internal dynamics, such as the FC voltage balancing, which results in increased switching frequency under the medium-load profile. The proposed MPC operates at the fixed switching frequency, and the internal dynamic is achieved by adjusting the applied duty cycles. In view of this, it is understandable that the output current performance of the classical MPC with a higher switching frequency is even worse than that of the proposed MPC.

As shown in Fig. 6, the voltage level of all the MPC schemes only steps to the adjacent voltage level, i.e., the voltage level 0 only steps to ± 1 in the next period, when the fundamental operation of the LFC is guaranteed. The waveforms of the output current and voltage without the fundamental operation of the LFC are presented in Fig. 8. The voltage level can step to a nonadjacent voltage level, which leads to large spikes in the output current, if fundamental operation of the LFC is not guaranteed. Therefore, the fundamental operation of the LFC can not only reduce the power losses but also improve the quality of the output current.

The steady-state performance of the 5L-ANPC converter, regulated by the three MPC schemes, is investigated, and the

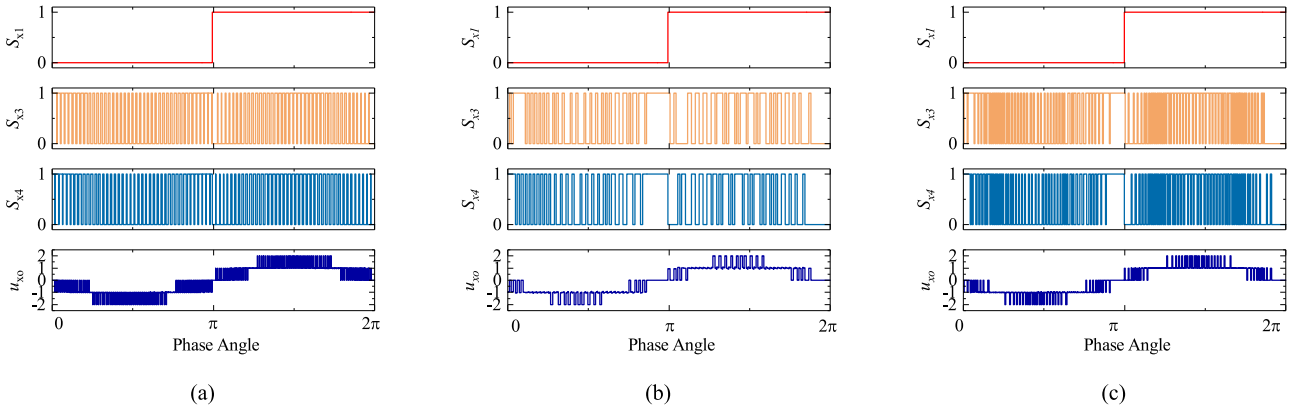

Fig. 6. Switching state diagram of the 5L-ANPC converter for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to down bottom are the switching signal of S_{x1}, switching signal of S_{x3}, switching signal of S_{x4}, and output voltage.

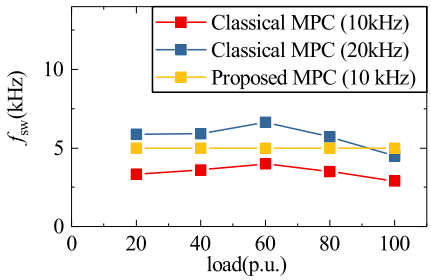

Fig. 7. Average switching frequency of the S_{x3}/S_{x4} at different load conditions.

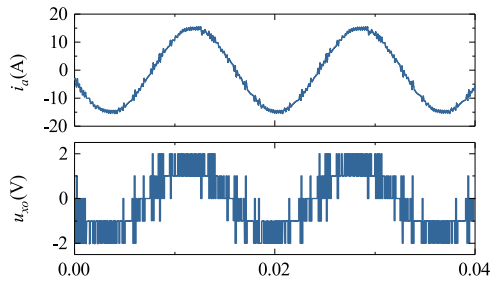

Fig. 8. Depiction of the output voltage and current without guaranteeing fundamental operation of the high-voltage cell. From top to bottom are output current and voltage of phase "a."

results are presented in Fig. 9. In the validation, the output power is set to 30 kW. The steady-state performance regulated by the proposed MPC with PS-PWM at 10 kHz sampling frequency is illustrated in Fig. 9(a). It can be seen that the load current is well regulated with the help of MPC methods. The ANPC converter operates stably with balanced dc-link and FC voltages. For comparison, the voltage and current waveforms of the ANPC with classical MPC operated at 10 and 20 kHz sampling frequencies are presented in Fig. 9(b) and (c), respectively. As shown in the results, the classical MPC can also achieve a well-regulated output current with balanced dc-link and FC voltages. However, the current ripples of the proposed MPC are much smaller even compared with the classical MPC, which operates at 20 kHz sampling frequency. The tracking performance of the three MPCs is also tested. As shown in Fig. 10, the proposed MPC presents the smallest tracking errors. The tracking error of classical MPC (10 kHz) is over 4 A, and that of classical MPC (20 kHz) is over 2 A, whereas that of the proposed MPC (10 kHz) is around 0.6 A. Therefore, it is evident that the proposed MPC can track the current references more accurately than that of the classical MPC.

In order to further validate the advantage of the proposed MPC in the steady state, the harmonic spectra of the load current are presented in Fig. 11. With the same sampling frequency, the load current total-harmonic distortion (THD) of classical MPC is 6.3%, which is much higher than that of the proposed MPC, which is 1.8%, proving the dramatic performance improvement in output current quality. The load current THD of the proposed MPC is even better than that of classical MPC operating at 20 kHz whose load current THD is 3.47%. It should be noted that for classical MPC, only one switching state is used in one control period, and the harmonic contents are distributed broadly, which are not easy to filter. On the contrary, by using the proposed MPC with PS-PWM, the switching frequency can be constant. The current harmonics concentrate on the 10, 20, and 30 kHz, which are in accordance with the equivalent switching frequency. This brings some benefits of the filter design.

B. Transient-State Performance Analysis

The dynamic response of the three MPC methods is evaluated in Fig. 12. The amplitude of the output power reference is changed from 30 to 15 kW at 0.2 s. It can be seen that the 5L-ANPC converter is stable during the large operation point step changes in all cases. As shown in the results, the transient response of the proposed hybrid MPC is very fast and the same as that of the classical MPC, indicating that the advantage of fast dynamic response in classical MPC is intact. The percentage of dc-link capacitor voltage difference is the same in the three cases. However, the proposed hybrid MPC presents the best output current and voltage quality.

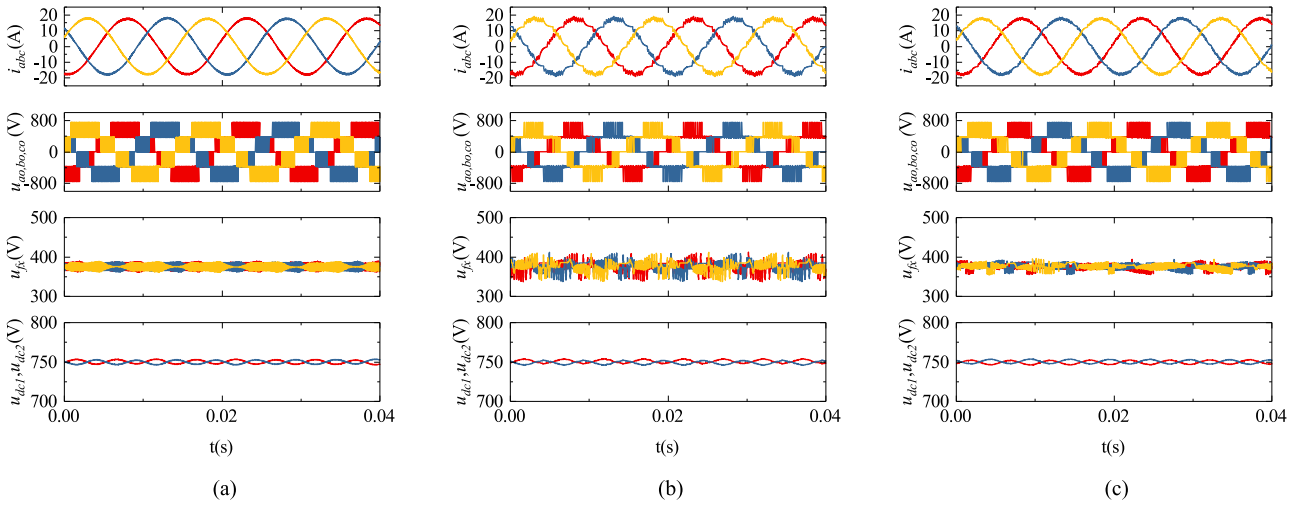

Fig. 9. Steady-state control performance for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. For each figure set, from top to down bottom are load currents, output voltages, FC voltages, and dc-link capacitor voltages.

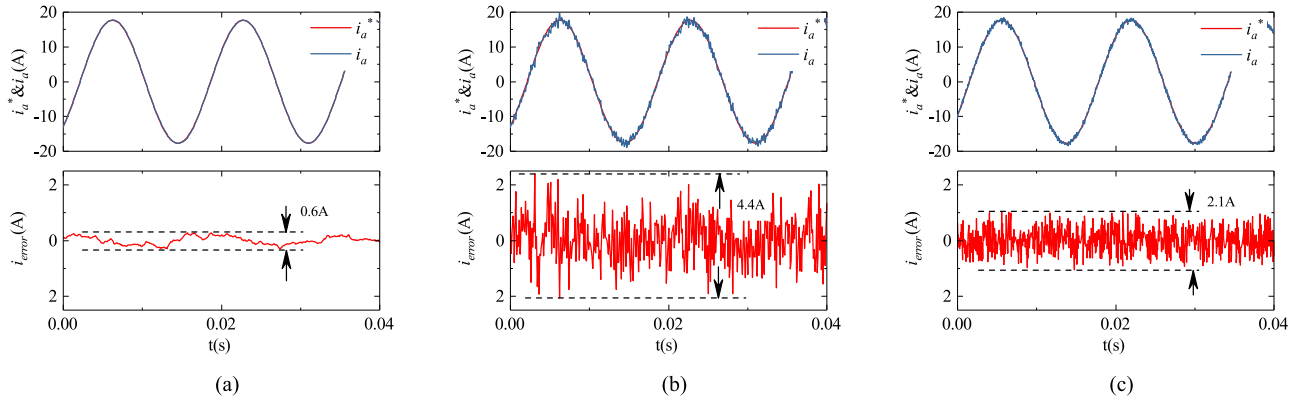

Fig. 10. Tracking errors of MPC for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to bottom, waveforms are reference current, output current, and their tracking errors.

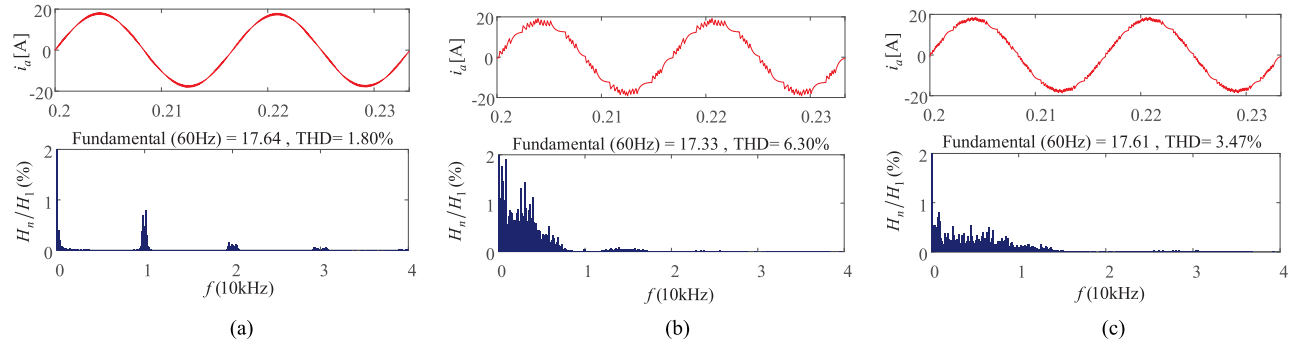

Fig. 11. FFT results for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to bottom, waveforms are the load current of phase "a" and its spectrum.

VI. Experimental Results

Apart from the simulation study, the proposed hybrid MPC is experimentally tested on a downscaled 5L-ANPC converter, where the experimental setup is illustrated in Fig. 13. The results obtained from classical MPC at 10 kHz sampling frequency and 20 kHz sampling frequency, which can guarantee the fundamental switching frequency of the LFC, are also presented for comparison. A dSPACE MicroLabBox DS1202 was adopted to implement the digital control, and a slave Xilinx

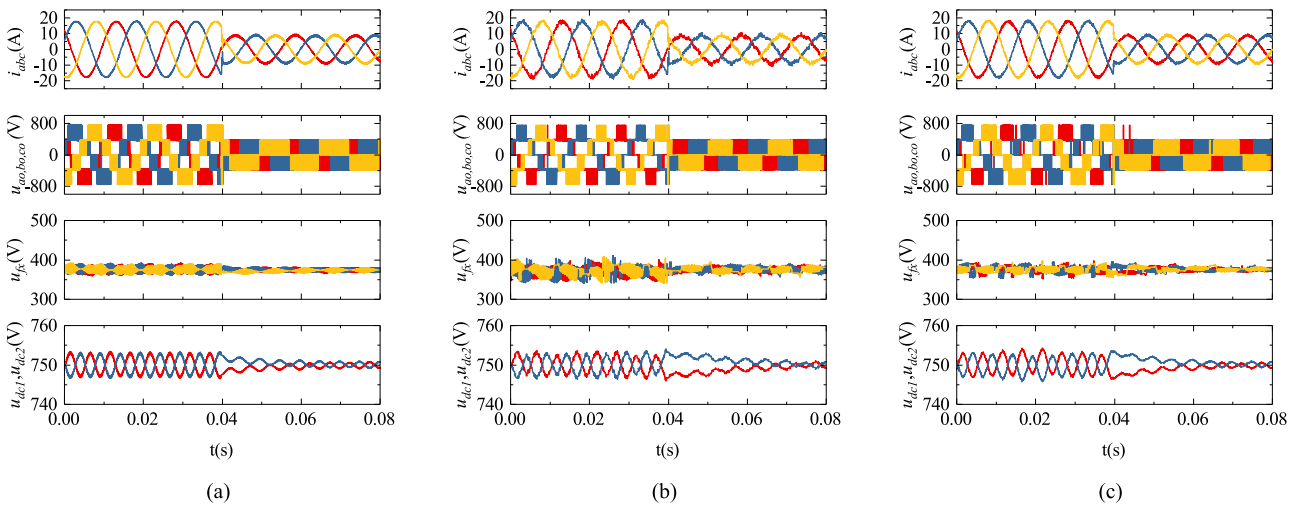

Fig. 12. Simulation results of transient-state performance for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to bottom, waveforms are load currents, output voltages, FC voltages, and dc-link capacitor voltages.

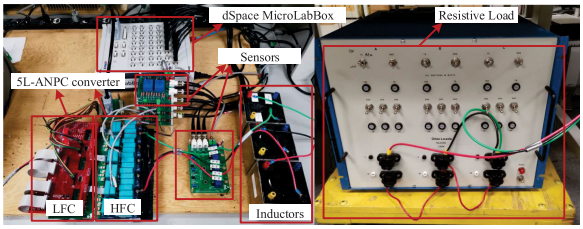

Fig. 13. Experimental setup.

was applied to generate the gate signals for each switch, implementing the digital-to-analog conversion. The LFC was implemented by insulated-gate bipolar transistors (IGBTs) (Infineon IKQ50N120CT2), whereas the HFC was implemented by GaN devices (GaN Systems GS66516). In the following tests, all the variables are directly measured by current and voltage probes, and are displayed on a digital oscilloscope via the current and voltage variables. The execution times of the classical MPC and the proposed MPC are 11.24 and 11.32 μs, respectively. It is evident that the proposed method has a similar calculation time compared to classical MPC.

Similar to Fig. 9, the steady-state performance of the MPC methods is first investigated. As shown in Fig. 14, the switching signal of S_{a1} is a pulse train with 60 Hz, indicating that the fundamental operation of the LFC is achieved in the proposed MPC methods. The stable operation of the 5L-ANPC converter with balanced dc-link and FC voltages can be achieved in all the schemes. At the same sampling frequency, the proposed MPC presents smaller output current ripples, smaller FC voltage ripples in comparison with that of the classical MPC. With the employment of the PS-PWM, better output voltage waveform of the proposed MPC is presented. Compared with the classical MPC at a sampling period of 20 kHz, the proposed MPC still presents smaller output current ripples, smaller FC voltage ripples, indicating the superiority of the proposed hybrid MPC scheme. In this regard, the proposed hybrid MPC can operate

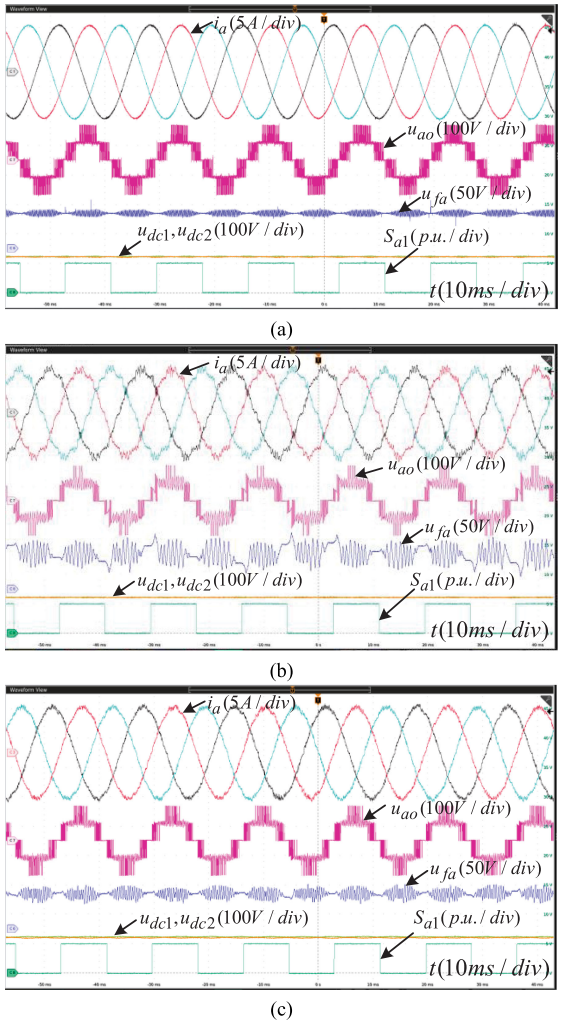

Fig. 14. Experimental results of steady-state performance for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to bottom, waveforms are load currents, phase "a" voltage, FC voltages, dc-link capacitor voltages, and switching signal of S_{a1}.

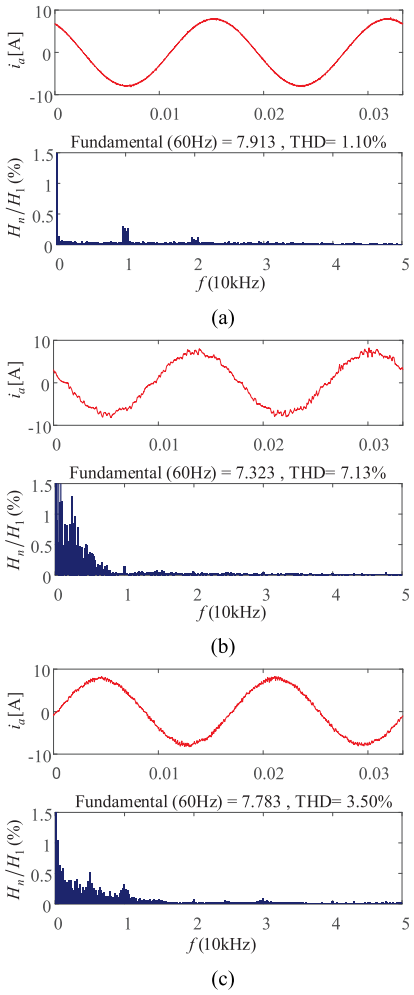

Fig. 15. FFT results of phase "a" current for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to bottom, waveforms are the load current of phase "a" and its spectrum.

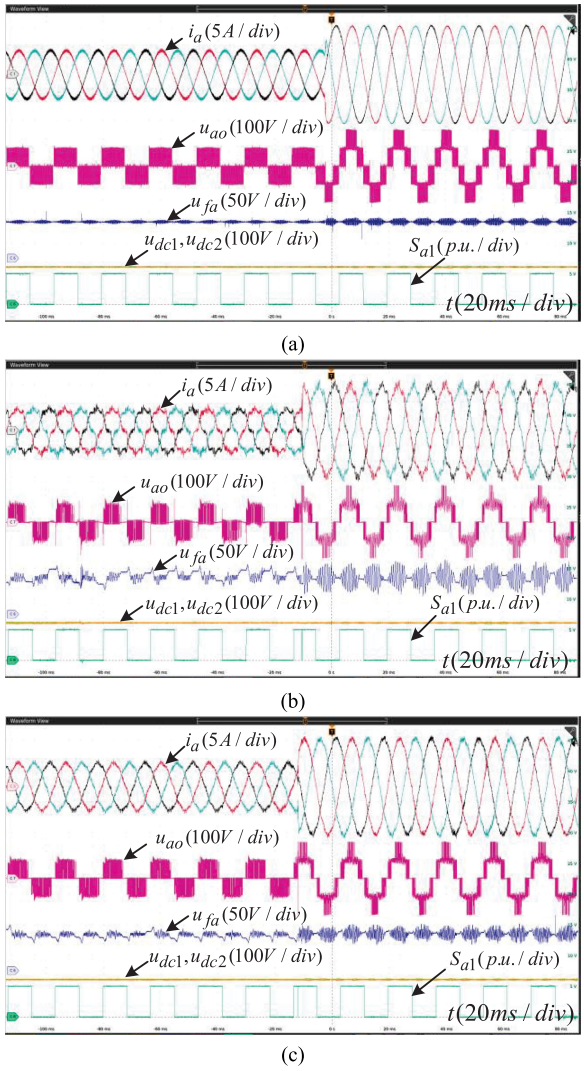

Fig. 16. Experimental results of transient-state performance for (a) proposed MPC at 10 kHz sampling frequency, (b) classical MPC at 10 kHz sampling frequency, and (c) classical MPC at 20 kHz sampling frequency. From top to bottom, waveforms are load currents, phase "a" voltage, FC voltages, dc-link capacitor voltages, and switching signal of S_{a1}.

at a low sampling frequency with the output waveform quality guaranteed.

In order to further validate the steady-state performance improvement by the proposed MPC, the phase "a" current harmonic spectra of the MPC methods are presented in Fig. 15. The load current THD of classical MPC is 7.13%, which is much higher than that of the proposed MPC, which is 1.1%, proving the dramatic performance improvement in output current quality. The load current THD of the proposed MPC is even better than that of classical MPC operating at 20 kHz whose load current THD is 3.5%. The current harmonics of the proposed hybrid MPC concentrate on the 10 and 20 kHz, whereas those of classical MPC distribute broadly. In the proposed MPC, the switching frequency can be set constant by adopting PS-PWM.

Apart from the steady-state performance comparison, the dynamic performance of the MPC methods is also investigated, where the current reference is set to 4 A, and then stepped changes to 8 A at 0.1 s. It can be seen that the ANPC converter system is stable during large operation point step changes in all cases, and the fundamental operation of the LFC can be guaranteed in the MPC methods. As shown, the transient response of the proposed MPC is very fast and the same as that of the classical MPC, indicating that the advantage of fast dynamic response in classical MPC is intact, whereas the proposed MPC presents much better steady-state performances than by the classical ones in terms of current ripples and FC voltage ripples. The results validate the excellent dynamic performance of the proposed MPC.

VII. Conclusion

In this article, a hybrid MPC strategy, where the classical MPC regulates the LFC while the duty-cycle-optimized MPC regulates the HFC, is proposed to guarantee the fundamental-frequency operation of the LFC and achieve fixed-switching frequency operation of the ANPC converter. The optimal duty cycle of the proposed MPC is calculated by the virtual switching state and applied by the PS-PWM. The steady-state and dynamic-state performance of the proposed method is investigated through full

comparison with the classical MPC. Compared to the classical MPC method, the proposed hybrid MPC method presents the following advantages: it can reduce current harmonic components and THD, obtaining a fixed switching frequency; and it can balance the capacitor voltage balance by adjusting the applied duty cycles, and achieve the fundamental frequency operation of the LFC by the decoupled operation of the 5L-ANPC, hence the tedious weighting factor tuning process is eliminated. Therefore, the proposed hybrid MPC method can be considered as a good candidate for high-performance control of the ANPC converters where decoupled operation of the LFC and HFC is required.

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