Frequency-Division Virtual Impedance Shaping Control Method for Grid-Connected Inverters in a Weak and Distorted Grid

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***Abstract*—Grid-connected current quality is seriously affected by the low-order background harmonics in the gird-inverter dynamic system. The point of common coupling voltage feedforward impedance reshaping method of the grid-connected inverter is generally applied to solve this problem, however about 90° phase lag of the inverter output impedance is brought in, which would deteriorate the adaptability of the inverter to the weak grid. To solve this problem, this article proposes a novel frequency-division virtual impedance shaping method, which shapes the output impedance of the grid-connected inverter with different coefficients in different frequency bands, respectively. The basic principles, parameters design, and application analysis are studied in detail. With the proposed scheme, the grid-connected inverter can be equipped with strong adaptability to a wide range of grid impedance and suppression ability to the background voltage harmonics simultaneously. Theoretical analysis and experimental results confirm the effectiveness of the proposed method.**

***Index Terms*—Grid-connected inverter, harmonics suppression, impedance shaping, virtual impedance, weak grid.**

I. Introduction

As FOSSIL energy dried up gradually, growing attentions and applications are imported into the new energy techniques such as wind and solar power techniques. Grid-connected inverter, as the energy interface between renewable energy and grid in the distributed power generation system (DPGS), therefore attracts interest of the worldwide researchers [1]–[3]. Stability and power quality are main desirable objectives for the control of the grid-connected inverter. However, with the large-scale grid-connection of DPGSs, the control performances of the grid-connected inverter are seriously challenged by the nonideal conditions at the point of common coupling (PCC). On one hand, due to the low power transformers and long distribution wires [4], [5], the public grid exhibits the characteristic of a weak grid in the DPGS, which is featured with non-negligible grid impedance. In the standards for DPGSs with electric power systems, the grid-connected inverter is required to work stably under all operation circumstances when the grid impedance varies from zero to 10% per-unit, which corresponds to the short-circuit ratio (SCR) of 10 [5], [6]. On the other hand, various low-order background harmonics are contained at the PCC voltage as a result of nonlinear load current flowing through the grid impedance [7], [8], which can certainly lead to poor power quality of the grid current [8]. In brief, the grid-connected inverter is supposed to be designed with strong adaptability to the weak grid and excellent suppression ability to the PCC voltage harmonics simultaneously [9].

PCC voltage feedforward methods, mainly including the proportion feedforward and differential feedforwards [10], [11], are typically adopted to suppress the harmonic components of the grid current caused by PCC voltage distortion. The power quality of the grid-connected inverter can be greatly improved by the above feedforward methods without the consideration of grid impedance. However, the grid impedance cannot be ignored in the weak grid [12]. When it comes to the weak grid, an additional grid-current positive feedback loop, introduced by the PCC voltage feedforward and grid impedance [13], can easily destabilize the grid-inverter system.

As for the adaptability of the grid-connected inverter to the weak grid, the improved feedforward scheme with a second-order general integrator (SOGI) is a feasible and simple strategy [14]. However, the rejection ability to the low-order harmonics in PCC voltage is much weakened because SOGI feedforward is equivalent to the fundamental feedforward of the PCC voltage and the other low-order voltage harmonics are filtered by SOGI. The adaptive feedforward method is another effective solution [13], [15]–[17]. The real-time phase margin compensation by the grid impedance online measurement technology [15], and the adaptive adjustment strategies of the control parameters [13], [16] are proposed to enhance the adaptability to the weak grid. However, in the above adaptive methods, harmonic sources, which are brought in intermittently by the grid impedance

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online measurement, would deteriorate the quality of grid current. Xu *et al*. [17] propose another adaptive feedforward algorithm without any grid impedance estimation, thus the harmonic sources introduced by the grid impedance estimation are avoided. Nevertheless, several band pass filters and fast Fourier transform (FFT) algorithms are required in [17], which are complex and would increase the burden of the digital controller. Impedance shaping methods based on virtual impedance are other approaches for the control of the grid-connected inverter in the weak and distorted grid [15], [18]–[20]. The shaping strategy with parallel and series virtual impedances is proposed in [19]. Actually, the parallel virtual impedance shaping is equivalent to the PCC voltage full feedforward strategy [15], [19], and the series virtual impedance shaping is equivalent to counteract the unstable positive feedback loop with a negative one by an additional virtual inductance. With this method, the stability is much improved, but the current-loop gain would be affected, which makes the control parameters design of the whole system more complicated.

To sum up, PCC voltage feedforward method is a promising way for the suppression of PCC background voltage harmonics, but its application in weak grid is seriously constrained by the grid impedance. Considering that the essence of PCC voltage feedforward strategy is the shaping of inverter output impedance, this article analyzes the effect of PCC voltage feedforward method on the stability of grid-inverter system from the perspective of inverter output impedance. On this basis, the frequency-division virtual impedance shaping control method is proposed, which is capable of improving the weak-grid-adaptability of the grid-connected inverter and maintaining sufficient suppression ability to PCC voltage harmonics simultaneously. Moreover, there is almost no interaction between the frequency-division virtual impedance and the current-inner loop from the view of the parameter design, and no complex algorithm is required. The basic principles, parameters design and verifications of the proposed method are discussed concretely.

The rest of this article is organized as follows. In Section II, the output impedance of the single-phase grid-connected inverter with *LCL* filter is briefly derived, and the shaping objectives of the grid-connected inverter are discussed in Section III. Then, Section IV analyzes the stability of the grid-inverter system with the PCC voltage feedforward impedance reshaping method. As a contrast, the frequency-division virtual impedance shaping method is proposed in Section V and its design rules are also provided. In Section VI, the validity of the proposal is verified by the experimental results. At last, Section VII concludes this article.

II. Descriptions and Modeling of the Grid-Connected Inverter

Fig. 1 gives a general structure of a single-phase inverter connected to the weak grid through an *LCL* filter. Where, $V_{\rm in}$ is the dc-link voltage, *LCL* filter is composed of inverter-side inductor L_1, filter capacitor C, and grid-side inductor L_2, $Z_{\rm g}$ is the grid impedance, i_2 is the grid current, $v_{\rm g}$ and $v_{\rm pcc}$ are the grid and PCC voltage, respectively. As for the control system, $K_{\rm c}$

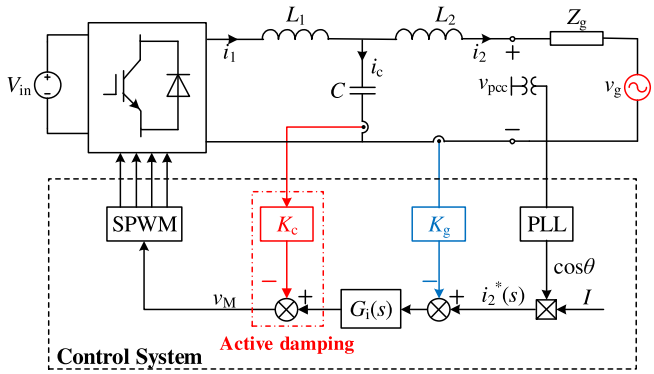


Fig. 1. General configuration of single-phase grid-connected inverter.

and $K_{\rm g}$ are filter-capacitance-current-feedback coefficient and grid-current-feedback coefficient respectively, and $G_{\rm i}(s)$ is the current regulator. In typical applications [3], [21], [22], the filter capacitor current is fed back with the coefficient $K_{\rm c}$ to damp the resonant peak of the *LCL* filter, and the grid current reference $i_2{}^*(s)$ is acquired by multiplying the amplitude reference I with the output angle information of phase locked-loop (PLL).

For the digital control system, digital control delay is an unavoidable problem, which mainly contains the sample-computation delay and the pulsewidth modulation (PWM) delay. Generally, the sample-computation delay is one sampling period T_s in most applications. Many existing methods can compensate or even completely eliminate the sample-computation delay and have acquired good performance [22], [23]. To ensure the universality of the proposed strategy, however, no control delay compensation method is applied in this article, and the sample-computation delay could be modeled as follows:

$$G_s(s) = e^{-sT_s}. \tag{1}$$

Moreover, due to the zero-order hold characteristic, the PWM reference could be kept constant within one sampling period after loading, and the corresponding PWM delay can be modeled as follows:

$$G_h(s) = \frac{1 - e^{-sT_s}}{s} \approx T_s e^{-0.5sT_s}. \tag{2}$$

Meanwhile, the sampler could be modeled as $1/T_s$ within the Nyquist frequency [24]. Thus, the total digital control delay combining the delays and the sampler could be presented as follows:

$$G_d(s) = G_s(s)G_h(s)/T_s \approx e^{-1.5sT_s}. \tag{3}$$

The digital control delay is generally approximated by the second-order Pade function, and the formula is as follows:

$$G_d(s) = e^{-s1.5T_s} \approx \frac{1 - 0.75sT_s + 0.083 \cdot (1.5sT_s)^2}{1 + 0.75sT_s + 0.083 \cdot (1.5sT_s)^2}. \tag{4}$$

With the aforementioned analysis, the linearized model of single-phase grid-connected inverter with digital control in s-domain can be deduced as shown in Fig. 2(a). It should be mentioned that the PLL has considerable influence on the stability of the grid-inverter system, and these effects could be effectively

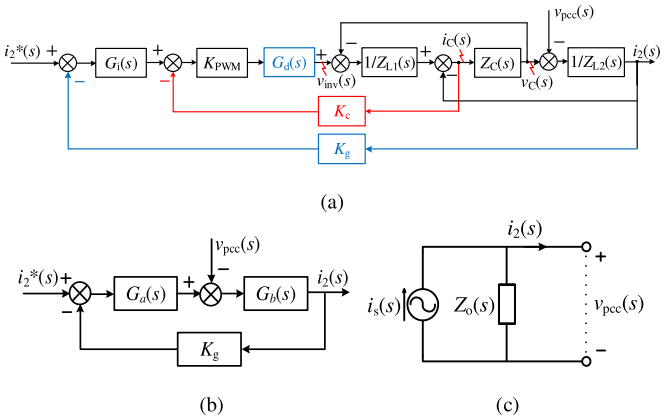


Fig. 2. Control block diagram of grid-connected inverter. (a) s-domain control diagram. (b) Equivalent transformation. (c) Norton equivalent model.

eliminated with the low-bandwidth PLL or other improved PLL [17], [19], [25]. Although the low-bandwidth PLL may reduce the dynamic performance of the system, a properly designed PLL would have almost no effect on the dynamic capabilities. The optimization design of the PLL and the impact on stability are not the topic of this article, which are not expanded in detail.

K_{PWM} in Fig. 2(a) is the gain of PWM inverter [10], which could be expressed as follows:

$$K_{\mathrm{PWM}} = \frac{V_{\mathrm{in}}}{V_{\mathrm{tri}}} \tag{5}$$

where V_{tri} is the amplitude of the triangular carrier. Furthermore, Fig. 2(a) could be transformed into Fig. 2(b) with the equivalent transformation principle of control diagram, where $G_{\mathrm{a}}(s)$ and $G_{\mathrm{b}}(s)$ are presented by

$$G_a(s) = \frac{K_{\mathrm{PWM}}G_d(s)G_i(s)}{s^2L_1C + sCK_cK_{\mathrm{PWM}}G_d(s) + 1} \tag{6}$$

$$G_b(s) = \frac{s^2L_1C + sCK_cK_{\mathrm{PWM}}G_d(s) + 1}{s^3L_1L_2C + s^2L_2CK_cK_{\mathrm{PWM}}G_d(s) + s(L_1 + L_2)}. \tag{7}$$

Here, the proportional integral (PI) current regulator is applied in this study, which could be expressed by

$$G_i(s) = K_p + \frac{K_i}{s} \tag{8}$$

where K_{p} is the proportional coefficient and K_{i} is the integral coefficient.

With Fig. 2(b) and (6) and (7), the current-loop gain could be derived as follows:

$$T_o(s) = G_a(s)G_b(s)K_g. \tag{9}$$

Thus, the grid current i_2 could be shown by

$$i_2(s) = i_s(s) - \frac{v_{\mathrm{pcc}}(s)}{Z_o(s)} \tag{10}$$

where $i_{\mathrm{s}}(s)$ is the tracking component of grid current and $Z_{\mathrm{o}}(s)$ is the output impedance of grid-connected inverter, expressed as follows:

$$i_s(s) = \frac{G_a(s)G_b(s)}{1 + G_a(s)G_b(s)K_g} i_2^*(s) \tag{11}$$

$$Z_o(s) = \frac{1 + G_a(s)G_b(s)K_g}{G_b(s)}. \tag{12}$$

On the basis of (10), Norton equivalent model of the grid-connected inverter could be derived and shown as Fig. 2(c), where the grid-connected inverter is presented by the parallel connection of the current source $i_{\mathrm{s}}(s)$ and the inverter output impedance $Z_{\mathrm{o}}(s)$.

III. Shaping Objectives of the Grid-Connected Inverter in a Weak and Distorted Grid

In a weak and distorted grid, the grid impedance cannot be ignored, and there are abundant low-order voltage harmonics at the PCC [17], [19]. According to Fig. 2(c) and (10), the low-order voltage harmonics in $v_{\mathrm{pcc}}(s)$ would cause serious distortion of the grid current. Moreover, the grid impedance in the weak grid would lead to resonance or instability of the grid-inverter system [12], [13]. The control objectives of the grid-connected inverter in a weak and distorted grid, therefore, are to acquire strong adaptability to grid impedance and sufficient suppression ability to grid current distortion caused by PCC voltage harmonics.

On one hand, in order to weaken or completely eliminate the influence of PCC voltage harmonic on the grid current, according to (10), it is necessary to increase the magnitude of the inverter output impedance as much as possible.

On the other hand, to ensure the stability of the grid-inverter system in a weak grid, the grid-connected inverter must satisfy the impedance-based stability criterion [12].

1) The grid-connected inverter is stable under the ideal power grid [i.e., grid impedance $Z_{\mathrm{g}}(s) = 0$].
2) Impedance ratio $Z_{\mathrm{g}}(s)/Z_{\mathrm{o}}(s)$ satisfies the Nyquist stability criterion.

The first requirement could be easily satisfied with the properly designed control parameters, and the satisfaction of the second criterion requires the phase margin of the grid-inverter system must be greater than zero (i.e., PM>0) when $Z_{\mathrm{g}}(s)/Z_{\mathrm{o}}(s)$ has no right-half-plane poles.

Here phase margin (PM) is expressed as follows:

$$\mathrm{PM} = 180^\circ - [\arg(Z_g(j2\pi f_i)) - \arg(Z_o(j2\pi f_i))] \tag{13}$$

where f_{i} is the intersection frequency of the output impedance $Z_{\mathrm{o}}(s)$ and grid impedance $Z_{\mathrm{g}}(s)$, as shown in Fig. 3. Moreover, to ensure satisfactory damping characteristic and dynamic performance of the grid-inverter system, considerable phase margin should be retained in practical applications [15].

From (13), since the phase of the grid impedance $\arg(Z_{\mathrm{g}}(j2\pi f_{\mathrm{i}}))$ is difficult to control, the most feasible way to improve stability-robustness is to boost the phase of the inverter output impedance.

Therefore, in order to achieve the control objectives of the grid-connected inverter in a weak and distorted grid, the output impedance of the grid-connected inverter need to be shaped with sufficient magnitude and phase.

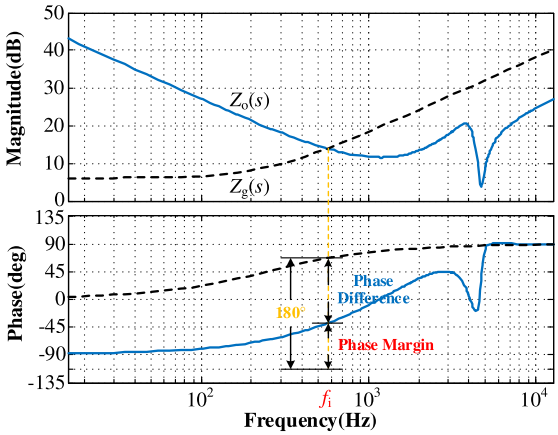


Fig. 3. Phase margin of the grid-inverter system according to impedance-based stability criterion.

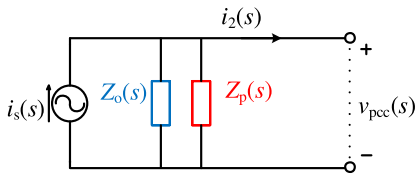


Fig. 4. Norton equivalent model of inverter with the parallel virtual impedance shaping method.

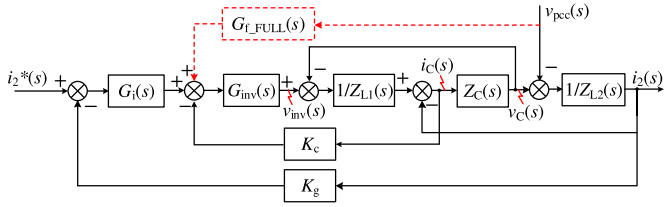


Fig. 5. Implementation control block diagram of the PCC voltage feedforward impedance reshaping method.

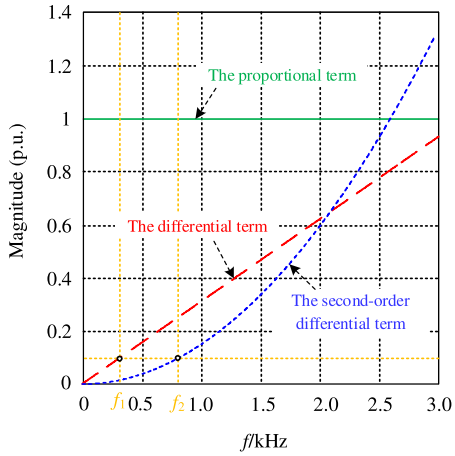


Fig. 6. Per unit values of the magnitude of the three feedforward components.

IV. PCC Voltage Feedforward Impedance Reshaping Method and System Stability Analysis

To significantly increase the magnitude of the inverter output impedance, the PCC voltage feedforward impedance reshaping method is widely applied [10], [11]. It is noticed that PCC voltage feedforward strategy is actually equivalent to the parallel virtual impedance shaping method [19].

Fig. 4 presents the Norton model of the grid-connected inverter with the parallel virtual impedance shaping method, where $Z_p(s)$ is the parallel virtual impedance [19], expressed as follows:

$$Z_p(s) = \frac{-Z_o(s)}{G_d(s)}. \tag{14}$$

From (14), the parallel virtual impedance $Z_p(s)$ is the opposite of the original output impedance $Z_o(s)$ in the low-frequency area, so the total parallel result of $Z_p(s)$ and $Z_o(s)$ can have infinite magnitude in theory. That is why the parallel virtual impedance shaping method could effectively reject the grid current distortion caused by the PCC voltage harmonics.

Typically, the parallel virtual impedance is implemented with PCC voltage full feedforward strategy [10], [11] as shown in Fig. 5, where $G_{f\_FULL}(s)$ is PCC voltage full feedforward function, expressed as (15), and the derivation process is detailed in the Appendix

$$G_{f\_FULL}(s) = \frac{1}{K_{PWM}} + sCK_cG_d(s) + \frac{s^2L_1C}{K_{PWM}}. \tag{15}$$

The expression of full feedforward function mainly contains three parts: proportion, differential, and second-order differential terms. On the basis of the magnitude of the proportional term, the per unit values curves of the magnitude of the differential term and the second-order differential term varying with the harmonic frequency of the PCC voltage are drawn, as shown in Fig. 6. From Fig. 6, we can see that the differential term is an order of magnitude smaller than the proportional term when v_{pcc} contains only 6th harmonic distortion, and that the second-order differential term is also an order of magnitude smaller than the proportional term when v_{pcc} contains harmonic distortion up to the 16th harmonic. This means that the second-order differential term could be omitted if v_{pcc} contains harmonic distortion within the 16th harmonic, and only the proportional term is needed if v_{pcc} contains harmonic distortion within the 6th harmonic. Since the high-order harmonics (more than 16 times) in the power grid are small [10] and it is hard to implement the second-order differential in practical applications because of its large amplification to noise [13], the second-order differential term can be omitted in the analysis.

Then, the expression of full feedforward function could be simplified as follows:

$$G_{f\_FULL}(s) \approx G_{f\_PD\_Gd}(s) = \frac{1}{K_{PWM}} + sCK_cG_d(s). \tag{16}$$

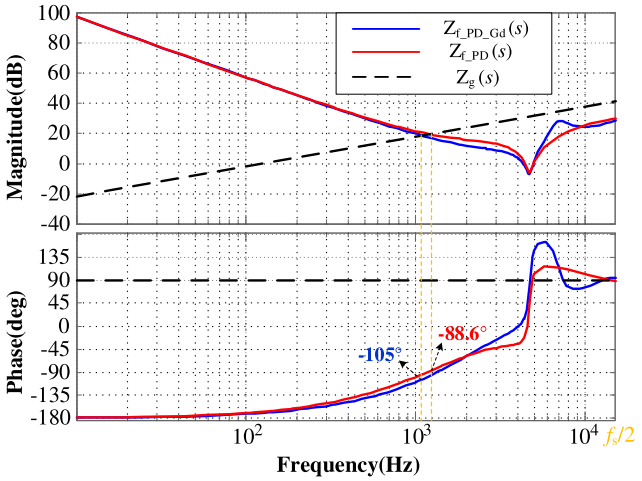


Fig. 7. Bode diagram of the inverter output impedance and grid impedance.

To further simplify the analysis, the expression that ignores the delay $G_{\mathrm{d}}(s)$ in the first-order term is defined as follows:

$$G_{\mathrm{f\_PD}}(s) = \frac{1}{K_{\mathrm{PWM}}} + sCK_c. \tag{17}$$

Furthermore, according to Fig. 5, with the PCC voltage feedforward impedance reshaping, the actual equivalent output impedance when using (16) and (17) as feedforward term respectively could be derived as follows:

$$Z_{\mathrm{f\_PD\_Gd}}(s) = \frac{\begin{bmatrix} s^3L_1L_2C + s^2L_2CK_cK_{\mathrm{PWM}}G_d(s) \\ +s(L_1+L_2) + G_i(s)K_{\mathrm{PWM}}G_d(s)K_g \end{bmatrix}}{s^2L_1C + sCK_cK_{\mathrm{PWM}}G_d(s) + 1 - K_{\mathrm{PWM}}G_d(s)} G_{\mathrm{f\_PD\_Gd}}(s) \tag{18}$$

$$Z_{\mathrm{f\_PD}}(s) = \frac{\begin{bmatrix} s^3L_1L_2C + s^2L_2CK_cK_{\mathrm{PWM}}G_d(s) \\ +s(L_1+L_2) + G_i(s)K_{\mathrm{PWM}}G_d(s)K_g \end{bmatrix}}{s^2L_1C + sCK_cK_{\mathrm{PWM}}G_d(s) + 1 - K_{\mathrm{PWM}}G_d(s)G_{\mathrm{f\_PD}}(s)}. \tag{19}$$

Bode diagrams of the inverter output impedance when using (18) and (19) and grid impedance are shown in Fig. 7 and the key parameters are listed in Table I. Since the resistor in grid impedance tends to increase the PM of the grid-inverter system at the intersection frequency and helps stabilizing the system [19], the pure inductor L_{g} is used for the stability analysis and experimental validation to draw the worst case of resistive-inductive grid impedance [i.e., $Z_{\mathrm{g}}(s) = sL_{\mathrm{g}}$]. As in the case of this article, the control system is examined with L_{g} varying up to 1.28 mH, which corresponds to a typical SCR of 10 and is the worst-case scenario.

As can be seen from Fig. 7, when the grid impedance is 1.28 mH, the phase margins of the systems using (18) and (19) are –15° and 1.4°, respectively. Both of them are easy to

TABLE I
SYSTEM PARAMETERS

Symbol	Parameter	Value
V_{in}	DC voltage	200V
V_{g}	Gird voltage (RMS)	110V
P_{o}	Rated output power	3kW
f_{sw}	Switching frequency	15kHz
f_{s}	Sampling frequency	30kHz
L_1	Inverter-side inductance	0.4mH
C	Filter capacitance	9.2uF
L_2	Grid-side inductance	0.3mH
V_{tri}	Carrier amplitude	1.694V
K_{c}	Filter capacitance current coefficient	0.045
K_{g}	Grid current coefficient	0.15

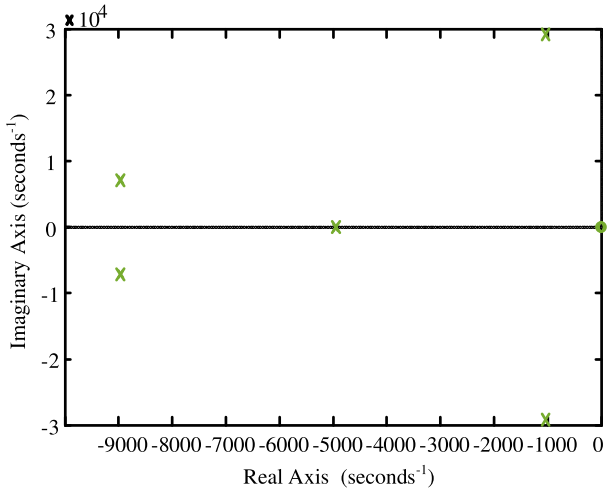


Fig. 8. Zero-pole diagram of $Z_{\mathrm{g}}(s)/Z_{\mathrm{f\_PD}}(s)$.

cause resonance or instability of the system. In high-frequency band, there are some differences in the amplitude-frequency and phase-frequency characteristics between the two systems. But according to the criterion of impedance stability, when the intersection of grid impedance and inverter output impedance is in this frequency band, systems remain stable. Therefore, it can be said that neglecting the digital control delay $G_d(s)$ of the first order differential term in the feedforward function would not cause the misjudgment of the stability of the system. Therefore, in this article, we use (17) as the expression of PCC voltage feedforward.

In this case, the stability of the system depends on whether the impedance ratio $Z_{\mathrm{g}}(s)/Z_{\mathrm{f\_PD}}(s)$ satisfies the Nyquist stability criterion. The zero-pole diagram of $Z_{\mathrm{g}}(s)/Z_{f\_\mathrm{PD}}(s)$ is shown in Fig. 8, which shows that $Z_{\mathrm{g}}(s)/Z_{\mathrm{f\_PD}}(s)$ has no right-half-plane poles. The stability of the system depends on the phase difference between the grid impedance $Z_{\mathrm{g}}(s)$ and the inverter output impedance $Z_{f\_\mathrm{PD}}(s)$.

Bode diagrams of the original output impedance $Z_{\mathrm{o}}(s)$ (blue solid line), equivalent output impedance $Z_{f\_\mathrm{PD}}(s)$ (red dash-dotted line) and grid impedance $Z_g(s)$ (black dotted line) are shown in Fig. 9. As is shown in Fig. 9, compared with the original output impedance $Z_{\mathrm{o}}(s)$, the impedance amplitude of $Z_{f\_\mathrm{PD}}(s)$ in low-frequency area is sharply promoted by the PCC voltage feedforward impedance reshaping method. The increase

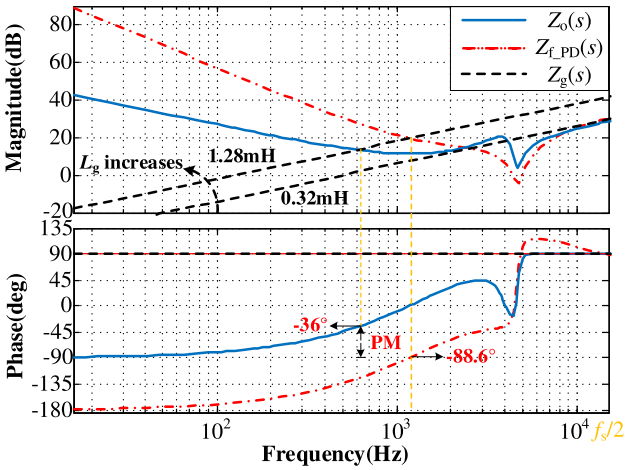


Fig. 9. Bode diagram of the inverter output impedance and grid impedance.

of impedance amplitude can certainly endow the inverter with much stronger suppression ability to PCC voltage harmonics. However, the phase lag of about 90° is brought in meanwhile. When L_g is 1.28 mH, the phase margin of the grid-inverter system is reduced from 54° to 1.4° after the PCC voltage feedforward impedance reshaping, which can easily cause the resonance or instability of the system.

In summary, with the PCC voltage feedforward impedance reshaping method, the inverter output impedance is shaped with adequate magnitude but insufficient phase. Therefore, the PCC voltage feedforward impedance reshaping method enhances the rejection ability to PCC voltage harmonic, but weakens the adaptability to the grid impedance.

V. Frequency-Division Virtual Impedance Shaping Control Method

In this section, the impact of the PCC voltage feedforward impedance reshaping on the inverter output impedance is further analyzed, and then a novel frequency-division virtual impedance shaping control method is proposed to maintain the suppression ability to PCC voltage harmonic and adaptability to grid impedance simultaneously. The associated details are also discussed to ensure the generality of the proposed strategy.

A. Output Impedance Ratio Analysis

According to Figs. 2(a) and 5, the output impedance ratio of grid-connected inverter, before and after the PCC voltage feedforward impedance reshaping, can be deduced as follows:

$$\frac{Z_{\mathrm{f\_PD}}(s)}{Z_o(s)} = \frac{1}{M(s)} = \frac{1}{1-F(s)} \tag{20}$$

where $M(s)$ is the reciprocal of the output impedance ratio, and $F(s)$ is the factor introduced by the PCC voltage feedforward impedance reshaping, expressed as follows:

$$F(s) = \frac{K_{\mathrm{PWM}}G_d(s)}{s^2L_1C + sCK_cK_{\mathrm{PWM}}G_d(s) + 1}G_{\mathrm{f\_PD}}(s) \approx G_d(s). \tag{21}$$

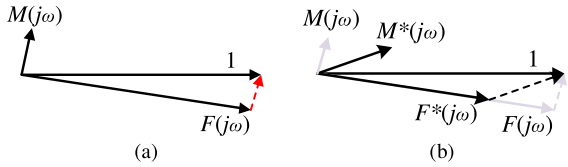


Fig. 10. Vector diagram of (a) $M(j\omega)$ and (b) $M^*(j\omega)$.

For the low-frequency range, the vector diagram of $M(s)$ can be roughly drawn as Fig. 10(a) on the basis of (4) and (20) and (21). From Fig. 10(a), since $F(s)$ is very close to the unit vector, the magnitude of $M(s)$ is pretty small, which could promote the output impedance magnitude according to (20), and thus enhance the suppression ability to PCC voltage harmonics. However, the leading phase angle of $M(s)$ would make the phase of the shaped output impedance lag behind that of the original output impedance.

To decrease the phase lag introduced by the PCC voltage feedforward impedance reshaping and thus improve the stability-robustness, an intuitive idea is to reduce the magnitude of $F(s)$, as shown in Fig. 10(b). From Fig. 10(b), the $F(s)$ with decreased magnitude [i.e., $F^*(s)$] diminishes the leading angle of $M^*(s)$, but makes the amplitude of $M^*(s)$ relatively larger meanwhile.

According to the above analysis, fixed $F(s)$ within the full-frequency range is hard to satisfy both requirements of output impedance magnitude and phase at the same time. Therefore, in order to ensure sufficient amplitude and phase of the output impedance simultaneously, the magnitude of $F(s)$ could be appropriately reduced in some frequency ranges, while remain unchanged in other frequency areas. That is the basic idea of frequency-division virtual impedance shaping method proposed in this article.

B. Characteristic Analysis and Simplification of the Inverter Output Impedance

From (21), it can be seen that the feedforward function $G_{f\_\mathrm{PD}}(s)$ is the only controllable part of $F(s)$, so the shaping strategy for $F(s)$ is actually the reconstruction of feedforward function $G_{f\_\mathrm{PD}}(s)$. Meanwhile, according to Figs. 4 and 5, the introduction of PCC voltage feedforward strategy is equivalent to introducing a traditional parallel virtual impedance. Therefore, the variable gain shaping strategy for $F(s)$ is in fact equivalent to introducing a novel parallel virtual impedance with the adjustable magnitude at different frequency bands.

Since the magnitude of the new parallel virtual impedance need to be regulated separately in different frequency bands, it is necessary to analyze the characteristic of output impedance in different frequency bands, and establish the simplified impedance model based on frequency-bands before shaping the inverter output impedance.

The expression of the inverter output impedance without any virtual impedance shaping [i.e., (12)] can be equivalently

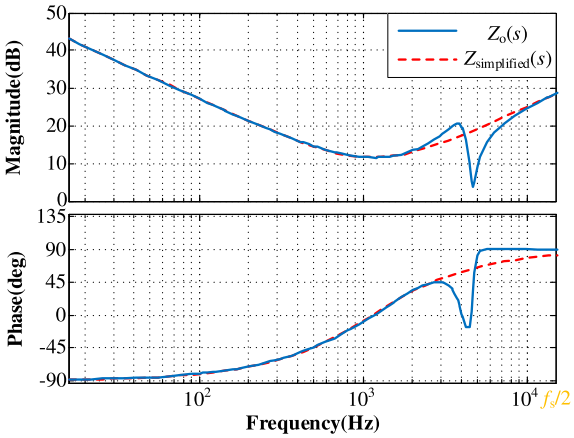


Fig. 11. Frequency characteristic of the original and simplified output impedance.

concerted as follows:

$$Z_o(s) = \left\{ \begin{array}{l} \dfrac{G_i(s)K_{\rm PWM}G_d(s)K_g}{s^2L_1C + sCK_cK_{\rm PWM}G_d(s) + 1} \\ \quad + \dfrac{sL_1}{s^2L_1C + sCK_cK_{\rm PWM}G_d(s) + 1} + sL_2 \end{array} \right\}. \tag{22}$$

In the low-frequency segment, the filter inductor L_1 and L_2 are close to short circuit, so the output impedance $Z_{\rm o}(s)$ can be simplified as follows:

$$Z_{\rm o\_LF}(s) \approx \frac{G_i(s)G_d(s)K_{\rm PWM}K_g}{s^2L_1C + sCK_cG_d(s)K_{\rm PWM} + 1}. \tag{23}$$

From (23), the frequency characteristic of the output impedance in the low frequency segment is mainly determined by the PI current regulator (capacitive in the low-frequency segment), so the output impedance mainly behaves capacitive in the low-frequency segment [26].

For the high-frequency range, the output impedance mainly becomes inductive due to the grid-side inductor L_2 [19], so the output impedance $Z_{\rm o}(s)$ can be simplified by

$$Z_{\rm o\_HF}(s) \approx sL_2. \tag{24}$$

Besides, for a deterministic linear system, there must be resistive–capacitive and resistive–inductive area as the connection from the capacitive region to the inductive region. Hence, the inverter output impedance is roughly similar to the resistor–capacitor–inductor network. It is mentioned that in order to better describe the frequency characteristic of the output impedance, the low-frequency or high-frequency region is used in this article, but it is just a qualitative expression for low-frequency area (e.g., 0 Hz) or high-frequency area (e.g., Nyquist frequency). Naturally, it is hard to get the precise mathematical definition of the low-frequency (or high frequency) area owing to the frequency differences in various systems.

Fig. 11 shows the frequency characteristic of the original output impedance $Z_{\rm o}(s)$ (blue solid line). According to Fig. 11, the output impedance is indeed capacitive in the low-frequency segment, inductive in the high-frequency band, and resistive–capacitive (or resistive–inductive) in the middle connection region. Based on frequency characteristic of the output impedance, therefore, the original output impedance $Z_{\rm o}(s)$ can be approximately equivalent to an *RLC* model $Z_{\rm simplified}(s)$, and it is presented as follows:

$$Z_o(s) \approx Z_{\rm simplified}(s) = \frac{1}{sC_0} + R_0 + sL_0 \tag{25}$$

where C_0, R_0, and L_0 are the equivalent capacitor, resistor, and inductor, respectively.

Correspondingly, the parameters of the *RLC* model can be calculated by the following steps.

1) Plotting the frequency characteristic diagram of the inverter output impedance without any parallel virtual impedance shaping.
2) Choosing any definitive frequency f_0 which is best to approach 0 Hz in the low-frequency area, and reading the relevant magnitude A_0, then the equivalent capacitor C_0 can be obtained by
$$C_0 = \frac{1}{2\pi f_0 10^{A_0/20}}. \tag{26}$$
3) Reading the frequency f_1 where the phase crosses through 0 degree and the corresponding amplitude A_1, then the equivalent resistor R_0 is calculated as follows:
$$R_0 = 10^{A_1/20}. \tag{27}$$
4) Choosing any definitive frequency f_2 which is best to approach the Nyquist frequency in the high-frequency part, and obtaining the homologous magnitude A_2, the equivalent inductor L_0 can be acquired by
$$L_0 = \frac{10^{A_2/20}}{2\pi f_2}. \tag{28}$$

By means of the system parameters listed in Table I, Fig. 11 and (26)–(28), the equivalent capacitor C_0, resistor R_0, and inductor L_0 can be achieved as $C_0 = 70.27$ μF, $R_0 = 3.8$ Ω, and $L_0 = 0.28$ mH. The Bode diagram of the simplified output impedance $Z_{\rm simplified}(s)$ is also presented in Fig. 11. It can be seen that the simplified model has great fitting with the original one in the most frequency area, but there are considerable mismatches in the high-frequency area. However, the simplified output impedance $Z_{\rm simplified}(s)$ is only used to obtain the new parallel virtual impedance and its corresponding PCC voltage feedforward function in the proposed method. In addition, the inverter output impedance used for stability analysis is the real output impedance after adopting the control method mentioned in this article, and there is no approximation. Therefore, mismatches in Fig. 11 would not cause the misjudging of the system stability.

C. Basic Principle of the Frequency-Division Virtual Impedance

Based on the simplified output impedance $Z_{\rm simplified}(s)$, a novel parallel virtual impedance $Z_{\rm c}(s)$ with the adjustable magnitude in different frequency bands, named the frequency-division

virtual impedance, is proposed as follows:

$$Z_c(s) = \frac{-\left(\frac{K_1}{sC_0} + K_2R_0 + sK_3L_0\right)}{G_d(s)}. \tag{29}$$

Here K_1, K_2, and K_3 are the coefficients in different frequency bands, respectively. Under special circumstances, when $K_1 = K_2 = K_3 = 1$, the frequency-division virtual impedance is in fact the traditional parallel virtual impedance. Therefore, it can also be said that the proposed frequency-division virtual impedance is the extension of the PCC voltage feedforward virtual impedance.

Similar to the PCC voltage feedforward impedance reshaping method, the proposed frequency-division virtual impedance $Z_c(s)$ is also parallel to the original output impedance. So the frequency-division virtual impedance can also be realized with the implementation block diagram of the parallel virtual impedance (i.e., Fig. 4), and the corresponding PCC voltage frequency-division feedforward function $G_{\mathrm{f\_FD}}(s)$ can be expressed as follows:

$$G_{\mathrm{f\_FD}}(s) = \frac{Z_{\mathrm{simplified}}(s)}{Z_c(s)}\frac{G_i(s)}{G_a(s)} \approx \lambda(s)G_{\mathrm{f\_PD}}(s) \tag{30}$$

where $\lambda(s)$ is the variable gain factor, expressed by

$$\lambda(s) = \frac{1 + sR_0C_0 + s^2L_0C_0}{K_1 + sK_2R_0C_0 + s^2K_3L_0C_0}. \tag{31}$$

The factor $\lambda(s)$ can be easily realized in practical applications, which means that the implementation of the proposed virtual impedance is as simple as that of parallel virtual impedance in the various applications.

Accordingly, with the frequency-division virtual impedance shaping, the equivalent inverter output impedance $Z_{\mathrm{f\_FD}}(s)$ is given by

$$Z_{\mathrm{f\_FD}}(s) = \frac{\begin{bmatrix} s^3L_1L_2C + s^2L_2CK_cK_{\mathrm{PWM}}G_d(s) \\ +s(L_1+L_2) + G_i(s)K_{\mathrm{PWM}}G_d(s)K_g \end{bmatrix}}{s^2L_1C + sCK_cK_{\mathrm{PWM}}G_d(s) + 1 - K_{\mathrm{PWM}}G_d(s)G_{\mathrm{f\_FD}}(s)}. \tag{32}$$

To intuitively illustrate the principle of the frequency-division virtual impedance shaping method, the output impedance ratio of the inverter with the proposed impedance shaping can be derived and analyzed by using the similar method. Based on (20), (21), and (30), the factor introduced by frequency-division virtual impedance shaping can be rewritten as follows:

$$F^*(s) = \frac{G_{\mathrm{inv}}(s)}{s^2L_1C + sCK_cG_{\mathrm{inv}}(s) + 1}G_{\mathrm{f\_FD}}(s) \approx \lambda(s)G_d(s). \tag{33}$$

There is an extra factor $\lambda(s)$ more than $F(s)$. The magnitude characteristic of $\lambda(s)$ is mainly determined by the coefficient K_1, K_2, and K_3 in different frequency bands, respectively. Therefore, with the reasonable design of K_1, K_2, and K_3, $\lambda(s)$ can appropriately reduce the amplitude of $F^*(s)$ in some frequency regions, but keep the amplitude almost unchanged in the other frequency areas, thus achieving the shaping target of this article. That is the basic principle of the frequency-division virtual impedance shaping method.

D. Parameters Design of the Frequency-Division Virtual Impedance

The control objectives of grid-connected inverter in the weak and distorted grid mainly include two aspects: stability and suppression ability to PCC voltage harmonics, so the parameters design of the frequency-division virtual impedance is also carried out in these two aspects.

In the low-frequency segment, sufficient magnitude of the inverter output impedance is required to reject the grid current distortion caused by the low-order PCC voltage harmonics; for the high-frequency region, there is almost no stability problem between the inductive or resistive–inductive inverter and resistive–inductive weak grid. So consistent with the PCC voltage feedforward impedance reshaping method, the low-frequency coefficient K_1, and high-frequency coefficient K_3 are set to 1, which can ensure sufficient magnitude of the output impedance. Finally, the key of parameters design is the reasonable design of the middle-frequency coefficient K_2.

1) Stability requirement: based on the impedance-based stability criterion, to keep the grid-inverter system stable, the phase of the output impedance $Z_{\mathrm{f\_FD}}(s)$ at the intersection frequency of the output impedance $Z_{\mathrm{f\_FD}}(s)$ and grid impedance $Z_{\mathrm{g}}(s)$ must be greater than minus 90° [12]. Moreover, considerable phase margin is supposed to be retained in practical application. That is

$$|Z_{\mathrm{f\_FD}}(j2\pi f_3)| = |Z_g(j2\pi f_3)| \tag{34}$$

$$\angle Z_{\mathrm{f\_FD}}(j2\pi f_3) > -(90-\theta)^\circ \tag{35}$$

where f_3 is the intersection frequency of the output impedance $Z_{\mathrm{f\_FD}}(s)$ and grid impedance $Z_{\mathrm{g}}(s)$, and θ is the phase margin allowance. According to (31) and (33), the higher K_2 would cause the lower magnitude of $F^*(s)$, which is certainly beneficial for the system stability. In other words, the lower limit value of K_2 that satisfies the stability requirement of the grid-inverter system can be calculated by (34) and (35).

2) Harmonic suppression ability requirement: The excessive K_2 would make the amplitude of the output impedance overly small, which weakens the suppression ability to PCC voltage harmonics. Therefore, the upper limit value of K_2 needs to be limited by the amplitude of output impedance.

For the practical grid-inverter systems, the output current of the inverter must comply with the current harmonic restriction even in a weak and seriously distorted grid. Concretely, every-order current harmonics are supposed to be lower than the corresponding distortion limits even with the highest voltage harmonics component permitted by the grid-connection standards. So the minimum magnitude of output impedance at each harmonic frequency that meets the harmonic suppression ability requirement can be defined as follows [27]:

$$|Z(j2\pi f_n)| = \frac{V_gV_n}{I_gI_n} \tag{36}$$

where V_g is the root mean square (rms) of the grid voltage, I_g is the rms of the grid current, I_n and V_n are the distortion restriction ratios of the grid current and grid voltage, respectively, and $|Z(j2\pi f_n)|$ is the desirable minimum impedance amplitude at the frequency f_n. According to the minimum magnitude curve of the output impedance defined by (36), it is easy to determine the desirable upper limit value of K_2 with the graphic method.

E. Design Example and Discussions

A 3 kW single-phase grid-connected inverter is presented here as the example and the key parameters are listed in Table I. The comprehensive design of the grid-connected inverter with the proposed frequency-division virtual impedance shaping method can be given as follows.

Step 1: *Control parameters design under the ideal grid*: First of all, according to the impedance-based stability criterion in Section III, the grid-connected inverter must be stable under the ideal grid, which is the objective of the control parameters (i.e., K_p, K_i, and K_c) design. In this article, using the design rule proposed in [28], the control parameters are given as $K_p = 0.3$, $K_i = 800$, and $K_c = 0.045$. With these control parameters, the phase margin of the system is about 40° with a cutoff frequency of 1.3 kHz, and the loop gain at the fundamental frequency f_o is 46 dB. These frequency-domain indicators ensure satisfactory stability, dynamic performance, and tracking error.

Step 2: *Simplification of the inverter output impedance without any virtual impedance shaping*: With the properly designed control parameters, the Bode diagram of the inverter output impedance without any virtual impedance shaping can be acquired as Fig. 11. Then, by means of (26)–(28), the parameters of the simplified output impedance can be calculated as $C_0 = 70.27\ \mu$F, $R_0 = 3.8\ \Omega$, $L_0 = 0.28$ mH, as shown in Section V-B.

Step 3: *Parameters design of the frequency-division virtual impedance*: In accordance with the design principle presented in Section V-D, the low-frequency coefficient K_1 and the high-frequency coefficient K_3 can be set to 1. Then the qualified range of the middle-frequency coefficient K_2 can be calculated by

1) Bring $L_g = 1.28$ mH into $Z_g(s) = sL_g$.
2) Bring (32) and $Z_g(s) = sL_g$ into (34), then the expression for f3 in terms of K2 is obtained.
3) Substituting $\theta = 35°$, the expression of f3 in terms of K2 and (32) into (35), then the desirable lower limit value $K_{2\_min} = 1.3$ can be obtained when (35) gets the equal sign.
4) With $V_g = 110$ V, $I_g = 21.2$ A, I_n required in IEEE Std. 929-2000 [29] and V_n required by EN 50160 [30], the desirable minimum impedance amplitude curve is plotted and shown as Fig. 12. The six solid lines (six different colors) are the magnitude curves of the output impedance, while K_2 increases from 1.1 to 1.7, and the red dotted line $Z(j2\pi f_n)$ is the desirable minimum amplitude defined by (35). Here the upper limit value K_{2_max} that meets the amplitude requirement is 1.5 after the graphic analysis. Based on the above calculation, the effective range of K_2 is [1.3, 1.5]. To maintain the adaptability to grid impedance and enough suppression ability to PCC voltage harmonics simultaneously, K_2 is set to an intermediate value 1.4 here.

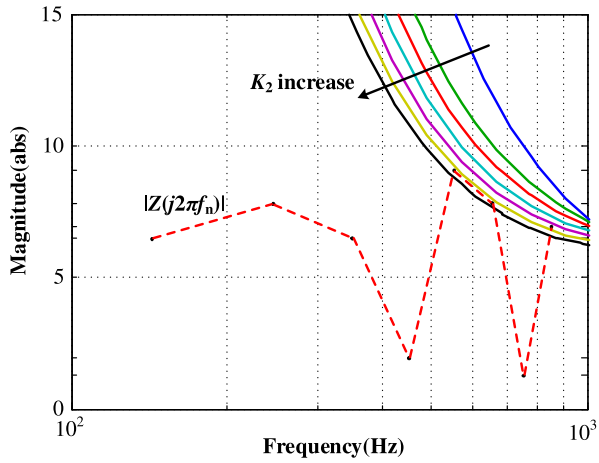


Fig. 12. Desirable minimum output impedance magnitude curve of the grid-connected inverter.

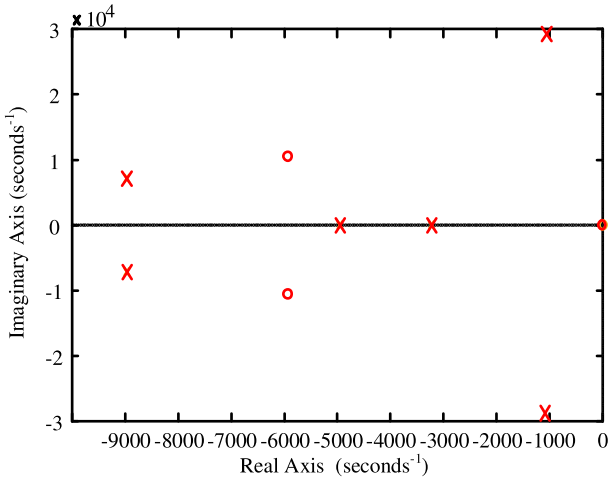


Fig. 13. Zero-pole diagram of $Z_g(s)/Z_{f\_PD}(s)$.

With the designed frequency-division virtual impedance in the above, the zero-pole diagram of $Z_g(s)/Z_{f\_FD}(s)$ is shown in Fig. 13, and the bode diagram of the equivalent output impedance $Z_{f\_FD}(s)$ is presented in Fig. 14. It can be seen that $Z_g(s)/Z_{f\_FD}(s)$ has no right-half-plane poles and the inverter output impedance with the proposed frequency-division virtual impedance shaping scheme has better phase-frequency characteristic in the middle-connection frequency area, compared with that of the PCC voltage feedforward impedance reshaping method. With the proposed scheme, the phase margin of the grid-inverter system can increase from 1.4° to 47.8° when L_g is 1.28 mH. Meanwhile, the inverter output impedance with the proposed scheme has considerable magnitude, which ensures

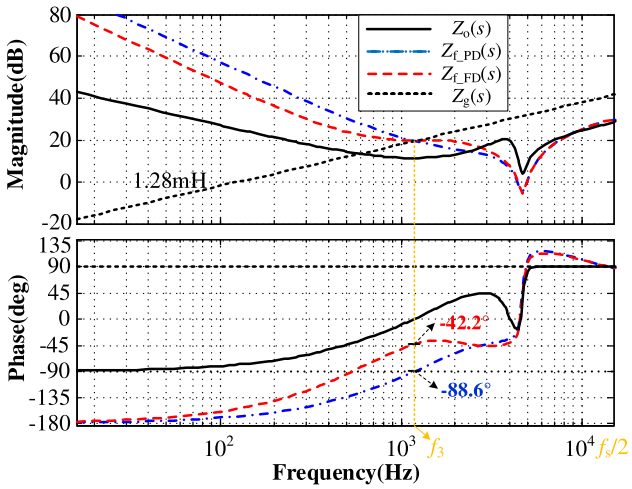


Fig. 14. Frequency characteristic of the grid impedance and inverter output impedance with the frequency-division impedance shaping method.

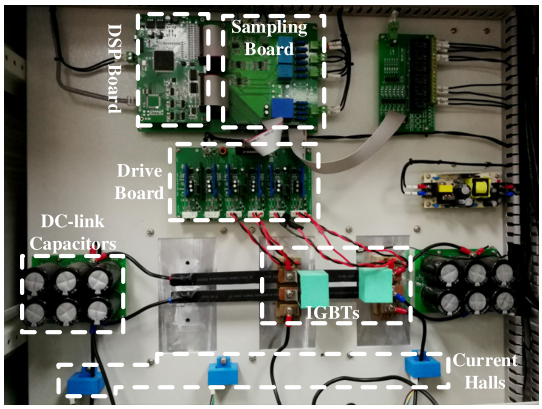


Fig. 15. Photo of the experimental prototype.

sufficient suppression ability to the low-order PCC voltage harmonics. That is, the shaping objectives of the grid-connected inverter in a weak and distorted grid are achieved.

Moreover, according to the aforementioned design process, the frequency-division virtual impedance has almost no impact on the design of the current-control loop, which means that the current-control loop can be designed independently, and thus makes the control parameters optimization of the whole system very simple.

VI. Experimental Verification

A. Experimental Setup

To verify the effectiveness of the proposed method, a prototype of 3 kW single-phase grid-connected inverter with an *LCL* filter is built in the lab for the experimental tests. The photo of the prototype is presented as Fig. 15 and the key parameters are given in Table I.

The experimental inverter is implemented by two insulated gate bipolar transistor modules 2MBI75VA, which are driven by TX-DA962. The PCC voltage used in the PLL is sensed by a voltage hall (LV25-P), the inverter-side current and grid current are sensed by the current halls (LA55-P). All control algorithms, including the dual-loop current control and PCC voltage feedforwards, are implemented by a high-speed digital signal processor (DSP) (TMS320F28335).

To get more precise verification of the proposed method, a bidirectional programmable ac voltage source (Ametek-MX45)

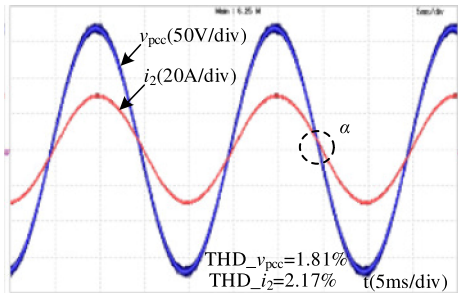
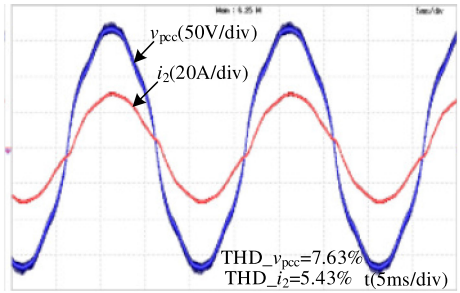
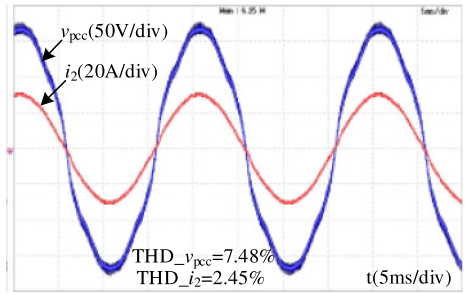


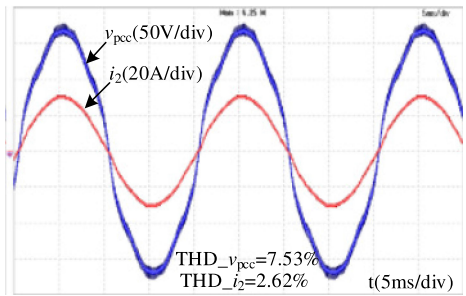
Fig. 16. Steady-state waveforms under the ideal grid condition.



(a)

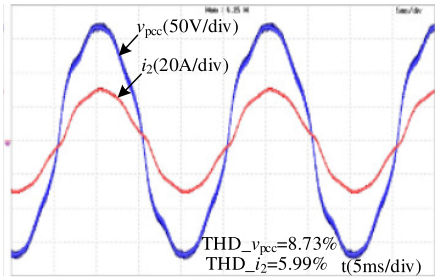


(b)

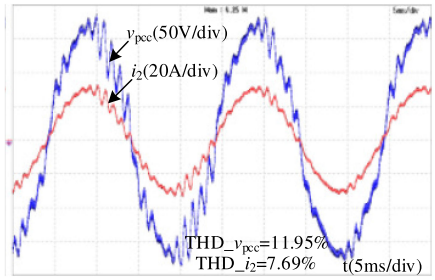


(c)

Fig. 17. Steady-state waveforms with (a) Strategy 1, (b) Strategy 2, and (c) Strategy 3 under the seriously distorted grid.



(a)



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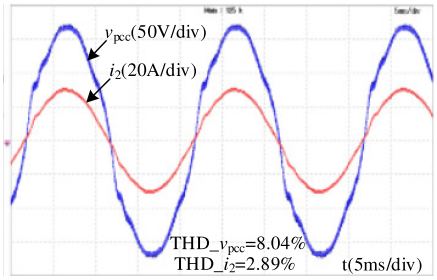
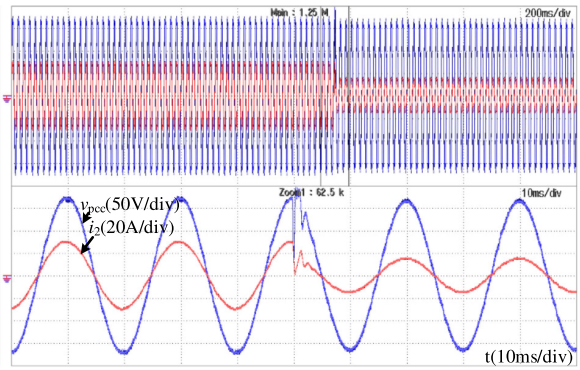
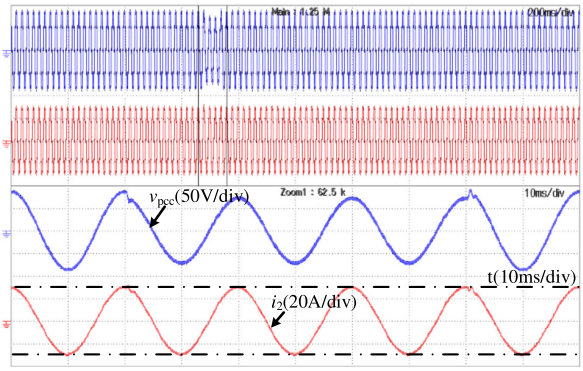


(c)

Fig. 18. Steady-state waveforms with (a) Strategy 1, (b) Strategy 2, and (c) Strategy 3 under the weak (L_g = 1.28 mH) and seriously distorted grid.



(a)



(b)

Fig. 19. Transient waveforms with Strategy 3 in the weak grid (L_g = 1.28 mH). (a) Step change of grid current. (b) Step change of grid voltage.

is applied to simulate the practical grid. In order to conservatively confirm the suppression ability to grid current distortion caused by PCC voltage harmonics, 5% 3rd–5th, 3% 7th, and 0.5% 9th–17th voltage harmonics are added into the ideal grid voltage. The total PCC voltage harmonic distortion is 7.8%, which is approximately the maximum voltage distortion limit of 8% in IEEE Std 519-2014 [31]. Moreover, an extern inductor is used to emulate the grid impedance.

B. Experimental Results

The steady-state waveforms of PCC voltage and grid current are presented in Fig. 16, while the grid impedance and PCC voltage harmonics are ignored. The PCC voltage and grid current are hardly distorted and the corresponding total harmonic distortion (THD) are 1.81% and 2.17%, respectively, which indicates the proper designs of *LCL* filter and control parameters. However, the grid current lags behind the PCC voltage with a certain angle $\alpha = 5.1°$, which is mainly caused by the fundamental component of PCC voltage.

The steady-state waveforms of PCC voltage and grid current are presented in Fig. 17 under the seriously distorted grid and no grid impedance. Here no virtual impedance shaping method (i.e., the typical dual-loop current control), the PCC voltage feedforward impedance reshaping method, and the proposed frequency-division impedance shaping strategy are denoted as Strategy 1, Strategy 2, and Strategy 3, respectively. With Strategy 1, due to the poor suppression ability to grid current distortion, the power quality of grid current is significantly reduced by PCC voltage harmonics and the total-harmonic distortion (THD) value of grid current is 5.43%, as shown in Fig. 17(a). Additionally, the phase lag of grid current still exists. As for Strategy 2 and Strategy 3, the grid currents are seldom distorted as a result of the greatly increased amplitude of the output impedance introduced by the virtual impedance shaping. The measured THD values of grid current in Fig. 17(b) and (c) are 2.45% and 2.62%, respectively, and there is no phase lag of grid currents. It is proved that with Strategy 3, the sufficient rejection ability to grid current distortion caused by PCC voltage harmonics could be acquired with the reasonable design of the frequency-division virtual impedance.

Fig. 18 presents the experimental waveforms with three control strategies in the weak and seriously distorted grid. As shown in Fig. 18(a), the stability of the inverter with Strategy 1 is seldom affected by the grid impedance. However, the grid impedance causes the further decline of grid current quality and the measured THD value of grid current is up to 5.99%. With Strategy 2 in the weak grid, the phase margin is greatly

decreased so that both PCC voltage and grid current resonate violently and the corresponding THD values reaches 11.95% and 7.69%. On the contrast, with the proposed Strategy 3, the system stability in the weak grid has been acquired and the grid current harmonics are well suppressed meanwhile. The measured THD value of the grid current is 2.89% and surely satisfactory. In summary, the steady-state experimental results are consistent with the theoretical analysis.

Furthermore, to show the generality of the proposed method, the transient experimental waveforms with the proposed Strategy 3 in the weak grid are provided in Fig. 19. Fig. 19(a) corresponds to the step change of the current reference *I* and the change action is intentionally set at the peak of the grid current i_2, which is the worst case. The results demonstrate that the grid current i_2 is still synchronous with the PCC voltage $v_{\rm pcc}$, with small oscillation after the step change of current reference *I*. In addition, the transient waveforms with the step change of the grid voltage are shown as Fig. 19(b), where the grid voltage is stepped down from 110 to 90 V, and vice versa. The change action is purposely set at the peak of the grid voltage to emulate the worst case. Results show that the magnitude of the grid current i_2 remains unchanged, only with small oscillation following the step change of the grid voltage. To sum up, the transient experimental results demonstrate that the proposed method has good dynamic performance.

VII. Conclusion

As for the problem that the PCC voltage feedforward impedance reshaping method may cause the instability of the grid-inverter system in the weak and distorted gird, this article proposes a novel frequency-division virtual impedance shaping method to maintain the adaptability to grid impedance and the suppression ability to PCC voltage harmonics simultaneously. The major outcomes of the presented study include the following.

1) The PCC voltage feedforward impedance reshaping method enhances the suppression ability to the grid current distortion caused by the PCC voltage harmonics, however, deteriorates the adaptability of the inverter to grid impedance meanwhile.
2) In the proposed control method, a novel frequency-division virtual impedance is employed to improve the phase-frequency characteristic of the inverter output impedance, and maintain considerable impedance magnitude as well.
3) The theoretical analysis and experimental results prove that the proposed method has good performances including: high suppression ability to PCC voltage harmonics, excellent adaptability to a wide range of grid impedance, allowing the current-control loop to be designed independently, and broad application scope.

Appendix

The detailed derivation process of $G_{\rm f\_FULL}(s)$ is as follows.

The simplified control block diagram of the system without PCC voltage feedforward is shown in Fig. 20.

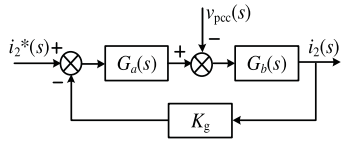


Fig. 20. Simplified control block diagram of grid-connected inverter.

Where $G_{\rm a}(s)$ and $G_{\rm b}(s)$ are presented by

$$G_a(s) = \frac{K_{\rm PWM}G_d(s)G_i(s)}{s^2L_1C + sCK_cK_{\rm PWM}G_d(s) + 1} \tag{a1}$$

$$G_b(s) = \frac{s^2L_1C + sCK_cK_{\rm PWM}G_d(s) + 1}{s^3L_1L_2C + s^2L_2CK_cK_{\rm PWM}G_d(s) + s(L_1 + L_2)}. \tag{a2}$$

With Fig. 20 and (a1) and (a2), the current-loop gain could be derived as follows:

$$T_o(s) = G_a(s)G_b(s)K_g. \tag{a3}$$

Thus, the grid current i_2 could be shown by

$$i_2(s) = i_s(s) - \frac{v_{\rm pcc}(s)}{Z_o(s)} \tag{a4}$$

where $i_{\rm s}$(s) is the tracking component of grid current and $Z_{\rm o}$(s) is the output impedance of grid-connected inverter, expressed as follows:

$$i_s(s) = \frac{G_a(s)G_b(s)}{1 + G_a(s)G_b(s)K_g}i_2^*(s) \tag{a5}$$

$$Z_o(s) = \frac{1 + G_a(s)G_b(s)K_g}{G_b(s)}. \tag{a6}$$

It can be seen from (a4) that the grid-connected current mainly consists of two parts: the instruction tracking component of reference current and the disturbance component introduced by PCC voltage. To ensure that the grid-connected current accurately tracks the instruction value of reference current, the error caused by the disturbance component should be minimized. If a negative $Z_{\rm o}(s)$ is parallel to the output of the system, the influence of disturbance component can be completely eliminated. The specific implementation is to introduce a transfer function $G_{\rm b}(s)$ between PCC voltage and grid current i_2 in Fig. 20. The block diagram is shown in Fig. 21(a).

If the feedforward point of $v_{\rm pcc}$ is moved from the output of $G_{\rm b}$(s) to the input of $G_{\rm a}$(s), Fig. 21(b) can be obtained, and the feedforward function becomes $1/G_{\rm a}$(s). Moreover, expand the simplified control block diagram and move the $v_{\rm pcc}$ feedforward point to the output of $G_{\rm i}$ (s). Then, the realization block diagram of full feedforward of PCC voltage is obtained in Fig. 21(c).

From Fig. 21, the expression of the full feedforward function $G_{\rm f\_FULL\_Gd}$(s) of PCC voltage can be deduced as follows:

$$G_{\rm f\_FULL\_Gd}(s) = \frac{G_i(s)}{G_a(s)} = \frac{s^2L_1C + sCK_{\rm PWM}K_cG_d(s) + 1}{K_{\rm PWM}} \cdot \frac{1}{G_d(s)}. \tag{a7}$$

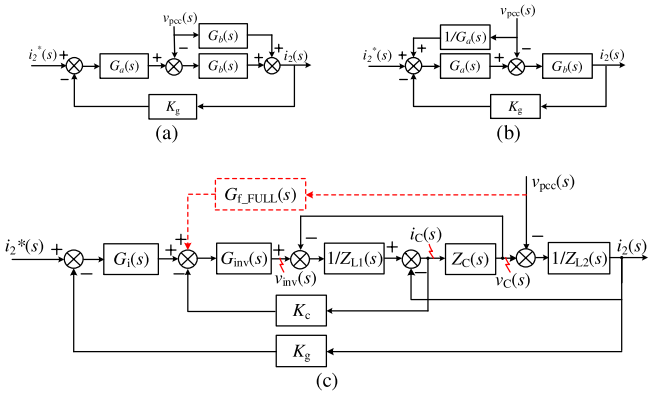


Fig. 21. Equivalent transformation block diagram of PCC voltage full feed forward method. (a) Equivalent transformation 1. (b) Equivalent transformation 2. (c) s-domain control diagram.

It can be seen that the implementation function contains a prediction component, given by

$$\frac{1}{G_d(s)} \approx e^{1.5sT_s}. \tag{a8}$$

Featuring the unity gain with a pure phase-leading, the prediction component cannot be realized physically. Therefore, the implementation function can only be closely approximated as follows:

$$G_{\mathrm{f\_FULL}}(s) = \frac{1}{K_{\mathrm{PWM}}} + sCK_cG_d(s) + \frac{s^2L_1C}{K_{\mathrm{PWM}}}. \tag{a9}$$

The above derivation of the PCC voltage full feed forward formula is indicated in Section III of this article.

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