Fast SPICE-Compatible Simulation of Low-Power On-Chip PWM DC–DC Converters With Improved Ripple Accuracy

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***Abstract*—The circuit averaging technique has long been used as the basis for modeling the behavioral effects of switched-mode pulsewidth-modulated (PWM) dc–dc power converter circuits due to its simplicity and efficiency in simulation. However, circuit-averaged models struggle to capture the effects of higher order harmonics on the output waveforms. Alternatively, multiharmonic models that capture high-frequency characteristics of output waveforms are typically very complex and computationally expensive. A general, efficient, and accurate multiharmonic modeling and simulation technique for low-power on-chip PWM dc–dc converters is presented in this article. The technique is based on the large-signal averaged model of the PWM switch cell and on the Fourier series expansion of the typical converter waveforms. Its applicability range includes current-mode-controlled dc–dc converters. The method is exemplified on a buck and on a boost converter and achieves a speedup of one order of magnitude with an accuracy loss below 3% over the transistor-level simulation. The method accounts for nonideal circuitry and supports any number of harmonics.**

***Index Terms*—Current-mode control (CMC), deep-submicrometer CMOS, Fourier series, large-signal averaged model, low-power on-chip dc–dc converter, multiharmonic modeling.**

I. Introduction

THE simulation of dc–dc converters is generally very time-consuming due to the coexistence of fast switching activities and slow load variations. Circuit averaging techniques average the switching behavior and focus on the cycle-to-cycle dynamics. The drawback of circuit-averaging techniques, however, is the lack of information on the dynamic behavior within a period and in their limited ability to accurately capture waveform ripples. State-space averaging has been a popular simulation technique of pulsewidth-modulated (PWM) dc–dc converters [1]–[3]. However, its main challenge lies in the circuit-specific approach, thereby limiting the ability to automate the modeling and simulation process on arbitrary dc–dc converter topologies. Alternatively, the PWM switch cell model, which was first introduced in [4] and [5] and which is a linearization of the three-terminal switch cell, can be readily applied to a wide range of dc–dc converters. Enhancements to this model were developed in [6]–[8]. While the PWM switch cell model is simple to apply and very efficient during simulation, its major limitation is that it neglects the dynamic behavior of dc–dc converters within one cycle and provides no information about the waveform ripples [9], [10].

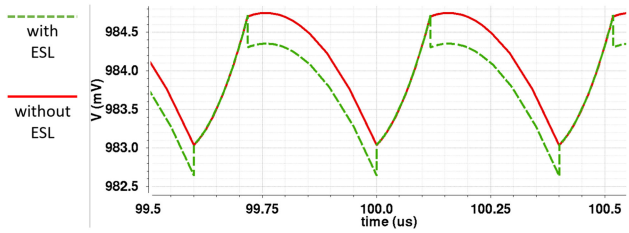

Fig. 1. Output voltage waveform of a buck converter with CMC with (dashed line) and without (solid line) ESL of the output capacitor.

To account for the ripples, a lot of work has been done on generalized averaging techniques [10]–[12]. In [13] and [14], a complete multiharmonic solution to low-power PWM dc–dc converter simulations was presented. The multifrequency model is general in the sense that it can be applied to many dc–dc converters, including buck, boost, and buck–boost converters without any modifications. However, it is important to note that the output signals of dc–dc converters contain several high-frequency characteristics and nonconventional looking ripple waveforms, such as the green curve shown in Fig. 1. Such waveform characteristics can be very difficult to capture without accounting for a high number of harmonics in the model. In that case, the developed model would become extremely complex. For this reason, analytical Fourier-series-based methods have been developed to accurately capture the output ripple waveforms using a large number of harmonics [15]–[20]. Since these methods are analytical in nature, they are based on circuit-specific equations that are expanded using Fourier series, which means that these models have to be derived for each converter topology. In [21], a general Fourier-series-based model is presented that is not circuit specific. The model focuses on capturing targeted small-signal properties and transfer functions, and it is, therefore, useful primarily as a tool for designing appropriate feedback control.

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Simulation methods that are particularly efficient in the transient analysis of switching converters have been developed and incorporated into the commercial tool SIMetrix/Simplis [22]. However, this simulation approach is applicable in the system-level analysis of switching converters realized with discrete components, not in the transistor-level simulation of low-power integrated switching converters, which is the target application area of this article's contribution.

In this article, we address the limitations of Fourier-series-based modeling techniques by presenting a simulation-based multiharmonic model that accurately captures the nonconventional characteristics of output waveforms in the steady state in conjunction with circuit averaging techniques. This method significantly reduces the simulation time even while accounting for a large number of harmonics. In our proposed model, the circuit averaging technique is first used to determine the dc operating point of the converter, from which the Fourier series coefficients are then extracted to accurately reconstruct the output ripple waveforms. The proposed model is general in the sense that it is not derived from topology-specific circuit equations, but from the common properties of dc–dc converters: the voltage and current waveforms at the PWM switch cell terminals. Therefore, the model can be adapted and applied to arbitrary converter circuit topologies. We will show that the model can be applied to low-power converters with current-mode control (CMC), which not many models account for in the literature. Of the existing work addressing converter topologies with CMC, the models in [21] and [23] are the most related to this article. They present small-signal models and apply to multiphase converter designs, while this article presents general large-signal models and targets low-power integrated circuit applications. Finally, we will show that our model brings one order of magnitude reduction in simulation time, while maintaining remarkable accuracy even for a large number of harmonics.

The presented approach is an abstraction level in-between averaged models and full transistor-level simulation. The method incorporates the state-of-the-art averaged model that allows for fast simulation of the transient response and the capability of performing small-signal analysis. While the averaged model does not provide information about the waveform ripple, this method presents a novel approach for ripple reconstruction, with an accuracy close to transistor-level simulation, but with a speed improvement of over one order of magnitude.

In more detail, the following new contributions are presented.

1) Test circuits for the dynamic characterization of the parameters of the PWM switch cell model are presented for buck and boost converters with CMC operating in a continuous conduction mode (CCM).
2) The Fourier series expansions for the currents and voltages at the PWM switch cell terminals are calculated.
3) The Fourier series coefficients and the small-signal transfer function, obtained through simulation, are used to reconstruct the ripple of any waveform in the circuit, for any number of harmonics.

The key characteristic of the method presented in this article, which distinguishes it from any previous similar work, is generality. Specifically, this method provides the following features with no additional modeling effort.

1) It covers any dc–dc converter topology with CMC. The applicability range is the same for this method as for the PWM switch cell model. The method can be easily transferred to architectures with other duty cycle control methods (e.g., voltage mode), by simply replacing the PWM switch cell model accordingly.
2) It accounts for any parasitic element (e.g., the equivalent series inductance (ESL) of the output capacitor, which is not included in any other modeling article).
3) It accounts for any transistor-level surrounding circuitry (e.g., error amplifier, current sensing), while all other modeling papers use ideal circuitry.
4) By increasing the number of harmonics, increasing levels of precision can be achieved (the choice is determined by the tradeoff between accuracy and computational effort/time).

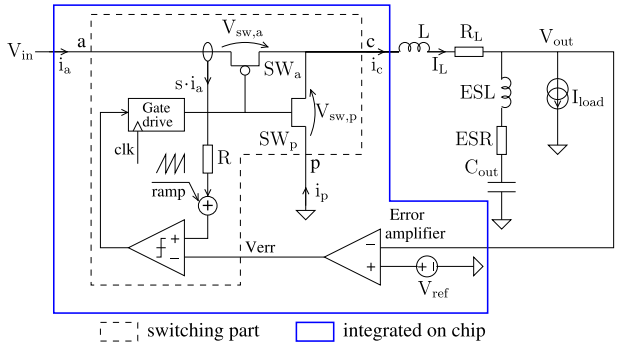

Fig. 2. Synchronous buck converter with peak current control. The circuit part integrated on chip is shown distinctively.

The method is particularly useful in the transistor-level simulation of integrated switching converters. At this simulation level, simulators (e.g., Spectre) are needed that can efficiently handle complex transistor models (e.g., BSIM). This method is implemented within the framework of the commercial tool Cadence Virtuoso.

The remainder of this article is organized as follows. Section II gives an overview of the characteristics and operation of current-mode-controlled buck and boost converters. Section III presents the PWM switch cell large-signal averaged model. Section IV describes the circuits for dynamic characterization of the PWM switch cell model parameters during simulation. Section V presents the Fourier series expansion for the voltages and currents at the PWM switch cell nodes and then the new simulation flow. The simulation flow is then illustrated by the experimental results in Section VI. Finally, Section VII concludes this article.

II. DC–DC Converters With CMC

A. Buck Converter

Fig. 2 shows the topology of a synchronous buck converter with peak current control. The inductor L is shown together with

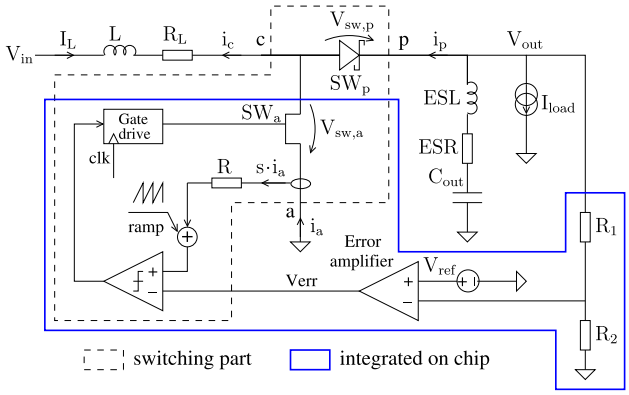

Fig. 3. Asynchronous boost converter with peak current control. The circuit part integrated on chip is shown distinctively.

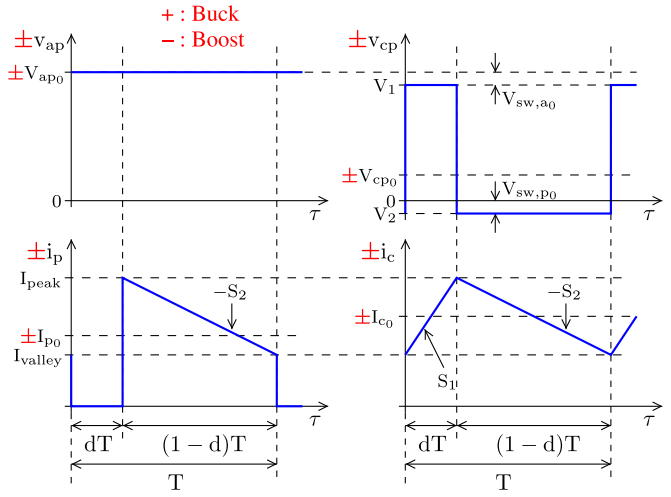

Fig. 4. PWM switch cell instantaneous terminal voltages and currents for a buck (+) and a boost (−) converter operating in the CCM.

its parasitic resistance R_L and the output capacitor C_{out} together with its parasitic elements: the equivalent series resistance (ESR) and ESL.

The blue box encircles the circuit elements integrated on a single chip. The elements implemented as discrete components are the following:

1) the inductor L, as integrated inductors have a poor performance;
2) the output capacitor C_{out}, as capacitances in the range of microfarads (typical value for the output capacitor of a dc–dc converter) are not feasible for integration.

The dashed box encloses the switching elements of the converter. The meaning of the terminals a, p, and c will be explained in Section III. The core of this subcircuit is composed of two switches: the high-side switch SW_a, implemented as a PMOS transistor, and the low-side switch SW_p, implemented as an NMOS transistor. The other elements of the subcircuit are part of the control loops.

The topology has two control loops. The first loop regulates the output voltage V_{out} by comparing it with the reference voltage V_{ref} by means of an error amplifier. The second loop regulates the duty cycle of the gate driving signal, which is controlled by the comparator. The error voltage V_{err} fixes the peak value, up to which the inductor current must increase before switching. Additionally, a compensation ramp is subtracted from V_{err} for stability purposes [7].

B. Boost Converter

Fig. 3 shows the topology of an asynchronous boost converter with peak current control. There are several similarities to the buck topology from the previous section.

1) The inductor L and the output capacitor C_{out} are shown together with their parasitic elements.
2) The dashed box encloses the switching part of the circuit. The core of this subcircuit consists of two switching elements: the high-side switch SW_p, implemented as a Schottky diode, and the low-side switch SW_a, implemented as an NMOS transistor. The meaning of the terminals a, p, and c will be explained in Section III.
3) The blue box encircles the circuit elements integrated on chip. In addition to the inductor L and the output capacitor C_{out}, the Schottky diode is also implemented as a discrete element.
4) There are two control loops: one for regulating the output voltage V_{out} and the other for regulating the duty cycle. The control loops work in a similar way to the buck example, as described in Section II-A.

Because the output voltage of the boost is larger than the input, it is divided on a resistive divider in order to be compared with the reference voltage V_{ref}.

III. PWM Switch Cell Large-Signal Averaged Model

Large-signal averaged models have been developed to reduce the computational cost of simulating switching circuits. The simulation based on such models produces the waveforms averaged over a switching period and is much faster than the simulation based on the switched model (since the small time step in the transient analysis is no longer needed). Also, by linearizing the large-signal averaged model, the small-signal model is obtained. The drawback of using the averaged model is the accuracy loss, as the simulated waveforms over a period contain the average value, without the ripple.

The PWM switch model replaces the switching network of the converter (marked with the dashed box in Figs. 2 and 3) with a three-terminal model, having the nodes a (*active*), p (*passive*), and c (*common*, the junction between the two switches) [7]. This approach has the great advantage of generality, as it fits all dc–dc converter topologies just through model rotations.

A. Voltage and Current Waveforms

Fig. 4 shows the PWM switch cell instantaneous terminal voltages and currents and their average values for a buck and for a boost converter operating in the CCM, where d represents the duty cycle and T the switching period. In the first phase, dT, the switch SW_a is ON, and the diode SW_p is OFF. In the

TABLE I
PWM SWITCH CELL TERMINAL VOLTAGES AND CURRENTS FOR BUCK AND BOOST CONVERTERS

	Buck	Boost
V_{ap_0}	V_{in}	$-V_{out}$
V_{cp_0}	V_{out}	$V_{in} - V_{out}$
I_{c_0}	I_{load}	$-I_{load}/d$
I_{p_0}	$I_{load}(1-d)$	$-I_{load}$

TABLE II
PWM SWITCH CELL VOLTAGE LEVELS AND CURRENT SLOPES AND LEVELS

	w/o losses	w/ losses
V_1	V_{ap_0}	$V_{ap_0} - V_{sw,a_0}$
V_2	0	$-V_{sw,p_0}$
S_1	V_{ac_0}/L	$(V_{ac_0} - V_{sw,a_0})/L$
S_2	V_{cp_0}/L	$(V_{cp_0} + V_{sw,p_0})/L$
I_{peak}	$I_{c_0} + S_1 dT/2$	
I_{valley}	$I_{c_0} - S_1 dT/2$	

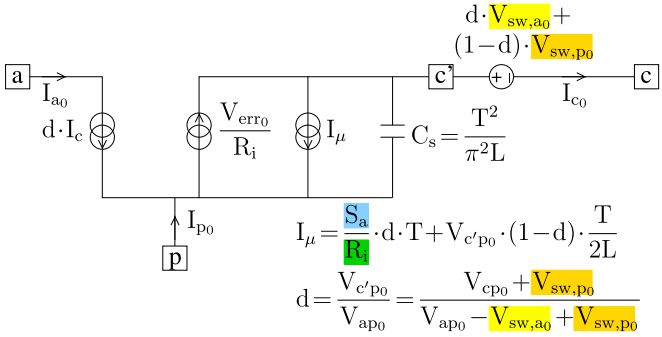

Fig. 5. Large-signal averaged model with voltage drops on switching elements for a dc–dc converter with peak current control.

second phase, $(1-d)T$, SW_a is OFF and SW_p is ON. This holds for both converters. The waveforms are the same for the buck and for the boost converter, except for the opposite sign. For example, v_{cp} for the buck overlaps $-v_{cp}$ for the boost. Also, in the boost converter i_c has an opposite direction with the inductor current, such that the bottom-right waveform of Fig. 4 represents $-i_c$. The average values of these waveforms are denoted with the index "0" and hereafter, called "index-0 components." The terminal voltages and currents and the inductor current slopes for the buck and for the boost converter are given in Tables I and II.

B. PWM Switch Cell Equivalent Circuit

The large-signal averaged model developed in [4] expresses a relationship between the index-0 components for an ideal dc–dc converter. Adding the voltage drops on the switching elements gives the final large-signal averaged model [7], as depicted in Fig. 5. In this model, V_{err} represents the output of the error amplifier, V_{sw,a_0} and V_{sw,p_0} are the voltage drops on SW_a and SW_p, respectively, during their ON-state, R_i is the equivalent sensing resistor for the inductor current, and S_a is the slope of the compensation ramp [7]. The current I_μ is a notation used for compactness purposes [7]. It represents that part of the current in node c dependent on the duty cycle d. The remaining part of I_c is dependent on V_{err}, the output of the error amplifier.

The capacitor C_s is introduced to model subharmonic oscillations [7]. The value of this capacitor is chosen such that it resonates with the inductor L at the frequency of the subharmonic oscillations, which is $F_{sw}/2$, half of the switching frequency. This creates a peak in the frequency response at $F_{sw}/2$, predicting the subharmonic instability.

The major advantage of the PWM switch cell model is its generality and flexibility: it holds both for the buck and for the boost converter (and also for other dc–dc converters [7]). The equivalent circuit of the PWM switch cell large-signal averaged model depends on the control method. Each control technique (e.g., voltage mode and current mode) has its own equivalent circuit for the PWM switch cell. The equivalent circuit of the PWM switch cell large-signal averaged model, shown in Fig. 5, corresponds to that of CMC. The test circuits and the simulation method presented in this article are applicable for any control technique, as long as the PWM switch cell equivalent circuit specific to each technique is modeled accordingly.

IV. DYNAMIC CHARACTERIZATION OF THE LARGE-SIGNAL AVERAGED MODEL PARAMETERS

A. Parameter Dynamic Characterization

The PWM switch cell model for CMC contains several parameters: L, T, V_{sw,a_0}, V_{sw,p_0}, R_i, and S_a. The inductance L and the switching period T are design parameters, which need to be provided before the start of the simulation. The rest of the parameters are extracted dynamically, during the simulation of the circuit with the averaged PWM switch cell model and will each be explained next.

The voltage drops on the switches, V_{sw,a_0} and V_{sw,p_0}, depend on the current flowing through the switches during their ON-state. In each phase, the current through the ON-switch (SW_a in the first phase and SW_p in the second phase) is equal to the inductor current. The inductor current equals i_c for the buck converter and $-i_c$ for the boost converter and is represented in the bottom-right plot of Fig. 4. Therefore, by injecting the averaged value over a period of this current ($I_{L_0} = |I_{c_0}|$) into a copy of the switch, one can get the averaged voltage drop over the switch, as illustrated in Fig. 6(a) for the synchronous buck converter and in Fig. 7(a) for the asynchronous boost converter.

The equivalent sense resistance R_i is also extracted during simulation, by replicating the sensing circuit and the active switch SW_a (in both examples from this article, the buck converter from Fig. 2 and the boost converter from Fig. 3, the current through the active switch is sensed), with the gate driven in the ON-state, and injecting the index-0 inductor current into it, as explained in Fig. 6(b) for the buck converter and in Fig. 7(b) for the boost converter. Then, having the voltage drop V_R and the current to be sensed I_{L_0}, the equivalent resistance R_i is obtained.

The last parameter is the slope of the compensation ramp, S_a. Unlike the other parameters, which depend on linear circuits, S_a is based on a switching circuit, as depicted in Fig. 8(a). At a time t after the switch is turned OFF, C_a is charged at the voltage $V_a = I_a \cdot t/C_a$. The linear circuit in Fig. 8(b) reproduces the state of the ramp generator at the time t. With two instances of this circuit, the state at two different time points within a period

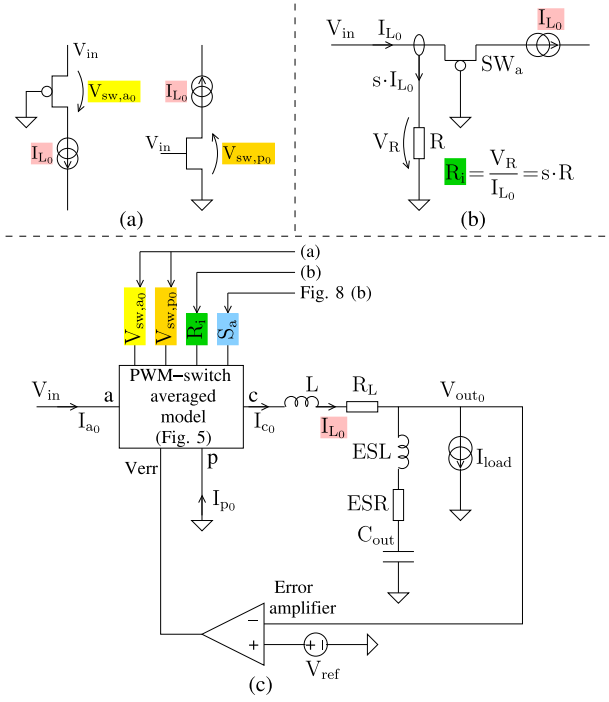

Fig. 6. Simulation setup for the synchronous buck converter with the PWM switch cell large-signal averaged model. (a) Main circuit. (b) Circuit for dynamic evaluation of index-0 voltage drop on the switches. (c) Circuit for dynamic evaluation of equivalent sense resistance.

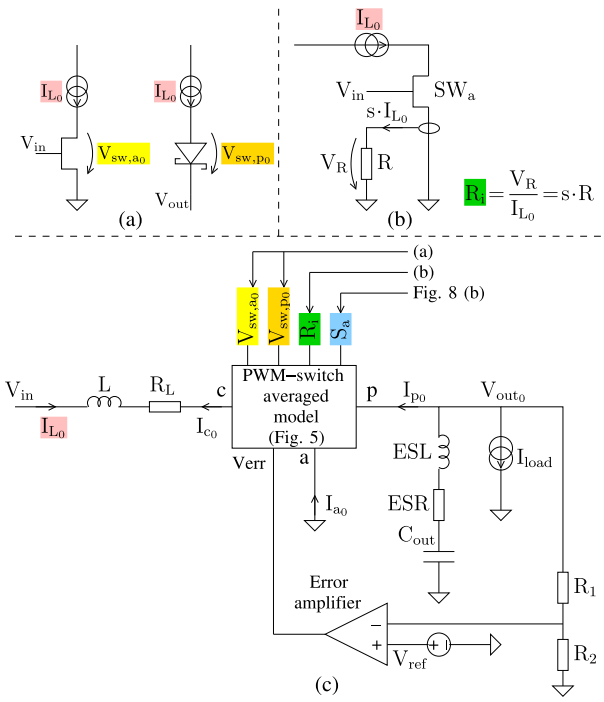

Fig. 7. Simulation setup for the asynchronous boost converter with the PWM switch cell large-signal averaged model. (a) Main circuit. (b) Circuit for dynamic evaluation of index-0 voltage drop on the switches. (c) Circuit for dynamic evaluation of equivalent sense resistance.

is reproduced: t_1, and t_2, when C_a is charged at V_{a_1}, and V_{a_2}, respectively. The time interval $\Delta t = t_2 - t_1$ is linked to the voltage difference $\Delta V_a = V_{a_2} - V_{a_1}$ by $\Delta t = C_a \cdot \Delta V_a / I_a$. Then, by making use of the linear increase in V_R and measuring this voltage for the two states, the compensation ramp is obtained: $S_a = (V_{R_2} - V_{R_1})/\Delta t$.

B. Simulation Testbench

The circuit blocks described in the previous section are assembled to form the simulation testbench for the large-signal averaged model. Fig. 6 shows the testbench for the buck converter and Fig. 7 for the boost converter. The testbench contains the following parts:

1) the dc–dc converter, shown in Figs. 6(c) and 7(c), respectively, in which the switching part (the dashed box in Figs. 2 and 3, respectively) is replaced by the PWM switch averaged model from Fig. 5;
2) the circuit for calculating the averaged voltage drops V_{sw,a_0} and V_{sw,p_0} on the switches SW_a and SW_p, shown in Figs. 6(a) and 7(a), respectively;
3) the circuit for calculating the equivalent resistance R_i for current sensing, shown in Figs. 6(b) and 7(b), respectively;
4) the circuit for calculating the slope of the compensation ramp, made up of two instances of the circuit from Fig. 8(b).

The circuit blocks from the averaged-signal simulation testbench form a feedback loop. For the buck converter, for example, the inductor current I_{L_0} from the main circuit from Fig. 6(c) is replicated and injected into the circuits from Fig. 6(a) and (b),

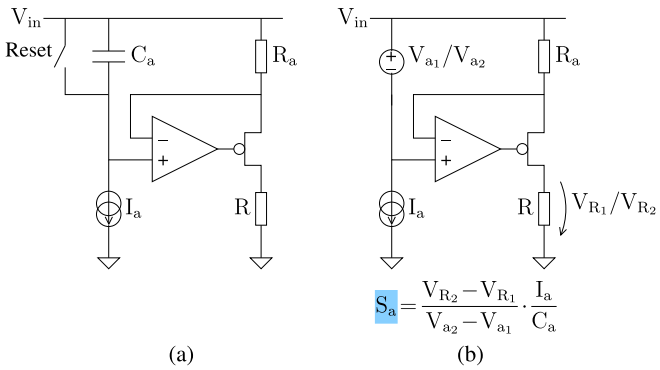

Fig. 8. Dynamic calculation of the slope of the compensation ramp. (a) Switching circuit. (b) Averaged model, which requires two instances of this circuit.

to calculate the parameters V_{sw,a_0}, V_{sw,p_0}, and R_i. The values of these parameters are then fed back to the main circuit from Fig. 6(c), namely to the PWM switch averaged model. The ramp generation circuit from Fig. 8(b) is also part of the testbench, but it provides the compensation ramp S_a to the model in an open loop. The same explanations hold for the boost converters (see Fig. 7).

V. Fourier Series Representation of PWM Switch Cell Signals

This section provides the Fourier series expansions for the signals from Fig. 4, the voltage v_{cp} and the currents i_c and i_p of a dc–dc converter operating in the CCM. Then, it will be shown

how the Fourier series of these three signals and the small-signal analysis of the circuit can be used to reconstruct other signals in the circuit.

A periodic signal with period T and angular frequency $\omega = 2\pi/T$ can be represented by its complex Fourier series

$$x(\tau) = \sum_{n=-\infty}^{\infty} X_n \exp(jn\omega\tau) \tag{1}$$

where the coefficients X_n are calculated as

$$X_n = \frac{1}{T}\int_t^{t+T} x(t)\exp(-jn\omega\tau)dt. \tag{2}$$

Then, the signal $x(t)$ can be reconstructed from its first N harmonics as

$$x(\tau) = X_0 + 2\sum_{n=1}^{N} |X_n|\cos(n\omega\tau + \arg(X_n)). \tag{3}$$

The precision in reconstructing $x(t)$ increases with the number of harmonics N.

Applying (2) to these waveforms from Fig. 4, the coefficients of the Fourier series expansion are obtained as

$$\begin{aligned} V_{cp_n} &= |V_{cp_n}|\exp(j\arg(V_{cp_n})) \\ I_{c_n} &= |I_{c_n}|\exp(j\arg(I_{c_n})) \\ I_{p_n} &= |I_{p_n}|\exp(j\arg(I_{p_n})) \end{aligned} \tag{4}$$

where

$$\begin{aligned} |V_{cp_n}| &= (V_1 - V_2)\frac{\sin(n\pi d)}{n\pi} \\ &= (V_{ap_0} - V_{\text{sw},a_0} + V_{\text{sw},p_0})\frac{\sin(n\pi d)}{n\pi} \\ \arg(V_{cp_n}) &= -\pi n d \end{aligned} \tag{5}$$

and

$$\begin{aligned} |I_{c_n}| &= \frac{T(S_1+S_2)}{2}\frac{\sin(n\pi d)}{(n\pi)^2} \\ &= \frac{T(V_{ac_0} - V_{\text{sw},a_0} + V_{cp_0} + V_{\text{sw},p_0})}{2\,L}\frac{\sin(n\pi d)}{(n\pi)^2} \\ \arg(I_{c_n}) &= -\pi(nd + 0.5). \end{aligned} \tag{6}$$

For the current i_p, the complex coefficients of the Fourier series expansion are calculated as

$$I_{p_n} = \frac{2\exp(-jn\pi d)\sin(n\pi d)\left(\frac{S_2\,T}{2n\pi} - jI_{\text{peak}}\right) + S_2T(1-d)}{2jn\pi} \tag{7}$$

where S_2 and I_{peak} are given in Table II. Because of the shape of this waveform, the expression is more complex than in the case of v_{cp} and i_c. Separating I_{p_n} into the magnitude and phase does not lead to simple compact expression. I_{p_n} is hence left in the complex form.

The index-0 components V_{ap_0}, V_{ac_0}, V_{cp_0}, V_{sw,a_0}, and V_{sw,p_0} are obtained from the simulation of the large-signal averaged model, using the simulation testbench described in Fig. 6 for the buck converter and in Fig. 7 for the boost converter. The duty cycle d is calculated from the index-0 components, as given in Fig. 5

$$d = \frac{V_{cp_0} + V_{\text{sw},p_0}}{V_{ap_0} - V_{\text{sw},a_0} + V_{\text{sw},p_0}}. \tag{8}$$

Having the index-0 components and the duty cycle, obtained from the averaged large-signal simulation, the Fourier series coefficients of v_{cp}, i_c, and i_p can be computed. Then, with the small-signal analysis, the transfer function of any voltage or current in the circuit relative to v_{cp}, i_c, or i_p at any integer multiple of the switching frequency is calculated. The small-signal transfer function at a specified frequency is a complex number with magnitude and phase. This transfer function is used to reconstruct the steady-state waveform of that signal. The following example will illustrate the method.

Consider the transfer function of v_{out} versus v_{cp} at frequency f, denoted as $H(v_{\text{out}}, v_{\text{cp}}, f)$, having a magnitude $|H(v_{\text{out}}, v_{\text{cp}}, f)|$ and a phase $\arg(H(v_{\text{out}}, v_{\text{cp}}, f))$

$$H(v_{\text{out}}, v_{\text{cp}}, f) = |H(v_{\text{out}}, v_{\text{cp}}, f)|\exp(j\arg(H(v_{\text{out}}, v_{\text{cp}}, f))). \tag{9}$$

The output voltage v_{out} has a small ripple around the average value V_{out_0}. Therefore, the small-signal assumption can be applied. Using the transfer function $H(v_{\text{out}}, v_{\text{cp}}, f)$ and the coefficients of the Fourier series expansion of v_{cp}, the harmonics (at multiples of the switching frequency $1/T$) of v_{out} are calculated

$$V_{\text{out}_n} = V_{cp_n}\cdot H\left(v_{\text{out}}, v_{\text{cp}}, \frac{n}{T}\right) = |V_{\text{out}_n}|\cdot\exp(j\arg(V_{\text{out}_n})) \tag{10}$$

where

$$\begin{aligned} |V_{\text{out}_n}| &= |V_{cp_n}|\cdot\left|H\left(v_{\text{out}}, v_{\text{cp}}, \frac{n}{T}\right)\right| \\ \arg(V_{\text{out}_n}) &= \arg(V_{cp_n}) + \arg(V_{\text{out}_n}) \end{aligned} \tag{11}$$

with $|V_{cp_n}|$ and $\arg(V_{cp_n})$ given in (5).

Afterwards, using (3), the signal $v_{\text{out}}(\tau)$ in the steady state can be reconstructed from its Fourier series expansion, with the desired number of harmonics N

$$v_{\text{out}}(\tau) = V_{\text{out}_0} + 2\sum_{n=1}^{N}|V_{\text{out}_n}|\cos\left(2\pi\frac{n}{T}\tau + \arg(V_{\text{out}_n})\right). \tag{12}$$

The same procedure is applied for any other signal in the circuit, relative to v_{cp}, i_c, or i_p. As it will be shown in the experimental results, the signal on which to refer is chosen depending on the converter type. For the buck converter, v_{cp} or i_c can be used with similar precision, while for the boost converter, using i_p provides the best precision. The flowchart shown in Fig. 9 summarizes the proposed modeling approach presented in this section.

VI. Simulation Results

In this section, the proposed multiharmonic averaged model is tested on a buck and on a boost converter, to demonstrate its accuracy and speedup. The proposed model is compared with the simulation results of the original transistor-level converter circuits, which are implemented in a standard CMOS 180-nm

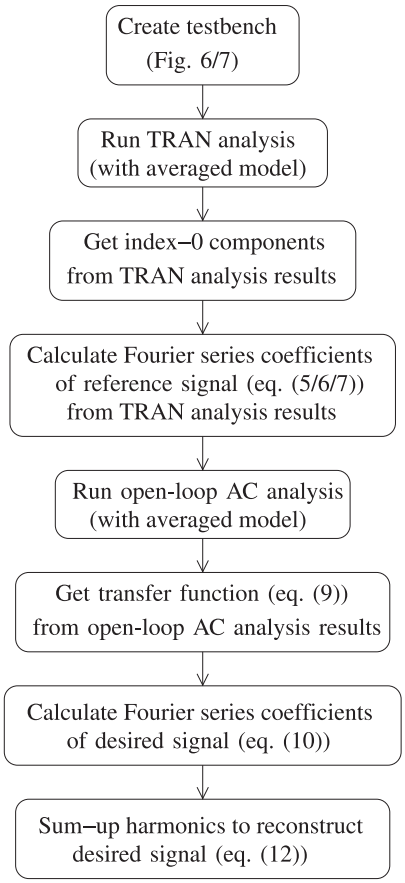

Fig. 9. Simulation flow based on the PWM switch cell averaged model and Fourier series.

5-V technology. The PWM switch cell large-signal averaged model is implemented in VerilogA. All circuits are simulated using the commercial tool Cadence Spectre on a Linux workstation with a 3.4-GHz Intel i5 processor and 8 GB of RAM. In the proposed model, the circuits are simulated in the same conditions, and then, the computation of the waveform ripples is done with a Cadence SKILL script.

Switching circuits cannot be simulated directly (at transistor level) in the frequency domain. This kind of analysis becomes possible by means of the large-signal averaged model of the PWM switch cell. Previous work proposed a linearized (small-signal) version of this model [4], [5], [7]. However, in modern simulators like Cadence Spectre, nonlinear devices (e.g., the MOS transistor and the PWM switch cell) are automatically linearized by the simulator for the small-signal analysis. Therefore, it is not necessary to manually implement a linearized version of the PWM switch cell model, but the small-signal analysis (e.g., open-loop ac analysis) can be applied directly to this model.

A. Buck Converter

The first example circuit is a synchronous buck converter operating in the CCM, with CMC of the duty cycle, as the one shown in Fig. 2. The converter receives an input voltage of $V_{\text{in}} = 4$ V (which is also the supply voltage of the entire circuit) and produces a desired output voltage $V_{\text{out}} = 1$ V at a load current $I_{\text{load}} = 2.5$ A. The switching frequency is $F_{\text{sw}} = 2.5$ MHz, equivalent to a switching period $T = 400$ ns. The component values are as follows:

1) inductance $L = 1$ μH, with parasitic ESR $R_L = 50$ mΩ;
2) output capacitance $C_{\text{out}} = 20$ μF, with parasitic ESR of 10 mΩ, and ESL of 100 pH.

Previous work dealing with multiharmonic buck converter modeling typically did not consider the ESL of the output capacitor, as this would significantly increase the complexity of the equations for the methods based on state-space averaging. However, for a converter operating at a high switching frequency, this parasitic element has a noticeable effect on the output voltage ripple, as shown in Fig. 1 in Section I, and, therefore, should not be ignored.

The buck converter is implemented at the transistor level. As it is a switching circuit, transient analysis is necessary to simulate its behavior. The analysis requires a small time step. The simulation is run over 1 ms, meaning 2500 periods, as the switching frequency is 2.5 MHz. For this simulation time, 1.3 M points are simulated, and the total computational time is 443 s in the transistor-level transient simulation.

The conventional averaged model provides much faster simulation capabilities. For the same simulation time of 1 ms, only 669 points are simulated, meaning 5000 times less than with the transistor model, and the transient analysis lasts only 1 s in this case. The disadvantage is that it produces only the waveform values averaged over a period.

On the other hand, by using the proposed method described in Section V, a good approximation of the transistor-level waveforms in the steady state can be obtained in a shorter time than with the transistor-level simulation. Note that, in addition to the transient analysis, a small-signal analysis (open-loop ac analysis) is necessary to obtain the small-signal transfer functions. Its CPU runtime is, however, negligible.

Figs. 10 and 11 visually compare the waveforms obtained from the original transistor-level circuit with the waveforms reconstructed using the proposed model with an increasing number of harmonics. Fig. 10 shows the output voltage V_{out}. This is the most important waveform in the circuit to be reconstructed, because common performance figures, like the output peak-to-peak ripple, are related to it. The output voltage is reconstructed with a gradually increasing number of harmonics: 1, 2, 10, 25, and 50, respectively. When considering only the first-order component, the reconstructed ripple is a sine wave. With components up to the tenth order, the waveform begins to look similar to the transistor-level waveform. With components up to the 50th order, the reconstructed waveform is almost identical to the transistor-level one.

The ripple waveform can be reconstructed for other signals in the circuit as well. Fig. 11 shows a comparison between the reconstructed ripple waveform (using two and ten harmonics) and the transistor-level ripple waveform for the error voltage (V_{err}, the output of the error amplifier). For the ripple waveform generated with two harmonics, the difference to the transistor-level model is visible, but with ten harmonics, the waveforms almost overlap. The same method can be applied for the inductor

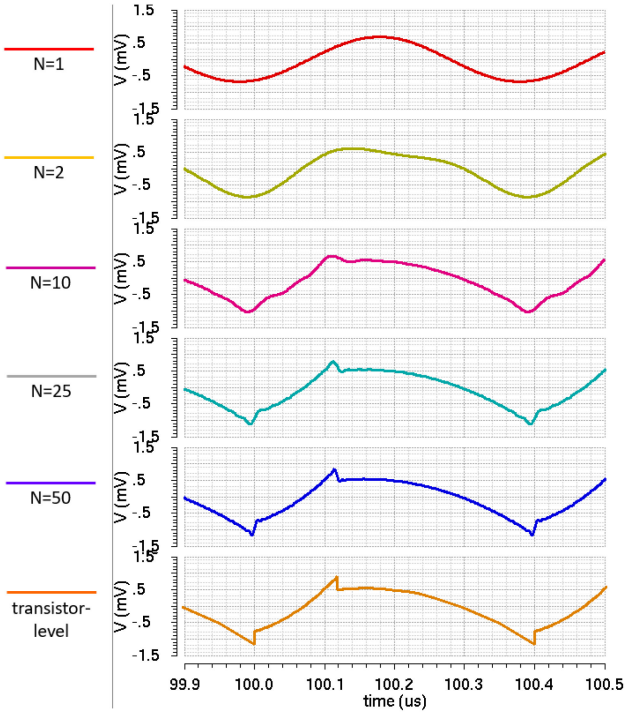

Fig. 10. Output voltage (V_{out}) ripple (total voltage minus average value) for the buck converter. Reconstructed waveforms, from the averaged-model simulation, with a gradually increasing number of harmonics: 1, 2, 10, 25, and 50, respectively. At the bottom, the waveform resulted from transistor-level simulation.

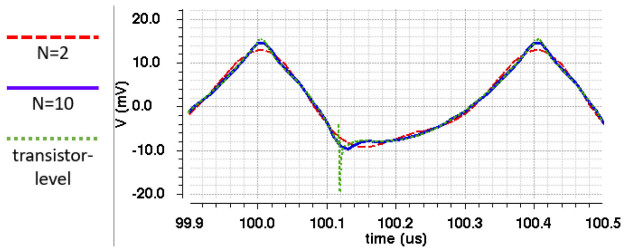

Fig. 11. Error voltage (V_{err}) ripple (total voltage minus average value) for the buck converter. Reconstructed waveforms, from the averaged-model simulation, with two and ten harmonics, respectively, and the waveform resulted from transistor-level simulation.

current I_L and the capacitor current I_{cap} (both have a triangular shape).

The ripple waveforms for the signals of a buck converter can be reconstructed by taking either the inductor current i_c or the voltage v_{cp} as the reference signal. The difference is insignificant, as seen in Table III, which quantitatively evaluates the accuracy of the waveforms generated using the proposed approach. The table shows the rms error of the reconstructed waveform versus the transistor-level waveform over one period in the steady state. The rms error, which is a standard error metric, is calculated as

$$\text{Error}_{\text{rms}} = \frac{1}{T}\sqrt{\int_t^{t+T}\left(\frac{x_{\text{out}}(\tau) - x_{\text{out},N}(\tau)}{X_{\text{out,pp}}}\right)^2 d\tau} \qquad (13)$$

TABLE III
RMS ERROR OVER ONE PERIOD OF RECONSTRUCTED BUCK WAVEFORM RIPPLES VERSUS COMPLETE WAVEFORM RIPPLE

Number of Harmonics N	V_{out}		V_{err}	
	vs. i_c	vs. v_{cp}	vs. i_c	vs. v_{cp}
1	9.6%	9.6%	8.3%	8.3%
2	5.0%	5.0%	4.1%	4.1%
10	2.1%	2.1%	2.1%	2.1%
25	1.3%	1.3%	2.0%	2.0%
50	1.0%	1.0%	2.0%	2.0%

TABLE IV
RMS ERROR OVER ONE PERIOD OF RECONSTRUCTED BUCK WAVEFORM RIPPLES VERSUS COMPLETE WAVEFORM RIPPLE WITH IDEAL AND NONIDEAL SWITCHES

Number of Harmonics N	V_{out}		I_L	
	non-ideal switches	ideal switches	non-ideal switches	ideal switches
1	9.6%	10.1%	8.7%	8.9%
2	5.0%	5.6%	2.5%	3.2%
10	2.1%	3.0%	0.4%	2.4%
25	1.3%	3.0%	0.1%	2.4%
50	1.0%	3.1%	0.1%	2.4%

where x_{out} is the ripple of transistor-level waveform, $x_{out,N}$ is the ripple reconstructed with N harmonics and $X_{out,pp}$ is the peak-to-peak magnitude of the transistor-level ripple. When computing the rms error, only the ripples were considered, centered around 0. Note that the averaged values are subtracted due to the small error introduced by the averaged model compared to the transistor-level model. The differences in the averaged values are in the order of millivolts. However, this is a limitation of the averaged model, not of the method based on Fourier series for reconstructing the ripple. In order to evaluate the accuracy of this method, Table III only compares the ripples. For V_{out}, the rms error is very close to 2% for ten harmonics and already at 1% for 50 harmonics. For V_{err}, the rms error for ten harmonics is very close to 2%. For a larger number of harmonics, there is almost no improvement in the accuracy of the reconstructed ripple of V_{err}. The reason for this is the negative spike of the transistor-level waveforms, as seen in Fig. 11. This spike does not appear in the reconstructed waveforms and so causes a systematic error. In order for it to be accounted for, the number of harmonics needs to be significantly larger than 50, which is impractical from the CPU runtime point of view.

The accuracy of the reconstructed waveforms is also a result of including nonideal elements. For example, the voltage drops on the switches during their ON-state, which have typical values of 50 to 100 mV, are considered, as described in the simulation setup from Fig. 6 and in the expressions for ripple calculation derived in Section V. Table IV shows the rms error for the reconstructed waveform (with and without considering voltage drops on the switches) versus the accurate transistor-level waveform (with nonideal switches). With no voltage drops on the switches, the error is larger. For V_{out}, the error drops below 1% with nonideal switches, but remains above 3% with ideal switches even for a large number of harmonics. For I_L, the error reaches 0.1% with switch voltage drops and remains above 2% with ideal switches.

TABLE V
PERCENTAGE ERROR OF PEAK-TO-PEAK RIPPLE MAGNITUDE OF RECONSTRUCTED WAVEFORM VERSUS COMPLETE WAVEFORM WITH IDEAL AND NONIDEAL SWITCHES

Number of Harmonics N	V_{out}		I_L	
	non-ideal switches	ideal switches	non-ideal switches	ideal switches
1	35%	38%	22%	26%
2	30%	32%	11%	14%
10	19%	21%	4.0%	7.2%
25	9%	12%	1.5%	5.1%
50	5%	7%	0.9%	4.5%

TABLE VI
RUNTIME COMPARISON—BUCK CONVERTER

Model	Number of harmonics	Simulation time	Ripple calculation	Total time	Speedup
transistor-level	N/A	443s (TRAN)	N/A	443s	1x
averaged	N=1	1s (TRAN+AC)	1s	2s	220x
	N=2		1s	2s	220x
	N=10		2s	3s	150x
	N=25		12s	13s	35x
	N=50		45s	46s	10x

The above-described rms error is an important indicator of the method's accuracy. It shows the accuracy of the reconstructed waveform compared to the transistor-level waveform. Properties like the peak-to-peak ripple magnitude and the harmonic distortion can be extracted. The former is a common performance figure for dc–dc converters. Table V shows the accuracy of the peak-to-peak ripple magnitude of the reconstructed waveform relative to the transistor-level waveform, calculated as

$$\text{Error}_{\text{ripple}} = \left| \frac{X_{\text{out,pp}} - X_{\text{out},N,\text{pp}}}{X_{\text{out,pp}}} \right| \tag{14}$$

where $X_{\text{out,pp}}$ and $X_{\text{out},N,\text{pp}}$ are the peak-to-peak ripple magnitudes for the transistor-level waveform and the waveform reconstructed with N harmonics, respectively. For V_{out}, the error is below 10% at 25 harmonics and 5% at 50 harmonics. For I_L, the error is below 2% at 25 harmonics and below 1% at 50 harmonics. As for the rms error, the accuracy is improved (especially for I_L) by considering the switch voltage drops. The proposed method also has the capability to account for arbitrary parasitic elements with no additional modeling effort. Fig. 1 shows how considering the parasitic inductance of C_{out} provides a more accurate peak-to-peak ripple.

Table VI presents the runtime comparison between the transistor-level model simulation and the averaged model simulation with ripple reconstruction based on Fourier series. The transient analysis runtime is negligible for the latter (1 s) compared to the former (443 s). The open-loop ac analysis runtime is negligible as well. With the averaged model, additional time is needed to calculate the ripple, time which increases with the desired accuracy, namely with the number of harmonics. The choice of the number of harmonics is determined by the tradeoff between accuracy and computational effort.

In this buck converter example, the ripple waveforms are generated with a time resolution of 1 ns, meaning $1/400$ of a period. By reconstructing the output voltage V_{out} with 25 harmonics, a 35× speedup is achieved, while having an accuracy loss of only 1.3%. With 50 harmonics, the speedup is still 10× and the accuracy loss is only 1%.

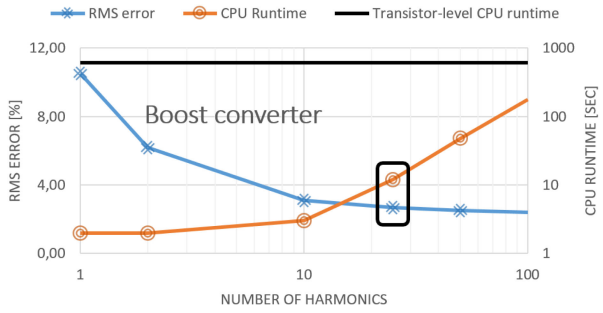

Fig. 12. Tradeoff between accuracy (measured by the rms error) and computational effort (measured by the CPU runtime), both in relation to the number of harmonics, for the buck converter. A typical tradeoff between accuracy and CPU effort is marked at 25 harmonics.

The results from Tables III and VI, discussed in the previous paragraphs, are graphically illustrated in Fig. 12, showing for the buck converter the tradeoff between accuracy (measured by the rms error) and computational effort (measured by the CPU runtime), both in relation to the number of harmonics.

Practical integrated circuits need to account for robustness in the design and verification process. Monte Carlo analysis is a common method, applied for various circuits, including dc–dc converters [24], [25]. Alternatively, deterministic approaches can be used, such as the worst-case distance approach. Both methods require a large number of simulations (typically, hundreds to thousands). Circuit optimization is another situation requiring a large number of simulations [26]. These methods would benefit significantly from the speedup of the individual simulations of dc–dc converters.

Consider the Monte Carlo analysis of the buck converter example from this section. The output voltage peak-to-peak ripple is a common performance figure. The averaged model produces no ripple information, while transistor-level simulation is computationally expensive. The method presented in this article provides a faster way to obtain the ripple information. In this example, the number of harmonics to reconstruct the ripple waveform for the output voltage can be chosen as 25, as this provides a good tradeoff between accuracy and speed, according to Tables III and VI and Fig. 12. For a Monte Carlo analysis with 100 simulations, the total runtime decreases from approximately 12 h and 30 min in the transistor-level approach to approximately 20 min with the proposed method.

B. *Boost Converter*

The second example is an asynchronous boost converter, shown in Fig. 3, operating in the CCM and with CMC of the duty cycle. The converter produces an output voltage $V_{\text{out}} = 19$ V at a load current $I_{\text{load}} = 400$ mA from an input voltage $V_{\text{in}} = 4$ V (which is also the supply voltage of the entire circuit). The switching frequency is $F_{\text{sw}} = 500$ kHz, equivalent to a switching period $T = 2\,\mu$s. The component values are:

1) inductance $L = 10\,\mu$H, with parasitic ESR $R_L = 50\,\text{m}\Omega$;

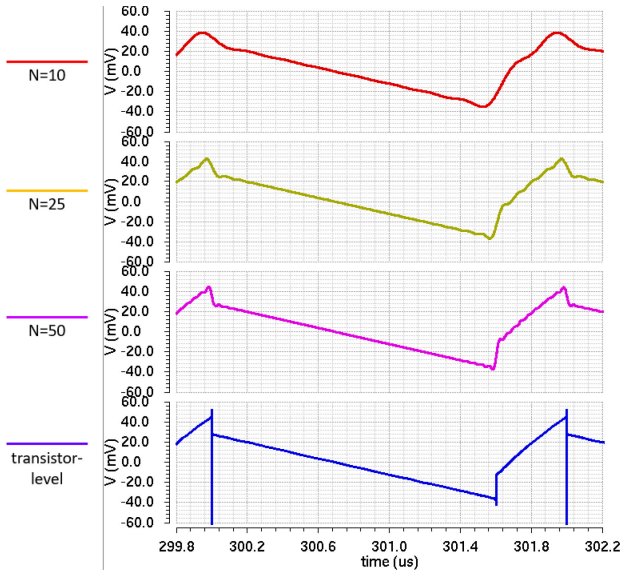

Fig. 13. Output voltage (V_{out}) ripple (total voltage minus average value) for the boost converter. Reconstructed waveforms, from the averaged-model simulation, for 10, 25, and 50 harmonics, respectively. At the bottom, the waveform resulted from transistor-level simulation.

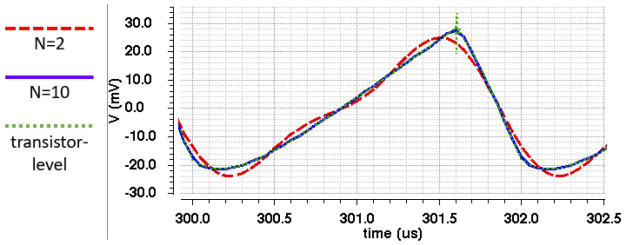

Fig. 14. Error voltage (V_{err}) ripple (total voltage minus average value) for the boost converter. Reconstructed waveforms, from the averaged-model simulation, with two and ten harmonics, respectively, and the waveform resulted from transistor-level simulation.

TABLE VII
RMS ERROR OVER ONE PERIOD OF RECONSTRUCTED BOOST WAVEFORM RIPPLES VERSUS COMPLETE WAVEFORM RIPPLE

Number of Harmonics N	V_{out}		V_{err}	
	vs. i_c	vs. i_p	vs. i_c	vs. i_p
1	10.5%	10.5%	9.7%	9.7%
2	6.2%	6.2%	3.9%	3.9%
10	3.3%	3.1%	1.1%	0.7%
25	2.9%	2.7%	1.1%	0.6%
50	2.7%	2.5%	1.1%	0.6%

2) output capacitance $C_{\text{out}=10\,\mu F}$, with parasitic ESR 10 mΩ. The ESL is not considered in this case, as it was not provided in the available output capacitor model.

Like the previous buck converter, the boost converter is implemented at transistor level, in the same technology.

The method for generating the output waveforms, described in the previous subsection for the buck converter, is applied in this subsection to the boost converter as well. Figs. 13 and 14 display the transistor-level and the reconstructed waveform ripples for the output voltage V_{out} and for the error voltage V_{err}, respectively. Then, Table VII shows quantitative results for the waveform reconstruction accuracy. Finally, Table VIII illustrates the runtime performance of the proposed method.

TABLE VIII
RUNTIME COMPARISON—BOOST CONVERTER

Model	Number of harmonics	Simulation time	Ripple calculation	Total time	Speedup
transistor-level	N/A	607s (TRAN)	N/A	607s	1x
averaged	N=1	1s (TRAN+AC)	1s	2s	300x
	N=2		1s	2s	300x
	N=10		2s	3s	200x
	N=25		11s	12s	50x
	N=50		47s	48s	13x

The waveform ripples are reconstructed based on the Fourier series expansion of the PWM switch cell signals, by referring to i_c and i_p, respectively. The rms errors presented in Table VII for V_{out} and V_{err} and calculated in the same way as for the buck converter show that referring to i_p provides slightly more accurate results. The reason is that, on the signal path, i_p is closer to the reconstructed signals. In the case of i_c or v_{cp}, additional distortion is introduced by the nonlinear behavior of the PWM switch cell model.

Fig. 13 shows the ripple of the output voltage V_{out}, reconstructed with a gradually increasing number of harmonics: 10, 25, and 50, respectively. With 25 harmonics, the generated waveform begins to look similar to the transistor-level waveform. This can be seen also from the rms error, which drops below 3% for 25 harmonics, as shown in Table VII. With 50 harmonics, the reconstructed waveform looks very close to the transistor-level one and the error drops to 2.5%. Even with 50 harmonics, the error is above 2%. There is a systematic error caused by the negative spike from the transistor-level waveform, as seen in Fig. 13. To account for such a spike, an impractically large number of harmonics would be needed.

Fig. 14 shows the waveform ripple for the error voltage V_{err} obtained from the transistor-level simulation and the waveform obtained using the proposed model with two and ten harmonics, respectively. With two harmonics, there is a visible difference to the transistor-level waveforms, indicated also by the rms error close to 2%, as shown in Table VII. With ten harmonics, the reconstructed waveform almost overlaps the transistor-level one. The rms error is 0.6% in this case. With further increases in the number of harmonics, the accuracy does not improve anymore, as seen in Table VII.

The numerical results of the runtime performance are summarized in Table VIII. For a fair comparison between the transistor-level simulation and the method proposed in this article and for a fair comparison with the buck converter from the previous subsection, a transient analysis over 2500 periods is applied to the boost converter. As the switching frequency is 500 kHz, the simulation time is 5 ms. Also, the ripples are reconstructed with a resolution of 1/400 of a period of 5 ns.

In this boost converter example, the CPU runtime of the transistor-level simulation is 607 s and 1.7M points are simulated. On the other hand, the transient analysis with the averaged model has a negligible runtime of 1 s. Only 144 points are simulated, meaning more than 10 000 less than in the transistor-level transient analysis. The open-loop ac analysis runtime, for getting the small-signal information, is also negligible. However, time is needed to reconstruct the waveform ripple, time which

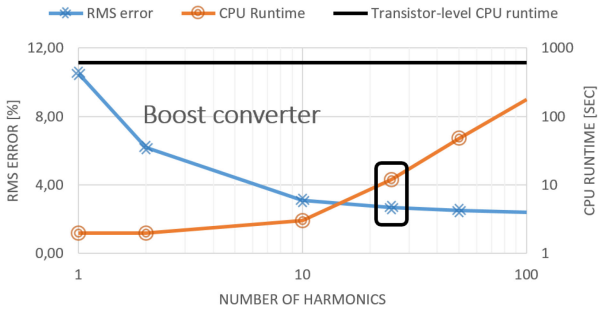

Fig. 15. Tradeoff between accuracy (measured by the rms error) and computational effort (measured by the CPU runtime), both in relation to the number of harmonics, for the boost converter. A typical tradeoff between accuracy and CPU effort is marked at 25 harmonics.

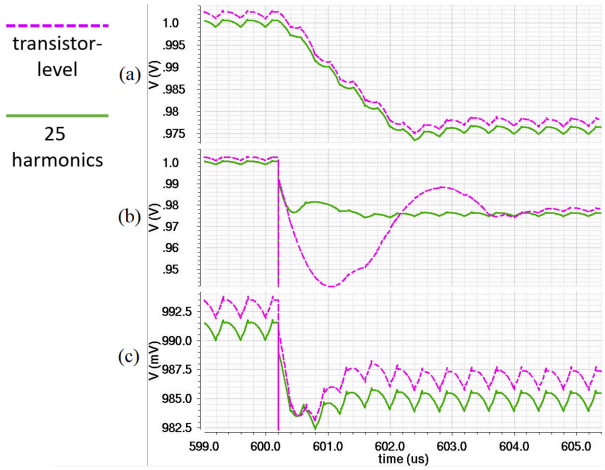

Fig. 16. Transient behavior of the buck converter for load current variation: comparison between the transistor-level waveform and the waveform reconstructed with 25 harmonics. The load current variation is: (a) slow and large, (b) fast and large, and (c) fast and small.

increases with the number of harmonics. For V_{out}, the loss of accuracy for the reconstructed waveform with 25 harmonics is below 3%, according to Table VII, while achieving a 50× speedup compared to the transistor-level simulation, as shown in Table VIII. With 50 harmonics, the accuracy is improved, as the error decreases to 2.5%, but the speedup also decreases to 13×.

The results from Tables VII and VIII are graphically illustrated in Fig. 15, showing for the buck converter the tradeoff between accuracy (measured by the rms error) and computational effort (measured by the CPU runtime), both in relation to the number of harmonics.

Monte Carlo analysis is a situation, where the method proposed in this article brings a significant CPU time reduction. According to the results from Tables VII and VIII and Fig. 15, with 25 harmonics, a good tradeoff can be achieved when reconstructing the ripple waveform for the output voltage. With this choice, the total runtime for 100 simulations decreases from approximately 18 h and 30 min in the transistor-level approach to approximately 20 min with the proposed method.

C. Dynamic Behavior

The previous experimental results have demonstrated the method's performance in steady-state conditions. However, the method is also applicable in dynamic conditions, e.g., in the case of a load step transient. The following results will illustrate the method's performance and limitation in such conditions: a good accuracy is obtained for slow and/or small variations of the load current (in other words, in quasi-steady-state conditions).

Fig. 16 shows the output voltage V_{out} of the buck converter. In three load current variation scenarios, the waveform simulated at the transistor level and the waveform reconstructed with 25 harmonics are compared. The results are illustrated for increasing load current. For decreasing load current, very similar results are obtained.

First, Fig. 16(a) shows the behavior for a large and slow load variation. The load increases from 1 to 3 A in a time equal to five switching periods. The reconstructed waveform reproduces the transistor-level waveform with good accuracy. The plot shows a systematic error of approximately 2 mV. This error is caused by the limitations of the equivalent averaged model of the PWM switch cell [7] and not by the ripple reconstruction. Moreover, this error is more than 10× smaller than the V_{out} variation due to load regulation (approximately 2 mV for load currents from 1 to 3 A). The variation of V_{out} with the operating conditions (e.g., load current) is a consequence of the limited loop gain (46 dB or 200) of this buck converter implementation. The boost converter presented in this article uses a different compensation method for the error amplifier and has a loop gain of 100 dB (or 100k). This makes the V_{out} regulation much more precise and is the reason why the averaged model does not suffer from the steady-state error in the boost converter. Therefore, the steady-state error is highly dependent on the circuit topology.

Second, in the scenario shown in Fig. 16(b), the load current variation is large and fast. The load increases from 1 to 3 A in a time much smaller than the switching period. In this case, the error is significant during the settling, reaching up to 40 mV in magnitude. The error is again mainly caused by the limitations of the averaged PWM switch cell model. In general, large-signal averaged models do not work well under dynamic conditions with large and sudden variations, since averaged models use an "averaged and continuous" representation of the original function over several periods [7], [27].

Third, in Fig. 16(c), there is again a fast change in the load, but this time the current variation is smaller (0.5 A instead of 2 A). The method shows here a good accuracy, with an error magnitude within 2 mV.

Fig. 17 quantitatively describes the meaning of "slow variations" and "small variations" for the buck converter example. For a fair comparison, the systematic steady-state error (approximately 2 mV) is subtracted from the total error. First, Fig. 17(a) shows that, for the maximum considered current variation of 2 A, the proposed method shows a good accuracy for rise/fall times starting from five switching periods. Second, Fig. 17(b) shows that, for fast load variations (the rise/fall time is much smaller than the switching period), a good accuracy is obtained for load steps up to 0.5 A.

The theory of the method was developed in steady-state conditions. However, it holds also under dynamic behavior, in quasi-steady-state conditions.

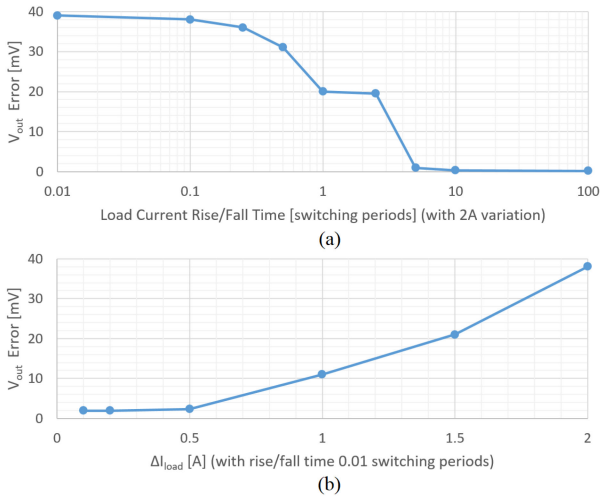

Fig. 17. Accuracy of proposed method versus transistor-level simulation in dynamic conditions: maximum error magnitude (minus the systematic error from steady state) in simulating the buck converter V_{out} with respect to (a) rise/fall time and (b) magnitude of load current step, respectively.

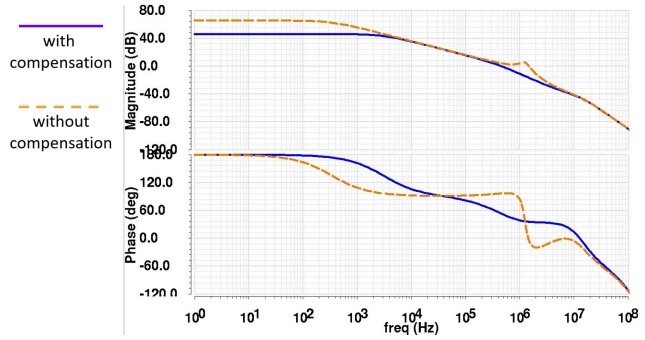

Fig. 18. Frequency response of buck converter with and without compensation ramp. The circuit with compensation ramp has a loop gain of 46 dB.

D. Stability

As most practical dc–dc converters include control loops, stability needs to be accounted for in the design process. In current-mode controlled dc–dc converters, subharmonic stability is a major issue. This is the reason why a compensation ramp is often needed in such converter designs [7].

The presented method is able to capture subharmonic oscillations through the averaged model. The state-of-the-art averaged model includes the capacitor C_s, introduced specifically for this purpose, as described in Section III-B. When present, oscillations are revealed in the frequency response, as well as in the transient waveforms. This is illustrated in the following for the buck converter example.

First, the frequency response is compared for the converter with and without compensation ramp in Fig. 18. When no such ramp is applied, the magnitude shows, at $F_{\text{sw}}/2 = 1.25$ MHz, a peak specific to subharmonic oscillations [7], which raises the gain above 0 dB at frequencies around $F_{\text{sw}}/2$. The unity gain frequency is about 1.5 MHz. The phase margin of -5° reveals instability. Adding the compensation ramp damps the peak and so removes the subharmonic oscillations. The unity-gain frequency decreases to 450 kHz and the phase margin of

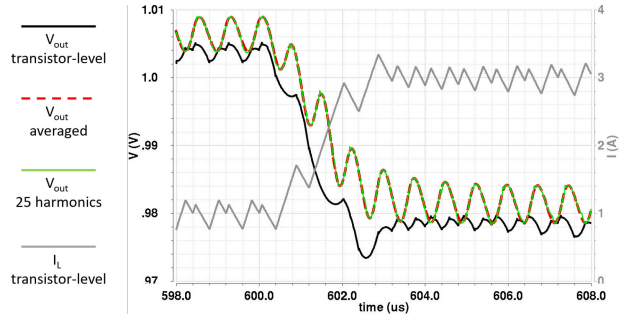

Fig. 19. Transient waveforms of buck converter with subharmonic oscillations.

53° indicates a stable loop. In this way, the averaged model, having the compensation ramp S_a as a parameter (see Fig. 5), can be used to design the compensation ramp of the circuit.

Second, the subharmonic oscillations are captured in the transient waveforms (of the converter without compensation ramp), in the steady state, as well as in dynamic conditions, as shown in Fig. 19. The output voltage obtained with the averaged model oscillates with the expected frequency, $F_{\text{sw}}/2 = 1.25$ MHz, revealing the instability of the circuit, in agreement with the transistor-level waveforms, which show subharmonic oscillations as well. The limitation of the proposed method is the inability to correctly predict the amplitude and the shape of the waveforms. The averaged model produces an oscillating instead of a constant (in the steady state) waveform (as in stable conditions). For V_{out}, applying the Fourier-series-based reconstruction produces a waveform nearly overlapping the index-0 waveform resulted from the averaged model, because the amplitude of the subharmonic sine wave is much larger than the harmonic ripple.

VII. Conclusion

A multiharmonic modeling and simulation technique for low-power PWM dc–dc converters was presented. The technique is based on the large-signal averaged modeling of the PWM switch cell and the Fourier series expansion of the voltages and currents at the switch cell terminals. The distinguishing feature of this technique is generality. With no additional modeling effort, it is applicable to a wide range of dc–dc converters, and it supports any parasitic element, any surrounding circuitry, and any number of harmonics. Circuits for dynamic characterization of the PWM switch cell parameters were presented as well and brought together with the PWM switch cell averaged model and the surrounding circuitry into the same testbench. The proposed method was illustrated for a buck and for a boost converter and achieved a speedup of one order of magnitude over the transistor-level model, with a loss of accuracy below 3%. The method works with a good accuracy in the steady state, as well as in dynamic conditions with slow and/or small variations. The method correctly predicts subharmonic instability.

References

[1] R. D. Middlebrook and S. Ćuk, "A general unified approach to modelling switching-converter power stages," *Int. J. Electron. Theor. Exp.*, vol. 42, no. 6, pp. 521–550, 1977.

[2] A. Davoudi, J. Jatskevich, and T. De Rybel, "Numerical state-space average-value modeling of PWM dc-dc converters operating in DCM and CCM," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1003–1012, Jul. 2006.
[3] J. Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein, and R. M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 482–492, Jul. 2001.
[4] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch—Part I: Continuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 490–496, May 1990.
[5] V. Vorpérian, "Simplified analysis of PWM converters using model of PWM switch—Part II. Discontinuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 497–505, May 1990.
[6] Y. Amran, F. Huliehel, and S. Ben-Yaakov, "A unified SPICE compatible average model of PWM converters," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 585–694, Oct. 1991.
[7] C. Basso, *Switch-Mode Power Supplies*. New York, NY, USA: McGraw-Hill, 2014.
[8] D. Tannir, Y. Wang, and P. Li, "Accurate modeling of nonideal low-power PWM dc-dc converters operating in CCM and DCM using enhanced circuit averaging techniques," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 21, no. 4, 2016, Art. no. 61.
[9] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 251–259, Apr. 1991.
[10] V. A. Caliskan, O. Verghese, and A. M. Stankovic, "Multifrequency averaging of DC/DC converters," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 124–133, Jan. 1999.
[11] D. Maksimović, A. M. Stanković, V. J. Thottuvelil, and G. C. Verghese, "Modeling and simulation of power electronic converters," *Proc. IEEE*, vol. 89, no. 6, pp. 898–912, Jun. 2001.
[12] J. M. Noworolski and S. R. Sanders, "Generalized in-plane circuit averaging," in *Proc. IEEE 6th Annu. Appl. Power Electron. Conf. Expo.*, 1991, pp. 445–451.
[13] Y. Wang, D. Gao, D. Tannir, and P. Li, "Multi-harmonic nonlinear modeling of low-power PWM dc-dc converters operating in CCM and DCM," in *Proc. Des., Autom. Test Eur. Conf. Exhib.*, 2016, pp. 409–414.
[14] Y. Wang *et al.*, "Multiharmonic small-signal modeling of low-power PWM dc-dc converters," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 22, no. 4, 2017, Art. no. 68.
[15] F. Misoc, M. M. Morcos, and J. Lookadoo, "Fourier-series models of DC–DC converters," in *Proc. North Amer. Power Symp.*, 2006, pp. 193–199.
[16] R. Trinchero, P. Manfredi, I. S. Stievano, and F. G. Canavero, "Steady-state analysis of switching converters via frequency-domain circuit equivalents," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 63, no. 8, pp. 748–752, Aug. 2016.
[17] E. Setiawan, T. Hirata, and I. Hodaka, "Accurate symbolic steady state modeling of buck converter," *Int. J. Elect. Comput. Eng.*, vol. 7, no. 5, pp. 2374–2381, 2017.
[18] M. Forouzesh, Y. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.
[19] R. Trinchero, I. S. Stievano, and F. G. Canavero, "Steady-state analysis of switching power converters via augmented time-invariant equivalents," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5657–5661, Nov. 2014.
[20] J. W. van der Woude, W. L. de Koning, and Y. Fuad, "On the periodic behavior of PWM dc-dc converters," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 585–595, Jul. 2002.
[21] Y. Yan, F. C. Lee, and P. Mattavelli, "Unified three-terminal switch model for current mode controls," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4060–4070, Sep. 2012.
[22] *SIMetrix/SIMPLIS—User's Manual*, Simetrix Technologies Ltd., Thatcham, U.K., 2015.
[23] S. Tian, F. C. Lee, J. Li, Q. Li, and P. Liu, "A three-terminal switch model of constant on-time current mode with external ramp compensation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7311–7319, Oct. 2016.
[24] O. A. Beg, H. Abbas, T. T. Johnson, and A. Davoudi, "Model validation of PWM dc–dc converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7049–7059, Sep. 2017.
[25] A. G. O. Dela-Cruz, C. C. Li, C. E. S. Tomboc, J. K. Ty, and R. Y. Yap, "CMOS implementation of hysteretic controller for a dc-to-dc buck converter using 0.35 um library," in *Proc. DLSU Res. Congr.*, 2018.
[26] T. C. Neugebauer and D. J. Perreault, "Computer-aided optimization of dc/dc converters for automotive applications," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 775–783, May 2003.
[27] G. Migoni, M. E. Romero, F. Bergero, and E. Kofman, "A mixed modeling approach for efficient simulation of PWM switching mode power supplies," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9758–9767, Oct. 2019.

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