Evaluation of Different Si/SiC Hybrid Three-Level Active NPC Inverters for High Power Density

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***Abstract*—Compared with full-SiC MOSFETs converters, the hybrid utilization of Si/SiC converters is an alternative approach to achieve the tradeoff between performance and cost. A systematic method is proposed to generate 2-SiC and 4-SiC hybrid three-level active neutral-point-clamped (3L-ANPC) inverter topologies from two types of switching cells based on the arrangement of freewheeling paths. The 2-SiC hybrid 3L-APNC inverter and the 4-SiC hybrid 3L-ANPC inverter are analyzed in detail with switching states and modulation strategies given. The power losses are quantitatively compared between the 2-SiC hybrid 3L-ANPC inverter and the 4-SiC hybrid 3L-ANPC inverter. The junction operating temperatures of active switches in different hybrid 3L-ANPC inverters are also estimated. With the same specifications and switching device parameters, the maximum output power of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I is almost 1.47 times than that of the 2-SiC hybrid 3L-ANPC inverter. A universal prototype for the full-SiC scheme, the full-IGBT scheme, and different Si/SiC hybrid schemes is built to evaluate these topologies at conversion efficiency and thermal characteristics. Experimental results and analysis show that the full-SiC 3L-ANPC inverter has the highest efficiency, whereas the 2-SiC hybrid 3L-ANPC inverter has the best cost performance. Further, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I has better thermal balance characteristic than that of the 2-SiC hybrid 3L-ANPC inverter, which shows significant superiority in high power density applications.**

***Index Terms*—3L-ANPC, inverter, multilevel inverter, SiC MOSFET, wide-bandgap devices.**

Manuscript received January 31, 2019; revised June 24, 2019 and October 16, 2019; accepted December 25, 2019. Date of publication December 29, 2019; date of current version April 22, 2020. This work was supported in part by the National Natural Science Foundation of China under Grants 51677054 and 51807176, in part by the 16th Six Talent Peaks Project in Jiangsu Province under Grant TD-XNY-001, and in part by the 111 project under Grant B14022. Recommended for publication by Associate Editor J. Biela. *(Corresponding authors: Feng Wu; Chushan Li.)*

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Digital Object Identifier 10.1109/TPEL.2019.2962907

I. Introduction

VOLTAGE source inverters are widely used in the grid-tied photovoltaic (PV) systems, motor drives for electric vehicles, and power supplies for modern data centers, etc. In these industrial applications, the efficiency as well as the power density is expected to be as high as possible, which means that the achievement of lower hardware cost. However, the power density of conventional voltage source inverters based on silicon (Si) devices is hard to be further improved, since the switching frequency of Si IGBTs is limited by their high switching losses. Therefore, conventional Si-based inverters are undergoing significant changes with the usage of wide bandgap semiconductor devices, such as silicon carbide (SiC), due to their higher switching frequency capability [1]–[5]. In the grid-tied PV systems, full-SiC MOSFETs five-level (5L) T-Type inverters were proposed to achieve extremely high efficiency [6]–[8]. In aerospace and more electric aircraft applications, an *LCL* filter two-level inverter with full-SiC MOSFETs was proposed to achieve high efficiency and high power density [9], [10]. However, the high price is always a big issue that slows down the pace of the SiC device entering the commercial market [11]. Therefore, compared with the full-SiC MOSFETs converters, the hybrid utilization of Si/SiC converters is an alternative approach to achieve the tradeoff between performance and cost.

A discrete package-based hybrid switch consisting of an Si IGBT in parallel with a SiC MOSFET was proposed in recent literature [12]–[14]. It facilitates the soft switching of the Si IGBT and enables the hybrid switch as a high-frequency switch. To reduce the cost, a hybrid switch with a high-current main Si IGBT and a low-current auxiliary SiC MOSFET connected in parallel was proposed in [15]. Since the low-current auxiliary SiC MOSFET may affect the thermal characteristic, short-circuit ability, and power losses of the hybrid switch, the Si/SiC current ratio of this hybrid switch has been further investigated [16]. Moreover, to keep the junction temperatures of both the SiC MOSFET and Si IGBT within their rated temperature ranges, and to minimize the total power losses, an optimal gate control pattern of this hybrid switch was proposed in [17]. The gate control pattern also depends on the different Si/SiC current ratios. As a result, the gate control pattern should be carefully designed.

In recent years, the circuit-based hybrid Si/SiC converters were reported to achieve an improved performance and cost tradeoff as well [18]–[23]. A fault-tolerant T-type multilevel

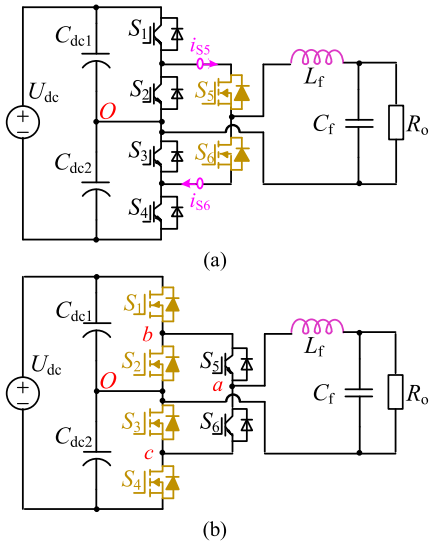

Fig. 1. 3L-ANPC inverters with hybrid Si/SiC switching devices. (a) 2-SiC hybrid 3L-ANPC topology. (b) 4-SiC hybrid 3L-ANPC topology.

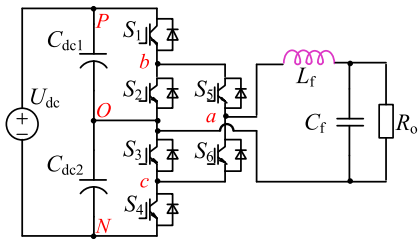

Fig. 2. 3L-ANPC inverter with full-IGBTs.

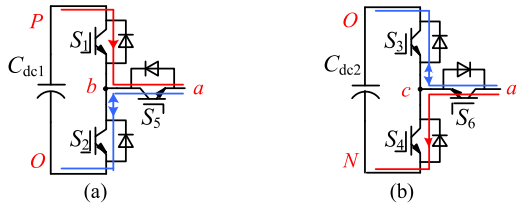

Fig. 3. ANPC switching cells. (a) P-ANPC switching cell. (b) N-ANPC switching cell.

inverter topology by adding a redundant SiC leg was proposed in [18]. The redundant SiC leg provides a fault-tolerant ability to any open-circuit and certain short-circuit switching faults. However, the conduction losses of the path from the neutral point to phase leg midpoint are increased. The three-level (3L) active-neutral-point-clamped (ANPC) converter was proposed to overcome the unequal semiconductor loss distribution of conventional NPC converters [24], [25]. In [11], a 3L-ANPC converter based on a hybrid utilization of SiC MOSFETs and Si-active switches was proposed. Instead of using the full-SiC MOSFETs, it consists of four Si-active switches and only two SiC MOSFETs, as shown in Fig. 1(a). A dedicated modulation strategy of the 3L-ANPC topology is also proposed to let the SiC MOSFETs operate with high frequency. The Si-active switches operate at low frequency by using redundant zero states. As a result, the maximum efficiency is up to 99% at the 45 kHz switching frequency. But it leads to the unequal loss distribution for the 2-SiC hybrid 3L-ANPC converter. In [22] and [23], a three-phase 3L-ANPC converter was developed for megawatt (MW) hybrid-electric propulsion system. There are two Si-active switches and four SiC MOSFETs in each phase leg. Due to the high output power, the stray inductance in commutation loops should be considered. Large and small commutation loops with different modulation schemes were well discussed in detail. To lower the influence of the stray inductance and the voltage overshoot, an improved modulation strategy with small commutation loops was proposed in [22]. However, quantitative evaluation of the 4-SiC hybrid 3L-ANPC inverter and the 2-SiC hybrid 3L-ANPC inverter are yet to be explored in terms of efficiency, thermal balance, and power density, which could provide the instructions for engineers to select preferred Si/SiC hybrid scheme in accordance with different requirements.

On the other hand, many power converters, such as dc-dc converters, voltage-source inverters, current-source inverters, and multilevel inverters, have been investigated from the basic switching cells to constructing the topology [26]–[29]. However, both of the 4-SiC hybrid 3L-ANPC topology and the 2-SiC hybrid 3L-ANPC topology have not been analyzed from the point of view of Si/SiC hybrid switching cells. The topology generation method of Si/SiC hybrid 3L-ANPC inverters is yet to be revealed as well.

This article is organized as follows. In Section II, a systematic method is proposed to generate 4-SiC and 2-SiC hybrid 3L-ANPC inverter topologies from two types of Si/SiC hybrid switching cells based on the arrangement of freewheeling paths. Evaluation of the 4-SiC hybrid 3L-ANPC inverter with different modulation strategies is presented in Section III. The calculated power losses and the estimated junction temperatures of the 4-SiC hybrid 3L-ANPC inverter and the 2-SiC hybrid 3L-ANPC inverter are addressed and compared. In Section IV, experimental results are given with efficiency and junction temperature comparison, and finally, Section V concludes this article.

II. Topology Generation of 2-SiC Hybrid and 4-SiC Hybrid 3L-ANPC Inverters

A. Idea of 3L Si/SiC Hybrid Switching Cells

The topology of the 3L-ANPC inverter with full-IGBTs is shown in Fig. 2. The positive output current condition at the positive half cycle is taken as an example for analysis.

As well known, the 3L-ANPC inverter can be generated by a positive ANPC (P-ANPC) switching cell and a negative ANPC (N-ANPC) switching cell. Both of the P-ANPC switching cell and the N-ANPC switching cell are depicted in Fig. 3.

Taking the positive half cycle as an example for analysis, the inductor current is flowing through S_1 and S_5 in the active mode. In the freewheeling mode, the inductor current has two potential freewheeling paths, which depends on the employed modulation strategy. The first inductor current freewheeling path is formed by S_2 and S_5, whereas the second inductor current freewheeling path is formed by S_4 and S_6. Therefore, whether the 3L-ANPC

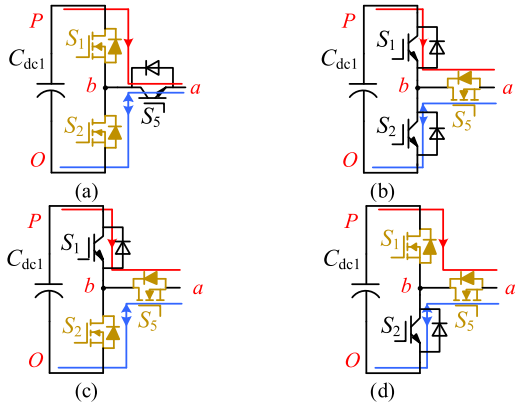

Fig. 4. Four types of the Si/SiC hybrid P-ANPC switching cells. (a) Type-I. (b) Type-II. (c) Type-III. (d) Type-IV.

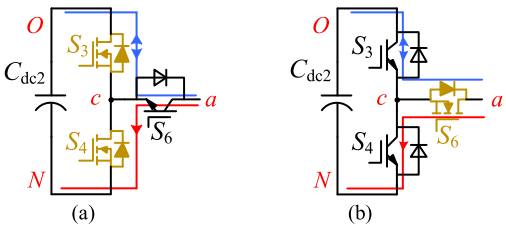

Fig. 5. Two significant types of the Si/SiC hybrid N-ANPC switching cells. (a) Type-I. (b) Type-II.

inverter is operating in the active modes or in the freewheeling modes, the inductor current has to be flowing through two series-connected IGBTs. Either of series-connected IGBTs can be replaced by a SiC MOSFET with high-frequency switching. Another IGBT is operated with low-frequency switching. As a result, for the P-ANPC switching cell, there are four types of Si/SiC hybrid P-ANPC switching cells, as illustrated in Fig. 4. In Fig. 4(c), there are two series-connected SiC MOSFETs in the inductor current freewheeling path. The switch S_5 is also located in the inductor current active path. Thus, for the switch S_2, using an IGBT instead of a SiC MOSFET is an effective way to reduce costs. As a result, the modified switching cell will be the same as the Si/SiC hybrid switching cell shown in Fig. 4(b). In Fig. 4(d), there are two series-connected SiC MOSFETs in the inductor current active path. The switch S_5 is also located in the inductor current freewheeling path. Thus, for the switch S_1, using an IGBT instead of a SiC MOSFET is an effective way to reduce costs. The modified switching cell will also be the same as the Si/SiC hybrid switching cell shown in Fig. 4(b). As a result, two types of P-ANPC switching cells, as depicted in Fig. 4(a) and (b), are well-accepted Si/SiC hybrid configurations. According to these two types of Si/SiC hybrid P- ANPC switching cells, two types of Si/SiC hybrid N-ANPC switching cells are proposed in Fig. 5.

B. 2-SiC Hybrid 3L-ANPC Inverter

From the above analysis, the 2-SiC hybrid 3L-ANPC inverter topology, as depicted in Fig. 1(a), can be generated by a type-II Si/SiC hybrid P-ANPC switching cell and a type-II Si/SiC hybrid N-ANPC switching cell. The modulation strategy of the 2-SiC hybrid 3L-ANPC inverter is shown in Fig. 6.

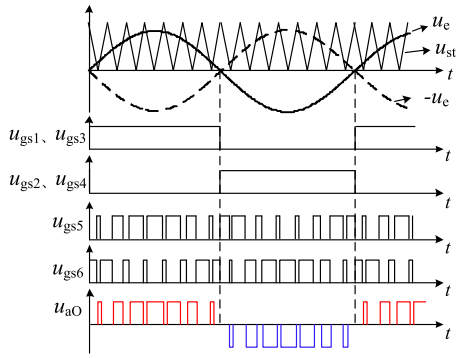

Fig. 6. Waveforms of the 2-SiC hybrid 3L-ANPC inverter modulation strategy.

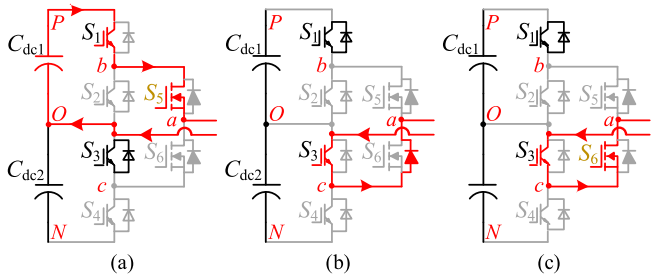

Fig. 7. Demonstration of commutation process at the positive half cycle with the positive output current. (a) $u_{aO} = 0.5U_{dc}$. (b) Deadtime. (c) $u_{aO} = 0$.

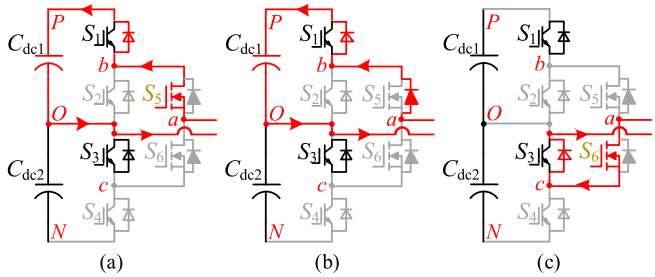

Fig. 8. Demonstration of commutation at the positive half cycle with the negative output current. (a) $u_{aO} = 0.5U_{dc}$. (b) Deadtime. (c) $u_{aO} = 0$.

In Fig. 6, u_e is the modulation signal, and u_{st} is the carrier signal. u_{gs1} to u_{gs6} represent the gating signals of the switches S_1 to S_6, respectively. u_{aO} is the voltage between terminal a and terminal O. u_{aO} has three levels, $0.5U_{dc}$, 0, and $-0.5U_{dc}$. It can be seen that during the operation, IGBT pairs S_1–S_3 and S_2–S_4 always share the same gating signals, respectively. These two IGBT pairs are low-frequency switching complementarity. Further, the SiC MOSFET S_5 and S_6 are high-frequency switching complementarity. To avoid the shoot-through issue, the deadtime should be set between the gating signals of S_5 and S_6.

The detailed commutation process under both the positive output current and the negative current conditions are demonstrated in Figs. 7 and 8. Under the positive output current condition, when u_{aO} is equal to $0.5U_{dc}$, the inductor current is flowing through S_1 and S_5, as shown in Fig. 7(a). The turning OFF of S_5 will force the inductor current commutate to S_3 and the

TABLE I
Si/SiC HYBRID 3L-ANPC SWITCHING PATTERNS

States	S_1	S_2	S_3	S_4	S_5	S_6	u_{aO}
P	1	0	1	0	1	0	$0.5U_{dc}$
$OU1$	0	1	0	0	1	0	0
$OU2$	0	1	1	0	1	0	0
$OL1$	0	0	1	0	0	1	0
$OL2$	0	1	1	0	0	1	0
N	0	1	0	1	0	1	$-0.5U_{dc}$

body diode of S_6, as displayed in Fig. 7(b). The turning ON of S_6 will let S_6 operate under synchronous rectifier mode, as depicted in Fig. 7(c), and the ZVS of S_6 is achieved. However, it should be noted that the inductor current flowing through S_3 and the body diode of S_6 will be commutated to S_1 and S_5 via a large commutation loop, and vice versa. The switch S_5 will suffer from hard turn-OFF in the large commutation loop by turning OFF S_5, and there will be voltage overshoot on S_5. The body diode of S_6 will suffer from hard turn-OFF in the large commutation loop by turning ON S_5. However, thanks to the SiC material, the reverse recovery current is relatively low, and the overshoot voltage on S_6 is also relatively low. The commutation process under the negative output current condition is illustrated in Fig. 8. In Fig. 8(a), the inductor current is flowing through the antiparallel diode of S_1 and S_5 channel. The turning OFF of S_5 will force the inductor current commutate to its body diode as displayed in Fig. 8(b). The turning ON of S_6 will let the inductor current commutate to S_6 and antiparallel diode of S_3, as shown in Fig. 8(c). Although the antiparallel diode of S_1 is turned OFF during this interval, S_1 is still ON and the OFF-state voltage on the antiparallel diode of S_1 is zero. It indicates that there is no reverse recovery loss on the antiparallel diode of S_1.

Based on the above analysis, it can be concluded that the four Si IGBTs only have conduction losses. Thus, the switching losses could be significantly reduced by using two SiC MOSFETs. The 2-SiC hybrid 3L-ANPC inverter can achieve the same switching loss performance compared with the full-SiC MOSFETs 3L-ANPC inverter. However, since all the switching events are moved to the SiC MOSFETs, the thermal characteristic of this topology is highly unbalanced.

III. EVALUATION OF 4-SiC HYBRID SCHEMES WITH DIFFERENT MODULATION STRATEGIES

From the analysis in Section II-A, the 4-SiC hybrid 3L-ANPC inverter topology, as depicted in Fig. 1(b), can be generated by a type-I Si/SiC hybrid P-ANPC switching cell and a type-I Si/SiC hybrid N-ANPC switching cell. Since either inductor current active paths or freewheeling paths have one independent SiC MOSFET, two modulation strategies could be derived by using redundant switching states. Table I lists some of the switching states for 3L-ANPC that are usually utilized.

For the 4-SiC hybrid 3L-ANPC inverter, taking the positive half cycle as an example, the inductor freewheeling path consists of S_2 and S_5, which is different from the 2-SiC hybrid 3L-ANPC inverter. On the other hand, S_3 can be operated with variable gating signals, which leads to different modulation strategies.

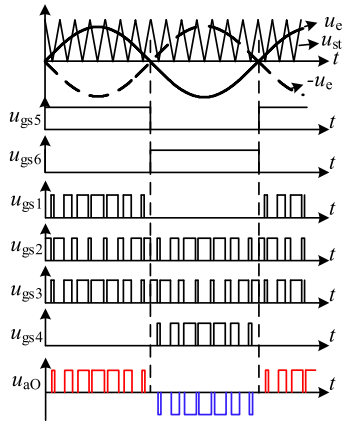

Fig. 9. Waveforms of the 4-SiC hybrid 3L-ANPC with modulation strategy I.

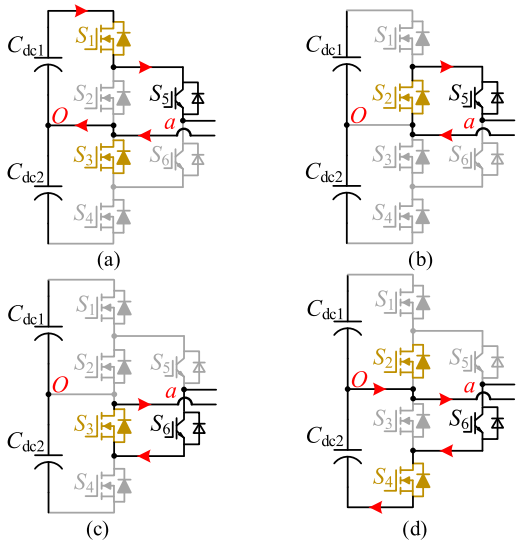

Fig. 10. Equivalent circuits of switching states. (a) State #1. (b) State #2. (c) State #3. (d) State #4.

A. Modulation Strategy I for 4-SiC Hybrid 3L-ANPC Inverter

The states P, $OU1$, $OL1$, and N in Table I are used as switching states in this strategy. The waveforms of the modulation strategy I are illustrated in Fig. 9. The SiC MOSFET S_2 and S_3 are high-frequency switching complementarity. At the positive half cycle, the gating signals of S_1 and S_3 are the same. S_2 and S_4 share the same gating signals at the negative half cycle. To avoid the shoot-through issue, the deadtime should be set between complementary gating signals. The equivalent circuits of switching states are shown in Fig. 10.

1) *State #1* [*Refer to* Fig. 10(a)]. State P in Table I, $u_{aO} = 0.5U_{dc}$. S_1, S_3, and S_5 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 10(a). Since S_3 is turned ON, the blocking voltages of S_4 and S_6 are clamped to $0.5U_{dc}$.

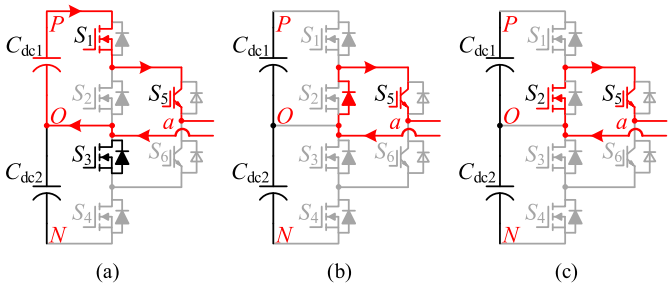

Fig. 11. Demonstration of commutation process between the *P* state and the *OU1* state under the positive output current condition. (a) $u_{aO} = 0.5U_{dc}$. (b) Deadtime. (c) $u_{aO} = 0$.

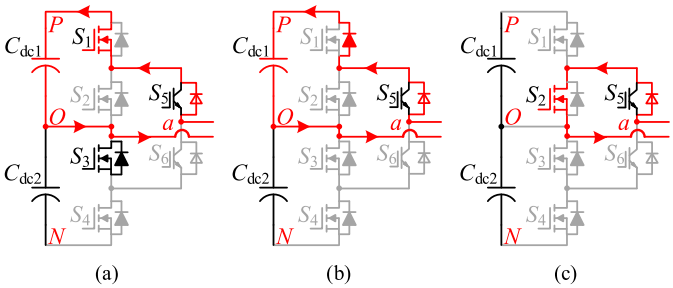

Fig. 12. Demonstration of commutation process between the *P* state and the *OU1* state under the negative output current condition. (a) $u_{aO} = 0.5U_{dc}$. (b) Deadtime. (c) $u_{aO} = 0$.

2) *State #2* [*Refer to* Fig. 10(b)]. State *OU*1 in Table I, $u_{aO} = 0$. S_2 and S_5 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 10(b), which let S_3 connect parallel with S_6, and then connect series with S_4. Therefore, the blocking voltages of S_3, S_4, and S_6 are determined by their junction capacitances.
3) *State #3* [*Refer to* Fig. 10(c)]. State *OL*1 in Table I, $u_{aO} = 0$. S_3 and S_6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 10(c), which let S_2 connect parallel with S_5, and then connect series with S_1. Therefore, the blocking voltages of S_1, S_2, and S_5 are determined by their junction capacitances.
4) *State #4* [*Refer to* Fig. 10(d)]. State *N* in Table I, $u_{aO} = -0.5U_{dc}$. S_2, S_4, and S_6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 10(d). Since S_2 is turned ON, the blocking voltages of S_1 and S_5 are clamped to $0.5U_{dc}$.

For the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I, the detailed commutation process under both the positive output current and the negative output current conditions are demonstrated in Figs. 11 and 12. Further, the relevant blocking voltages diagram of active switches is shown in Fig. 13.

As shown in Fig. 11(a), the inductor current is flowing through S_1 and S_5. In Fig. 11(b), the turning OFF of S_1 and S_3 will force the inductor current to commutate from S_1 to the body diode of S_2. During the deadtime, S_3 is parallel-connected with S_6. Thus, as illustrated in Fig. 13, the blocking voltage of S_3 is increased to U_{paral}, whereas the blocking voltages of S_4 and S_6

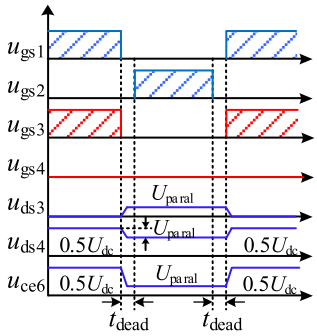

Fig. 13. Blocking voltage diagram of active switches with modulation strategy I.

are decreased to ($0.5U_{dc}$-U_{paral}) and U_{paral}, respectively. As a result, charging and discharging losses of junction capacitors are generated during this interval. The value of U_{paral} depends on the junction capacitances of the switches S_3, S_4, and S_6. As depicted in Fig. 11(c), the turning ON of S_2 will let S_2 operate under synchronous rectifier mode, and the ZVS of S_2 is achieved. In fact, the junction capacitance of the switch is variable with its blocking voltage. However, to simplify the analysis and calculation, the junction capacitance is regarded as a constant value in the following analysis.

When the output voltage is in phase with the inductor current, the commutation under the positive output current condition is the same as demonstrated in Fig. 11. Otherwise, the commutation under the negative output current condition is shown in Fig. 12. In Fig. 12(a), the inductor current is flowing through S_1 and antiparallel diode of S_5. The turning OFF of S_1 and S_3 will force the inductor current to commutate from S_1 channel to its body diode as displayed in Fig. 12(b). The turning ON of S_2 will let the inductor current commutate to S_2, as depicted in Fig. 12(c). In Fig. 12(c), S_3 is parallel-connected with S_6. Thus, the blocking voltages of S_3, S_4, and S_6 are changed and dependent on their junction capacitances. Although S_4 and S_6 are turned-OFF at the positive half cycle, the varied voltages of their junction capacitors lead to switching losses in S_3 and S_1, respectively.

From the above analysis, it can be concluded that the two Si IGBTs have only conduction losses. Thus, the switching loss could be reduced by using four SiC MOSFETs as well. Compared with the 2-SiC MOSFETs 3L-ANPC inverter, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I can achieve the same switching losses and potential better thermal balance characteristic.

B. Modulation Strategy II for 4-SiC Hybrid Topology

The states *P*, *OU*2, *OL*2, and *N* in Table I are selected as switching states in this strategy. The waveforms of modulation strategy II are depicted in Fig. 14. At the positive half cycle, SiC MOSFET S_1 and S_2 are high-frequency switching complementarity. The SiC MOSFET S_3 and S_4 are high-frequency switching complementarity at the negative half cycle. To avoid the shoot-through issue, the deadtime should be set between complementary gating signals. Compared with the modulation

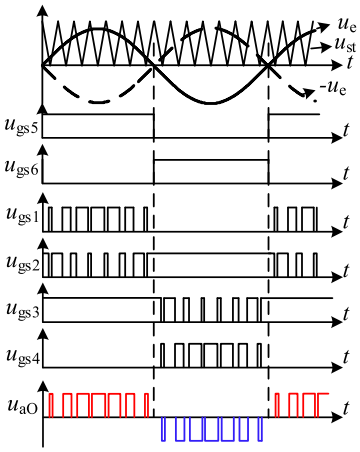

Fig. 14. Waveforms of modulation strategy II.

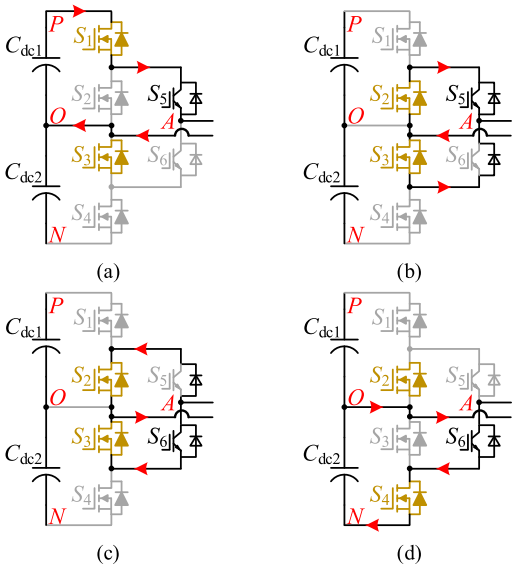

Fig. 15. Equivalent circuits of switching states. (a) State #1. (b) State #2. (c) State #3. (d) State #4.

strategy I, the switch S_3 is ON during the positive half cycle, and the switch S_2 is ON during the negative half cycle. The equivalent circuits of switching states are shown in Fig. 15.

The positive half cycle is taken as an example for analysis, switching state #1 of modulation strategy II is the same as that of the modulation strategy I in Fig. 10(a). As shown in Fig. 15(b), since S_3 is ON, the blocking voltage of S_6 is equal to 0. Apparently, in such a *OU*2 state, there are two freewheeling paths for conducting the inductor current, either through S_2 and S_5, or through S_3 and the antiparallel diode of S_6. The inductor current sharing of these two freewheeling paths depends on their ON-state voltages.

For the 4-SiC hybrid 3L-ANPC inverter with modulation strategy II, the detailed commutation under the positive output current condition is demonstrated in Fig. 16, and the relevant blocking voltage diagram of active switches is depicted in Fig. 18. The turning OFF of S_1 will force the inductor current to commutate from S_1 to the body diode of S_2, as displayed in

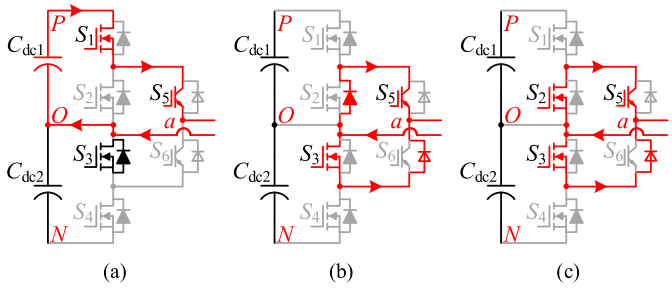

Fig. 16. Demonstration of commutation process between the *P* state and the *OU2* state under the positive output current condition. (a) $u_{aO} = 0.5U_{dc}$. (b) Deadtime. (c) $u_{aO} = 0$.

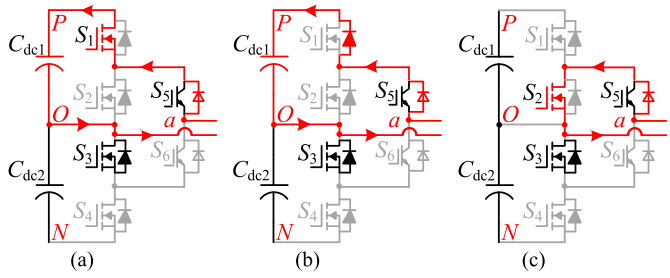

Fig. 17. Demonstration of commutation process between the *P* state and the *OU2* state under the negative output current condition. (a) $u_{aO} = 0.5U_{dc}$. (b) Deadtime. (c) $u_{aO} = 0$.

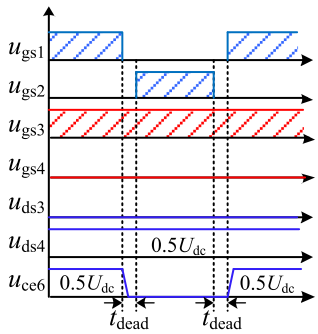

Fig. 18. Blocking voltage diagram of active switches with modulation strategy II.

Fig. 16(b). Since S_3 is ON, as shown is Fig. 18, the blocking voltage of S_6 is decreased from $0.5U_{dc}$ to zero, and the junction capacitor discharging loss is generated. The turning ON of S_2 will let S_2 operate under synchronous rectifier mode, and the ZVS of S_2 is also achieved, as illustrated in Fig. 16(c). However, compared with the modulation strategy I, in the next transition, from *OU*2 state to the *P* state, the antiparallel diode of S_6 has reverse recover losses.

The commutation under the negative output current condition is shown in Fig. 17. In Fig. 17(a), the inductor current is flowing through S_1 and antiparallel diode of S_5. The turning OFF of S_1 will force the inductor current to commutate from S_1 channel to its body diode, as displayed in Fig. 17(b). The turning ON of S_2 will force the inductor current to commutate from the body diode of S_1 to S_2, as depicted in Fig. 17(c). The reverse recovery loss of the body diode of S_1 is very low, owing to the SiC material.

TABLE II
CALCULATED POWER LOSSES ON DEVICE (@U_{DC} = 800 V, M = 0.78, P_O = 2 kW)

Schemes	Description	S_1(W)	S_2(W)	S_3(W)	S_4(W)	S_5(W)	S_6(W)	Total(W)
4-SiC	Switching losses	3.406	0.278	0.278	3.406	0	0	7.368
	Conduction losses	2.043	1.936	1.936	2.043	5.219	5.219	18.396
	Total losses	5.449	2.214	2.214	5.449	5.219	5.219	25.764
2-SiC	Switching losses	0	0	0	0	3.432	3.432	6.864
	Conduction losses	3.037	2.183	2.183	3.037	3.979	3.979	18.398
	Total losses	3.037	2.183	2.183	3.037	7.411	7.411	25.262

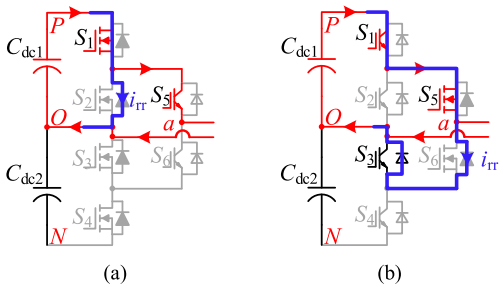

Fig. 19. Diagram of reverse recovery current. (a) 4-SiC hybrid 3L-ANPC inverter. (b) 2-SiC hybrid 3L-ANPC inverter.

TABLE III
COST OF UNIT-SWITCHING DEVICES AND INVERTERS

Configurations	S_1, S_4	S_2, S_3	S_5, S_6	*Cost / Normalization*
Full-Si-IGBT	9.02	9.02	9.02	27.84 / 100%
Full-SiC-MOSFET	33.46	33.46	33.46	100.38 / 360%
2-SiC Hybrid	9.02	9.02	33.46	51.5 / 184%
4-SiC Hybrid	33.46	33.46	9.02	75.94 / 273%
Si IGBT (Infineon-IKW30N60H3)				4.51
SiC MOSFET (ROHM-SCT3080AL)				16.73

Note: Cost is in US dollars, and referred to www.digikey.com

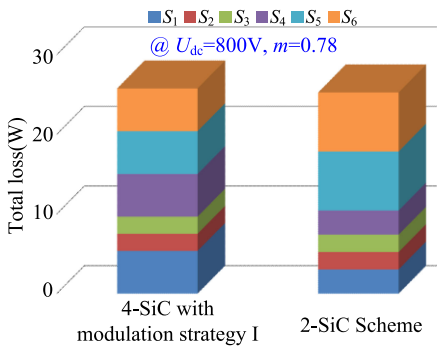

Fig. 20. Theoretical switching device losses for two Si/SiC hybrid schemes with 2-kW output power.

Therefore, it can be concluded that, except for conduction losses, reverse recovery losses of antiparallel diodes are generated in these two Si IGBTs. Thus, the switching losses of modulation strategy II are slightly higher than that of modulation strategy I. On the other hand, the conduction losses are hard to be calculated exactly, since the inductor current sharing of two freewheeling paths cannot be estimated clearly. Therefore, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I is compared with the 2-SiC hybrid 3L-ANPC inverter in terms of efficiency and thermal characteristic.

C. Comparisons of Different Si/SiC Hybrid Schemes

For the 4-SiC hybrid 3L-ANPC inverter and the 2-SiC hybrid 3L-ANPC inverter, the inductor current always flows through a SiC MOSFET and an Si IGBT. Thus, the conduction losses of two hybrid schemes are almost the same. All the switching losses are moved to SiC MOSFETs, either in the 4-SiC hybrid 3L-ANPC inverter or in the 2-SiC hybrid 3L-ANPC inverter. From *OU*1 state to the *P* state, the reverse recovery current of 4-SiC hybrid 3L-ANPC inverter has a shorter commutation loop than that of the 2-SiC hybrid 3L-ANPC inverter, as illustrated in Fig. 19. The reverse recovery loss is very low, thanks to the SiC material. On the other hand, there are charging and discharging losses of junction capacitors during deadtime in the 4-SiC hybrid 3L-ANPC inverter. Therefore, the switching losses of 4-SiC hybrid 3L-ANPC inverter is a little bit higher than that of the 2-SiC hybrid 3L-ANPC inverter. But the switching losses of 4-SiC hybrid 3L-ANPC inverter are distributed on four SiC MOSFETs, which is beneficial to realize thermal balance.

The calculated power losses on switches of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I and the 2-SiC hybrid 3L-ANPC inverter, with the same parameters as that of the 2-kW prototypes are illustrated in Table II and Fig. 20. Both of the process and equations of the calculation mentioned are in accordance with [30]–[33] and not included in this article. It is worth to mention that total losses in Fig. 20 are the sum of switching losses and conduction losses. The driving losses are very low and included in the switching losses. As it can be seen in Table II and Fig. 20, the total losses of 4-SiC 3L-ANPC inverter are a little bit higher than that of the 2-SiC 3L-ANPC inverter. However, the thermal balance characteristic of 4-SiC 3L-ANPC inverter is much better than that of the 2-SiC 3L-ANPC inverter. The calculated junction temperatures on switching devices of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I and the 2-SiC hybrid 3L-ANPC inverter are depicted in Fig. 21.

From Table II, the power losses of S_1, S_2, and S_5, whether in the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I

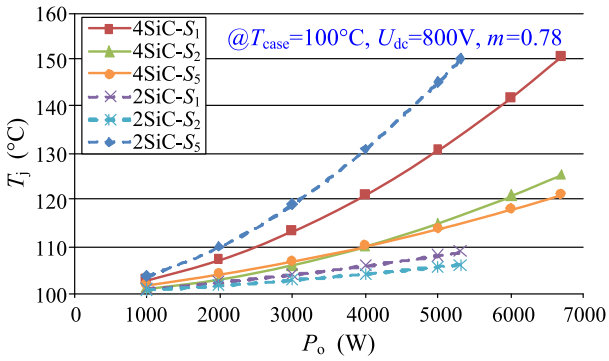

Fig. 21. Estimated junction temperatures of different Si/SiC hybrid schemes.

or in the 2-SiC hybrid 3L-ANPC inverter, are the same as that of S_4, S_3, and S_6, respectively. Therefore, only the junction temperatures of S_1, S_2, and S_5 with different output power are drawn in Fig. 21. The solid lines represent junction temperatures of the 4-SiC hybrid 3L-ANPC inverter. The dashed lines represent junction temperatures of the 2-SiC hybrid 3L-ANPC inverter. The case temperature is set as 100 °C and regulated with a constant value. The thermal resistance from the junction to the case of SiC MOSFET is 1.12 °C/W, whereas the thermal resistance from the junction to the case of Si IGBT is 0.8 °C/W. Both of the thermal resistance parameters are included in their datasheet. To simplify the calculation process, the static drain-source on-state resistance of SiC MOSFET is equal to 0.12 Ω. Since both the maximum junction temperatures of SCT3080AL and IKW30N60H3 are equal to 175 °C, the maximum junction temperatures of the switching devices are limited by 150 °C in this case. From Fig. 21, it can be seen that, the maximum output power of the 2-SiC hybrid 3L-ANPC inverter is 5.3 kW, which is limited by the junction temperature of S_5. The maximum output power of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I can reach 6.7-kW, which is limited by the junction temperature of S_1. Therefore, the maximum output power of 4-SiC hybrid 3L-ANPC inverter with modulation strategy I is almost 1.47 times than that of the 2-SiC hybrid 3L-ANPC inverter. As a result, with the same switching device parameters, the 4-SiC 3L-ANPC inverter can provide more output power over the 2-SiC 3L-ANPC inverter. In other words, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I has higher power density than that of the 2-SiC hybrid 3L-ANPC inverter.

The total cost of the inverter under four different configurations is given in Table III. Obviously, the full-SiC MOSFET 3L-ANPC inverter is the most expensive one. Compared with the 4-SiC hybrid 3L-ANPC inverter, the total cost of the 2-SiC hybrid 3L-ANPC inverter is decreased by 23%. The unit cost of each device is referred from the website.[1]

IV. Experimental Results and Analysis

A. Test Conditions

A 3L-ANPC prototype was built to verify the feasibility of different hybrid schemes. Fig. 22 presents the photo of the universal experimental prototype. The specifications of the prototype are listed in Table IV. The efficiencies of different Si/SiC hybrid schemes were measured by a power analyzer WT1800. To estimate the efficiencies fairly, the modulation indices of different Si/SiC hybrid 3L-ANPC are set the same and equal to 0.78.

The schematic diagram of gating drive circuit is shown in Fig. 23, and detailed parameters are listed in Table V.

[1]https://www.digikey.com

TABLE IV
Parameters of the Experimental Prototype

Parameter	Value
Input voltage	800V
Output voltage/ frequency	220V/ 50Hz
Rated power	2 kW
Switching frequency	40 kHz
Filter inductor L_f	1.4 mH
Filter capacitor C_f	4.7 uF
SiC MOSFET	SCT3080AL
Si IGBT	IKW30N60H3

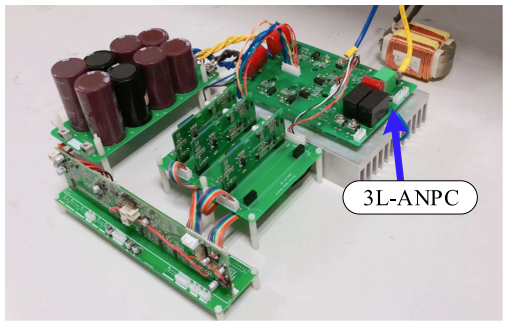

Fig. 22. Prototype of the Si/SiC hybrid 3L-ANPC.

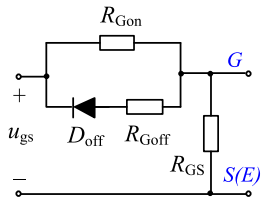

Fig. 23. Schematic diagram of gating drive circuit.

TABLE V
Parameters of the Gating Drive

	SiC MOSFET	Si IGBT
	ROHM-SCT3080AL	Infineon-IKW30N60H3
u_{gs}	+18 V/-2 V	+15 V/-9 V
R_{Gon}	10 Ω	10 Ω
R_{Goff}	5 Ω	5 Ω
R_{GS}	20 kΩ	20 kΩ
D_{off}	1N4148	1N4148

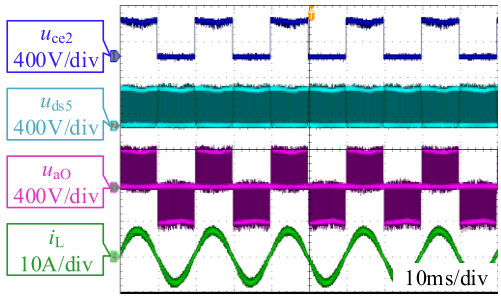

Fig. 24. Steady-state waveforms of 2-SiC hybrid 3L-ANPC.

B. Steady-State Waveforms

The steady experimental results of the 2-SiC hybrid 3L-ANPC inverter under the positive output current condition are shown in Fig. 24, where u_{ce2} represents the collector-emitter voltage of S_2, u_{ds5} represents the drain-source voltage of S_5, u_{aO} represents the output voltage between terminal a and O, and i_L represents the inductor current. The modulation strategy shown in Fig. 6 is employed. It can be seen that, S_5 is high-frequency switching. The blocking voltage of S_2 is clamped to $0.5U_{dc}$ at the positive half cycle. Therefore, all the high-frequency switching events are moved to SiC MOSFETs.

The active turn-ON and active turn-OFF transients of S_5 and S_6 are tested, as shown in Fig. 25, where u_{gs5} and u_{gs6} represent the gating drive signals of S_5 and S_6, i_{S5} and i_{S6} represent the drain-source currents of S_5 and S_6, respectively. u_{ds5} and u_{ds6} represent the drain-source voltages of S_5 and S_6, respectively. The drain-source current is measured by a 60 A Rogowski current waveform transducer. The reference drain-source current direction is defined as purplish red arrows in Fig. 1(a).

Based on the analysis in Section II-B, when S_5 is turned OFF, the inductor current flowing through S_1 and S_5 will be commutated to S_3 and the body diode of S_6 via a large commutation loop. Thus, as shown in Fig. 25(a), the drain-source voltage overshoot of S_5 is almost 100 V. The voltage ringing phenomena of S_5 is also caused by the stray inductance. As shown in Fig. 25(b), when S_5 is turned ON, the body diode of S_6 will be blocked. The inductor current flowing through S_3 and the body diode of S_6 will be commutated to S_1 and S_5 via a large commutation loop. However, thanks to the SiC material, the overshoot drain-source voltage of S_6 is relatively low, as shown in Fig. 25(c). From Fig. 25(d), it is clear that the turn-ON of S_6 is ZVS.

Under positive output current conditions, the steady-state experimental results of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I and modulation strategy II are shown in Figs. 26 and 27, where u_{ds3} and u_{ds4} represent the drain-source voltages of S_3 and S_4, respectively. u_{ce5} and u_{ce6} represent the collector-emitter voltage of S_5 and S_6, u_{aO} represents the output voltage between terminal a and O, u_{gs1} represents the gating signal of the switch S_1, and i_L represents the inductor current.

From Fig. 26(a), it can be seen that, the differential voltage (u_{aO}) of 4-SiC hybrid 3L-ANPC inverter with modulation strategy I has three levels, $+0.5U_{dc}$, 0, and $-0.5U_{dc}$. From Fig. 26(b), it can be seen that, at the positive half cycle, although

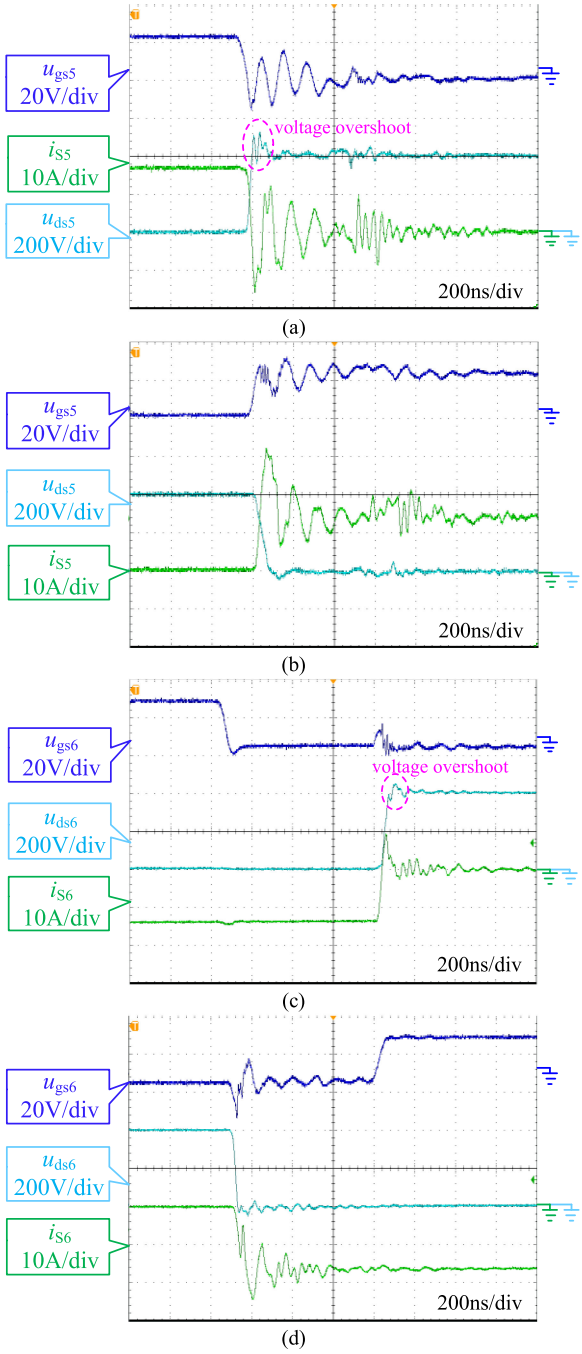

Fig. 25. Turn-ON and turn-OFF waveforms of S_5 and S_6 at the positive half cycle. (a) Turn-OFF voltage and current of S_5. (b) Turn-ON voltage and current of S_5. (c) Turn-OFF voltage and current of S_6. (d) Turn-ON voltage and current of S_6.

S_4 and S_6 are OFF, the blocking voltages of them are still varied at the switching frequency. Apparently, charging and discharging losses of their junction capacitors are generated. Thus, the experimental results are consistent with the theoretical analysis in Section III-A.

From Fig. 27(a), it can be seen that, the differential voltage (u_{aO}) of 4-SiC hybrid 3L-ANPC inverter with modulation strategy II also has three levels. From Fig. 27(b), it can be seen that, at the positive half cycle, although S_4 and S_6 are

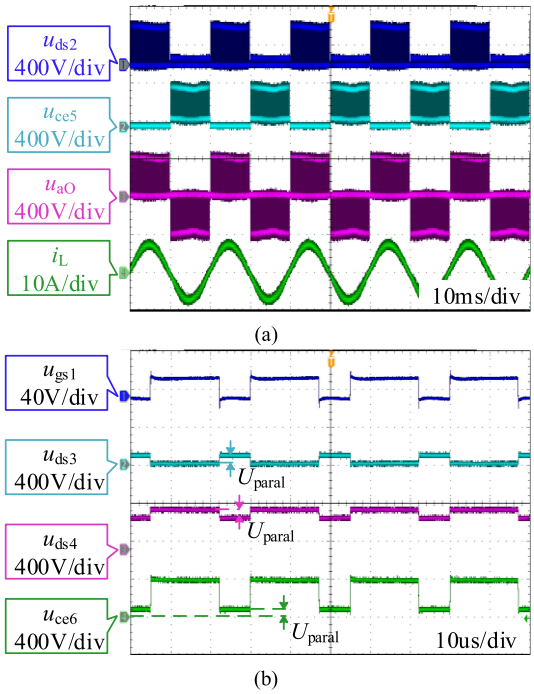

Fig. 26. Steady-state waveforms of 4-SiC hybrid 3L-ANPC inverter with modulation strategy I. (a) Voltage stress on S_2 and S_5. (b) Voltage stress on S_3, S_4, and S_6.

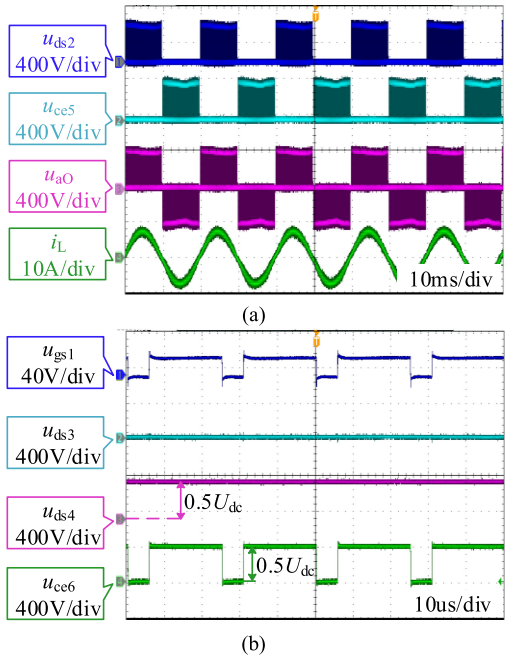

Fig. 27. Steady-state waveforms of 4-SiC hybrid 3L-ANPC inverter with modulation strategy II. (a) Voltage stress on S_2 and S_5. (b) Voltage stress on S_3, S_4, and S_6.

OFF, the blocking voltage S_4 is equal to $0.5U_{dc}$. However, the collector-emitter voltage of S_6 is decreased to zero, when the switch S_1 is OFF. It indicates that there are two freewheeling paths for conducting the inductor current, either through S_2 and S_5, or through S_3 and the antiparallel diode of S_6.

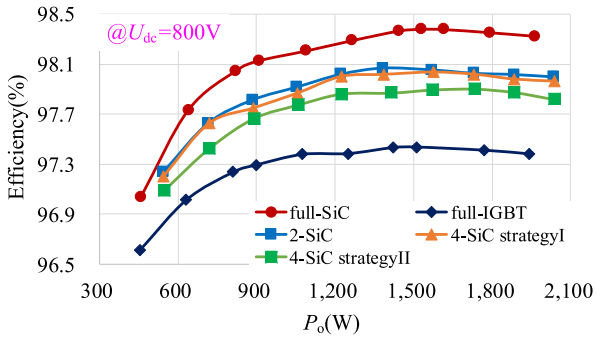

Fig. 28. Efficiencies comparison among different Si/SiC hybrid schemes.

Fig. 28 is the conversion efficiencies comparison result. The modulation indices of different schemes are set the same and equal to 0.78. It is clear that the full-SiC scheme has the highest efficiency, and the full-IGBT scheme has the lowest efficiency. The modulation of these two schemes are the same as that of the 2-SiC hybrid 3L-ANPC inverter. The efficiency of 2-SiC hybrid 3L-ANPC inverter is slightly higher than that of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I. On the other hand, it is worth mentioning that the efficiency of 2-SiC 3L-ANPC inverter is lower than that of the 2-SiC 3L-ANPC rectifier presented in [10]. Because SiC MOSFET, Si-active switches used in [10] have a higher current rating, which leads to lower conduction losses. Further, the inductance is also different.

C. Junction Temperature Measurement and Comparison

The junction temperature measurements were performed with an FOTRIC 285 professional infrared imaging system. The scanner camera operates at a frame rate of 50 Hz with a resolution of 320 × 240 pixels. The emissivity was set as a typical value 0.95. The junction temperatures of S_1, S_2, and S_5 were automatically recorded by the camera every 10 s. The heatsink temperature was recorded as well. On the other hand, it is worth mentioning that to shorten the junction temperature measurement duration, both the output power of the 2-SiC hybrid 3L-ANPC inverter and the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I are increased to 3-kW. Both of them were operating with natural cooling. Both of the input voltages are 800-V, and both of the modulation indices are 0.78. The junction temperatures versus time is depicted in Fig. 29. To draw the temperature curves clearly, we extract the recorded data every 5 min. From Fig. 29, it can be seen that the heatsink temperatures of the 2-SiC hybrid 3L-ANPC inverter and the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I are the same. It indicates that they are operating under similar cooling conditions. From Fig. 29(a), it can be seen that the SiC MOSFET S_5 has the highest temperature 110 °C, and Si IGBT S_2 has the lowest temperature. The temperature difference value is almost 30 °C. From Fig. 29(b), it can be seen that the SiC MOSFET S_1 has the highest temperature 90 °C, and SiC MOSFET S_2 has the lowest temperature. The temperature difference value is only 10 °C, which is beneficial to cooling design. Therefore, the thermal

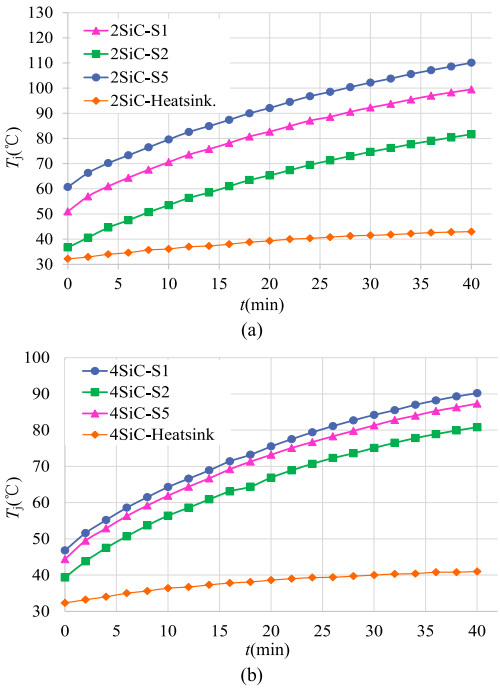

Fig. 29. Measured junction temperatures versus time. (a) 2-SiC hybrid inverter. (b) 4-SiC hybrid inverter with modulation strategy I.

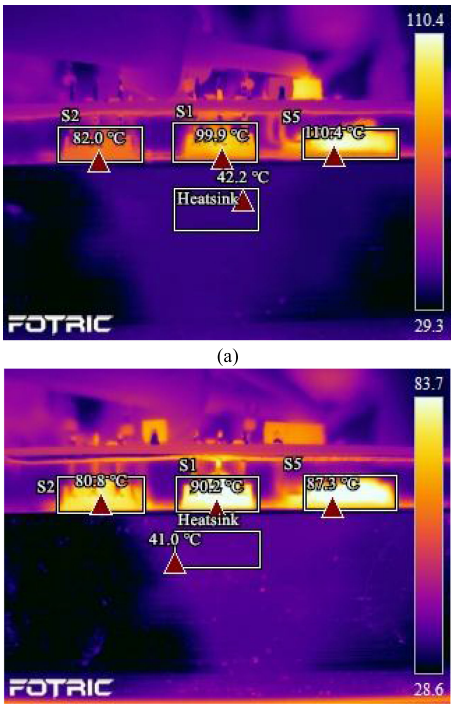

Fig. 30. Infrared pictures of different Si/SiC hybrid schemes. (a) 2-SiC hybrid inverter. (b) 4-SiC hybrid inverter with modulation strategy I.

balance characteristic of the 2-SiC hybrid 3L-ANPC inverter is worse than that of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I. On the other hand, the lower maximum temperature of the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I indicates that it can provide more output power. In other words, with the same switching device parameters, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I has higher power density than that of the 2-SiC hybrid 3L-ANPC inverter.

Furthermore, at 40 min of the measurement, S_1, S_2, S_5, and heatsink of the 2-SiC hybrid 3L-ANPC inverter and 4-SiC hybrid 3L-ANPC inverter are recorded in one camera view, respectively. The infrared pictures are shown in Fig. 30. The measurement results are consistent with the analysis above.

V. Conclusion

Two types of Si/SiC hybrid ANPC switching cells have been introduced for Si/SiC hybrid 3L-ANPC inverter topology generation. A systematic method has been proposed to develop the 2-SiC hybrid 3L-ANPC and 4-SiC hybrid 3L-ANPC inverter topologies based on the basic switching cell concept. Analysis and evaluation of the 2-SiC hybrid 3L-ANPC topology and 4-SiC hybrid 3L-ANPC topology are presented in terms of efficiency, thermal characteristic, and power density. Analysis and experimental results demonstrate the following features of different Si/SiC hybrid 3L-ANPC inverter topologies.

1) The 2-SiC hybrid 3L-ANPC inverter has the highest efficiency and the lowest cost. However, since all the switching events are moved to the two SiC MOSFETs, the thermal balance characteristic of this topology is the worst.
2) For the 4-SiC hybrid 3L-ANPC inverter, the modulation strategy I features a higher efficiency than that of the modulation strategy II.
3) Compared with the 2-SiC hybrid 3L-ANPC inverter, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I has better thermal balance characteristic. In other words, with the same switching device parameters, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I has higher power density performance than that of 2-SiC hybrid 3L-ANPC inverter.

Therefore, the 2-SiC hybrid 3L-ANPC inverter is certainly the preferred choice to its 4-SiC hybrid 3L-ANPC inverter counterpart to be considered for cost-sensitive applications. In contrast, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I is certainly the preferred choice to its 2-SiC hybrid 3L-ANPC inverter counterpart to be considered for high power and high power density applications.

Ultimately, the proposed Si/SiC hybrid switching cells and systematic method can generate other multilevel ANPC inverter and rectifier topologies.

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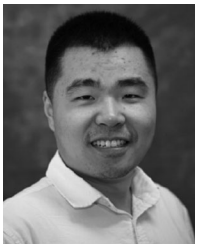

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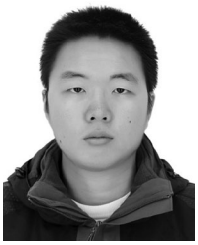

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