Dynamic Temperature Measurements of a GaN DC–DC Boost Converter at MHz Frequencies

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***Abstract*—For reliability predictions, gallium nitride transistors require accurate estimations of the peak operating temperatures within the device. This article presents a new application of thermoreflectance-based temperature measurements performed on a gallium nitride high electron mobility transistor. The submicron spatial and nanosecond temporal resolutions of the measurement system enables for the first time, the dynamic temperature measurement of a transistor operating up to 5 MHz. The gallium nitride transistor is first biased in class-A and excited with a 1 MHz ac signal to demonstrate the dynamic temperature measurement. The transistor is, then, incorporated in a 20–40 V dc–dc boost converter to measure the dynamic temperature distributions across the semiconductor die operating under real loading conditions at 1 and 5 MHz switching frequencies. This technique captures the temperature variations that occur during the switching of the transistor and the recorded peak temperatures are 7.4 °C higher compared with conventional measurement and simulation approaches.**

***Index Terms*—Boost converter, gallium nitride (GaN), power transistor, thermoreflectance measurement.**

I. Introduction

As THE development of silicon (Si)-based electronics approaches its theoretical performance limits, wide bandgap semiconductor devices, such as gallium nitride (GaN) high electron mobility transistors (HEMT), are promising candidates for high-frequency and high-efficiency power electronics. GaN-based switching devices enable faster switching transients with lower power losses and can operate at higher temperatures, due to their superior physical properties namely their high electron mobility, low on-state resistance, $R_{\mathrm{DS(on)}}$, high breakdown voltage, and low input and output capacitances [1]. Enabling higher switching frequency is desired in an effort to reduce the power converter size. However, the increase in the switching frequency for GaN-based transistors can influence trapping, and this can lead to degradation in the converter efficiency [2]–[4]. Several research groups have recently presented high power GaN based dc–dc converters reaching efficiencies higher than 95% at MHz switching frequencies [5], [6]. The impact of increasing the switching frequency on the converter efficiency is shown in [7], where a GaN HEMT boost converter was tested between switching frequencies of 500 kHz to 2 MHz with a corresponding conversion efficiency decrease from 98.2% to 96.6%. In [8], the same efficiency degradation is shown on a GaN double heterostructure field effect transistor boost converter, which was tested between switching frequencies of 512 and 845 kHz with a corresponding efficiency decrease from 96.1% to 93.9%.

The reliability of Si power transistors is well established and there are many standardized tests that accurately estimate device lifetime and determine failure rates. GaN-based devices have not reached full maturity, and the long-term reliability standards of GaN HEMTs in power switching applications are still being developed. Companies such as Transphorm are utilizing the standard Joint Electron Device Engineering Council (JEDEC) qualification testing to ensure the long-term reliability of its GaN products aimed for power applications [9]. Texas Instruments is also following a similar approach to adapt the standard Si JEDEC testing methodology to GaN HEMTs, used in hard-switched power converters [10]. Multiple research groups are focusing on developing the reliability requirements for GaN HEMTs used in automotive applications and high voltage applications [11], [12].

The degradation processes for power devices are accelerated by increased temperatures, according to the Arrhenius law. The acceleration factor (AF), expressed in (1), determines the device lifetime projections and calculates the time acceleration value that results from operating a device at an elevated temperature. By definition, the AF is the device time to failure at low temperature divided by the time to failure at higher temperature [13]

$$\mathrm{AF} = \exp\left(\frac{E_a}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]\right) \quad (1)$$

where T_1 is the device low operating temperature, T_2 is the device higher operating temperature, E_a is activation energy (eV), and k is Boltzmann's constant. The accuracy of

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the measured operating temperature directly impacts these estimates. Present measurement techniques are not sufficiently accurate to capture the self-heating swings experienced by the transistor, due to their poor spatial and temporal resolutions, capturing average temperature over a wide area despite the transistor going through a periodic temperature variation during the switching of the device.

The power losses within a transistor occur due to the dynamic overlap of the current and voltage waveforms [14]. This overlap creates dynamic self-heating that is difficult to measure, as it occurs at nano-second time scales for devices operating in the MHz frequency range. To measure the dynamic temperature, the temporal resolution of the measurement system must be sufficiently fast to capture multiple temperature points within a single period. Additionally, thermal measurements are usually performed at the surface of the device and, therefore, the combined thermal response of the materials situated between the junction and the surface of the device has to be sufficiently fast to allow the temperature to reach its peak and cool down within a single period. The measurement of the dynamic temperature variations during operation allows for more accurate peak temperature readings [15].

The most common measurement techniques used to measure the transistor temperature are classified as thermo-sensitive electrical parameters (TSEP), physical, and optical methods. Unfortunately, the majority of these measurement techniques cannot provide the required resolution and are unable to measure over a large area to capture the dynamic temperature swings across the entire transistor die. TSEP only provides the average temperature over the entire die and the measurement technique is limited to 100 μs temporal resolution [16]. Physical methods such as thermocouples and thermistors require direct contact, which may alter the device performance and are limited by the thermal response of the probe. Infrared microscopy technique is limited to 3 to 5 μm spatial resolution and can achieve approximately 1 μs minimum time resolution [17]. Finally, Raman spectroscopy has submicron spatial and nanosecond temporal resolutions but lacks the ability to capture measurements over the full transistor [18].

Thermoreflectance thermography is an optical and noninvasive thermal measurement technique that can achieve nanosecond time and submicron spatial resolutions. By using different illumination wavelengths, the technique can directly measure the temperature of the gate, drain, and source metals or of the channel area situated at the GaN/AlGaN interface of the HEMT [19]. The measurement technique can also capture large areas that enables the measurement of temperature distributions across entire transistor die.

This article presents a unique application of the thermoreflectance measurement technique, where the dynamic peak temperature across a GaN HEMT operating in a high-frequency dc–dc boost converter is measured. The dynamic measurement methodology allows obtaining the instantaneous temperature waveform experienced by the GaN HEMT during the switching transients, since the measurement time steps are much smaller than the switching times. The measurement is performed with a spatial resolution of 405 μm at 50-ns temporal resolution and the transistor used in the converter is a 25-W Cree GaN HEMT, as shown in Fig. 1. Depending on the frequency of the switching and the thermal profile of the device, the instantaneous temperature can be much higher than the average temperature over the full switching cycle, same as how the average power is lower than the instantaneous power. Thus, the dynamic measurement methodology can capture more accurate temperature profiles, directly impacting the design of reliable GaN HEMTs used in the power converter systems.

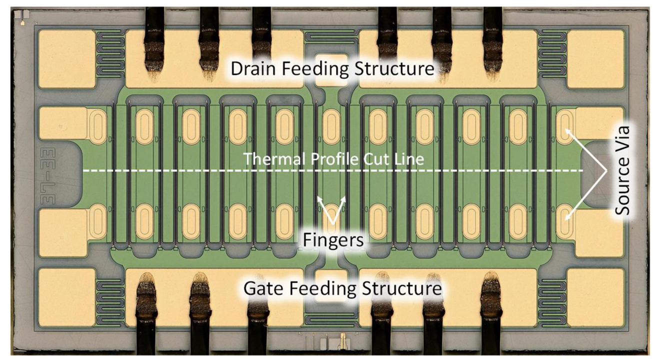


Fig. 1. Photograph of a 25-W 20-finger Cree GaN HEMT die. The cutline indicates the position where the thermal profile is measured using the thermoreflectance system.

II. Measurement Methodology

A. Methodology

Thermoreflectance spectroscopy has been widely used since the 1960s to study the band structures and the dielectric response function of semiconductors [20]. Only recently, has thermoreflectance thermography been used to measure temperature within transistors. The thermoreflectance imaging technique measures the fractional change in the surface reflectance, ΔR, caused by temperature change, ΔT, within the sample. A first-order relationship between the normalized change in optical reflectance ($\Delta R/R_0$) and the change in temperature is expressed as

$$\frac{\Delta R}{R_0} = \left(\frac{1}{R_0}\frac{\delta R}{\delta T}\right)\Delta T = C_{tr}\Delta T \tag{2}$$

where R_0 is the intensity of light reflected from the sample surface at a given temperature T_0, and C_{tr} is the thermoreflectance coefficient. The thermoreflectance coefficient, which is material and wavelength dependent, is obtained during a calibration process where the sample is externally heated to two temperatures by using a thermoelectric heating stage. A charge coupled device (CCD) camera measures the change in reflectance caused by the induced temperature difference. By obtaining the reflectance change and the temperature difference, the C_{tr} is determined using (2). A wavelength sweep is required to determine the maximum C_{tr} of a material, which improves the temperature resolution of the measurement. Since the thermoreflectance coefficient is small (10^{-6} to 10^{-4} K^{-1}) a lock-in technique is employed to extract the small magnitude of the C_{tr} from the background noise.

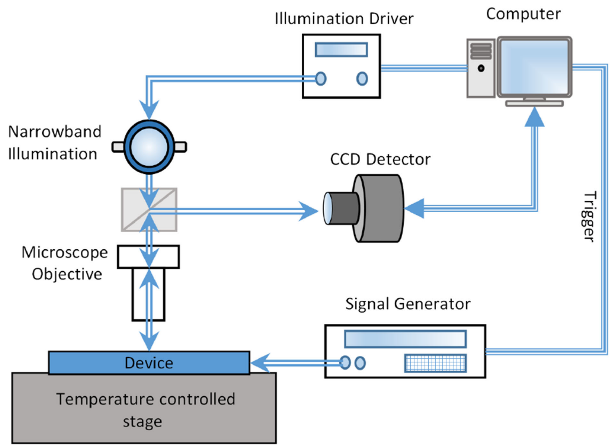


Fig. 2. Schematic diagram of the thermoreflectance measurement configuration that includes the CCD detector, illumination source, microscope objective, and the temperature controlled stage.

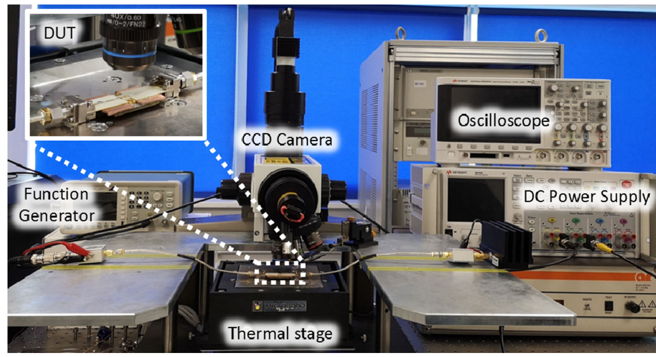


Fig. 3. Photograph of the thermoreflectance measurement set-up used to extract the dynamic temperature variations of the GaN transistor.

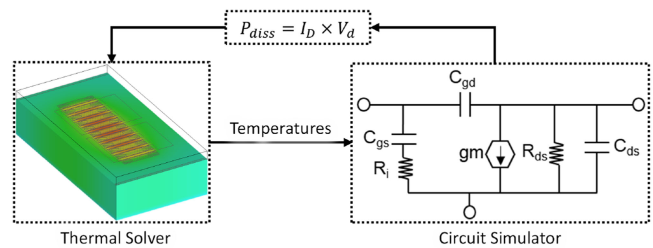


Fig. 4. Electrothermal simulation loop composed of the dissipated power calculated by the circuit-simulator, which is read by the thermal solver to compute the temperatures for each power source.

In Fig. 2, the measurement configuration of the thermoreflectance-based imaging technique is presented. The transistor is placed under a microscope with normal incident illumination provided by a narrowband source, typically a light emitting diode (LED) or a laser. An electrical excitation pulse is applied to the transistor, which induces a change in temperature and corresponding change in reflectance. An image of the reflectance change over the device surface is, then, recorded by the CCD camera attached to the microscope. This image is converted to temperature by scaling each pixel in the image by its corresponding thermoreflectance coefficient extracted from calibration. The illumination wavelengths used are in the visible spectrum, and, therefore, the diffraction limited spatial resolution is approximately 0.3 μm. To obtain a temperature resolution of 0.1°C, averaging over multiple excitation cycles is required [21]. By employing a box-car averaging scheme where the LED pulses are synchronized to the CCD camera shutter and device excitation pulses, transient temperature measurements are enabled [22]. Temporal resolutions of 50 ns [22] and 800 ps [23] are possible depending on the choice of the illuminating source.

B. Measurement Configuration

The measurement configuration used to measure the dynamic temperature variations is shown in Fig. 3. The configuration is composed of a Micorsanj NT220B thermoreflectance system, a Tecktronix signal generator, a Keysight N6705BDC power supply, and a 100-MHz bandwidth Keysight InfiniiVision digital oscilloscope.

To extract the C_{tr} and measure the temperature of the GaN material, the ceramic lid of the transistor needs to be removed to expose the channel regions to the system's CCD camera. The calibration was performed by placing the GaN transistor on the thermal chuck and measuring the reflectance change, while the temperature varied between 20 and 120°C. Both the calibration and temperature measurement are performed with a 365-nm LED wavelength, which yields the maximum reflectance change for the GaN material [24]. The Abbe diffraction limited spatial resolution of the thermal measurements performed with this wavelength is 405 μm.

The signal generator is used to apply a pulsed ac signal to the transistor gate terminal, the dc power supply controls the dc gate and drain biases, and the digital oscilloscope measures the output ac drain voltage. The drain current is measured, with the digital oscilloscope, across a current sense resistor soldered on the drain terminal. The instantaneous drain power loss can be computed by multiplying the measured drain current and voltage waveforms.

III. Device Model Description

The simulation of the transistor is performed using a 3-D electrothermal analysis program, ADS Electro-Thermal, which uses an electrical circuit-simulator and a finite element method (FEM)-based thermal solver. The circuit-simulator computes the power dissipated by each transistor finger, which is read into the thermal simulation to compute the temperature. The temperatures are sent back into the circuit-simulator to complete an electrothermal simulation loop iteration, as shown in Fig. 4, which continues until both temperature and power are mutually consistent.

The nonlinear electrical compact model of the CGH40025F packaged Cree GaN HEMT is used to generate the time-dependent power dissipation of the device. The effect of the parasitics of the package and bondwires are ignored as they have negligible influence at these switching frequencies.

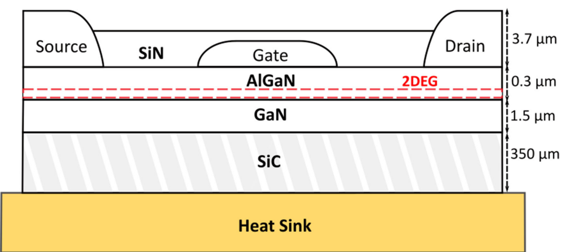


Fig. 5. Structural diagram of the device layers used in the simulation software. For clarity, the device is drawn without the field plate.

The electrical model computes the total dissipated power of the device, which is, then, scaled down to 1/20 to represent the power losses of a single transistor finger. In this way, each finger is individually simulated, which allows for the extraction of the junction temperature associated with their respective dissipated power.

During thermal simulations, the GaN HEMT had the bottom of the semiconductor substrate attached to a heat sink, where the temperature is kept at a constant level, while all the other surfaces are set to adiabatic boundaries. The power sources for all 20 fingers are defined between the GaN/AlGaN layer interface and along the length of the gate fingers, in the active region of each transistor finger [25]. It is assumed that the heat dissipation is uniformly distributed over the power source area. The thermal properties of the various device materials that form the semiconductor die, such as thermal conductivity, density, and volumetric heat capacity were taken from [26]. The geometry and dimensions of the device structure are shown in Fig. 5. The top surface dimensions of the die were measured with Keyence VHX-5000 digital microscope, which were used to create the surface layout of the die for simulation.

IV. Thermal Measurements

In this section, the transistor is initially biased to perform steady-state dc thermoreflectance measurements to showcase the spatial accuracy of the system. Afterwards, the transistor is biased in class-A, and then ac excitation is applied to demonstrate the dynamic temperature measurement technique and its comparison with thermal simulations. In Section V, we proceed to use this technique to capture for the first time the dynamic temperature variations of an HEMT operating in a dc–dc converter.

A. DC Measurements

The thermoreflectance measurements are performed across the surface of a commercially available 25-W CGH40025F Cree GaN HEMT. The gate threshold voltage of this device is −3.8 V, the maximum drain current is 6 A at $V_{GS} = 2$ V, and the drain-source breakdown voltage is 120 V.

The GaN transistor was positioned in a microstrip test-fixture with two 50-Ω transmission lines, as shown in Fig. 6. The fixture and two bias-tees were used to bias the transistor to $V_{DS} = 28$ V, $I_{DQ} = 200$ mA. The ceramic lid of the package was removed, as shown in Fig. 1, to expose the die surface to the CCD camera and enable the temperature measurement of the GaN channel areas. The temperature distribution was measured after the device has reached thermal steady state. The temperature was measured at 20-times magnification and the extracted thermal image is shown in Fig. 7(a). This magnification enables the temperature measurement of the entire die while allowing a submicron spatial resolution readings of each exposed GaN channel region, as shown in the inset of Fig. 7(a). The temperature values for each transistor finger were averaged across the gate width and extracted along the thermal profile cutline, as shown in Fig. 1, and plotted in Fig. 7(b). The measured thermal profile has the expected inverse-U shape, with the middle fingers hotter that the outer fingers and a peak temperature of 49 °C.

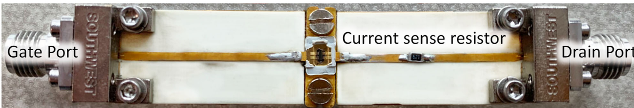


Fig. 6. Photograph of the package Cree GaN transistor with its ceramic lid removed in a 50-Ω test fixture used for dc temperature measurements.

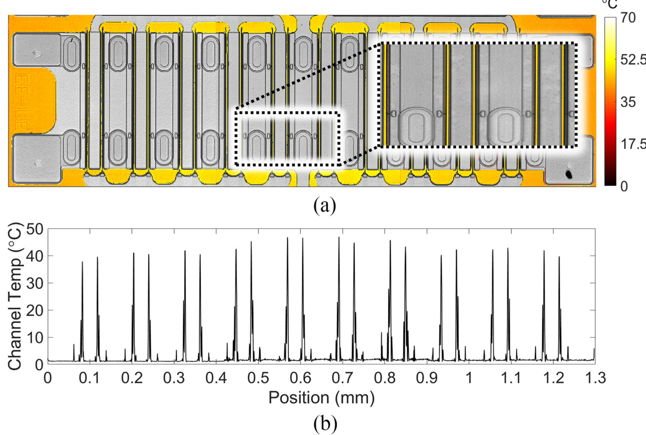


Fig. 7. (a) Thermal image of the transistor's die obtained during dc operation, and (b) temperature distribution results measured along the thermal profile cut line, as shown in Fig. 1.

B. Temperature Variations Due to AC Heating

During the dc operation of the transistor, the losses are constant, resulting in a static operating temperature. When an ac excitation is also present, the power losses vary in time which results in a time-dependent temperature change. To demonstrate a measurement of the dynamic temperature variations, the transistor was biased in class-A and excited using a pulsed ac signal. The signal is pulsed because the thermoreflectance measurement system requires a differential measurement to extract temperatures, meaning a thermal "reference image" is obtained during the dc operation and an "ON image" is obtained during the dc+ac operation of the device. These operational states are shown in Fig. 8. The maximum theoretical drain efficiency, under ideal conditions, of class-A operation is 50%.

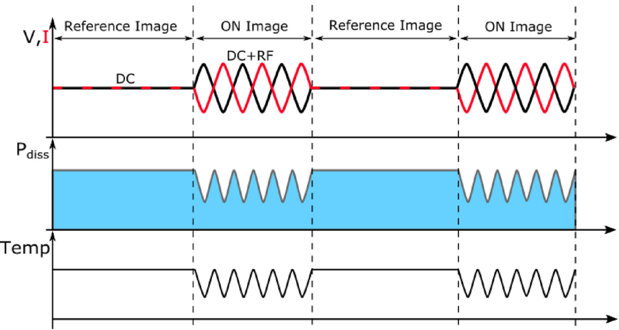


Fig. 8. Illustration of the drain current and voltage waveforms, power dissipation, and instantaneous temperature of a transistor operating in class-A transistor operation. During the thermoreflectance measurements, the transistor ac excitation is pulsed while the dc is constantly applied.

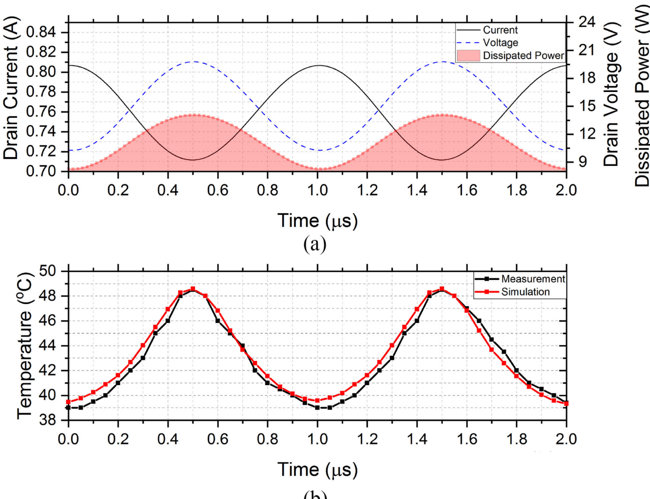
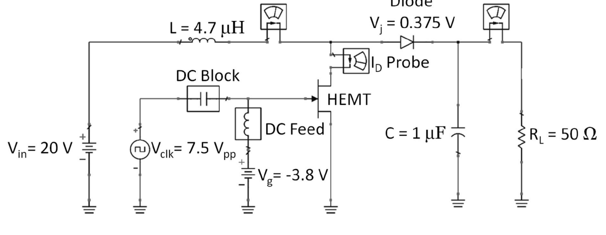


Fig. 9. (a) Measured drain current, voltage, and calculated power dissipation of the GaN HEMT operating in class-A. (b) Measured and simulated temperature variation of a single transistor finger operating in class-A measured with a temporal resolution of 50 ns.

The transistor operating in class-A is more efficient during the dc+ac operation compared to just the dc operation. The drain current and voltage waveforms, power dissipation, and dynamic temperature variation of an ideal class-A operation of a transistor are illustrated in Fig. 8. Since the power losses during the dc operation are higher than the losses during the dc+ac operation of the device, the measured dynamic temperature during the dc+ac operation is expected to have a negative variation with respect to the temperature obtained during the dc operation of the device. The dc bias conditions of the GaN HEMT were set to 20 and -2.6 V on the drain and gate, respectively. A 300-μs, 10% duty cycle ac pulse of 0.7-V_{pp} amplitude was used to excite the transistor at 1 MHz. The temporal resolution of the NT220B system was set to 50 ns, allowing 20 sampling points per period. The temperature results were extracted along the thermal profile cut line as shown in Fig. 1.

The measured drain IV waveforms and power dissipation of the transistor are shown in Fig. 9(a). The measured dynamic temperature variation of a single transistor finger captured 298 μs after the device is excited, is shown in Fig. 9(b). As expected, the measured dynamic temperature variation closely follows the power dissipation curve and ranges between 49 °C and 38.5 °C.

Electrothermal simulations of the GaN HEMT operating in class-A were performed to compare with the measured thermal results. The transient simulation time step was set to 1-ns to provide a detailed time response of the simulated temperature. To mimic the temperature acquisition of the NT220B system, the simulation results were averaged over 50 points, replicating the 50-ns temporal resolution used for the measurement. A good agreement between the simulated and measured temperature results is shown in Fig. 9(b).



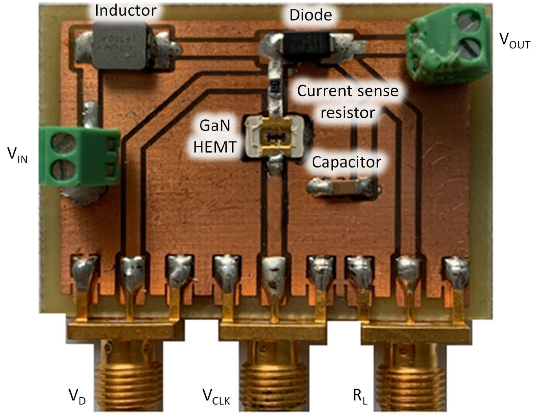


Fig. 10. Schematic diagram and photograph of the GaN dc–dc boost converter. The converter includes an inductor, a diode, a capacitor, and the transistor. A dc source is used to provide the input voltage ($\mathrm{V_{in}}$), a signal generator provides the square wave ($\mathrm{V_{CLK}}$), and the output power is dissipated into a 50-Ω load resistor ($\mathrm{R_L}$).

V. DC–DC Boost Converter

A. *Description and Theory*

To demonstrate how the measurement technique is able to capture the dynamic temperatures across transistors working in power converters, the GaN HEMT is used as the switching element of a 20–40 V dc–dc boost converter. The converter achieves 89% efficiency, which is lower than previously proposed designs but suits the purposes of this article. The converter was assembled on an FR4 1.5-mm double-sided PCB, where the passive-components are surface-mounted. The GaN HEMT is mounted on an aluminum baseplate providing the ground and heatsink for the circuit. The circuit diagram and photograph of the fabricated boost converter are shown in Fig. 10. The transistor was controlled through a gate-source voltage pulse swinging between pinch-off and open-channel voltages. The duty cycle of the gate signal was set to 50%.

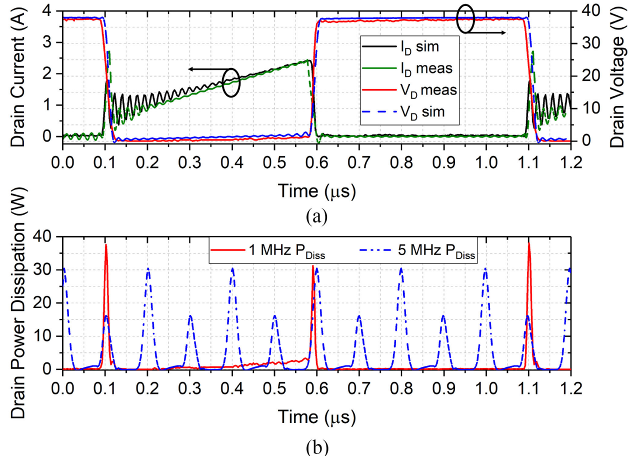


Fig. 11. (a) Measured and simulated drain current and voltage waveforms at the switching frequency of 1 MHz. (b) Calculated power dissipation from the product of the drain current and voltage measured at 1 and 5 MHz.

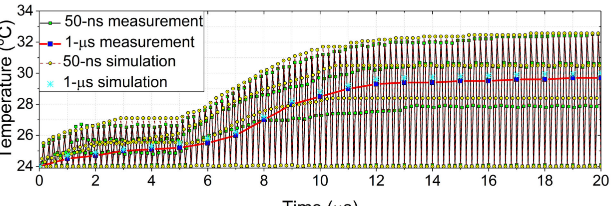


Fig. 12. Transient temperature FEM simulation and thermoreflectance measurement results of a single GaN transistor finger extracted with 50-ns and 1-μs time resolutions.

The boost converter circuit is composed of a 1-μF capacitor, a 4.7-μH inductor with a 0.15-Ω resistance and 3-A rated current, a Schottky rectifier diode with 0.3-V forward voltage and 0.14-Ω resistance, and a 150-pF capacitor. The load is a 50-W, 50-Ω resistor attached through an SMA connector.

B. Instantaneous Temperature Measurements

The circuit model of the dc–dc boost converter computes the time-dependent drain voltage and current waveforms of the transistor, from which the power loss is calculated. During the thermoreflectance measurement of the device, the drain waveforms are measured with a digital oscilloscope to calculate the device total power dissipation, which is compared to the electrical simulation results at 1 MHz. A good agreement between the simulated and measured waveforms is shown in Fig. 11(a).

Temperature measurements and simulations were performed across the GaN HEMT at both 1 and 5 MHz switching frequencies. The operating conditions of the transistor were set to $V_D = 20$ V, $I_D = 1.64$ A, and $V_G = -3.8$ V. During the thermoreflectance measurements, the drain voltage and the gate dc bias are continuously applied, while the gate ac signal is pulsed for 100 μs, at 10% duty cycle. Therefore, the measurement system captures the thermal "reference image" during the dc operation of the transistor and the "ON image" during the dc and pulsed ac operation. The temperature difference between the two modes of operation will be positive, as during the dc operation of the converter, the transistor is not conducting any current.

During the dynamic temperature measurements, the temporal resolution of the NT220B system was set to 50 ns, allowing 20 temperature sampling points per period at 1 MHz and four sampling points at 5 MHz. Similarly to Section IV, transient electrothermal simulations, for both frequencies, are performed in time steps of 1 ns and, then, averaged over 50 points to mimic the thermal measurement acquisition time. The measured and simulated dynamic temperature variations for one switching period at 1 MHz switching frequency are shown in Fig. 13. The 3-D graph shows a subtle increase in temperature toward the middle transistor fingers compared to the outer fingers, and a good agreement between the simulation and measurement results is achieved. The dynamic temperature variation is the product of the combined effect between the conduction and switching losses. It can be seen that within a single switching period of 1 μs, the measured dynamic temperature reaches a peak of 38.3 °C and cools down to the ambient temperature. The transistor experiences this temperature variation continuously during the operation of the dc–dc converter. The temperature variation is directly related to the dissipated power in the transistor, as shown in Fig. 11(a). Focusing on Fig. 11(a), at 0.1 μs, the ON switching power loss occurs resulting in a rapid increase in the dynamic temperature. The temperature does not have enough time to completely cool down before the conduction loss starts taking effect, which keeps the temperature constant until the OFF switching loss occurs, at 0.6 μs, where the dynamic temperature starts cooling down to the ambient temperature. Higher fidelity measurement of the dynamic temperature variation can be achieved if the temporal resolution of the measurement system can be further enhanced.

The dynamic temperature variations at 5 MHz are also shown in Fig. 13(b). This is the maximum switching frequency at which the NT220B system can perform dynamic temperature variations measurements, although laser-based thermoreflectance systems can measure the dynamic temperature occurring at higher switching frequencies due to the 800 ps temporal resolution. The temperature variations are more frequent due to the increased frequency and the peak temperature across the device was measured to be 32.8 °C. The peak temperature measured at 1 MHz is higher than at 5 MHz due to the higher instantaneous switching losses, as shown in Fig. 11(b). The fast thermoreflectance technique allows the measurement of the peak temperatures caused by the instantaneous losses occurring within the switching cycle. This shows the advantage of the thermoreflectance technique as it can measure the peak temperature inside the switching period during the operation of the boost converter, unlike infrared microscopy that can only measure the average temperature across multiple switching periods.

To demonstrate the benefits of using the dynamic temperature measurement methodology that is sufficiently fast enough to capture the peak temperatures that occur during the switching, we have generated a comparison between the peak temperatures, measured by the thermoreflectance technique and FEM electrothermal simulations performed at 1 μs and 50 ns time resolutions. These are shown in Fig. 12. The 1-μs resolution was selected so that the temperature acquisition time of the

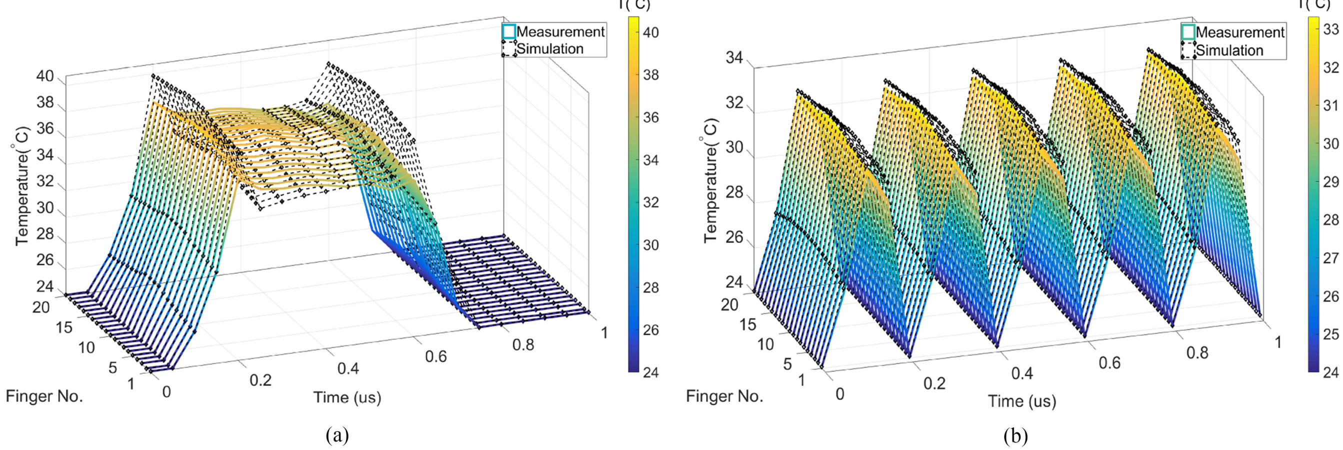


Fig. 13. Measured and simulated dynamic temperature variation distribution results across the GaN transistor die operating at (a) 1 and (b) 5 MHz.

thermoreflectance system is higher than multiple switching periods of the HEMT operating at 5 MHz. For clarity, the 1-μs time resolution of the system means that the temperature is averaged every 1 μs during transient measurements. This has the effect of smoothing out the temperature peaks due to switching and results in a lower overall temperature. Therefore, the 1-μs measurement and simulation results fail to capture the temperature transients during the switching cycle resulting in a lower peak temperature measurement compared to the 50-ns results.

The ability to measure the dynamic temperature allows for a more accurate assessment of the self-heating behavior in transistors. Conventional measurement techniques, such as IR microscopy [16]–[18], [27], [28], cannot capture the dynamic temperatures, due to their slow response relative to the MHz switching frequencies or they detect the average temperature over the chip. The measurement of the temperature variations within a GaN HEMT operating at MHz frequencies is for the first time measured. The capability of capturing the dynamic temperature across the entire transistor die can be used to assess the performance of each individual finger, enabling direct visualization of their performance. This information can, then, be used to verify finite element based thermal models and to improve the design of the semiconductor by changing its layout to improve the electrothermal behavior of the transistor.

VI. Conclusion

A thermoreflectance-based system was used to capture the dynamic temperature variations across a GaN HEMT biased under various operating conditions and MHz switching frequencies. The measurement results are compared with electrothermal simulations performed to verify the accuracy of the measurement methodology. First, the device was biased in class-A, to show how the dynamic temperature variations are measured with the thermoreflectance system. The GaN HEMT is, then, incorporated in a 20–40 V boost converter to measure, for the first time, the dynamic temperature variations that occur during the switching of the transistor at 1 and 5 MHz. The measurement methodology captures a more accurate representation of the thermal behavior of transistors working in dc–dc converters. This methodology can be used to verify thermal models, improve the thermal design of the semiconductor die and more accurately assess the self-heating behavior of transistors. Furthermore, the knowledge of the dynamic temperature swings can further enhance reliability estimations associated with temperature-based failure mechanisms.

References

[1] E. A. Jones, F. F. Wang, and D. Costinett, “Review of commercial GaN power devices and GaN-based converter design challenges,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[2] H. Li, C. Yao, L. Fu, X. Zhang, and J. Wang, “Evaluations and applications of GaN HEMTs for power electronics,” in *Proc. Int. Power Electron. Motion Control Conf.*, Hefei, China, 2016, pp. 563–569.

[3] Y. Cai, A. J. Forsyth, and R. Todd, “Impact of GaN HEMT dynamic on-state resistance on converter performance,” in *Proc. Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 1689–1694.

[4] B. Hughes, J. Lazar, S. Hulsey, D. Zehnder, D. Matic, and K. Boutros, “GaN HFET switching characteristics at 350V/20A and synchronous boost converter performance at 1 MHz,” in *Proc. Appl. Power Electron. Conf.*, Orlando, FL, USA, 2012, pp. 2506–2508.

[5] F. Gamand, M. D. Li, and C. Gaquiere, “A 10-MHz GaN HEMT DC/DC boost converter for power amplifier applications,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 11, pp. 776–779, Nov. 2012.

[6] J. Das *et al.*, “A 96% efficient high-frequency DC/DC converter using E-mode GaN DHFETs on Si,” *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1370–1372, Oct. 2011.

[7] Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, “A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz,” *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 824–8262, Aug. 2008.

[8] W. Saito *et al.*, “A 120-W boost converter operation using a high-voltage GaN-HEMT,” *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 8–10, Jan. 2008.

[9] K. Smith and R. Barr, “Reliability lifecycle of GaN power devices,” Transphorm, Tech. Rep., Mar. 2017. [Online]. Available: https://www.transphormusa.com/en/document/white-paper-reliability-lifec ycle-gan-power-devices/

[10] S. Bahl, “A comprehensive methodology to qualify the reliability of GaN products,” Texas Instruments, Tech. Rep., Mar. 2015. [Online]. Available: http://www.ti.com/lit/wp/slyy070/slyy070.pdf

[11] T. Kachi, D. Kikuta, and T. Uesugi, “GaN power device and reliability for automotive applications,” in *Proc. Rel. Phys. Symp.*, Anaheim, CA, USA, 2012, pp. 3D.1.1–3D.1.4.

[12] S. G. Khalil, S. Hardikar, S. Sack, E. Persson, M. Imam, and T. McDonald, “HV GaN reliability and status,” in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, 2015, pp. 21–23.

[13] R. A. Coutu *et al.*, "Benefits of considering more than temperature acceleration for GaN HEMT life testing," *Electronics*, vol. 6, no. 3, pp. 1–14, 2016.

[14] P. J. Tasker, "Practical waveform engineering," *IEEE Microw. Mag.*, vol. 10, no. 7, pp. 65–76, Dec. 2009.

[15] M. Musallam, P. P. Acarnley, C. M. Johnson, L. Pritchard, and V. Pickert, "Open loop real-time power electronic device junction temperature estimation," in *Proc. IEEE Int. Symp. Ind. Electron.*, Ajaccio, France, 2004, pp. 1041–1046.

[16] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters: A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[17] A. Hefner, D. Berning, D. Blackburn, C. Chapuy, and S. Bouche, "A high-speed thermal imaging system for semiconductor device analysis," in *Proc. 17th Annu. Semicond. Therm. Meas. Manage. Symp.*, San Jose, CA, USA, 2001, pp. 43–49.

[18] M. Kuball *et al.*, "Time-resolved temperature measurement of AlGaN/GaN electronic devices using micro-raman spectroscopy," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 86–89, Feb. 2007.

[19] G. Pavlidis, D. Kendig, L. Yates, and S. Graham, "Improving the transient thermal characterization of GaN HEMTs," in *Proc. 17th IEEE Intersociety Conf. Therm. Thermomech. Phenomena Electron. Syst.*, San Diego, CA, USA, 2018, pp. 208–213.

[20] E. Matatagui, A. G. Thompson, and M. Cardona, "Thermoreflectance in semiconductors," *Phys. Rev.*, vol. 176, no. 3, pp. 950–960, Dec. 1968.

[21] P. Mayer, D. Lueerssen, R. J Ram, and J. Hudgings, "Theoretical and experimental investigation of the thermal resolution and dynamic range of CCD-based thermoreflectance imaging," *J. Opt. Soc. Am. A.*, vol. 24, no. 4, pp. 1156–1163, May 2007.

[22] K. Maize, J. Christofferson, and A. Shakouri, "Transient thermal imaging using thermoreflectance," in *Proc. 24th Annu. IEEE Semicond. Thermal. Meas. Manage. Symp.*, San Jose, CA, USA, 2008, pp. 55–58.

[23] K. Maize *et al.*, "High resolution thermal characterization and simulation of power AlGaN/GaN HEMTs using micro-raman thermography and 800 picosecond transient thermoreflectance imaging," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, La Jolla, CA, USA, 2014, pp. 1–8.

[24] D. Kendig *et al.*, "UV thermal imaging of RF GaN devices with GaN resistor validation," in *Proc. 91st Microw. Meas. Conf.*, Philadelphia, PA, USA, 2018, pp. 1–4.

[25] D. Denis, C. M. Snowden, and I. C. Hunter, "Coupled electrothermal, electromagnetic, and physical modeling of microwave power FETs," *IEEE Trans. Microw. Theory Technol.*, vol. 54, no. 6, pp. 2465–2470, Jun. 2006.

[26] K. Belkacemi and R. Hocine, "Efficient 3D-TLM modeling and simulation for the thermal management of microwave AlGaN/GaN HEMT used in high power amplifiers SSPA," *J. Low Power Electron. Appl.*, vol. 8, no. 3, Jun. 2018.

[27] D. L. Blackburn, "Temperature measurements of semiconductor devices - A review," in *Proc. 20th Annu. Semicond. Therm. Meas. Manage. Symp.*, San Jose, CA, USA, 2004, pp. 70–80.

[28] K. R. Bagnall, O. I. Saadat, S. Joglekar, T. Palacios, and E. N. Wang, "Experimental characterization of the thermal time constants of GaN HEMTs via micro-raman thermometry," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2121–2128, May 2017.

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