Design of a High Accuracy PSR CC/CV AC–DC Converter Without Auxiliary Winding

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***Abstract*—A high accuracy ac–dc converter without auxiliary winding has been proposed in this article. The converter adopts primary-side regulation (PSR) topology, sampling output voltage and current from primary inductance, then adjusting switching frequency and primary peak current of the power converter to regulate output. By switching the main power transistor and the auxiliary switching transistor alternately ON and OFF, and using base charge storage effect to generate driving voltage, the converter charges chip-powering capacitor by primary-side current, instead of auxiliary winding. Compared to the traditional three-winding topology, the proposed converter not only achieves higher performance, but also eliminates one winding, which means fewer external components are used, transformer becomes simpler, and system cost is lower. The control chip was implemented in NEC 1-μm HVCMOS process, and a 5 V/1 A prototype has been built to verify its feasibility. Experimental results show that the control chip can be powered perfectly, and the deviations of output voltage and current are within $\pm 1.3\%$ and $\pm 2.5\%$ under different input and load conditions, whereas maximum conversion efficiency can reach a level of 78.9%.**

***Index Terms*—AC–DC converter without auxiliary winding, constant voltage/current (CV/CC), primary-side charging, primary-side regulation (PSR).**

I. Introduction

FLYBACK converter is a commonly used low power energy conversion circuit. Due to its simple structure, low cost and low standby power consumption, it is very widely adopted as the ac–dc power adapters, such as the battery charger of cellphone and laptop [1]–[4].

With the rapid growth of the portable electronic products, the demand for ac–dc power supplies has also been increasing rapidly in recent years. In these commercial applications, higher performance and lower cost are always pursued, which are also exactly the current developing trend of the flyback converters [5]–[9].

Compared to the traditional secondary-side regulation (SSR) topology, currently more flyback converters adopt primary-side regulation topology [10]–[13], whose structure is shown in Fig. 1. Because it does not need optical coupler, it has smaller size and lower cost. In this kind of topology, the transformer contains three windings, where primary and secondary windings are used for the power conversion, while auxiliary winding senses output information and powers the chip. However, extra winding increases the complexity of the transformer and power system, resulting in higher cost. Besides, the energy consumed by the auxiliary winding has a bad influence on the conversion efficiency of the transformer, and reduces output accuracy.

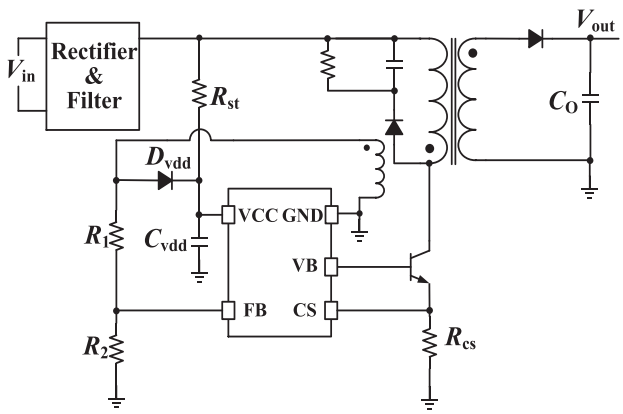

Fig. 1. Traditional PSR flyback converter with three windings.

For the market demand of higher performance and lower cost, a lot of structures to eliminate the auxiliary winding have been proposed in recent years [14]–[16]. Chen *et al.* [14] powered the control chip by the start-up resistor (see $R_{\rm st}$ in Fig. 1), and detecting the output current at the drain of the power MOSFET to regulate output current. However, the large current on the start-up resistor consumes too much energy, leading to large standby power consumption. A digital topology was proposed in [15], which also detects output from the primary side. To power the control chip, an extra power chip was used, which makes system complicated and large. Bai *et al.* [16] used two switching MOSFETs that work alternately, taking the advantage of capacitance bootstrap effect of the power MOS, thus to power the chip through the primary-side current in the end of conduction period of the system. However, primary-side current does not flow through sampling resister (see $R_{\rm cs}$ in Fig. 1) when chip-powering capacitor (see $C_{\rm vdd}$ in Fig. 1) is being charged, which means its peak value cannot be controlled accurately, therefore, decreases output accuracy and causes the security problem.

Based on the previous research, a novel flyback CC/CV converter without auxiliary winding is proposed in this article.

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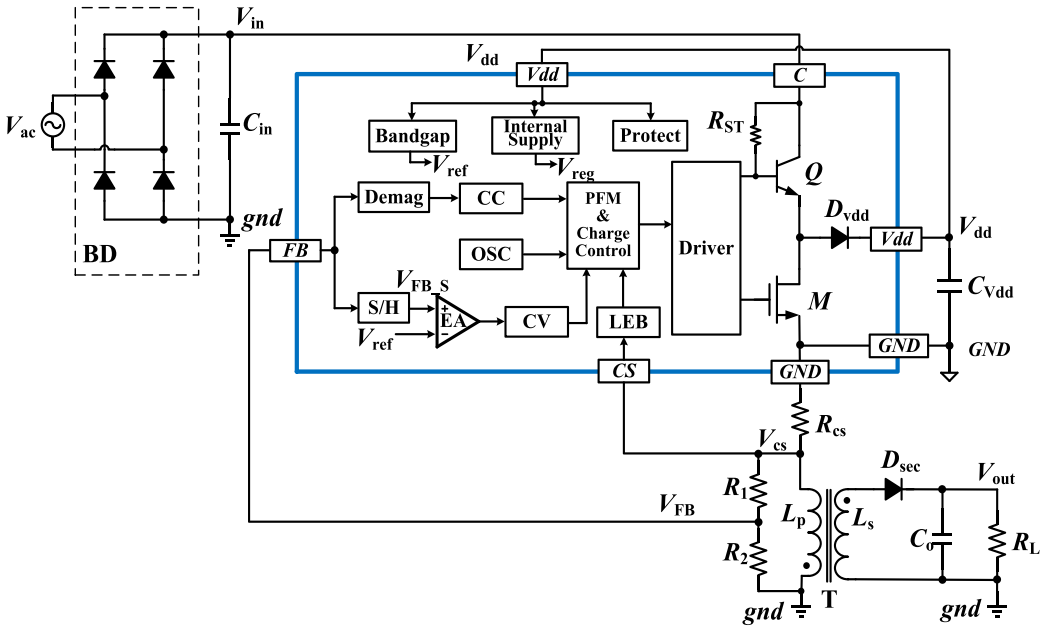

Fig. 2. System diagram of the proposed PSR ac–dc converter.

The converter adopts the PSR structure, sampling output current and voltage from the primary-side inductance, then adjusting switching frequency and primary peak current of the system to regulate the output. Taking the advantage of the base charge storage effect of the power transistor, $C_{\rm vdd}$ is charged at the near end of the conduction period, which increases the chip-powering efficiency. To monitor the primary current on the entire time, $R_{\rm cs}$ is series linked to $C_{\rm vdd}$. Compared to the traditional three-winding flyback, the proposed topology not only realizes higher output accuracy and conversion efficiency, but also eliminates an extra auxiliary winding and several external devices, thus simplifies the system structure, reduces costs, and is more in line with current commercial needs.

This article first introduces the system structure and CC/CV principle in Section II. Then, the driver module and powering method will be presented in Section III. The Section IV analyzes the simulation and experimental results. Finaly, Section V concludes this article.

II. Design of PSR AC–DC Control Chip

A. System Review

The proposed PSR ac–dc converter and the control chip are depicted in Fig. 2. The system only includes two sides. The primary side mainly consists of a rectifier bridge BD, an input capacitor $C_{\rm in}$, a current sensing resistor $R_{\rm cs}$, feedback resisters R_1 /R_2, a chip-powering capacitor $C_{\rm vdd}$, a primary-side inductor L_p, and a control chip. The secondary side consists of a free-wheeling diode $D_{\rm sec}$, a secondary- side inductor L_s, an output capacitor C_0, and a load R_L. It can be seen that compared to the three-winding topology shown in Fig. 1, the proposed converter integrates the start-up resister $R_{\rm st}$ and chip-powering diode $D_{\rm vdd}$ into the control chip, and saves one winding, thus becomes simpler. It should be noted that the ground potential of the chip is different from that of the system, which are labeled as "*GND*" and "*gnd,*" respectively.

The chip mainly contains a power transistor *Q,* an auxiliary switching transistor *M*, a reference voltage module (see Bandgap in Fig. 2), an internal power supply module, a protect module, a sample&hold module (S/H), an error amplifier (EA), a constant voltage controller (CV), a demagnetization detection (Demag), a constant current controller (CC), an oscillator, a leading edge blanking, a PFM&charge controller, and a driver. It should be noted that $R_{\rm cs}$ is linked in series with $C_{\rm vdd}$, which means primary-side current always flows through $R_{\rm cs}$, and can be monitored in real time and precisely controlled by the chip, thus increasing the output accuracy.

The proposed converter works in discontinuous conduction mode (DCM). When $V_{\rm dd}$ is high enough and $C_{\rm vdd}$ does not need charge, *M* keeps on. The key waveforms of this time are shown in Fig. 3, where V_B is driving voltage of *Q*. When system works in the conduction period ($T_{\rm on}$), *Q* turns ON, and the primary-side current I_p increases linearly, storing electromagnetic energy into the transformer. Once I_p reaches to the set threshold value $I_{\rm pp}$, *Q* turns OFF immediately, and system enters the demagnetization period (T_d). Then, energy is passed to the secondary side, and the transformer begins to demagnetize, whereas secondary-side current I_s also decreases from its peak value $I_{\rm sp}$. After this, the system enters the dead period ($T_{\rm off}$), primary side does not work, and the output is supplied by C_o, until next conduction period arrives. $V_{\rm FB}$ is the feedback signal from the primary winding, which characterizes the value of the output voltage and current. Because of leakage inductance of the transformer and parasitic capacitance of the transistor, oscillation occurs when the period switches.

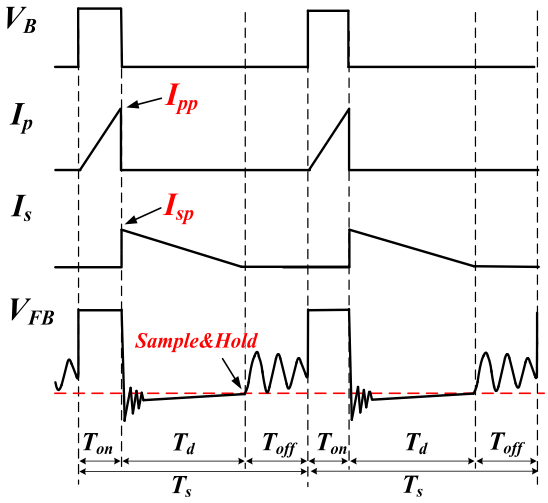

Fig. 3. Key working waveforms of the proposed flyback converter.

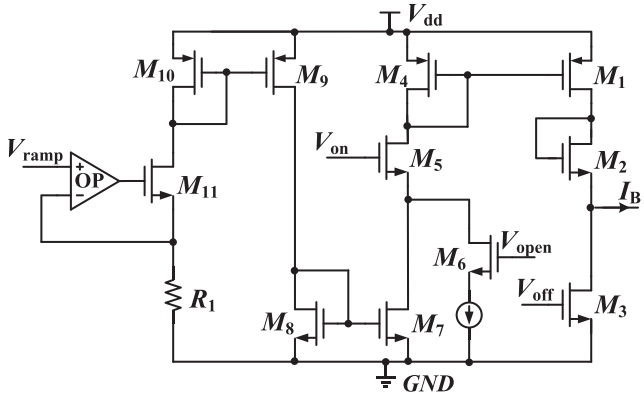

Fig. 4. Schematic of the driver module.

B. Principle of CV&CC Control

During one working cycle, the energy transferred from the input of the system to the output can be expressed as

$$\frac{L_p \cdot {I_{\rm pp}}^2}{2 \cdot T_s} \cdot \eta = \frac{{V_{\rm out}}^2}{R_L} \tag{1}$$

where T_s is the switching period and η is the conversion efficiency. Thus output voltage $V_{\rm out}$ can be calculated as

$$V_{\rm out} = I_{\rm pp} \cdot \sqrt{\frac{\eta \cdot R_L \cdot L_P}{2 \cdot T_s}}. \tag{2}$$

During demagnetization, if not considering the oscillation, the relation of $V_{\rm out}$ and the $V_{\rm FB}$ is

$$V_{\rm FB} \cdot \frac{R_1 + R_2}{R_2} = -\frac{N_P}{N_S} \cdot (V_{\rm out} + V_{\rm fs}) \tag{3}$$

where N_p and N_s are primary and secondary-side turns of the transformer, and $V_{\rm fs}$ is the voltage drop across $D_{\rm sec}$. As the calculation of $V_{\rm FB}$ is relative to *gnd*, and no current flows through $R_{\rm cs}$ during this time, the relation between $V_{\rm FB}$ and $V_{\rm FB\_S}$ can be obtained as

$$V_{\rm FB} - V_{\rm FB} \cdot \frac{R_1 + R_2}{R_2} = V_{\rm FB\_S} \tag{4}$$

where $V_{\rm FB\_S}$ is relative to *GND*. At the end of demagnetization, I_s drops to zero. At this time the control chip samples $V_{\rm FB}$ as $V_{\rm FB\_S}$, which can accurately reflect the value of the output voltage, as Fig. 3 shows. Then, EA compares $V_{\rm FB\_S}$ with a built-in reference voltage $V_{\rm ref}$, and outputs the result to the CV module and PFM module, adjusting T_s and $I_{\rm pp}$. Eventually, $V_{\rm out}$ will keep stable at

$$V_{\rm out} = \frac{N_S}{N_P} \cdot \frac{R_1 + R_2}{R_1} \cdot V_{\rm FB\_S} = \frac{N_S}{N_P} \cdot \frac{R_1 + R_2}{R_1} \cdot V_{\rm ref}. \tag{5}$$

At the moment Q turns OFF, the energy transferred from the primary to the secondary side can be expressed as

$$\frac{1}{2} \cdot \eta_1 \cdot L_P \cdot I_{\rm pp}^2 = \frac{1}{2} \cdot L_S \cdot I_{\rm sp}^2 \tag{6}$$

where η_1 is the conversion efficiency of the transformer. The relationship between L_P and L_S is related to the turns ratio of the transformer, and can be obtained as

$$\frac{L_P}{L_S} = \left(\frac{N_P}{N_S}\right)^2. \tag{7}$$

Then, $I_{\rm out}$ can be calculated as

$$I_{\rm out} = \frac{1}{2} \cdot \frac{T_d}{T_s} \cdot I_{\rm SP} = \frac{1}{2} \cdot \sqrt{\eta_1} \cdot \frac{N_P}{N_S} \cdot \frac{T_d}{T_s} \cdot I_{\rm pp} \tag{8}$$

where $I_{\rm pp}$ is determined by $V_{\rm pp}$ and $R_{\rm cs}$. After acquiring $V_{\rm FB}$, the control chip detects the demagnetization time T_d through the Demag module, and adjusting T_s through CC module and PFM module, ensuring demagnetization duty cycle T_d/T_s keeps constant, thereby achieving constant output current.

As (2) and (8) show, the regulated $V_{\rm out}$ and $I_{\rm out}$ will be influenced by η and η_1. In the traditional three-winding structure, an auxiliary winding is used to charge $C_{\rm vdd}$, which means the energy transferred from primary to secondary side is lessened. What's worse is that the lessened energy will vary with load and input condition. Thus, $V_{\rm out}$ and $I_{\rm out}$ are hard to be regulated very accurately.

III. Chip Powering Principle

A. Design of the Driver Module

The proposed converter adopts a primary-side powering scheme. First, Fig. 4 shows the driver module of the main power transistor Q, where I_B is the base driving current, and it is regulated by the pull-up transistor M_1 and pull-down transistor M_3, which are controlled by $V_{\rm on}$ and $V_{\rm off}$, respectively.

Q starts working when $V_{\rm on}$ turns high. Then, I_B will be controlled by $V_{\rm open}$ and $V_{\rm ramp}$. $V_{\rm open}$ is a start-up signal, generating a high current at the short beginning of $T_{\rm on}$, which is injected into Q and makes it quickly open. $V_{\rm ramp}$ is a ramp signal, which is converted into a ramp current through op, and then passed to M_1 through three current mirrors. $V_{\rm ramp}$ makes I_B rise linearly with primary-side current I_p (I_E), ensuring Q to be switched ON. Compared to the fixed high current, the ramp current can save a lot of power consumption during this process. As Q always works in the saturation region, its equivalent conduct-resistance

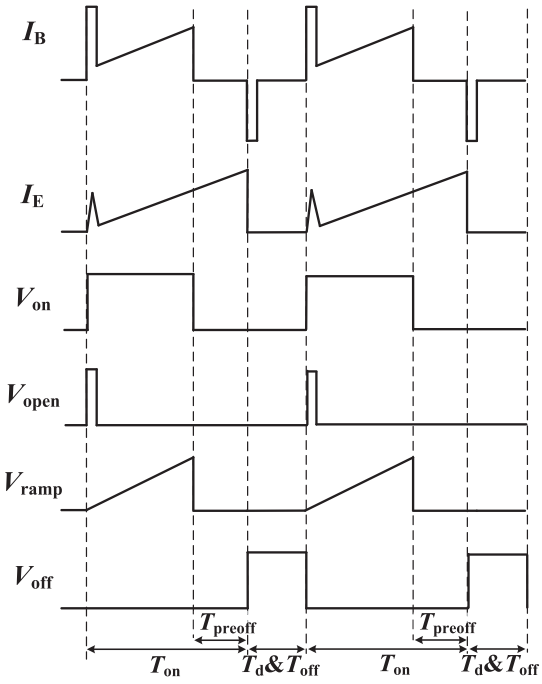

Fig. 5. Key waveforms of driver module.

would hardly rise, thus would not increase the conduction loss of the power system.

$V_{\rm off}$ is the control signal of M_3, which determines the turn-OFF time of Q. The system samples I_p through $R_{\rm cs}$ and feeds it back to the control chip. When it detects that I_p reaches to the shutdown threshold $I_{\rm pp}$, $V_{\rm off}$ will be pulled high. Then, M_3 turns ON, extracting stored carriers from the base of Q, turning it OFF, then system enters the demagnetization period. Key waveforms of this module are depicted in Fig. 5.

When Q turns ON and enters the saturation state, the emitter current I_E will not keep rising if I_B rises above a certain level. At this time there will be a lot of electrons and holes accumulated in the base region. When I_B suddenly drops to 0, these excess stored carriers would be gradually taken away by I_E. During this time Q still remains on, until most of these excess carriers are extracted. This phenomenon is called the "base charge storage effect."

Using this effect, at a short time before Q turns OFF, the circuit pulls $V_{\rm on}$ low and turns M_1 OFF. As M_3 is also OFF, I_B will rapidly drop to 0, which means no current is injected into or drew out of Q. Due to the base charge storage effect, Q will continue conducting. Until I_p rises to $I_{\rm pp}$, M_3 turns ON and turns Q OFF. This period is called the "pre-OFF" period, and it is shown as $T_{\rm preoff}$ in Fig. 5. Its max value can be calculated as

$$T_{\rm preoff\_max} = \tau_s \cdot \ln \frac{\beta \cdot I_B}{I_E} \tag{9}$$

where β is current amplification of Q, and τ_s is storage time. By designing an appropriate pre-OFF time, a large amount of driving current can be saved, thus reducing the power consumption of the chip.

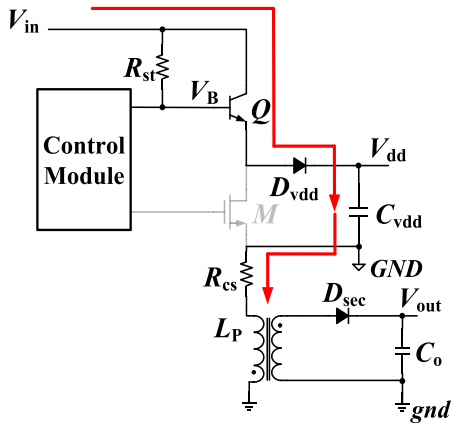

Fig. 6. Circuit diagram of charging time.

B. Chip Powering Strategy

As mentioned above, when $C_{\rm vdd}$ is not being charged, the auxiliary switching MOS M turns ON, and the charging diode $D_{\rm vdd}$ turns OFF, no current flows into $C_{\rm vdd}$. When $V_{\rm dd}$ drops to a low level and $C_{\rm vdd}$ needs charge, the control circuit turns M OFF during $T_{\rm on}$ period. Then, I_p flows through $C_{\rm vdd}$ and reach primary inductor L_P as Fig. 6 shows, charging $C_{\rm vdd}$, and making $V_{\rm dd}$ increase. As the most part of $V_{\rm in}$ still drops on L_p, the transformer can be charged almost unaffected.

The difficulty of this method is how to generate the driving signal V_B. When $C_{\rm vdd}$ is charged, the emitter voltage V_E of Q is lifted, and V_B equals to

$$V_B = V_{\rm BE} + V_f + V_{\rm dd} \tag{10}$$

where $V_{\rm BE}$ is the conduction voltage of Q, and V_f is the voltage drop of $D_{\rm vdd}$. Equation (10) shows that V_B has to be higher than $V_{\rm dd}$. In general, V_B is generated by the driver module of the chip. As I_B is required to be quite large, a high-power charge pump is needed to generate the driving signal, which will seriously increase the complexity and layout area of the chip, and it also has bad disturbance to other control signals.

To solve this problem, a bootstrapping method is proposed. Using the base charge storage effect, $C_{\rm vdd}$ will be charged in $T_{\rm preoff}$ period. Under the influence of parasitic capacitance, V_B will self-rise to the required high potential, keeping Q constant. The specific working process is expounded as following.

When the conduction period $T_{\rm on}$ comes, Q and M turn ON together, and $C_{\rm vdd}$ is not charged. At this time, V_E is connected to *GND* via M, and V_B is at a relatively low voltage level, which can be generated by the chip normally. When system enters pre-OFF period $T_{\rm preoff}$, the current path between the chip and Q is cutoff, so the base node is in a high-impedance state. At the same time, M is turned OFF, then I_p will flow into $C_{\rm vdd}$, and V_E is raised to $V_{\rm dd} + V_f$. Under the effect of parasitic capacitance between BE junction, V_B is also raised up. Since node B is approximately floating, and no charge flows in or out, V_B will keep remaining at this potential, making Q hold on until the end of the conduction period. Then, Q is turned OFF, and the system finishes charging. The key waveforms of this process are shown

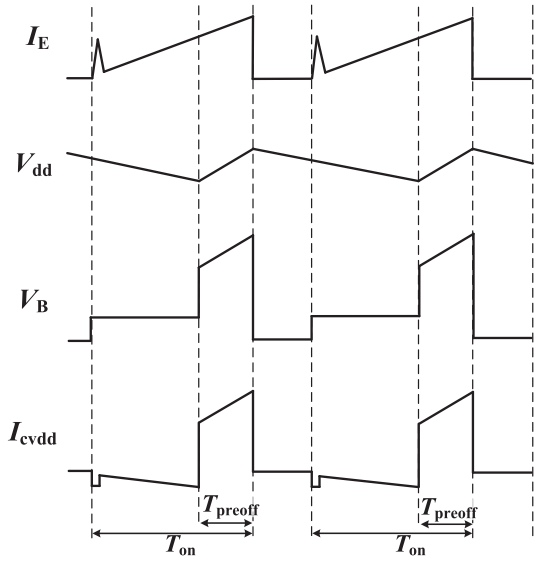

Fig. 7. Key waveforms when C_{vdd} is charged.

in Fig. 7, where I_{cvdd} represents the current on C_{vdd} whose positive direction indicates the current flowing in.

During one T_{preoff} period, the average charging current can be expressed as

$$\overline{I_{cha}} = I_{pp} \cdot \left(1 - \frac{T_{preoff}}{2 \cdot T_{on}}\right). \tag{11}$$

The charging power can be calculated as

$$P_{cha} = V_{dd} \cdot I_{pp} \cdot \left(1 - \frac{T_{preoff}}{2 \cdot T_{on}}\right) \cdot \frac{T_{preoff}}{T_S}. \tag{12}$$

As (12) shows, in order to improve powering capability, it is necessary to increase T_{preoff}. That is, to advance the pre-OFF time point, which can be achieved by increasing I_B, as shown in (9). In this article, T_{preoff} is set to 1/3 of T_{on}. Using this method, the chip can be powered perfectly, and it does not require a charge pump.

IV. Simulation and Experimental Results

Based on the NEC 1-μm HVCMOS process, the control IC was designed by Cadence Virtuoso. In this section, simulation results of driver module and C_{vdd} charging are first given, then the experimental results of a prototype are presented and analyzed.

A. Simulation of Key Modules

Transient simulation result of the driver module is shown in Fig. 8, where I_B is the base current of Q, I_E is the emitter current (which equals to primary side current I_p), and V_{on} is the conduction signal. At the beginning of T_{on}, there is a large current pulse of I_B, which turns Q ON quickly. Then, I_E rises linearly. During the T_{preoff} time, I_B stops being injected, while Q remains ON and I_E still rises. At the end of T_{on}, the driver draws a large amount of current out of the base and turns Q OFF. The max value of I_B before pre-OFF is 42 mA, maintaining Q turning ON 1 μs more, and the max value of I_p (I_E) is 475 mA.

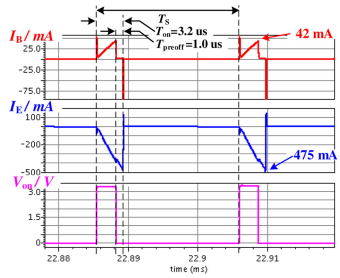

Fig. 8. Transient simulation results of the driver module.

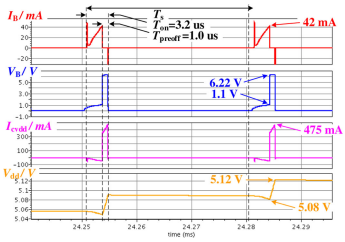

Fig. 9. Key transient simulation waveforms when C_{vdd} is charged.

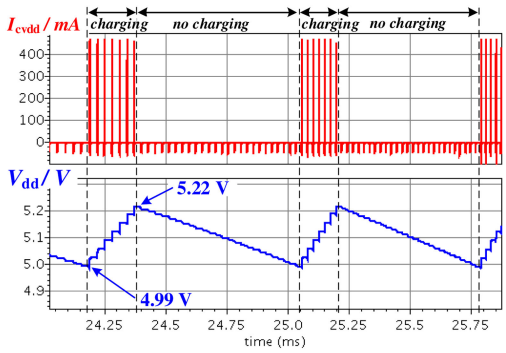

Fig. 10. Transient simulation results of the hysteresis charging control scheme.

Fig. 9 is the transient simulation result when C_{vdd} is being charged, where V_B is base driving voltage of Q, I_{cvdd} is the current on C_{vdd}, and V_{dd} is the chip supply voltage. During T_{preoff}, M turns OFF, and I_p is redirected to C_{vdd}. At the same time, the pull-up MOS and the pull-down MOS in the driver module are both turned OFF, making the base node of Q floating. Influenced by the BE junction capacitance, V_B jumps from 1.1 to 6.22 V. After 1-μs charging, V_{dd} increases from 5.08 to 5.12 V.

In practical, the power consumption of the chip will vary with input and load. In order to make the power supply equal to the consumption, a hysteresis charging control scheme is designed. The simulation result is showed in Fig. 10. It can be seen that when V_{dd} drops to about 4.99 V, system starts charging the C_{vdd}. Once V_{dd} rises to 5.22 V, system stops charging. With such a control scheme, V_{dd} can always remain between approximately 5$\sim$5.2 V.

B. Experimental Results of the System

The layout of the control IC is shown in Fig. 11. Key modules are labeled, where pins are italic. The power transistor Q

TABLE I
KEY COMPONENTS AND PARAMETERS

Components	Symbol	Value or Specification
Bridge rectifier	BD	1N4007
Primary-side inductance	L_p	1.7 mH
Transformer core	T	EE13
Transformer turn's ratio	N_P / N_S	135 / 9
Feedback resistor	R_1 / R_2	6.8 kΩ / 200 kΩ
Primary current sense resistor	R_{cs}	1.3 Ω
Output capacitor	C_0	1000 uF
Secondary-side Freewheel diode	D_{sec}	PFS5L40

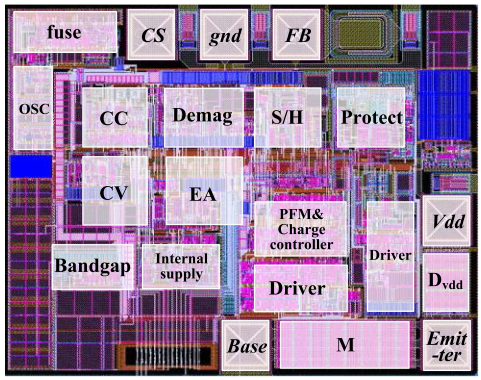

Fig. 11. Layout of the control IC.

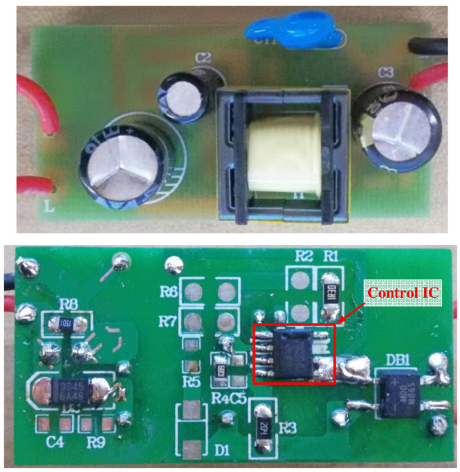

Fig. 12. Photographs of the PCB prototype.

is an independent device and packaged together with the chip, so it is not shown in the layout. Besides, a 5-V/1-A prototype is fabricated. The PCB photographs are shown in Fig. 12. Its size is 4.36 × 2.15 cm. It can be seen that only a few external devices are used on the PCB, and its size is relatively small. The key parameters of the components are listed in Table I.

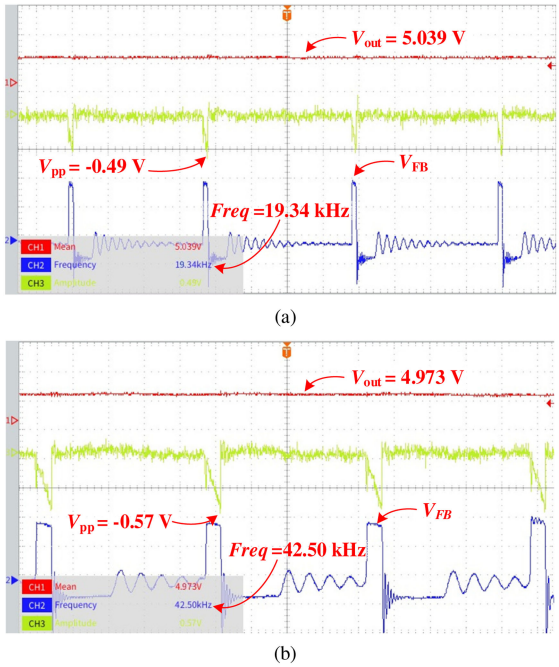

Fig. 13. Experimental results under different load currents in 230 V rms and 50 Hz-V_{in}. (a) $I_{out} = 0.3$ A. (b) $I_{out} = 0.7$ A.

The key waveforms under 230 V rms input are shown in Fig. 13, and the load current I_{out} are (a) 0.3 A and (b) 0.7 A, respectively. The three waveforms from top to down are V_{out}, V_{cs}, and V_{FB}, where V_{cs} is the voltage drop cross R_{cs}. The switching frequency and the primary peak voltage V_{pp} are indicated as well. As the chip adopts floating ground structure, V_{cs} becomes negative voltage to the chip. It can be seen that as I_{out} rises, the system increases T_{on} (reflected in the increase of V_{pp}) and the switching frequency, thus to ensure that V_{out} is always maintained at around 5 V. The switching frequency in this work can vary from 700 Hz (no load) to 65 kHz (full load).

Fig. 14 shows the curves of V_{out} verse I_{out} at 90 V rms/60 Hz- and 265 V rms/50 Hz-input, respectively. It shows that the proposed circuit has good accuracy on output voltage in the CV mode, where the deviation is limited to ±1.3%. When I_{out}

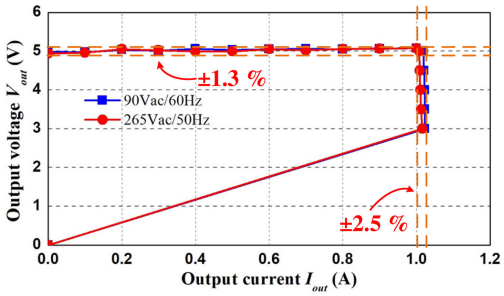

Fig. 14. Load characteristics of the system under 90 V rms-60 Hz and 265 V rms-50 Hz $V_{\rm in}$.

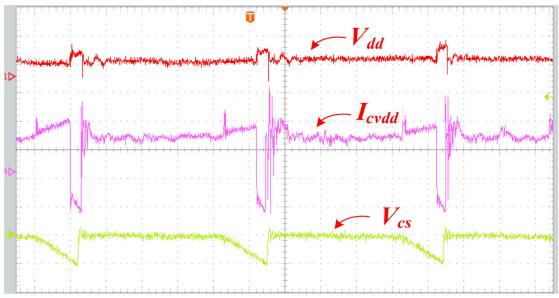

Fig. 15. Measured waveforms when $C_{\rm vdd}$ is being charged in 230 V rms and 50 Hz-$V_{\rm in}$.

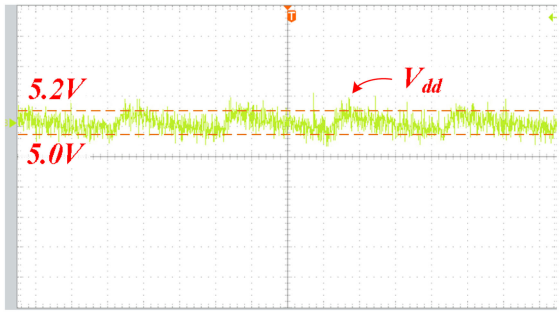

Fig. 16. Measured waveform of hysteresis charging in 230 V rms and 50 Hz-$V_{\rm in}$.

becomes larger than 1 A, the system switches to CC mode, and the current deviation is less than ±2.5%.

To verify the charging process of $C_{\rm vdd}$, Fig. 15 shows the test curves of $V_{\rm dd}$, $I_{\rm cvdd}$, and $V_{\rm cs}$. Here the positive direction of $I_{\rm cvdd}$ indicates the current flowing out of $C_{\rm vdd}$. It can be seen that in the early period of $T_{\rm on}$, $I_{\rm cvdd}$ rises linearly, indicating that a large-current flows out of $C_{\rm vdd}$, which is used as the driving current of Q. In $T_{\rm preoff}$ time, Q turns OFF, leading I_p flows into $C_{\rm vdd}$, so there is a negative high pulse of $I_{\rm cvdd}$. Affected by the equivalent series resistance (ESR) of $C_{\rm vdd}$, there is a small step of $V_{\rm dd}$ during charging. When the charging is finished, the step disappears.

In order to verify the hysteresis charging control, Fig. 16 shows the test waveform of $V_{\rm dd}$. It can be seen that by intermittently charging $C_{\rm vdd}$, system can always maintain $V_{\rm dd}$ at about 5∼5.2 V, which is consistent with the simulation result.

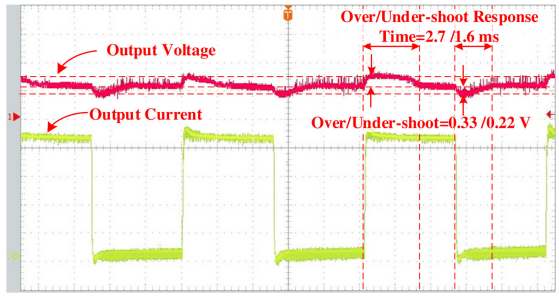

Fig. 17. Measured waveforms when load steps in 230 V rms and 50 Hz-$V_{\rm in}$.

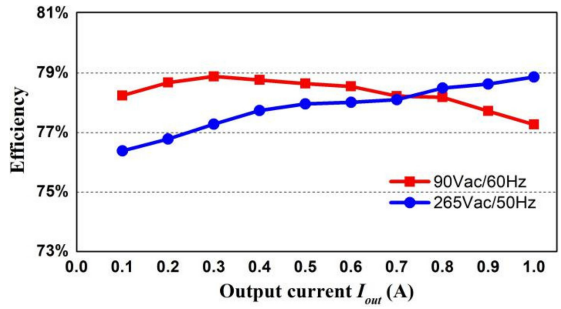

Fig. 18. Efficiency versus $I_{\rm out}$ under 90 V rms/60 Hz-input and 265 V rms/50 Hz-$V_{\rm in}$.

In practical applications, load jumping always occurs. In order to verify the dynamic capacity of the system, the relative test was made under 230 V rms/50 Hz-$V_{\rm in}$ and the results are shown in Fig. 17. Here $I_{\rm out}$ jumps periodically between 0.1 and 0.9 A. It can be seen that $V_{\rm out}$ will return to 5 V after a short time. The max overshoot and undershoot are 0.33 and 0.22 V, whereas their response time are 2.7 and 1.6 ms, respectively.

The conversion efficiency is tested at 90 V rms/60 Hz- and 265 V rms/50 Hz-input as shown in Fig. 18. Overall, the efficiency is between 76.5% and 78.9%.

The comparison results with the existing method are shown in Table II. It can be seen that compared with the traditional three-winding structure, the proposed two-winding converter eliminates one winding and several external components, so the cost is lower, and the output accuracy and conversion efficiency are slightly improved as well. Compared with the two-winding structure of [14] and [15], the proposed converter can achieve not only constant current output, but also constant voltage output, which can better meet the need of the consumer electronics market.

V. Conclusion

In this article, a CC/CV ac–dc converter without auxiliary winding is proposed. The output information is sampled from the primary side inductor, and the ON-time and the working frequency of the system are adjusted to regulate output voltage or current. During the pre-OFF period, the driving signal is generated using the base charge storage effect of the power bipolar transistor, and the chip-powering capacitor is charged by primary side current. Compared with the traditional flyback converter, the proposed converter is simpler in structure, lower

TABLE II
COMPARISONS BETWEEN THE PROPOSED METHOD AND THE PRIOR ARTS

Parameter	This work	[12]	[13]	[14]	[15]	[16]
Structure	Two windings	Three windings	Three windings	Two windings	Two windings	Two windings
Output	CC&CV	CC&CV	CC&CV	CC	CC	CC&CV
CV accuracy	±1.3%	±2.5%	±1.5%	-	-	±2%
CC accuracy	±2.5%	±5%	±3%	±1 %	<5%	±2%
Efficiency (Condition: output of 5 W)	76.5%~78.9%	-	76.5%~78%	~84%(output of 3 W)	68%	76.29%~79.15%
No-load loss	45~97 mW	-	-	142 mW	-	<70 mW

in cost, and higher in performance, at the price of a little more complicated control chip.

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