A Reduced-Switch-Count Family of Soft-Switched High-Frequency Inductive AC-Link Converters

Khalegh Mozaffari, *Member, IEEE*, and Mahshid Amirabadi, *Member, IEEE*

***Abstract*—This article introduces a new family of partial-resonance high-frequency ac-link converters with a reduced number of switches, which contributes to enhanced reliability and reduced size. The proposed family of converters can be configured to interface various number of single-/multiport dc and/or single-/multiphase ac systems of sources and loads through a partial-resonance parallel *LC* link. The *LC* link is composed of a small inductor and a very small ac capacitor without the use of bulky and short life-cycle electrolytic capacitors. The high-frequency ac link is responsible for transferring power between different ports of the system entirely or partially as well as realizing zero voltage switching for all the power switches/diodes over the full load range, which results in minimized stress over the switches as well as low electromagnetic interference (EMI). This class of converters, which only employs two-quadrant switches, is inherently bidirectional with voltage step-up/step-down capability. It allows variable frequencies and power factors between the input and output terminals in one stage of power conversion. The proposed converters can function in buck–boost, buck, and/or boost modes of operation to step up and/or step down the input voltage. Functioning in buck or boost modes of operation can significantly reduce the link peak current and voltage, contributing to reduced power loss, size of components, voltage/current stress of power switches/diodes, and EMI. Furthermore, the proposed converters are robust against the open-circuit/short-circuit problems of input, output, and link inductors/capacitors, which place emphasis on improved reliability of the system. They are also capable of minimizing poor recovery issues and related losses of the body diodes of switches by using external fast recovery diodes in series with the main switching devices. In view of these features, this class of converters is expected to exhibit improved reliability, efficiency, power density, functionality, and flexibility compared to most existing power converters. A current modulation approach is also developed for each function to regulate the input and output currents on a switching cycle-by-cycle basis. A detailed performance analysis to investigate the challenges of each function in terms of frequency, power factor, and voltage amplitude is presented. The effectiveness of the proposed configurations along with the modulation schemes is verified theoretically using simulation software and experimentally via a low-power laboratory prototype at different operating conditions.**

***Index Terms*—AC–AC converter, ac–dc converter, ac-link converter, high-frequency ac link, inverter, reduced switch count, reliability, three-phase, zero voltage switching (ZVS).**

Manuscript received June 15, 2019; revised October 15, 2019 and December 16, 2019; accepted December 29, 2019. Date of publication January 9, 2020; date of current version April 22, 2020. Recommended for publication by Associate Editor T. Mishima. *(Corresponding author: Khalegh Mozaffari.)*

K. Mozaffari is with the Enphase Energy Inc., Austin, TX 78758 USA (e-mail: kmozaffari@enphaseenergy.com).

M. Amirabadi is with the Electrical and Computer Engineering Department, Northeastern University, Boston, MA 02115 USA (e-mail: m.amirabadi@northeastern.edu).

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.2965582

I. Introduction

AC–AC power converters are the major parts of many industrial applications, such as variable-speed ac drives, solid-state transformers, direct conversion systems in wind generators, power regulators, and dynamic voltage restorers to perform voltage/power regulating, isolating, conditioning, and filtering under fixed/variable frequency condition. Double-stage dc-link back-to-back active front-end converters [1] and [2], which include an active front-end rectifier, dc-link capacitors, along with a pulsewidth modulation (PWM) inverter, are the most industrially established topology to supply a load with an arbitrary voltage and frequency. This is mainly because the converter stages are to a large extent decoupled for the control process, which gives rise to control structure simplicity and flexibility. However, the energy storage element in the form of bulky and short life-cycle electrolytic capacitors implemented in these converters degrades the reliability of the system. Employing external three-phase low-frequency transformer, which is very bulky and heavy with the high loss [3], for galvanic isolation and a massive low-pass filter [4] at the front end are other drawbacks of the converters. To maximize the functionality of these converters, another stage, which is composed of a dc–dc converter with high-frequency isolation, as a middle power stage is added to the converter. The isolated stage can be a parallel resonant [5], series resonant [6], series/parallel resonant [7], *LLC* resonant [8], *CLLC* resonant [9], or dual-active bridge [10]. However, these multistage converters suffer from complex circuit configuration with a large number of passive components in addition to reduced system efficiency and reliability.

Direct PWM ac–ac converters, which are originally derived from their dc–dc counterparts, are other candidates for ac–ac power conversion. These types of converters include buck-type [11], boost-type [12], buck–boost type [13], Cuk-type [14], *Z*-source [15]–[17], switched-capacitor [18], [19], and switching cell [20]–[23] ac–ac converters to perform voltage regulation. The proposed switched-capacitor power converters in [18] and [19], which are composed only of capacitors and switches without using any magnetic components, can achieve a significant size reduction. However, the voltage gain in these converters is not flexible. Although direct PWM ac–ac converters offer single-stage power conversion, simple circuit configuration, and ease of

control, they are applicable where only voltage regulation with the fixed frequency operation is required. Alternatively, matrix converters, which allow the conversion of a fixed three-phase ac source to an alternative flexible three-phase ac load with variable amplitude and frequency without intermediate dc-link capacitors, are advanced. Due to their remarkable features of single-stage power conversion, bidirectional power transfer, and controllable input power factor, effort devoted to the studies of matrix converters focusing on their modeling and control [3], [24]–[26], topological development [27]–[29], and applications [30], [31]. However, they have achieved low market penetration due to their inherent shortcomings, including low/limited voltage transfer ratio, commutation problem, protection challenge, isolation issue, and complex modulation [32].

Nonetheless, all of these existing ac–ac converters are hard-switched, which leads to high switching losses, high stress over the power semiconductors devices, significant electromagnetic interference (EMI), and consequently a lower efficiency and reliability. Soft-switched high-frequency partial-resonance ac-link converters have attracted an increasing interest as an outstanding solution for ac–ac power conversion due to many practical advantages, such as fast dynamic response, step-up/step-down capability, high efficiency, low EMI, compact size, absence of electrolytic capacitors, small link components, and high reliability. The topologies proposed in [33]–[37], which employ two-quadrant switches, experience a long resonating interval during which no power is transferred, and this can negatively affect the performance of the converter. The link inductor current in these configurations has a dc component as a result of charging and discharging the link inductor in only one direction. A modified configuration to allow the link inductor to be charged and discharged in both positive and negative directions at the cost of utilizing four-quadrant switches is proposed in [38] and [39]. As a result, the link inductor can optimally be utilized and a lower total harmonic distortion (THD) can be ensured. However, this topology requires a large number of switches, 24 unidirectional switches. Several reduced-switch versions of this configuration called sparse [40], ultra sparse [41], and extremely sparse [42], [43] parallel ac-link converters are reported in the literature. However, these parallel ac-link configurations [38]–[43] may face challenges for medium-power and high-power applications due to discontinuous switch currents with considerable peak values, which result in high power loss and stress over the main switching devices. To solve this drawback, a multifunction class of series ac-link converters is recently introduced in [44], which can significantly reduce the peak of the link current. However, this family of converters requires 24 unidirectional switches and introduces a complex control structure. Moreover, they are vulnerable to short-circuit of input, output, and link capacitors, which can cause large current spikes over the switches and consequently degrade the reliability.

To enhance reliability, decrease volume, and improve power density of partial-resonance ac-link converters while maintaining high performance, an innovative class of high-frequency inductive ac-link converters with a reduced number of switches is proposed in this article. This single-stage family of converters, which only employs two-quadrant switches, integrates functionalities of buck, boost, and buck–boost modes of operation. These functionalities enable the converter to partially or entirely transfer the power from the input side toward the output side through a small link inductor. It features step-up/step-down capability, bidirectional power transfer, modular structure, controllable input and output power factors with arbitrary frequencies. The proposed converters, which can be configured to interface various single- and/or multiport dc and/or single- or multiphase ac sources and loads simultaneously, have the advantages of providing sinusoidal output voltage with extremely low THD and achieving zero voltage switching (ZVS) of all the power switches over the full load range regardless of the line and load conditions via using a very small ac film capacitor connected in parallel with the link inductor. The total number of active switches in the proposed three-phase ac–ac configuration is 16, thus leading to a reduction in the number of switches by 33% when compared to its counterpart converter proposed in [44]. The potential advantage of the proposed converters in terms of reducing the number of active switches and consequently gate drives and cooling system can be fully realized when a multiport operation is demanded. They are immune from short-circuit and open-circuit problems of input, output, and link capacitors and inductors in addition to eliminating the problems associated with reverse recovery of body diodes of switches including their corresponding losses. As a result, further improvement on the reliability of the system can be achieved. Furthermore, a new modulation scheme, which offers a simpler control algorithm, for each function of the converter is developed. A detailed analysis is also performed to investigate the performance and challenges of each function under different operating conditions. Detailed operating principles and modulation approaches of the proposed converters along with the simulation and experimental validations are presented in this article.

II. Proposed Family of Converters

Fig. 1 demonstrates three typical circuit configurations of the proposed family. Fig. 1(a)–(c) illustrates a three-phase ac–ac configuration, a generic multiphase configuration transferring power from an m-phase source to an n-phase load, and a typical multiport configuration of the proposed family interfacing a dc source, a three-phase ac source, a dc load, and a three-phase ac load. While only three configurations of the proposed family are presented in this article, it can be configured to interface various single-/multiport dc and/or single-/multiphase ac sources and/or loads for other applications as well. For instance, by adding one switch and removing one phase leg from the input and output switch bridges, the topology presented in Fig. 1(a) can be reconfigured to interface a photovoltaic (PV) array, battery bank, and single-phase ac load for a stand-alone PV system. Similarly, by adding additional bidirectional/unidirectional dc and/or ac bridges a multiport configuration for microgrid applications can be realized. This family of converter has a modular structure, which can empower multilevel configurations for high-voltage high-power applications. Moreover, the modular nature of the proposed family of converter in terms of reducing the number of active switches results in a total cost reduction and a more

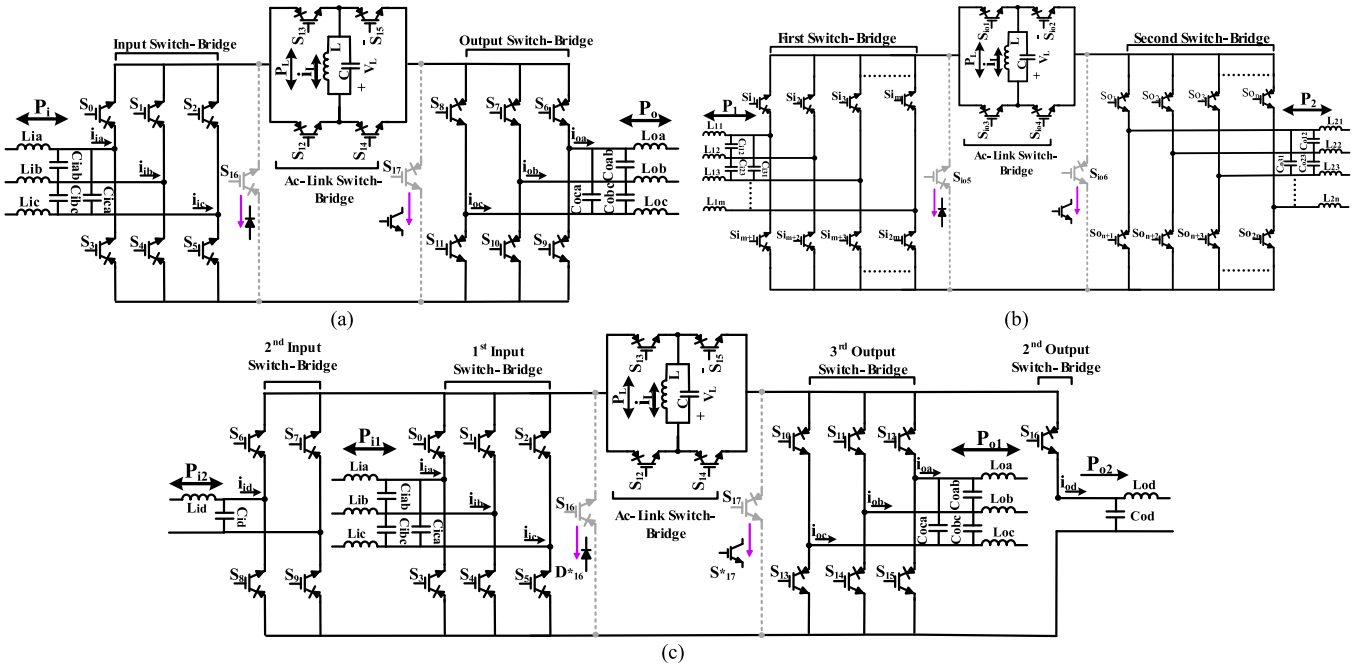


Fig. 1. Proposed partial-resonance inductive ac-link converter topologies. (a) Proposed bidirectional three-phase ac–ac configuration. (b) Proposed bidirectional generic multiphase $m \times n$ configuration. (c) Multiport configuration of the proposed family.

compact design, which can be fully realized when multiple sources and/or loads are required. For instance, with the proposed family of converter when a multiport configuration, as presented in Fig. 1(c), is demanded, the number of switches reduces from 33 to 21 compared to its counterpart [44].

In these families of converter, transferring power entirely or partially is accomplished via the link inductor L. The link capacitor C is connected in parallel across the link inductor to provide partial resonance and consequently reinforce the converter with the soft-switching operation.

The proposed converters consist of an input switch bridge, an output switch bridge, an ac-link switch bridge, an *LC* resonance tank, and two low-pass filters. The input, output, and ac-link switch bridges comprise switches that have bidirectional voltage blocking capability but conduct current in one direction. Each switch can be implemented with a series combination of an insulated-gate bipolar transistor (IGBT)/MOSFET with a diode or a reverse blocking IGBT (RB-IGBT). RB-IGBTs are currently available in the market. In this converter, RB-IGBTs are preferable due to offering a lower total ON-state voltage and consequently lower conduction losses, and providing a more compact converter design without any module customization. The resonance tank comprises a parallel connection of a small ac capacitor and an inductor. Power transfer between different ports of the system partially or entirely is carried out by the link inductor. The link capacitor facilitates soft-switching operation for all power switches/diodes. The ac-link bridge is responsible to facilitate charging and discharging the link inductor in both positive and negative directions. The small low-pass filters are embedded at the front and load ends of the converter to mitigate high-frequency harmonics. In this family of configurations, in order to achieve a higher level of efficiency, two additional semiconductor devices, S_{16}/D^*_{16} and S_{17}/S^*_{17}, as shown in Fig. 1, can be placed across the ac-link switch bridge. For the applications where bidirectional power flow is demanded, two bidirectional voltage blocking switches, S_{16} and S_{17}, are employed, whereas they can be replaced with a diode D^*_{16} and a unidirectional-blocking forward-conducting switch S^*_{17} for unidirectional power flow applications.

III. Operating Principles of the Proposed Family of Converters

A. Overall Description of the Proposed Family

In this family of converters, the charging and discharging occur within the same switching period to regulate the input and output currents. The operation of the converter is composed of several active and resonating modes depending on the configuration. Depending on the direction of the power flow, the link inductor is partially or fully charged through the input phases, which serve as a source, and then the link inductor is discharged into the output phases, which serve as a load. By exchanging the input and output modes, the reverse power flow from the output to the input can be realized although the converter utilizes unidirectional current conducting switches. In this converter, charging and discharging of the link inductor in both positive and negative directions are carried out, leading to an alternating link current. The alternating link current results in better utilization of the link inductor and a lower level of THD.

In this converter, there is a partial-resonance mode, which is caused by a resonance of inductance and the capacitance of the link, between each active mode to facilitate a zero-voltage turn-ON and a soft turn-OFF for all the power switches/diodes. The frequency of charge and discharge of the link inductor in a

complete inductor current cycle is called the link frequency f_L and is typically much higher than the input/output line frequencies. The proposed family of converters can function in buck, boost, or buck–boost modes of operation, and a combination of these modes of operation is also feasible. Higher efficiency can be obtained when the converter is operated under buck or boost function; however, they impose some limitations in terms of frequency, voltage, and power factors, depending on the configuration and the modulation technique. On the other hand, arbitrary power factors and frequencies at the input and output sides along with voltage step-up/step-down capability can be achieved in buck–boost function, but a lower conversion efficiency is expected with this function.

Since all the topologies derived from this family follow the same operation, this article only focuses on the three-phase ac–ac configuration, as shown in Fig. 1(a). In the proposed three-phase ac–ac converter, each charging mode and discharging mode is split into two separate modes. This means that during one-half cycle, all three input and output phases are involved, which allows to have more control on the input and output currents, achieve higher performance, and minimize the input and output filter requirements. In this way, the converter has 16 modes of operation including eight active and eight short partial-resonance modes to create a soft transition between active modes. Fig. 2 illustrates a typical full cycle of the link current i_L, link voltage v_L, and unfiltered input i_{ia}, i_{ib}, i_{ic} and output i_{oa}, i_{ob}, i_{oc} currents in buck–boost, boost, and buck functions of this configuration on an interval over a line cycle.

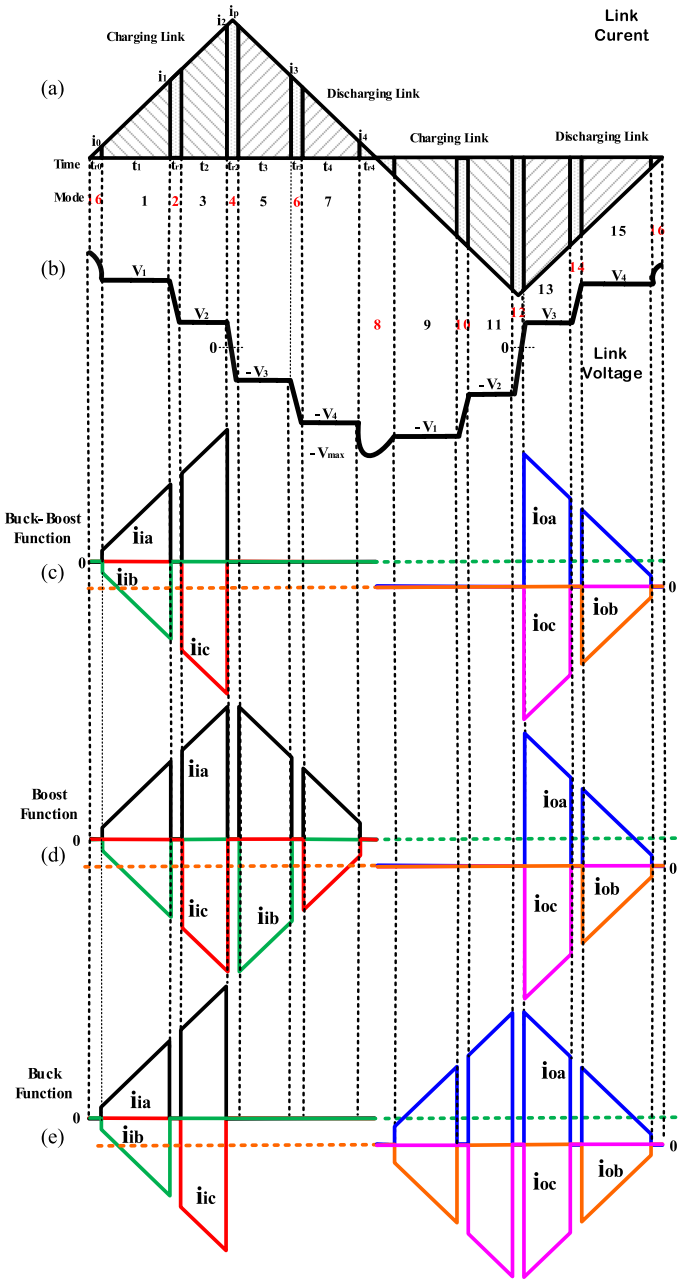


Fig. 2. Typical waveforms of the proposed three-phase ac–ac converter on the interval that $|v_{ian}^{+}| > |v_{ibn}^{-}| > |v_{icn}^{-}|$ and $|v_{oan}^{+}| > |v_{obn}^{-}| > |v_{ocn}^{-}|$ during modes 1–16. (a) Link voltage. (b) Link current. (c) Unfiltered input and output phase currents in buck–boost function. (d) Unfiltered input and output phase currents in boost function. (e) Unfiltered input and output phase currents in buck function.

B. Behavior of the Proposed Three-Phase AC–AC Configuration

In this section, the behavior of the proposed soft-switched bidirectional ac-link three-phase ac–ac configuration in the forward power flow in buck, boost, and buck–boost functions using the developed switching algorithms is discussed. In a three-phase balanced system, since the arrangement of phase and line-to-line voltages and currents in terms of the highest, second highest, and lowest values changes every 30° periodically, a specific interval needs to be considered to investigate the behavior of the converter accurately. Here, the third course of 30° is assumed. This interval happens when the reference current of phase a i_{ia}^{*} at the input side and phase b i_{ob}^{*} at the output side have the highest amplitudes with a positive polarity, the reference current of phase b i_{ib}^{*} and phase c i_{ic}^{*} at the input side, and the reference current of phase c i_{oc}^{*} and phase a i_{oa}^{*} at the output side have the second highest and lowest amplitudes with a negative polarity, respectively. In order to charge and discharge the link inductor via all the input phases and output phases in half of the link cycle, one of the phases at the input side and output side, which are the phases carrying the highest amplitude of current, is maintained common during the whole link cycle. In a balanced three-phase system, in order to satisfy input–output power balance of the converter, only two of the phase pairs at the input side and output side require to stay connected to the link in each link cycle. After determining the common mode at the input and output sides, the order in which the other two phases are naturally selected depends on the amplitude of the voltages across the possible phase pairs. Consequently, it is assumed that at the input side $|V_{iab}|$, the voltage across the input phase pair ab, is higher than $|V_{iac}|$, the voltage across the input phase pair ac, and at the output side $|V_{obc}|$, the voltage across the output phase pair bc, is higher than $|V_{oba}|$, the voltage across the output phase pair ba. The polarities of V_{iab}, V_{iac}, V_{obc}, and V_{oba} are all considered to be positive. The positive direction of current in the link and the input and output phases are

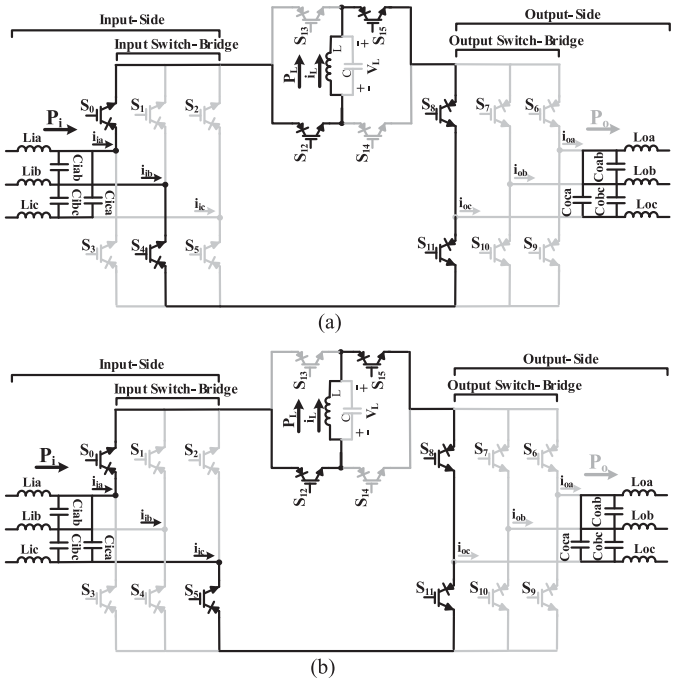


Fig. 3. Behavior of buck–boost and boost functions in modes 9 and 11. (a) Mode 9: when link inductor is being charged from phase pair iab. (b) Mode 11: when link inductor is being charged from phase pair iac.

defined from top to bottom and left to right, respectively. Due to behavioral similarities of the converter between operating modes 1–8 and operating modes 9–16, the behavior of the converter when the link current is negative, which means that the converter is operating in modes 9–16, is only detailed.

1) Modes 8–12. Buck–Boost and Boost Functions: In buck–boost and boost functions, the power is fully transferred from the input phases to the link inductor during modes 1, 3 with a positive link current and modes 9, 11 with a negative link current. Before starting mode 9, the appropriate switches at the input switch bridge, the link switch bridge, and the output switch bridge are gated-ON during mode 8. According to the assumption, switches S_0, S_4, S_5, S_{12}, S_{15}, S_8, and S_{11} are selected to be gated-ON. When the link voltage is equal to the highest line-to-line input voltage $|V_{iab}|$, all the switches except for switch S_5 become forward biased and start conducting with zero switching loss. Mode 9, as shown in Fig. 3(a), continues to charge the link inductor until the absolute average current delivered to phase *b* over half of the link cycle equals to its reference current. Once this happens, switch S_4 is turned OFF and mode 9 ends. Afterward mode 10, which is a resonating mode, begins, as illustrated in Fig. 4. The link voltage drops slowly with a slope that depends on the link capacitance. This means that voltage across switch S_4 increases slowly. Consequently, switch S_4 experiences a soft turn-OFF. In general, the soft turn-OFF occurs for all the switches in different modes in this converter. Mode 10 is over when the link voltage drops to a value, which is equal to $|V_{iac}|$. Mode 11, as demonstrated in Fig. 3(b), ends when the average condition for phase *a* is satisfied, which coincides with turning OFF switches S_0, S_5. After that, resonating mode 12 initiates and the converter is prepared for discharging modes.

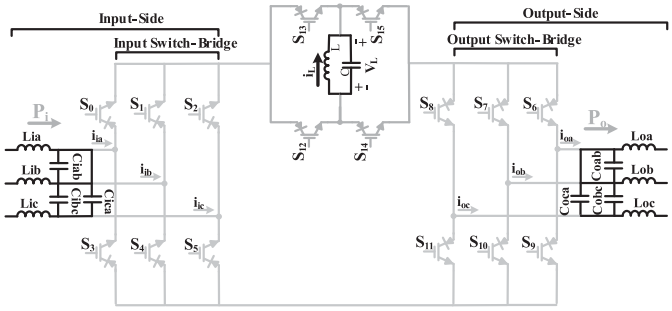


Fig. 4. Modes 8, 10, 12, 14, and 14: when link is resonating.

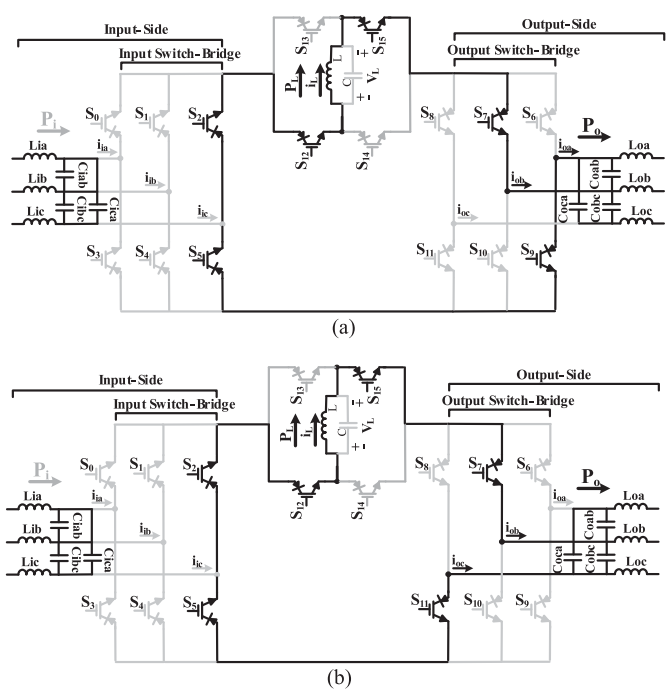


Fig. 5. Behavior of buck–boost and buck functions in modes 13 and 15. (a) Mode 13: when link is being discharged into phase pair *oba*. (b) Mode 15: when link is being discharged into phase pair *obc*.

2) Modes 12–16. Buck–Boost and Buck Functions: Similarly, in buck–boost and buck functions during modes 5, 7 and 13, 15, the power is entirely transferred through the link inductor, which is discharged into the output phases. During mode 12, the link voltage drops and its polarity is reversed. Once this happens, the proper switches S_7, S_9, and S_{11} from the output switch bridge, S_{12} and S_{15} from the link switch bridge, and S_2 and S_5 from the input switch bridge are gated-ON to discharge the link inductor in modes 13 and 15. The proper switches in mode 13, as shown in Fig. 5(a), start to conduct under ZVS conditions as soon as the link voltage is equal to the second highest output line-to-line voltage $|V_{oba}|$. When the current of phase *a* meets its reference, this active mode ends and its corresponding switch S_9 is turned OFF. The link components resonate, and the link voltage starts to fall until the link voltage becomes equal to the highest output line-to-line voltage $|V_{obc}|$.

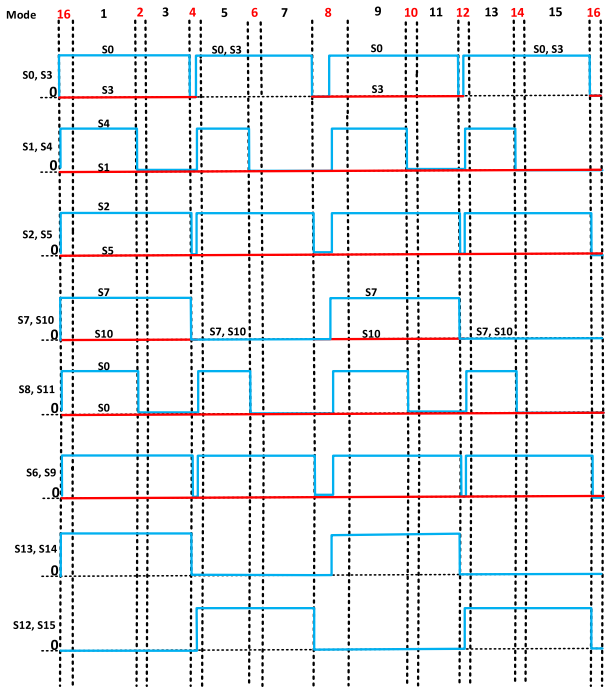


Fig. 6. Gate driver signals in buck–boost function.

At this moment, switch S_{11} starts to conduct and the link inductor is discharged into the load further, as shown in Fig. 5(b).

The link inductor in mode 15 continues to be discharged until the remaining energy in the link is only sufficient to peak the link voltage at $|V_{\max}|$, which is higher than the highest line-to-line voltage at the input side in buck–boost function or the highest line-to-line voltage difference at the input side and the output side in buck function. Subsequently, another resonating mode, which is mode 16, initiates after the termination of this active mode. Under step-up operation in which the amplitude of the output voltage is higher than the input voltage, the link can be fully discharged since the link voltage can always reach a value higher than the highest input voltage after the resonating mode of 16. In this way, ZVS at turn-ON can be always guaranteed as long as the proper incoming switches are turned ON before the start of mode 1. The gate driver signal of the switches in buck–boost function is shown in Fig. 6.

3) Modes 8–12. Buck Function: In buck function during modes 1, 3 and 9, 11, the input power is partially transferred to the link inductor, which is charged by involving both input and output phases. The rest of the input power is directly transferred to the load. Proper switches at the input and output switch bridges corresponding to the highest input and output line-to-line voltages along with switches S_{12} and S_{15} at the link switch bridge are gated-ON during mode 8. According to the assumption, the input phase pair ab and output phase pair bc are connected to the link to charge the link inductor during mode 9 through switches S_0, S_4, S_7, and S_{11}, as shown in Fig. 7(a). The link continues to be charged until the average condition for phase b is met. Subsequently, switches S_4, S_{11} and switches S_5, S_9 are turned OFF and turned ON instead, respectively. This partial

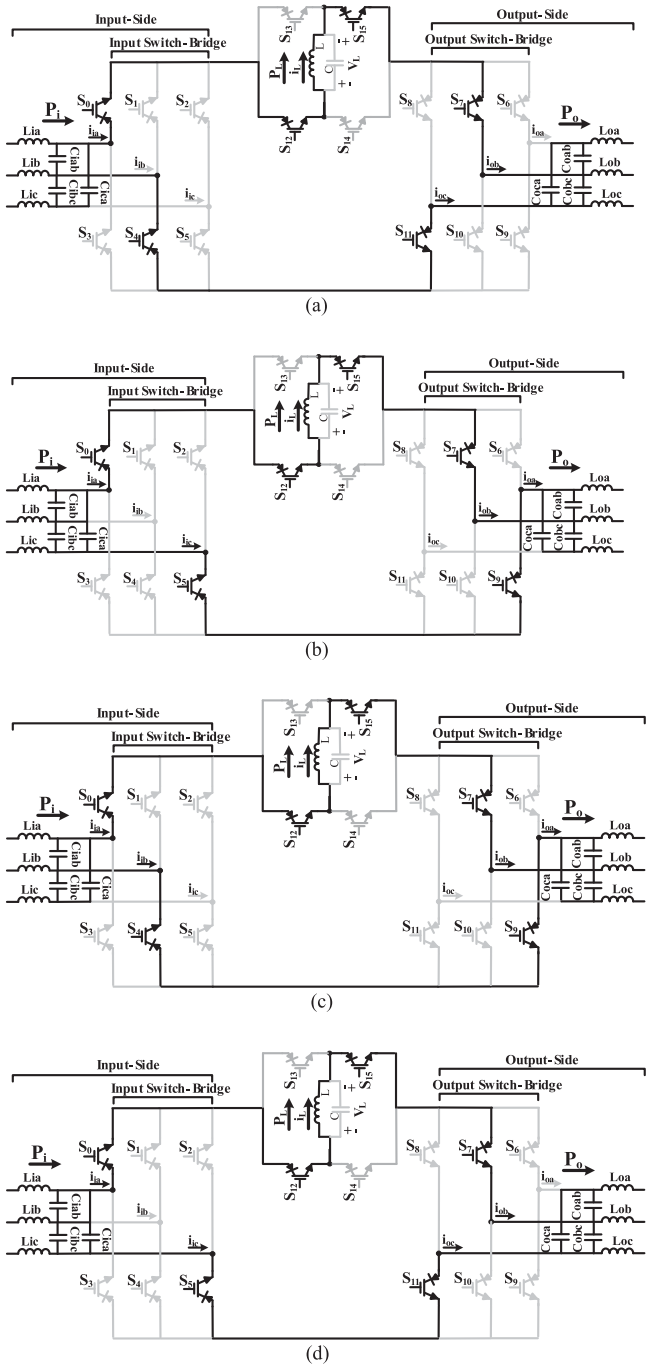


Fig. 7. Behavior of the converter in buck and boost functions. (a) Mode 9 in buck function: link is being charged in buck function through phase pairs iab and obc. (b) Mode 11 in buck function: link is being charged in buck function through phase pairs iac and oba. (c) Mode 13 in boost function: link is being discharged in boost function through phase pairs iac and oba. (d) Mode 15 in boost function: link is being discharged in boost function through phase pairs iac and obc.

resonance continues until the link voltage becomes equal to the $V_{iab} - V_{obc}$, which is negative. At this point, mode 11 begins to charge the link further, as demonstrated in Fig. 7(b). The termination of this mode coincides with satisfying the average condition for phase a. At this moment, all the switches are turned OFF and another resonating mode, which is mode 12, begins.

TABLE I
INPUT-SIDE SWITCH SELECTION BASED ON INPUT REFERENCE CURRENTS IN THREE-PHASE AC–AC CONFIGURATIONS

Input Currents*	$\lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert$	$\lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert$	$\lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert$	$\lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert$	$\lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert$	$\lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert$
i_i^* Polarity	$i_{ia}^{*+}, i_{ib}^{*-}, i_{ic}^{*-}$	$i_{ia}^{*-}, i_{ib}^{*+}, i_{ic}^{*+}$	$i_{ib}^{*+}, i_{ic}^{*-}, i_{ia}^{*-}$	$i_{ib}^{*-}, i_{ic}^{*+}, i_{ia}^{*+}$	$i_{ic}^{*+}, i_{ia}^{*-}, i_{ib}^{*-}$	$i_{ic}^{*-}, i_{ia}^{*+}, i_{ib}^{*+}$
Switch Selection	S_0, S_4, S_5	S_3, S_1, S_2	S_1, S_5, S_3	S_4, S_2, S_0	S_2, S_3, S_4	S_5, S_0, S_1

TABLE II
OUTPUT-SIDE SWITCH SELECTION BASED ON OUTPUT REFERENCE CURRENTS IN THREE-PHASE AC–AC CONFIGURATIONS

Output Currents*	$\lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert$	$\lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert$	$\lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert$	$\lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert$	$\lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert$	$\lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert$
i_o^* Polarity	$i_{oa}^{*+}, i_{ob}^{*-}, i_{oc}^{*-}$	$i_{oa}^{*-}, i_{ob}^{*+}, i_{oc}^{*+}$	$i_{ob}^{*+}, i_{oc}^{*-}, i_{oa}^{*-}$	$i_{ob}^{*-}, i_{oc}^{*+}, i_{oa}^{*+}$	$i_{oc}^{*+}, i_{oa}^{*-}, i_{ob}^{*-}$	$i_{oc}^{*-}, i_{oa}^{*+}, i_{ob}^{*+}$
Switch Selection	S_6, S_{10}, S_{11}	S_9, S_7, S_8	S_7, S_{11}, S_9	S_{10}, S_8, S_6	S_8, S_9, S_{10}	S_{11}, S_6, S_7

4) Modes 12–16. Boost Function: In boost function during modes 5, 7 and 13, 15, similarly the load power is partially provided through the link inductor, which is discharged into the output phases by aiding the input phases. The rest of the load power is provided directly from the input phases during modes 5, 7, 13, and 15. During mode 8, switches S_0, S_4, and S_5 from the input switch bridge, S_7, S_9, and S_{11} from the output switch bridge, and S_{12} and S_{15} from the link switch bridge are gated-ON. As a result, there are four combinations that lead to zero volt-second balance across the link inductor. Consequently, the voltage across the link during modes 5 and 7 can take four cases: $V_{iac} - V_{oba}$, $V_{iac} - V_{obc}$, $V_{iab} - V_{oba}$, and $V_{iab} - V_{obc}$, which are all positive. Among them, the switches corresponding to the highest line-to-line voltage at the input side and switches corresponding with the second highest line-to-line voltage at the output side are automatically selected to discharge the link inductor. In this way, switches S_0, S_4, S_{12}, S_{15}, S_7, and S_9 are activated as soon as the link voltage becomes equal to $V_{iab} - V_{obc}$ to initiate mode 13, as demonstrated in Fig. 7(c). This active mode is terminated when the average current condition is met for phase a, which coincides with turning OFF switches S_4 and S_9. Subsequently, the link components resonate during mode 14. This partial resonance continues until the link voltage is equal to $V_{iac} - V_{obc}$, which has a positive value. As a result, the link inductor is discharged into the output phase pair bc, whereas the input phase pair ac aids transferring the power to the load, as shown in Fig. 7(d). This discharging mode, mode 15, is maintained until the remaining energy left in the link reaches a certain amount to peak the link voltage at $-V_{\max}$. Afterward, all the switches are turned OFF and subsequently resonating mode 16 begins.

In this converter, during the entire switching cycle regardless of the functionality of the converter, ZVS transition for turning ON the incoming switches and soft turn-OFF transition for the outgoing switches are provided without using lossy snubbers. Furthermore, intentionally introduced deadtime and overlap states, which are typically required for transitions of switches in voltage-source and current-source converters, are not needed to be considered in this converter. As a result, the distortion problem at terminals of the converter resulting from the introduced deadtime and overlap times can be avoided. The remaining modes, modes 1–8, are similar to modes 9–16 except that switches S_{13}, S_{14} at the link switch bridge have to be selected during modes 9–16 to charge and discharge the link inductor in a positive direction.

The input and output switch selections based on the input and output reference currents in buck, boost, and buck–boost functions are tabulated in Tables I and II, respectively.

IV. PERFORMANCE ANALYSIS

In this section, the performance of the proposed three-phase ac–ac converter in different functions with different modulation techniques under different operating conditions is analyzed. Limitations of the converter in each function in terms of the input and output power factors, the input and output voltage amplitudes, and input and output frequencies are investigated. For simplicity in the analysis, the following assumptions are made.

1) The link frequency is much higher than the frequency of the ac line voltages such that the ac line voltages can be treated as a constant value in each link period.
2) Resonating modes, which are much shorter than active modes, are neglected.
3) The input and output filter capacitors are large enough so that the ripple of the ac line voltages can be neglected.

The same design procedure presented in [44] can be followed to design the link components for the desirable performance of the proposed converter. The following analysis is made for modes 1–8 and the same analysis can be followed for modes 9–16 with the only difference that the link is charged and discharged in the reverse direction.

A. Buck–Boost Function

The proposed converter in buck–boost function can convert ac electrical power of one frequency into ac electrical power of another frequency with the capability of providing the arbitrary input and output voltage amplitudes, input and output power factors, and bidirectional power flow. For the case that power requires to be transferred from the output terminals to the input terminals, the proposed converter converts the output currents of frequency f_o into input currents of frequency f_i. As there is no direct power transfer from the input side to the output side in buck–boost function and the phase currents are directly controlled, the converter benefit from the indirectly decoupled operation. Thus, the converter can operate at arbitrary input and output power factors and frequencies in addition to providing voltage step-up/step-down capability. In buck–boost function, the charging modes are not affected by a change in the output conditions including the output power factor, output frequency,

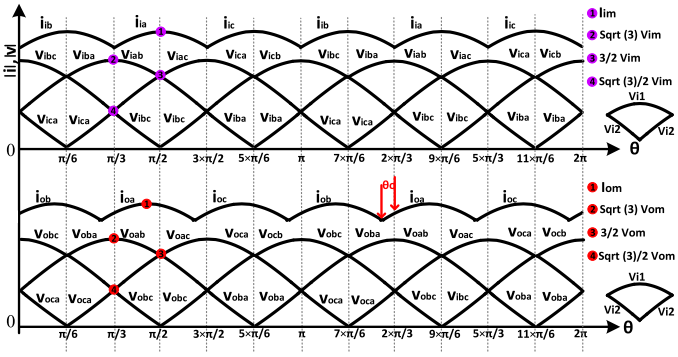


Fig. 8. Input and output phase-pair voltages and phase currents with the highest amplitude in a course of ac input and output cycles.

and output voltage amplitude as long as the output power keeps constant. A similar scenario is valid for the discharging modes when the input conditions change.

The link peak current and link frequency in this function can be formulated by [44]

$$i_p = 2 \times \sqrt{p_L} \times \left(\frac{\sqrt{p_1}}{v_{i1}} + \frac{\sqrt{p_L} - \sqrt{p}_1}{v_{i2}} + \frac{\sqrt{p_L} - \sqrt{p}_4}{v_{o2}} + \frac{\sqrt{p_4}}{v_{o1}} \right) \quad (1)$$

$$f_L = \frac{(p_L = p_i = p_o)}{L \times {i^2}_p} \quad (2)$$

where p_L is the total link inductor power. In buck–boost function, p_L is equal to input power p_i and output power p_o in a lossless system. v_{i1}, v_{i2}, v_{o1}, and v_{o2} are the amplitudes of the highest input line-to-line voltage, the second highest input line-to-line voltage, the highest output line-to-line voltage, and the second highest output line-to-line voltage, respectively. For a given output power, according to (1) and (2), the maximum link peak current and voltage and the link frequency vary with a change in voltage transfer ratio of the converter. The link peak current contributes to the power losses and determines the maximum current stress of the switches, and on the other hand the maximum link voltage specifies the maximum voltage stress of switches. It can be shown that the converter experiences minimum values of I_p, maximum link peak current, and $V_{\max}$ when voltage transfer ratio is one, and these values increase by pushing the voltage transfer ratio to a higher or a lower value. In this way, although the voltage transfer ratio is not limited theoretically in buck–boost function, in practice the effects of changing voltage transfer ratio on maximum allowable power loss and rating of switches and components in the converter have to be considered for the final design.

Fig. 8 depicts the input and output phase-pair voltages along with phase currents with the highest amplitude at the input side and the output side. As shown in Fig. 8, v_{i1}, v_{i2}, v_{o1}, and v_{o2} vary between $\sqrt{3}V_{im}$ and $1.5V_{im}$, $1.5V_{im}$ and $\sqrt{3}/2V_{im}$, $\sqrt{3}V_{om}$ and $1.5V_{om}$, and $1.5V_{om}$ and $\sqrt{3}/2V_{om}$, respectively. From this and according to (1) and (2), it can be expected that in this function the link frequency slightly changes over the input and output ac cycles due to a resultant slight change in the duration of the active modes 1, 3, 5, and 7. As discussed in the previous section, two phase pairs at the input side and the output side based on the amplitude of input and output phase currents and line-to-line voltages are selected by the control algorithm to charge and discharge the link inductor during modes 1, 3 and 5, 7, respectively.

Zero-voltage turn-ON of the switches is realized when the activation of the switches coincides with the equality of the link voltage with v_{i1} in mode 1, v_{i2} in mode 3, v_{o2} in mode 5, and v_{o1} in mode 7. Furthermore, the soft turn-OFF operation is granted to all power switches due to the existence of the link capacitor, which results in a slow change in voltages of the switches. The natural extension of the soft transition between active modes is realized because v_{i1} is higher than or equal to v_{i2} and v_{o2} is lower than or equal to v_{o2}. Likewise, the natural transition between modes 3 and 5 happens because the voltage seen across the link inductor during mode 5 in essence is negative or lower than v_{i2}. However, for a case where nonunity output power factor and step-up operation are demanded, the natural range of v_{o1} and v_{o2} depending on the output power factor changes. Consequently, if the load power factor, lagging or leading, drops lower than a certain value, the link voltage during mode 5 becomes positive with an absolute value higher than the link voltage during mode 3. This is where the proper operation of the converter with the introduced modulation technique is disturbed and some of the switches experience hard-switching operation, which is not desirable in this converter. To find this condition in the step-up operation, the arrangement of phase currents and line voltages in the second and third 30° intervals, as shown in Fig. 8, is considered here. It is also assumed that the input power factor is unity. The instantaneous input and output phase voltages and currents in a balanced three-phase ac system can be considered as

$$i_{ia} = I_{im} \sin(\omega_i t),\ i_{ib} = I_{im} \sin\left(\omega_i t - \frac{2\pi}{3}\right)$$

$$i_{ic} = I_{im} \sin\left(\omega_i t - \frac{4\pi}{3}\right) \quad (3)$$

$$i_{oa} = I_{om} \sin(\omega_o t + \theta_o),\ i_{ob} = I_{om} \sin\left(\omega_o t + \theta_o - \frac{2\pi}{3}\right)$$

$$i_{oc} = I_{om} \sin\left(\omega_o t + \theta_o - \frac{4\pi}{3}\right) \quad (4)$$

$$v_{ia} = V_{im} \sin(\omega_i t),\ \ v_{ib} = V_{im} \sin\left(\omega_i t - \frac{2\pi}{3}\right)$$

$$v_{ic} = V_{om} \sin\left(\omega_i t - \frac{4\pi}{3}\right) \quad (5)$$

$$v_{oa} = V_{om} \sin(\omega_o t),\ v_{ob} = V_{om} \sin\left(\omega_o t - \frac{2\pi}{3}\right)$$

$$v_{oc} = V_{om} \sin\left(\omega_o t - \frac{4\pi}{3}\right) \quad (6)$$

where I_{im}, I_{om}, V_{im}, V_{om}, and θ_o are, respectively, the peak values of the input phase currents, output phase currents, input phase voltages, output phase voltages, and the phase angle of the

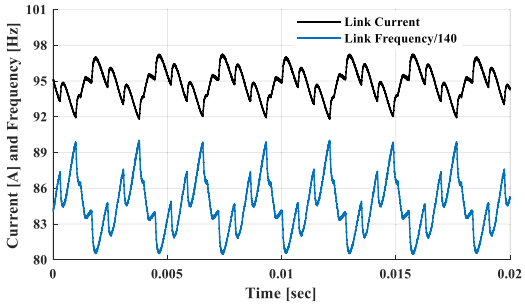


Fig. 9. Link peak current and link frequency when f_o is four times as large as f_i with 0.9 leading input and 0.9 lagging output power factors in buck–boost function.

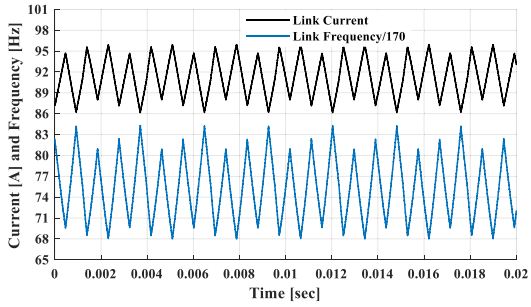


Fig. 10. Link peak current and link frequency when f_i is three times as large as f_o with unity input and 0.9 lagging output power factors in buck–boost function.

output phase currents with respect to their corresponding output phase voltages, which is called output phase shift θ_o. To avoid the situation in which the hard-switching operation occurs, when f_i is equal to f_o, the following inequality should be satisfied:

$$-\sqrt{3}V_{om}\sin\left(\omega t-\frac{\pi}{6}\right)<\sqrt{3}V_{im}\sin\left(\omega t+\frac{\pi}{6}\right)$$

$$\frac{\pi}{3}-\theta_o<\omega t<\frac{2\pi}{3}-\theta_o,\quad \omega_i=\omega_o=\omega. \tag{7}$$

By solving this inequality, a critical output phase shift θ_{oc}, which describes the load power limitation of the converter in terms of input and output voltage amplitudes, can be obtained as follows:

$$\theta_{oc}=\tan^{-1}\left(\frac{\sqrt{3}\times V_{im}}{2\times V_{om}+V_{im}}\right)+\frac{\pi}{6},\quad 0\le\theta_{oc}\le\frac{\pi}{3}. \tag{8}$$

For the case where $f_i<f_o$, a set of nonlinear inequalities should be solved to find θ_{oc} as

$$V_{om}\sin(\theta_p)\le V_{im}\cos\left(k\frac{\theta_p}{m}+\frac{\pi}{6}\right),\quad \theta_{oc}=\frac{\pi}{6}+\theta_p$$

$$0\le\theta_p\le\frac{\pi}{6},\quad m=\frac{f_o}{f_i},\quad k=1,\ldots,m/2\quad k\in N. \tag{9}$$

Similarly, a set of nonlinear inequalities should also be solved for finding θ_{oc} where $f_o<f_i$

$$V_{om}\sin(\theta_p)\le V_{im}\cos\left(km\theta_p+\frac{\pi}{6}\right),\quad \theta_{oc}=\frac{\pi}{6}+\theta_p$$

$$0\le\theta_p\le\frac{\pi}{6},\quad m=\frac{f_i}{f_o},\quad k=1,\ldots,m/2\quad k\in N. \tag{10}$$

Although this is not within the scope of the article, an improved control approach can be developed to extend the output power factor range when a low output power factor for the step-up operation is demanded.

In order to investigate the performance and load power factor limitation of the converter in the step-up operation, a three-phase ac system with an input voltage/frequency of 208 V/60 Hz, output voltage/frequency of 380 V/60 Hz, and output power of 8 kW is considered. The link inductance is 100 μH. Fig. 9 depicts the link peak current and scaled link frequency when $f_o=4f_i=240$ Hz with 0.9 leading input and 0.9 lagging output power factors. Fig. 10 shows the link peak current and scaled link frequency when $f_i=3f_o=180$ Hz with unity input and 0.9 lagging output power factors. As seen from these two figures, the converter experiences a lower level of link peak current and consequently a higher level of link frequency when the input frequency is higher than the output frequency.

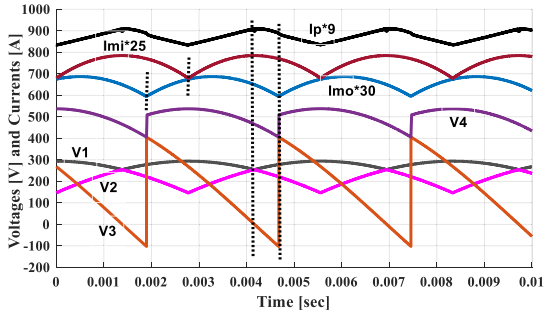


Fig. 11. Scaled maximum input current, scaled maximum output current, scaled link peak current, voltage levels during modes 1, 3, 5, and 7 when f_o is equal to f_i with unity input and 0.75 lagging output power factors in buck–boost function.

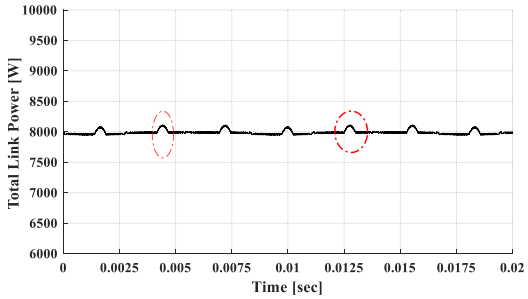


Fig. 12. Total power transferred through the link inductor when f_o is equal to f_i with unity input and 0.75 lagging output power factors in buck–boost function.

Fig. 11 illustrates the voltage levels during modes 1, 3, 5, and 7, scaled maximum input current, maximum output current, and link peak current, when the load power factor is decreased to 0.75 lagging and the input and output frequencies are both 60 Hz. According to Fig. 12, which illustrates the total power transferred through the link inductor for this case, there is an interval in mode 5 during which the link voltage becomes positive instead of being negative to discharge the link inductor. Under

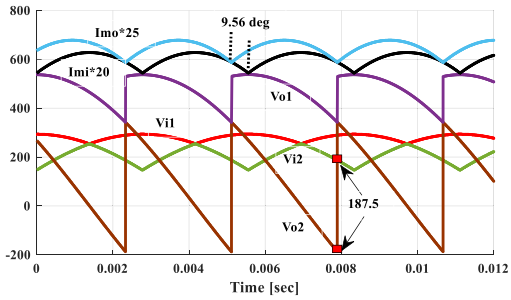


Fig. 13. Scaled maximum input current, scaled maximum output current, voltage levels during modes 1, 3, 5, and 7 when f_o is equal to f_i with unity input and 0.63 lagging output power factors in buck–boost function.

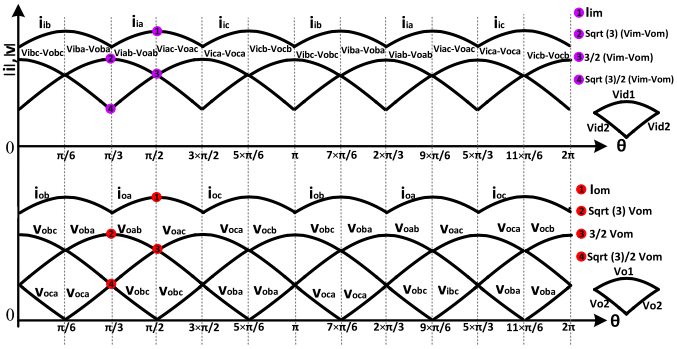


Fig. 14. v_{id1}, v_{id2}, output phase-pair voltages, and phase currents with the highest amplitude in a course of ac input and output cycles.

this condition, the link inductor is charged during mode 5 rather than being discharged, which results in increasing the power transferred through the link inductor, as shown in Fig. 12. To show the condition where the critical load power factor happens, the load power factor is further decreased to 0.63 lagging for the given characteristics. Fig. 13 demonstrates a case where the converter faces a critical load power factor. This figure clearly conceptualized the point where v_{i2} and v_{o2} become equal at $\theta_o = 50.44^{\circ}$. The same critical output phase shift is obtained by (8), which verifies the accuracy of the analysis.

B. Buck Function

In buck function, since there is a partial direct power transfer from the input side to the output side, the input and output sides are not completely decoupled. Unlike the buck–boost function, the charging modes are affected by a change in the output conditions including the output power factor, output frequency, and output voltage amplitude in buck function. Therefore, depending on the modulation technique, this imposes a limitation on the converter. Fig. 14 illustrates the link voltage levels in modes 1, 3, 5, and 7 and phase currents with the highest amplitude in a course of ac input and output cycles in buck function. As can be realized from Fig. 14, the shortest duration of resonating modes 2 and 6 happens when the link voltage in mode 1, v_{id1}, becomes equal to the link voltage in mode 3, v_{id2}, and v_{o1} becomes equal to v_{o2}, respectively. Under this situation, the converter directly goes to mode 3 from mode 1, and to mode 7 from mode 5 without experiencing any resonating modes, respectively.

The link peak current and link frequency in buck function can be given by [44]

$$i_p = 2 \times \sqrt{p_L} \times \left(\frac{\sqrt{p_1}}{v_{id1}} + \frac{\sqrt{p_L} - \sqrt{p_1}}{v_{id2}} + \frac{\sqrt{p_L} - \sqrt{p_4}}{v_{o2}} + \frac{\sqrt{p_4}}{v_{o1}} \right) \tag{11}$$

$$f_L = \frac{p_L}{L \times {i^2}_p}. \tag{12}$$

In this function, p_L is lower than input power and output power. This part focuses on the limitations of the converter in buck function when amplitudes of the voltage difference of the highest line-to-line voltages at the input side and output side during mode 1, v_{id1}, and the voltage difference of the second highest line-to-line voltages at the input side and output side during mode 3, v_{id2}, are positive. To realize this, the following inequality should be satisfied:

$$\begin{aligned} |v_{iac} - v_{oac}| > 0 \Rightarrow \sqrt{3} V_{im} \sin\left(\omega_i t - \frac{\pi}{6}\right) \\ - \sqrt{3} V_{om} \sin\left(\omega_o t - \frac{\pi}{6} + \theta_o\right) > 0 \\ \forall f_o > f_i \quad \frac{\pi}{3} - \theta_o < \omega_i t < \frac{2\pi}{3} - \theta_o \\ |v_{iac} - v_{oac}| > 0 \Rightarrow \sqrt{3} V_{im} \sin\left(\omega_i t - \frac{\pi}{6}\right) \\ - \sqrt{3} V_{om} \sin\left(\omega_o t - \frac{\pi}{6} + \theta_o\right) > 0 \\ \forall\ f_i > f_o \quad \frac{\pi}{3} - \theta_o < \omega_o t < \frac{2\pi}{3} - \theta_o. \end{aligned} \tag{13}$$

By solving (13), when f_i is equal to f_o, a simplified inequality, which describes the relation between input voltage, output voltage, and load power factor, can be obtained as

$$\frac{V_{im}}{V_{om}} > \frac{\sin\left(\theta_o + \frac{\pi}{3}\right)}{\cos\left(\theta_o + \frac{\pi}{6}\right)}, \quad 0 \le \theta_o \le 30. \tag{14}$$

Equation (14) implies that the peak amplitude of the input phase voltage requires to be slightly higher than the peak amplitude of output phase voltage when the output power factor is unity. If the input voltage is higher than twice the output voltage, there is no limitation in voltage ratio of the converter in buck function imposed by the load power factor, but the same limitation considered in buck–boost function needs to be investigated to avoid hard-switching operation when v_{o2} becomes positive and higher than v_{id2}. As it can be realized from the nonlinear inequality of (13), depending on the frequency ratio (f_i/f_o), different relation between input and output voltage amplitudes and power factor can be obtained. It can be shown that a general solution to satisfy (13) for different input and output frequencies and power factor is to have $V_{im} \ge 2V_{om}$. Under this condition, still there can be an interval where v_{id2} is higher than v_{id1}, which can cause hard-switching operation. To avoid this scenario, the input voltages can be estimated to select

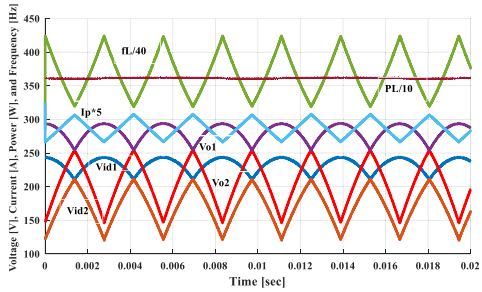


Fig. 15. Voltage levels during modes 1, 3, 5, and 7, the scaled link frequency, total link power, and link peak current with unity input and output power factors in buck function.

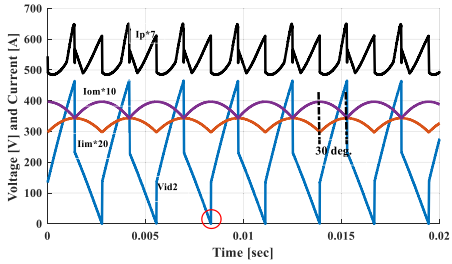


Fig. 16. Voltage level during mode 3, scaled maximum input current, maximum output current, the link peak current with unity input power factor and 0.86 lagging load power factor in buck function.

proper switches to guarantee that v_{id1} is always higher than v_{id2}, or switches corresponding to the highest line-to-line voltage, and the second highest line-to-line voltages at the input side and the output side need to be simultaneously gated-ON before mode 1 to charge the link inductor during modes 1 and 3.

A three-phase ac–ac converter with the input voltage/frequency of 380 V/60 Hz, output voltage/frequency of 208 V/60 Hz, output power of 8 kW, and the link inductance of 75 μH is considered. The voltage levels during modes 1, 3, 5, and 7, the scaled link frequency, link peak current, and total link power when the input and output power factors are unity are demonstrated in Fig. 15. As shown in this figure, only a portion of power (3.62 kW) is transferred by the link inductor.

Fig. 16 depicts the scaled maximum input current, maximum output current, link peak current, voltage levels during mode 1 when the output voltage is decreased to 190 V and the load and input power factors are 0.86 lagging and unity, respectively. As this figure clearly shows, a load phase shift limitation of 30° is resulted with the given input and output voltages, which is in exact match with (14).

v_{id1}, v_{id2}, v_{o1}, v_{o2}, and the scaled link peak current when the output voltage is decreased to 152 V and $f_o = 2f_i = 120$ Hz are shown in Fig. 17. Fig. 18 demonstrates v_{id1}, v_{id2}, v_{o1}, v_{o2}, and the scaled link peak current when $f_i = 3f_o = 180$ Hz. As obvious from Figs. 17 and 18, there are intervals during which v_{id2} is higher than v_{id1}, which can cause hard-switching operation with the proposed modulation technique.

C. Boost Function

Similar to buck function, a portion of power is directly transferred from input side toward output side in boost function.

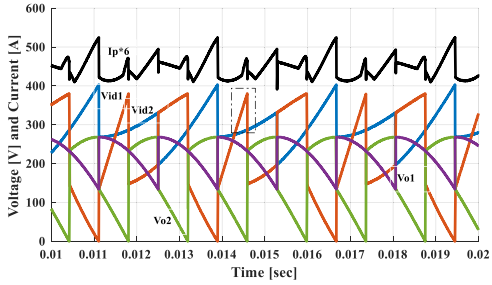


Fig. 17. Voltage levels during modes 1, 3, 5, and 7, and the scaled link peak current when $V_{im} = 2.5V_{om} = 380$ V and $f_o = 2f_i = 120$ Hz with unity input power factor and 0.86 lagging load power factor in buck function.

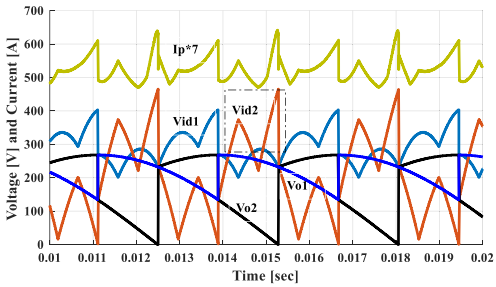


Fig. 18. Voltage levels during modes 1, 3, 5, and 7, and the scaled link peak current when $V_{im} = 2.5V_{om} = 380$ V and $f_i = 3f_o = 180$ Hz with unity input power factor and 0.86 lagging load power factor in buck function.

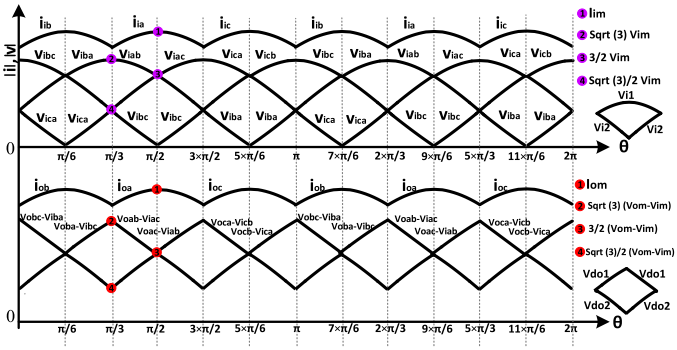


Fig. 19. v_{od1}, v_{od2}, input phase-pair voltages, and phase currents with highest amplitude in a course of ac input and output cycles.

To be more precise, in boost function discharging the inductor is realized by involving both input and output phases, which makes the output side and input side affected by each other. Therefore, it can be expected that this lack of decoupling between the input side and output side imposes a limitation on the converter, which is investigated in this part for the proposed modulation technique. Fig. 19 demonstrates amplitudes of the voltage difference of the highest line-to-line voltages at the input side and the second highest line-to-line voltages at the output side during mode 7, v_{od1}, the voltage difference of the second highest line-to-line voltages at the input side and the highest line-to-line voltages at the output side during mode 5, v_{od2}, and highest phase currents in course of ac input and output cycles.

The link peak current and link frequency in boost function can be obtained as [44]

$$i_p = 2 \times \sqrt{p_L} \times \left(\frac{\sqrt{p_1}}{v_{i1}} + \frac{\sqrt{p_L} - \sqrt{p_1}}{v_{i2}} + \frac{\sqrt{p_L} - \sqrt{p_4}}{v_{od2}} + \frac{\sqrt{p_4}}{v_{od1}} \right) \tag{15}$$

$$f_L = \frac{p_L}{L \times {i^2}_p}. \tag{16}$$

In boost function, p_L is lower than p_i and p_o. The limitation of the converter in boost function in terms of frequency and load power factor under the condition that the link voltage during mode 5 v_{od2} and mode 7 v_{od1} is negative is investigated. According to Fig. 19, the limitation can be described by

$$\begin{aligned} |v_{oac} - v_{iab}| > 0 \Rightarrow \sqrt{3} V_{om} \sin\left(\omega_o t - \frac{\pi}{6} + \theta_o\right) \\ - \sqrt{3} V_{im} \sin\left(\omega_i t + \frac{\pi}{6}\right) > 0 \\ \forall f_o > f_i \quad \frac{\pi}{3} - \theta_o < \omega_i t < \frac{2\pi}{3} - \theta_o \\ |v_{oac} - v_{iab}| > 0 \Rightarrow \sqrt{3} V_{om} \sin\left(\omega_o t - \frac{\pi}{6} + \theta_o\right) \\ - \sqrt{3} V_{im} \sin\left(\omega_i t + \frac{\pi}{6}\right) > 0 \\ \forall\ f_i > f_o \quad \frac{\pi}{3} - \theta_o < \omega_o t < \frac{2\pi}{3} - \theta_o. \end{aligned} \tag{17}$$

Equation (17) can be expressed as follows:

$$\frac{V_{om}}{V_{im}} > \frac{\cos(\theta_o)}{\cos\left(\frac{\pi}{3} + \theta_o\right)}, \quad 0 \le \theta_o < 30. \tag{18}$$

Equation (18) implies that in order to operate the converter properly in this function with the proposed modulation technique under the unity load power factor, the output voltage needs to be higher than twice the input voltage. To mitigate this problem, in mode 5, the proper switches corresponding to the second highest line-to-line voltages at the input side and output side can be turned ON. It can be shown that if (18) is met, the converter can operate properly with arbitrary input and output frequencies. Furthermore, using the proposed switching algorithm, the converter does not face the situation in which v_{od1} is lower than v_{od2}, causing an unwanted hard-switching operation.

A three-phase ac–ac converter with input voltage/frequency of 208 V/60 Hz, output voltage/frequency of 420 V/60 Hz, and the link inductance of 75 μH operating at 8 kW is considered. The voltage levels during modes 1, 3, 5, and 7, the scaled link frequency, link peak current when the input and output power factors are unity and output frequency is three times as large as the input frequency are shown in Fig. 20. Fig. 21 shows v_{i1}, v_{i2}, v_{od1}, v_{od2}, scaled maximum input current, and maximum output current when the input frequency is four times as large as the output frequency and the input and output power factors are 0.95 leading and unity, respectively. As evident from these two figures and expected from the analysis, the modulation technique enables the converter to operate with arbitrary input and output

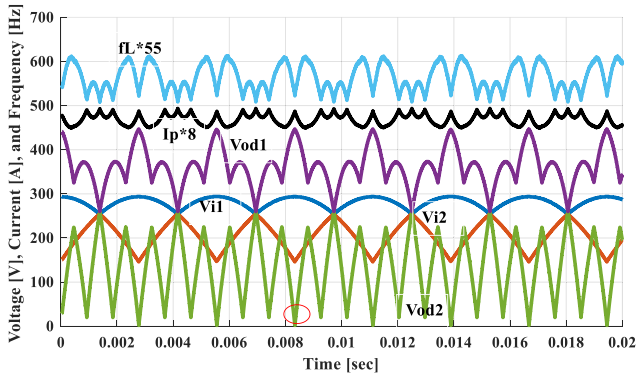


Fig. 20. Voltage levels during modes 1, 3, 5, and 7, scaled link frequency, and link peak current with unity input and output power factors when $f_o = 3f_i = 180$ Hz in boost function.

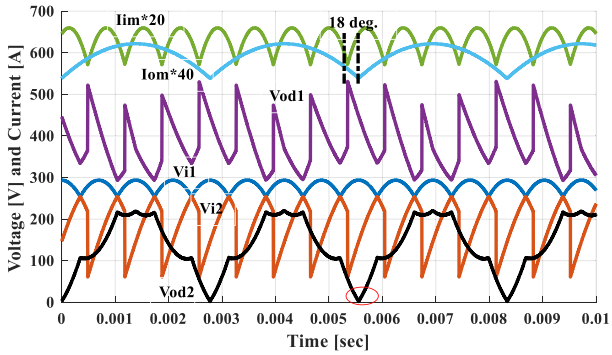


Fig. 21. Voltage levels during modes 1, 3, 5, and 7, scaled maximum input and output currents with unity output power factor and 0.95 leading input power factor when $f_i = 4f_o = 240$ Hz in boost function.

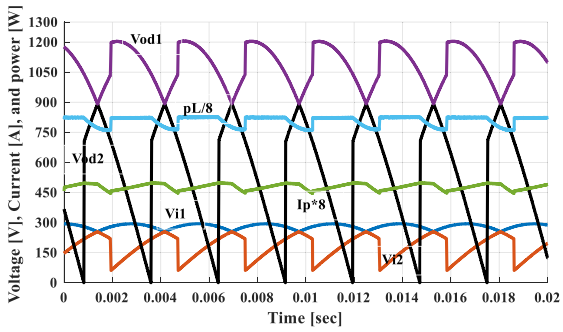


Fig. 22. Voltage levels during modes 1, 3, 5, and 7, scaled link peak current, and total link power with 0.95 leading input and 0.95 lagging output power factors when $f_i = f_o = 60$ Hz in boost function.

frequencies without experiencing any hard-switching intervals as long as (18) is valid. Fig. 22 demonstrates v_{i1}, v_{i2}, v_{od1}, v_{od2}, scaled link peak current, and total link power when the input and output frequencies are the same (60 Hz) and the input and output power factors are 0.95 leading and 0.95 lagging, respectively. As shown in Fig. 22, only a portion of power, varying between 6.1 and 6.6 kW, is transferred by the link inductor.

The idea behind the proposed switching algorithm for selecting proper phase pairs in buck–boost function is to minimize

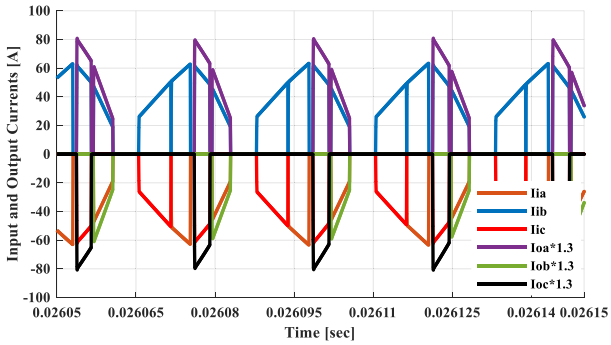


Fig. 23. Unfiltered input and output phase currents in boost function.

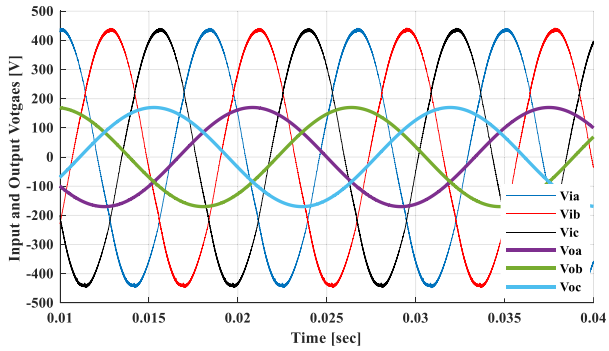


Fig. 24. Input and output phase voltages in boost function.

partial-resonance intervals while maximizing the performance of the converter via natural extension of the modulation. This is why the switches corresponding to the highest input line-to-line voltages and then the second highest input line-to-line voltages are allowed automatically to conduct in modes 1, 9 and 3, 11 to charge the link inductor while keeping the input phase with the maximum current as the common input phase. Similarly, the switches corresponding to phase pairs forming the second highest output line-to-line voltages and then the highest output line-to-line voltages are allowed to conduct in modes 5, 13 and 7, 15 to discharge the link inductor while keeping the output phase with the maximum current as the common output phase. The proposed switching algorithms in buck and boost functions are targeted to minimize the link peak current while meeting the desired performance. Since, depending on the configuration and demanded application, the possible combinations of input and/or output phase pairs, which results in zero volt-second balance over the link inductor, in buck and boost functions are not unique, various modulation patterns with different levels of complexity and limitations can be applied. Therefore, the proposed modulation techniques in buck and boost functions are not unique and not necessarily optimized. In this way, improved modulation patterns for buck and boost functions can be introduced to remove or mitigate the limitations imposed on the converter.

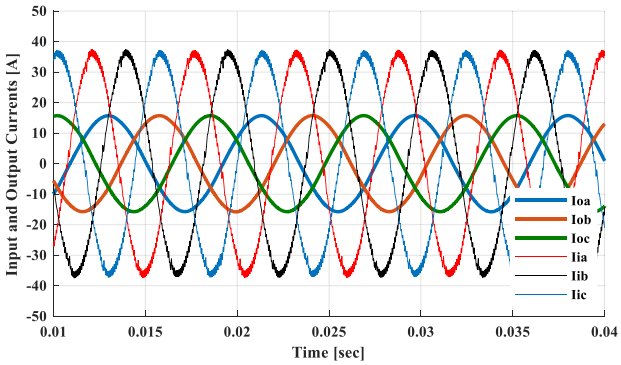


Fig. 25. Filtered input and output currents in buck–boost function.

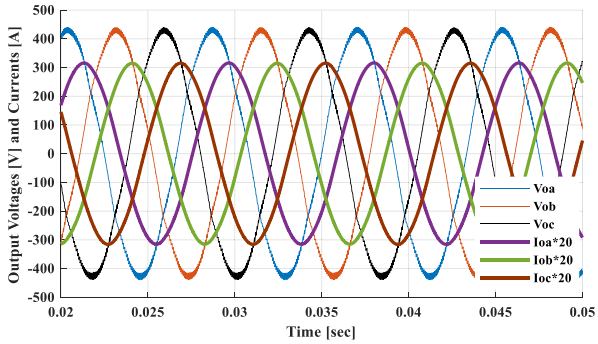


Fig. 26. Filtered output currents and voltages in buck–boost function.

V. Simulation and Experimental Results

A. Simulation Results

In order to validate the performance of the proposed converter in different functions under different operating conditions, an 8-kW three-phase ac–ac converter is designed and simulated using PSIM software. The link inductance and capacitance are selected as 65 μH and 75 nF, respectively. Two sets of simulations for step-up and step-down operations are carried out.

Figs. 23–26 depict simulation results for the step-up operation in which the capacitance and inductance of the input and output filters are 20 μF, 7 μF, 50 μH, and 25 μH, respectively. In this operation, the input and output voltages are considered as 208 and 540 V, respectively. The simulation results of the converter with the input and output frequencies of 60 and 120 Hz when the output is connected to a resistive load are demonstrated in Figs. 23 and 24. Fig. 23 displays the unfiltered input and output currents in boost function. As expected, in boost function the input phases are involved in both charging and discharging modes. The input and output load phase voltages in boost function are represented in Fig. 24. As this figure clearly shows and (17) and (18) verify, the converter is operating properly even though the output frequency is twice the input frequency. The maximum link frequency in this function is 28.3 kHz, which is in good agreement with (16). Figs. 25 and 26 show the simulation results in buck–boost function under a test condition in which the input frequency is changed to 180 Hz while the converter is supplying a 10.66-kVA inductive load at 0.75 lagging power factor. The filtered input and output currents, which are well-regulated, are

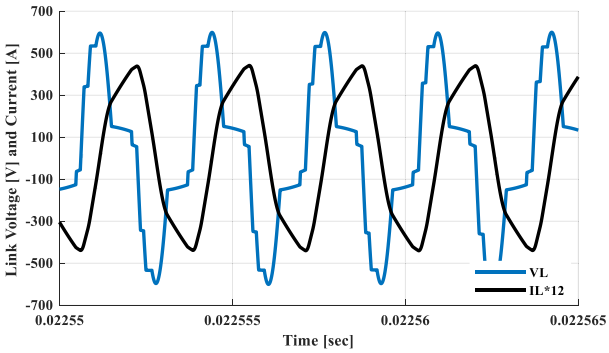


Fig. 27. Link voltage and current in boost function.

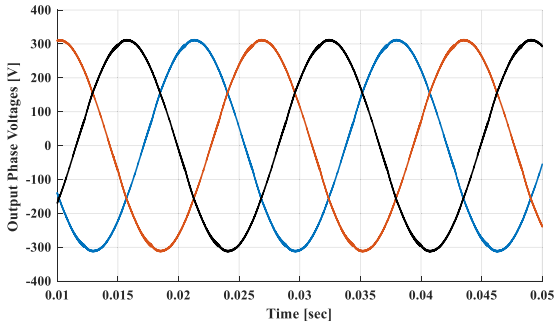


Fig. 28. Load phase voltages in boost function.

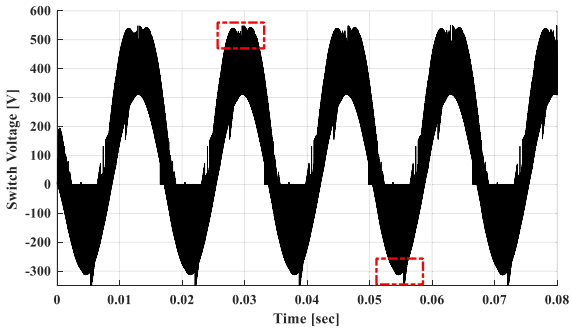


Fig. 29. Voltage profile across switch S_6 in buck function.

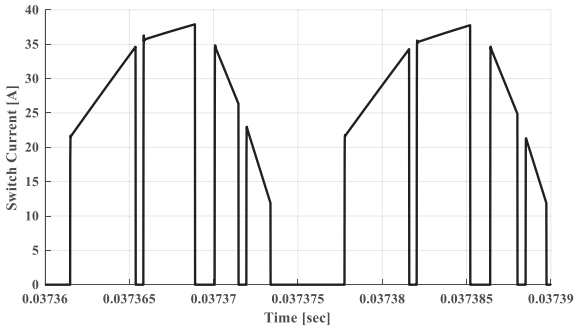


Fig. 30. Maximum current passing through switch S_6 in buck function.

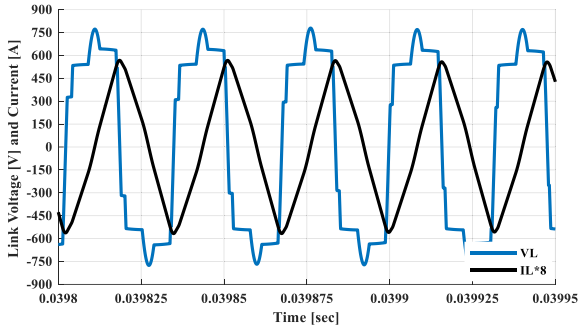


Fig. 31. Link voltage and current in buck–boost function.

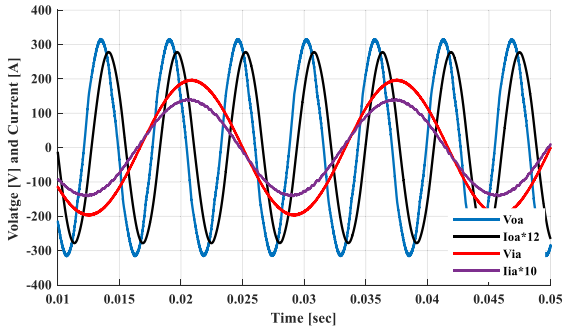


Fig. 32. Input and output phase currents and voltages.

shown in Fig. 25. Fig. 26 depicts the output phase currents and voltages while the converter is properly functioning to provide the demanded reactive power. These two figures verify that although the load power factor is not unity (0.75 lagging) and the input and output frequencies are different, the input power factor of the proposed converter remains at unity. This is in agreement with (8)–(10) and supports the fact that there is no direct power transfer from the input to the output in buck–boost function.

The step-down operation of the proposed converter is validated under a case where the input voltage, output voltage, capacitance, and inductance of input and output filters are 480 V, 380 V, 12 μF, 12 μF, 90 μH, and 25 μH, respectively. Figs. 27–30 show the simulation results corresponding to the buck function in which the input and output frequencies are both set at 60 Hz while a three-phase resistive load is connected to the output side. The link voltage with the maximum value of 610 V and the link current with the maximum value of 38.2 A, which exactly matches (11), are represented in Fig. 27. Smooth sinusoidal currents are injected to the load with the THD of 0.9%. The output phase voltages are illustrated in Fig. 28. This figure supports the analysis presented in (12). The profile of voltage across switch S_6 and current passing through this switch are demonstrated in Figs. 29 and 30, respectively. The peak values of voltage and current of switch S_6 in this case reach 537 V and 38.2 A, respectively. Figs. 31–34 depict the simulation results in buck–boost function when the converter is supplying an inductive load with power factor of 0.75. In this test condition, the input and output frequencies are 60 and 180 Hz, respectively. The link voltage and link current are shown in Fig. 31. In this function, the maximum link current is 69.7 A, which is approximately 1.82 times that of buck function.

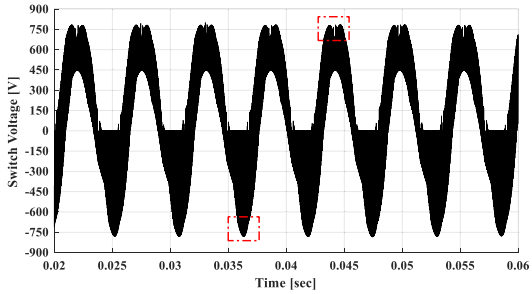


Fig. 33. Voltage profile across switch S_6 in buck–boost function.

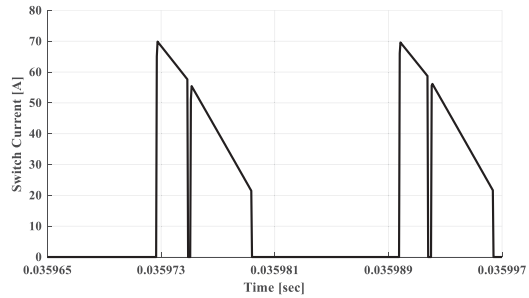


Fig. 34. Maximum current passing through switch S_6 in buck–boost function.

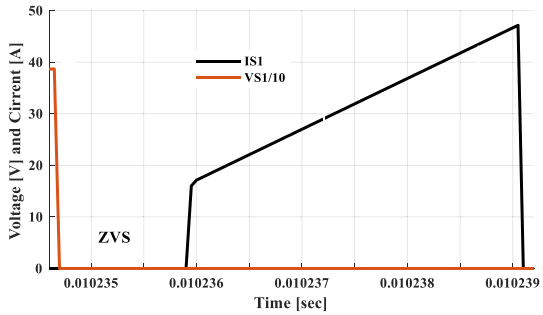


Fig. 35. Voltage and current of switch S_1.

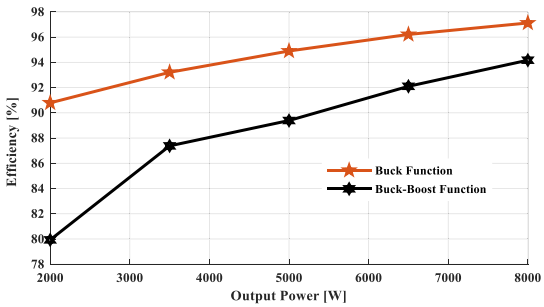


Fig. 36. Conversion efficiency of the converter versus output power in buck–boost and buck functions.

Fig. 32 illustrates the input and output phase voltages and currents. As clearly shown in this figure, although the required input and output frequencies are different, the converter exhibits the complete capability of injecting reactive power with the demanded load power factor, whereas the unfiltered input phase currents are controlled effectively to achieve an almost unity power factor at the input side. The profile of voltage across switch S_6 and the current passing through this switch are demonstrated in Figs. 33 and 34, respectively. As these figures show, the peak values of voltage and current of the switch in buck–boost function are 782 V and 69.7 A, respectively. By comparing Figs. 29, 30 and Figs. 33, 34, it can be deduced that the switches in buck–boost function experience a higher level of current stress and voltage stress compared to that of buck function. The maximum link frequency in buck and buck–boost functions reaches 31.9 and 30.8 kHz, which are in compliance with (3) and (8), respectively.

ZVS at turn-ON of switch S_1 in buck function is demonstrated in Fig. 35. Fig. 36 manifests the conversion efficiency of the converter versus the output power in buck and buck–boost functions where the converter is designed to be operated with the input voltage/frequency of 480 V/60 Hz to supply an 8-kW three-phase resistive load with the voltage/frequency of 380 V/60 Hz. The estimated efficiency of the converter at the nominal operating condition in buck and buck–boost functions is 97.12% and 94.17%, respectively. For estimating the efficiency, accurate models of the components to accommodate the real condition as close as possible in the simulation are considered. In this simulation, a series combination of a power IGBT (IKQ75N120CT2 1200 V, 75 A) and a power diode (VS80APS 1200 V, 80 A) is employed to realize a switch with bidirectional voltage blocking capability.

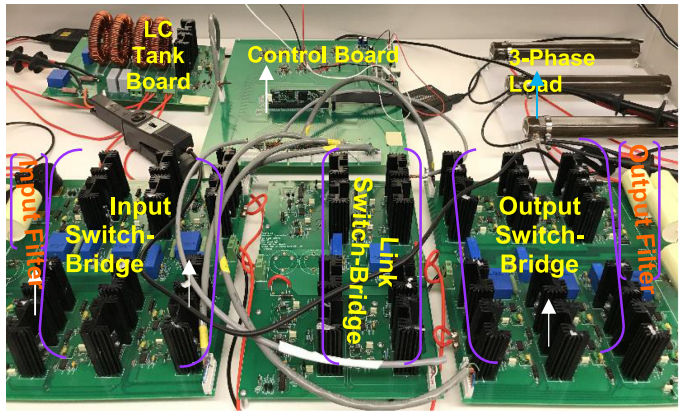


Fig. 37. Annotated photograph of the proposed proof-of-concept converter prototype.

B. Experimental Results

To experimentally verify the performance of the proposed three-phase ac–ac converter in different functions, a low-power proof-of-concept prototype, the size of which is not optimized, is designed, fabricated, and tested under different operating conditions. Fig. 37 illustrates an annotated photograph of the prototype. Each leg of the input switch bridge, link switch bridge, and output switch bridge is composed of four IGBTs

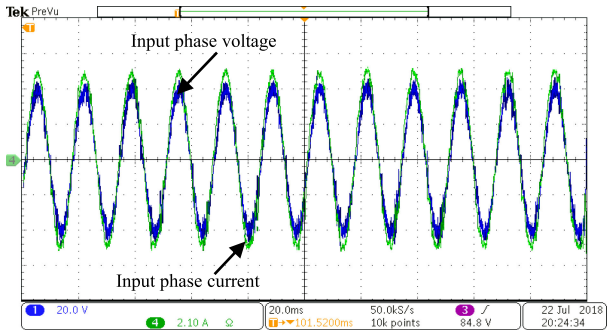


Fig. 38. Filtered input current and input voltage across the capacitor of phase *b* in boost function.

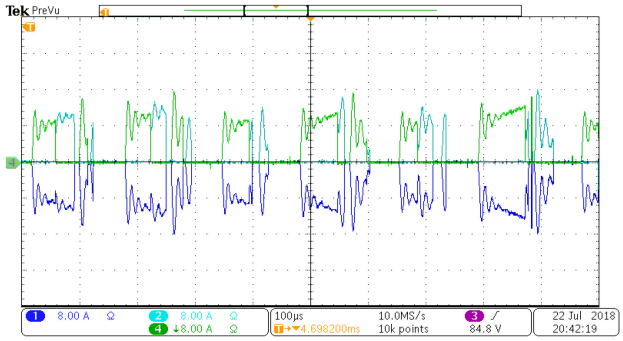


Fig. 39. Unfiltered input phase currents in boost function.

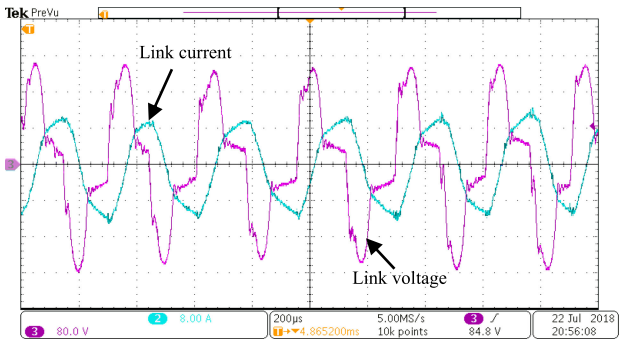


Fig. 40. Link voltage and link current in boost function.

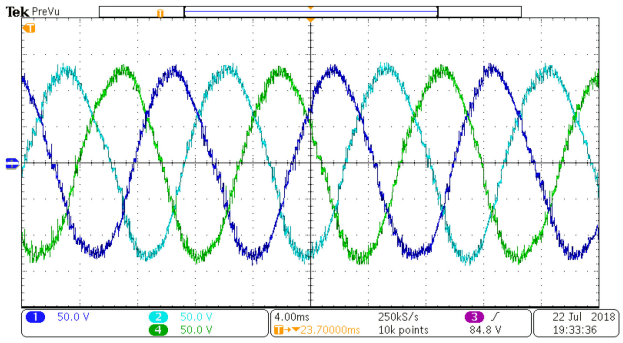


Fig. 41. Load phase voltages in boost function.

(IRG7PH42UDPbF 1200 V, 45 A), two of which are intentionally always kept OFF to serve as two power diodes for realizing unidirectional current conducting bidirectional voltage blocking switches. In order to control the converter effectively, a TMS320F28335 digital signal processor (DSP) with a sampling time of 4.8 μs, which includes the required processing time and analog-to-digital conversion time, is employed. In order to be able to control the converter properly with the soft-switching operation, the link frequency requires to be much smaller than the sampling frequency of DSP. To realize this, the link inductance and capacitance are selected to be 785 μH and 0.7 μF, respectively. This keeps the link frequency low enough to achieve enough number of samples for the closed-loop controller in each switching cycle. As a result, the inductance of input and output filters is considered as 470 μH. This practical limiting factor of the maximum allowable link frequency, which is imposed by the digital controller, can be removed by using a faster digital controller, field-programmable gate array, or an integrated analog design.

To show the performance of the converter in both step-up and step-down modes of operation, two sets of experiment, while the converter is connected to a three-phase resistive load at the output side, are considered. In the first set of experiment, the converter is tested in boost function when the input source with input voltage/frequency of 52 V/60 Hz supplies a restive load with the output voltage/frequency of 172 V/90 Hz at 225 W. The input and output filter capacitors are 45 and 10 μF, respectively. The filtered current and voltage of input phase *c* are demonstrated in Fig. 38. As shown in this figure, the input power factor of the proposed converter remains at almost unity, whereas the input phase current is well-regulated. The unfiltered input phase currents are displayed in Fig. 39. As expected, the input phases become involved in both charging and discharging modes in boost function.

Fig. 40 depicts the link voltage and current; the maximum values of link voltage and current are 220 V and 11 A, respectively. Fig. 41 illustrates the load phase voltages with the peak voltage of 140 V while the output phase current THD is 4.1%. Although the frequency of the output current is 1.5 times as large as the input frequency, the load phase voltages are not affected. Figs. 38–41 verify the capability of the proposed converter in controlling the frequency of the input and output phase currents and the analysis made for the detailed performance behavior of the converter. The conversion efficiency of the converter in boost function is around 85.9%. The efficiency of the converter is expected to be significantly improved at higher power and voltage levels, especially when using RB-IGBTs or silicon-carbide devices.

In order to verify the performance of the converter in a step-down operation, the converter is run with the input voltage/frequency of 208 V/60 Hz to supply a 450-W resistive load with the output voltage/ frequency of 74 V/90 Hz. The capacitance of the input and output filters in this case is selected to be 20 and 45 μF, respectively. The experimental results for this operation in buck–boost function are represented in Figs. 42–47. Fig. 42 shows the filtered current and voltage of input phase *a*.

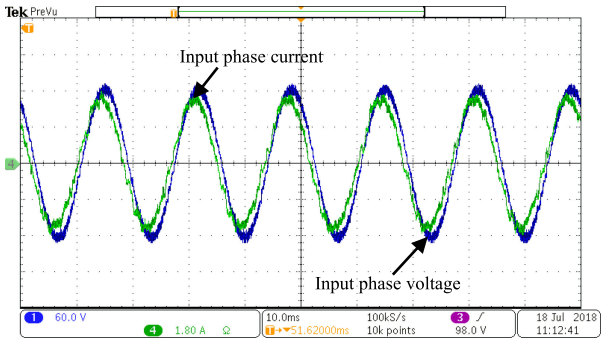


Fig. 42. Filtered input current and input voltage across the capacitor of phase *a* in buck–boost function.

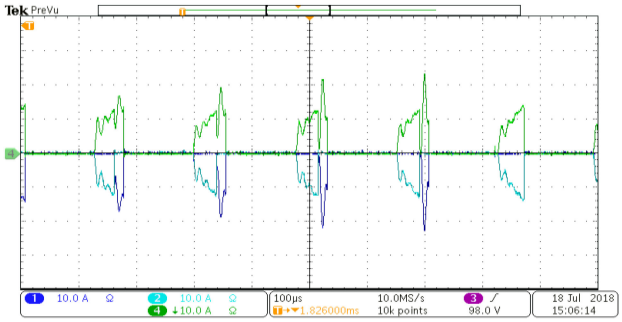


Fig. 43. Unfiltered input phase currents in buck–boost function.

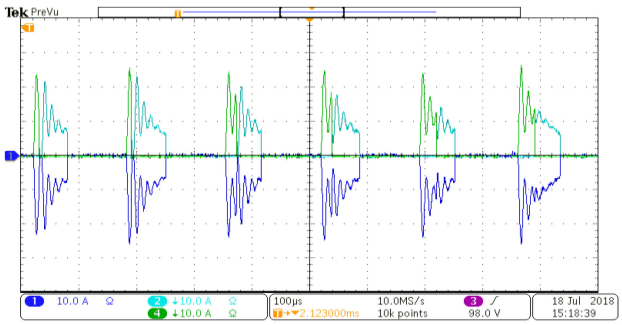


Fig. 44. Unfiltered output phase currents in buck–boost function.

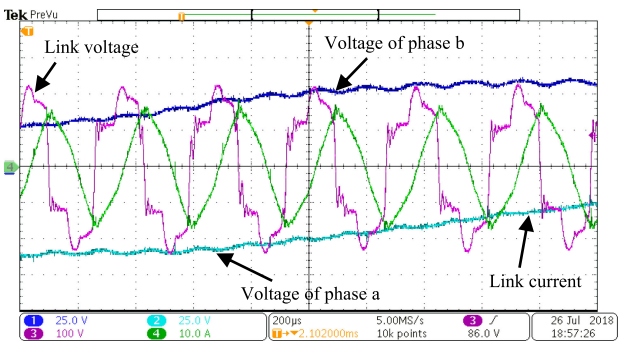


Fig. 45. Link voltage, link current, and phase voltage of phases *a* and *b* in buck–boost function.

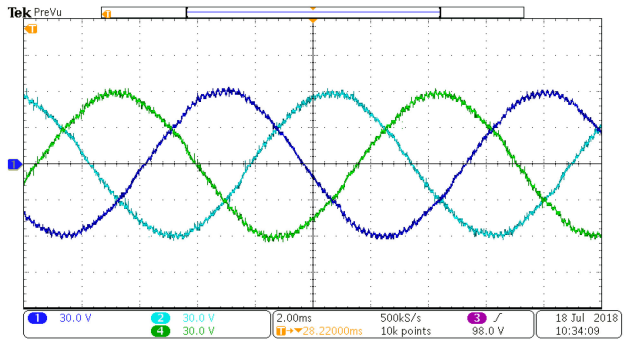


Fig. 46. Load phase voltages in buck–boost function.

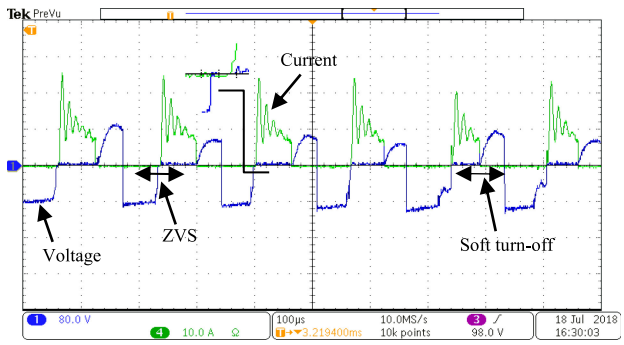


Fig. 47. Voltage and current of switch S_6 in buck–boost function.

Although the input power factor of the unfiltered input currents is set to unity, it can be observed that the input power factor is drifted from unity. This is because the input-side filter causes the filtered input currents to get slightly shifted from their corresponding unfiltered currents. The measured input power factor in this case is 0.955 leading. In this converter, as the input filter capacitance increases, the input power factor drops more from unity. However, the unfiltered input current can be controlled such that a unity power factor is yielded regardless of the size of input filter components, as shown in the simulation part. The unfiltered input and output phase currents are demonstrated in Figs. 43 and 44, respectively. The oscillations observed in the unfiltered phase currents are due to parasitic components of the switches and stray inductance of the printed circuit board. Fig. 45 illustrates the load voltage of phases *a* and *b*, and the link voltage and current with the maximum link frequency of 3.3 kHz. The load phase voltages the frequency and peak of which are 90 Hz and 60 V are demonstrated in Fig. 46. The voltage and current of switch S_6 are depicted in Fig. 47, which verify the soft-switching feature of the converter. As demonstrated in this figure, the switch voltage at the turn-ON and turn-OFF instants is zero and almost zero, respectively.

The proposed configuration is compared with the existing three-phase ac–ac topologies in Table III. It should be mentioned that in case an RB-IGBT is not utilized in the proposed converter, a series combination of a MOSFET/IGBT and a diode should be used to realize a bidirectional blocking switch.

TABLE III
COMPARISON OF THREE-PHASE AC–AC TOPOLOGIES

	This work	Ref. [44]	Ref. [39]	Ref. [37]	Ref. [36]	Ref. [42]	Ref. [24]	Ref. [18]
Power rating	8 kW	10 kW	450 W	10 kW	50 kW	1.5 kW	6.8 kW	3.5 kW
Number of active switches/diodes	16[1]/0	24/0	24	12[1]/0 13[1]/1	14[1]/0	16[1]/0	15/18	12/0
Number of energy transferring elements	1	1	1	1	1	1	0	9
Functionalities	[2]BB, [3]BU, [3]BO	BB, BU, BO	BB	BB, BU, BO	BB	BB	BU, Limited voltage gain	BU, fixed voltage gain
Frequency control capability	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Resonance Swing	Short	Short	Short	Long	Long	Short	-	-
Link quadrant	4	4	4	2	2	4	2	2
Number of dc caps	0	0	0	0	0	0	0	0
HF transformer possibility	No	Yes	Yes	Yes	Yes	No	No	No
Soft-switching feature	Full range	Full range	Full range	Full range	Full range	Full range	No	No
Efficiency	BB: 94.17% BU:97.12%	BB: 93.15% BO:97.38% BU:95.83%	90%	BB: 92.98% BU:94.47% %	97.4%	-	-	95.1%

[1]16, 12, 12, 16 extra diodes in [36], [37], and [42] need to be used if RB-IGBTs are not utilized, respectively. [2]BB: Buck–boost. [3]BU: Buck. [4]BO: Boost.

VI. CONCLUSION

A new class of soft-switched high-frequency ac-link power converters, which can be configured in various structures to provide dc–dc, dc–ac, ac–dc, and/or ac–ac in single stage of power conversion, is introduced in this article. The proposed family, which can function in buck, boost, or buck–boost modes of operation, is capable of performing step-up and step-down operations in both forward and reverse directions with the input and output operating at arbitrary voltages, frequencies, and power factors. In this converter, voltage step-up/step-down capability can also be achieved through various combinations of buck, boost, and buck–boost operation modes. For each function, a developed modulation approach is presented. By operating the converter in either buck mode or boost mode, the switch current stress and the link peak current are dramatically reduced and consequently the efficiency is improved. However, depending on the modulation technique, these two modes of operation may face limitations in terms of load power factor, frequency, and voltage ratio. On the other hand, although a lower efficiency and higher level of voltage and current stress are expected in buck–boost function compared to buck and boost functions, the converter can operate without sacrificing its performance under different input and output conditions. In this converter, all the power switches benefit from a full range of soft-switching operation, which leads to an improved efficiency, reduced EMI, and minimized stress over the power switches. The proposed family also enjoys enhanced reliability as it is immune from the short-circuit problem of the input, output, and link capacitors, and the open-circuit problem of input, output, and link inductors in addition to the elimination of large electrolytic capacitors. It can also eliminate reverse-recovery issues of the body diodes and the corresponding losses to further improve the efficiency. The effectiveness of the proposed converter is validated via simulation and low-power experimental results, and the detailed performance analysis supports the behavior of the proposed topology.

REFERENCES

[1] R. Lai *et al.*, "A systematic topology evaluation methodology for high density three-phase PWM AC-AC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2665–2680, Nov. 2008.

[2] P. Alemi, Y.-C. Jeung, and D.-C. Lee, "DC-link capacitance minimization in T-type three-level ac/dc/ac PWM converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1382–1391, Mar. 2015.

[3] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three phase PWM AC-AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[4] M. J. Newman, D. G. Holmes, J. G. Nielsen, and F. Blaabjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1744–1753, Nov./Dec. 2005.

[5] Y.-G. Kang and A. K. Upadhyay, "Analysis and design of a half-bridge parallel resonant converter," *IEEE Trans. Power Electron.*, vol. PE-3, no. 3, pp. 254–265, Jul. 1988.

[6] A. F.Witulski and R.W. Erickson, "Design of the series resonant converter for minimum component stress," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-22, no. 4, pp. 356–363, Jul. 1986.

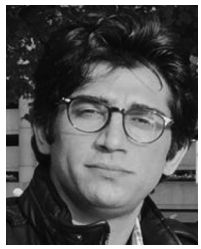
[7] A. K. S. Bhat, "Analysis and design of a series-parallel resonant converter," *IEEE Trans. Power Electron.*, vol. 8, no. 1, pp. 1–11, Jan. 1993.

[8] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An LLC resonant DC–DC converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.

[9] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "Bi-directional CLLC converter with synchronous rectification for plug-in electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 998–1005, Mar./Apr. 2018.

[10] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[11] H. Sarnago, O. Lucia, A. Mediano, and J. M. Burdio, "Direct AC-AC resonant boost converter for efficient domestic induction heating applications," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1128–1139, Mar. 2010.
[12] J. H. Kim, B. D. Min, B. H. Kwon, and S. C. Won, "A PWM buck–boost AC chopper solving the commutation problem," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 832–835, Oct. 1998.
[13] J. Hoyo, J. Alcala, and H. Calleja, "A high quality output AC/AC cuk converter," in *Proc. 35th Annu. Conf. IEEE Power Electron. Spec.*, 2004, pp. 2888–2893.
[14] F. Z. Peng, L. Chen, and F. Zhang, "Simple topologies of PWM ac–ac converters," *IEEE Power Electron. Lett.*, vol. 1, no. 1, pp. 10–13, Mar. 2003.
[15] Y. Tang, S. Xie, and C. Zhang, "Z-source ac-ac converters solving commutation problem," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2146–2154, Nov. 2007.
[16] F. Zhang, X. P. Peng, and Z. M. Qian, "A new three-phase ac-ac Z-source converter," in *Proc. Int. Conf. IEEE Appl. Power Electron.*, 2006, pp. 123–126.
[17] L. He, S. Duan, and F. Peng, "Safe-commutation strategy for the novel family of quasi-Z-source AC/AC converter," *IEEE Trans. Ind. Inform.*, vol. 9, no. 3, pp. 1538–1547, Aug. 2013.
[18] T. B. Lazzarin, R. L. Anderson, and I. Barbi, "A switched-capacitor threephase AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 735–745, Feb. 2015.
[19] R. L. da Silva, T. B. Lazzarin and I. Barbi, "Reduced switch count step-up/step-down switched-capacitor three-phase AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8422–8432, Nov. 2018.
[20] H. Shin, H. Cha, H. Kim, and D. Yoo, "Novel single-phase PWM ac-ac converters solving commutation problem using switching cell structure and coupled inductor," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2137–2147, Apr. 2015.
[21] A. A. Khan, H. Cha, and H.-G. Kim, "Three-phase three-limb coupled inductor for three-phase direct PWM AC-AC converters solving commutation problem," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 189–201, Jan. 2016.
[22] A. A. Khan, H. Cha, and H. F. Ahmed, "A new reliable three-phase buck-boost AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1000–1010, Feb. 2018.
[23] U. A. Khan, A. A. Khan, H. Cha, H. Kim, J. Kim and J. Baek, "Dual-buck ac–ac converter with inverting and non-inverting operations," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9432–9443, Nov. 2018.
[24] J. W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, "Novel three-phase AC-AC sparse matrix converters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1649–1661, Sep. 2007.
[25] C. Klumpner, P. Nielsen, I. Boldea, and F. Blaabjerg, "A new matrix converter motor (MCM) for industry applications," *IEEE Tran. Ind. Electron.*, vol. 49, no. 2, pp. 325–335, Apr. 2002.
[26] Y. Sun, X. Li, M. Su, H. Wang, H. Dan, and W. Xiong, "Indirect matrix converter-based topology and modulation schemes for enhancing input reactive power capability," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4669–4681, Sep. 2015.
[27] D. Casadei *et al.*, "Large-signal model for the stability analysis of matrix converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 939–950, Apr. 2007.
[28] H. Hojabri, H. Mokhtari, and L. Chang, "A generalized technique of modeling, analysis, and control of a matrix converter using SVD," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 949–959, Mar. 2011.
[29] M. Vijayagopal, P. Zanchetta, L. De Lillo, L. Empringham, L. Tarisciotti, and P. Wheeler, "Control of a direct matrix converter with modulated model predictive control," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2342–2349, May 2017.
[30] S. Vidhya and T. Venkatesan, "Quasi-Z-source indirect matrix converter fed induction motor drive for flow control of dye in paper mill," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1476–1486, Feb. 2018.
[31] R. K. Gupta, K. K. Mohapatra, A. Somani, and N. Mohan, "Direct-matrix converter-based drive for a three-phase open-end-winding ac machine with advanced features," *IEEE Power Ind. Electron.*, vol. 57, no. 12, pp. 4032–4042, Dec. 2010.
[32] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002.
[33] H. Keyhani and H. A. Toliyat, "A soft-switched three-phase ac-ac converter with a high-frequency ac link," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2637–2647, Jul./Aug. 2014.
[34] H. Keyhani and H. A. Toliyat, "Isolated ZVS high-frequency-link AC-AC converter with a reduced switch count," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4156–4166, Aug. 2014.
[35] I. D. Kim and C. G.-Hyeong, "New bilateral zero voltage switching ac/ac converter using high frequency partial-resonant link, " in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, Pacific Grove, CA, USA, Nov. 2–6, 1990, pp. 857–862.
[36] H. Chen and D. Divan, "Soft-switching solid-state transformer (S4T)," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2933–2947, Apr. 2018.
[37] K. Mozaffari and M. Amirabadi, "A highly reliable and efficient class of single-stage high-frequency ac-link converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8435–8452, Sep. 2019.
[38] W. C. Alexander, "Universal power converter," U.S. Patent US20080013351 A1, Jan. 17, 2008.
[39] M. Amirabadi, J. Baek, H. A. Toliyat, and W. C. Alexander, "Soft-switching ac-link three-phase ac–ac buck–boost converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 3–14, Jan. 2015.
[40] M. Amirabadi, J. Baek, and H. A. Toliyat, "Sparse ac-link buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3942–3953, Aug. 2014.
[41] M. Amirabadi, H. A. Toliyat, and J. Baek, "Ultra-sparse ac-link converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 448–458, Jan./Feb. 2015.
[42] S. A. K. H. Mozaffari Niapour and M. Amirabadi, "Extremely sparse parallel ac-link universal power converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2456–2466, May/Jun. 2016.
[43] K. Mozaffari, M. Amirabadi, and Y. Deshpande, "A single-phase inverter/rectifier topology with suppressed double-frequency ripple," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9282–9295, Nov. 2018.
[44] K. Mozaffari and M. Amirabadi, "A versatile family of partial-resonance inductive-ac-link universal converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7292–7309, Aug. 2019.



Khalegh Mozaffari (Member, IEEE) received the B.S. degree (first-class hons.) from Islamic Azad University, Kazerun, Iran, in 2007, the M.S. degree (first-class hons.) from the University of Tabriz, Tabriz, Iran, in 2011, and the Ph.D. degree from Northeastern University, Boston, MA, USA, in 2019, all in electrical engineering.

He is currently with the Enphase Energy Inc., Austin, TX, USA, as a Senior Power Electronics Engineer.

Mahshid Amirabadi (Member, IEEE) received the B.S. degree from Shahid Beheshti University, Tehran, Iran, in 2002, the M.S. degree from the University of Tehran, Tehran, Iran, in 2006, and the Ph.D. degree from Texas A&M University, College Station, TX, USA, in 2013, all in electrical engineering.

Following receipt of the Ph.D. degree, she joined the University of Illinois at Chicago as an Assistant Professor. Since August 2015, she has been with Northeastern University, Boston, MA, USA, where she is currently an Assistant Professor. Her research interests and experience include design, analysis, and control of power converters, renewable energy systems, and variable speed drives.

Dr. Amirabadi is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and the IEEE TRANSACTIONS ON POWER ELECTRONICS.