A Novel Fault Ride-Through Strategy Based on Capacitor Energy Storage Inside MMC

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***Abstract*—Once modular multilevel converter (MMC) dc-side short-circuit fault occurs, the conventional fault ride-through (FRT) strategy indeed eliminates dc fault current quickly with the utilization of full-bridge submodules. Thereupon, ac-side active power declines sharply. However, instantaneous high power outage will cause ac-grid power and frequency oscillation and voltage instability, especially in MMC-based high-voltage direct-current transmission system. In order to solve this problem, a novel FRT strategy based on capacitor energy storage (CES) inside MMC (FRT-CES) is proposed, which can accomplish the clearance of dc fault current, ac-side grid support, and stable operation of MMC simultaneously. Through theoretical analysis and mathematical derivation, the prerequisite of CES utilization and universal design of improving ac-side transient characteristics are proposed and quantified. Based on the quantified results, the potential capability of MMC inner CES can be excavated to attenuate the transient change of ac-side active power after dc fault. Also, the proposed universal design is applicable to other MMCs with different capacity ratings. Finally, the threat of dc fault and its negative impact propagating into ac grid are both suppressed. Simulation and experimental results are provided to demonstrate the validity of the proposed FRT-CES strategy.**

***Index Terms*—AC-side transient characteristics, capacitor energy storage (CES), controller parameter optimization, dc-side short-circuit fault, fault ride-through (FRT), modular multilevel converter (MMC).**

I. Introduction

MODULAR multilevel converter (MMC) has become a promising candidate in high-voltage direct-current (HVdc) transmission system for large-scale renewable generations over long distances, due to its superiority of modularity, scalability, high efficiency, superior harmonic performance, and low switching frequency. [1]–[4]. During power transmission through overhead lines, dc short-circuit faults, like pole-to-pole (PTP) short-circuit fault, may be caused by lightning strikes, pollution, and broken tree branches because of insulation breakdown [5], [6]. Nowadays, half-bridge submodule (HBSM)-based MMC is widely employed in applications, such as Trans Bay Cable project [7] and Zhoushan five-terminal MMC-HVdc project in China [8]. A large inrush current will be induced once dc-side short-circuit fault occurs, but HBSM-based MMC cannot stop ac grid feeding the dc fault current due to its lack of dc fault handling capability. The power semiconductors of MMC suffer from overcurrent stress and will be damaged. What is worse, the security and reliability of the entire HVdc grid are threatened, especially in multiterminal MMC–HVdc system.

TABLE I
Fault Handling Time in Some Literature

Fault handling manner	Handling time (ms)					
	[2]	[17]	[18]	[15]	[19]	[20]
Fault blocking	< 3	< 0.4	0.5	—	—	3
FRT	—	—	—	Several	Several	0.4

Gradually, dc fault handling methods attract more attention. Li *et al.* [5] employ double thyristors paralleling with HBSMs to convert the dc fault to ac short-circuit fault. However, the large dc fault current will take a long time to be extinguished naturally due to the small dc line impedance. In order to cope with dc fault, other submodule (SM) topologies have been put forward, such as full-bridge submodule (FBSM) [9], [10], clamp double SMs [11], self-blocking SM [12], [13], etc. The evolution and variation of these SM topologies are analyzed in detail in [14]. The dc fault current can be cleared by blocking MMC because SM capacitor voltages can generate adequate back electromotive force to stop ac grid feeding the fault current. This fault handling manner is called as dc fault blocking [15]. Although the dc fault current can be cleared, the disconnection of the converter will threaten the stability of the adjacent ac network.

Another fault handling manner, called as dc fault ride-through (FRT), is also proposed in [15]. That is, dc fault current can be eliminated quickly by utilizing the negative-level output capability of FBSMs to control MMC dc-side terminal voltage to zero [9], [10]. Meanwhile, reactive power can be still provided to support ac grid voltage by MMC, which operates like a STATCOM. Obviously, the FRT manner is better than the fault blocking manner. However, the number of devices, cost, and power loss are almost doubled in FBSM-based MMC. Therefore, hybrid SMs-based MMC (half HBSMs and half FBSMs) is thought as an optimal solution, which possesses FRT capability as well [6], [15], [16].

The existing studies mainly focus on the dc-side characteristic during the fault, i.e., fault current should be eliminated quickly. Table I provides the fault handling durations in [2], [15] and

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[17]–[20]. The accurate handling durations are not considered and provided in [15] and [19], but they are about several milliseconds (ms). Although the specific configurations of MMCs in these studies are different, their fault handling durations are less than 3 ms in general. Nevertheless, the ac-side transient characteristics caused by dc fault are not considered in these literature.

After dc fault, ac-side active power will decline rapidly. Unfortunately, the instantaneous high power outage will lead to power and frequency oscillation and voltage instability, which seriously threatens the security and stability of ac grid. But few literatures take into consideration the negative impact caused by dc short-circuit fault. In ac grid system, when power mismatching occurs, battery energy storage systems (BESSs) are usually used to fill up the power shortage for providing enhanced frequency response [21]–[23]. For example, frequency oscillation will be caused by power mismatching in grid-connected photovoltaic generation system [24]. After a BESS is plunged to regulate active and reactive power for improving system damping, the frequency response is significantly improved. Noticeably, different from other converters, there is capacitive energy stored in MMC itself.

Therefore, in order to ride through the dc fault and suppress its negative impact propagating into ac grid system, a novel FRT strategy based on the capacitor energy storage inside MMC (FRT-CES) is proposed in this article. The main advantages and contributions of this article are to accomplish the clearance of dc fault, ac grid support, and the stable operation of MMC simultaneously. The potential capability of MMC inner CES is excavated to provide short-term frequency support for ac grid after dc fault. This can even gain time for ac-grid primary and secondary reserve sources providing frequency support in larger time scales due to the slow response of these reserve sources. The proposed prerequisite of the CES utilization and universal design of improving ac-side transient characteristics are both quantified through mathematical analysis, which can be applicable to other MMCs with different capacity ratings. As a result, the threat of dc-side short-circuit fault to the security and stability of MMC and ac grid system will be suppressed.

II. Fault Ride-Through Strategy Based on Inner Capacitor Energy Storage

The main-circuit configuration of three-phase hybrid SMs-based MMC is depicted in Fig. 1. Each arm is composed of $N/2$ HBSMs and $N/2$ FBSMs in series with an arm inductor L. Based on the previous studies upon MMC modeling and control [6], [25], MMC ac-side and dc-side terminal behaviors as well as internal characteristics can be decoupled and controlled independently. In normal operation, dc supply power $P_{\rm dc}$ provides the demand of ac-side transmission power $P_{\rm ac}$ and also provides the absorbing power of MMC $P_{\rm MMC}$ to compensate power dissipation $P_{\rm dis}$. Therefore, the dc power is given as

$$P_{\rm dc} = P_{\rm ac} + P_{\rm MMC} \tag{1}$$

in which $P_{\rm MMC} = P_{\rm dis}$.

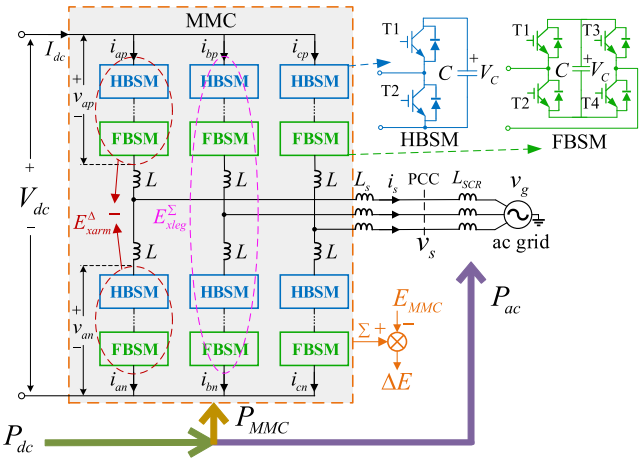

Fig. 1. Main circuit configuration of three-phase hybrid SMs-based MMC.

Once the worst PTP fault occurs in MMC dc side, ac-side transmission power loses abruptly. Usually, grid frequency characteristic is closely related to active power in ac grid. The instantaneous high power outage leads to power mismatching, which will further cause ac-grid frequency oscillation and voltage instability. From (1), it is clear that two control variables of the three are free variables. Since the dc power $P_{\rm dc}$ is zero after dc fault, only the power $P_{\rm MMC}$ can be utilized and extracted temporarily from MMC to attenuate the transient change of ac-side active power $P_{\rm ac}$, due to the stored energy in SM capacitors. In order to provide a new thought for realizing frequency support, a novel FRT-CES is proposed in this article, which considers both dc-side and ac-side transient characteristics after dc fault. When dc fault is detected, MMC dc-side terminal voltage will be controlled to zero with the negative-level insertion of FBSMs, which can eliminate dc fault current quickly. And reactive power is also provided to support ac grid voltage. Furthermore, MMC inner CES is utilized to attenuate the transient change of ac-side active power $P_{\rm ac}$, which can provide short-term frequency support to ac grid. Therefore, the threat of ac-grid power and frequency oscillation and voltage instability can be suppressed. The comprehensive control schematic based on the proposed FRT-CES strategy is presented in Fig. 2, which is applicable in both normal operation and postfault operation.

Since MMC inner CES contributes to active power regulation with the proposed strategy, the main control framework is composed of ac-side active power control, dc-side power control, and MMC inner CES control, which are distinguished with different underpaintings in Fig. 2. Both ac-side and dc-side power control employ proportional-integral (PI) controllers to act on their plants. AC-side power control is realized in the dq-reference frame, and the rated transmission power is $P_{\rm rate}$. The modulation process is brought by digital control and usually equivalent to an inertial link with the time constant equaling to 1.5 times of sampling periods ($\tau_0 = 1.5T_s$) [26]. Remarkably, in normal operation, the red switch sw is open ($sw = 0$) so that the capacitor energy storage deviation controller (CESDC) can maintain the CES deviation ΔE to zero by absorbing power from dc source to compensate the power dissipation $P_{\rm dis}$. ΔE is the difference

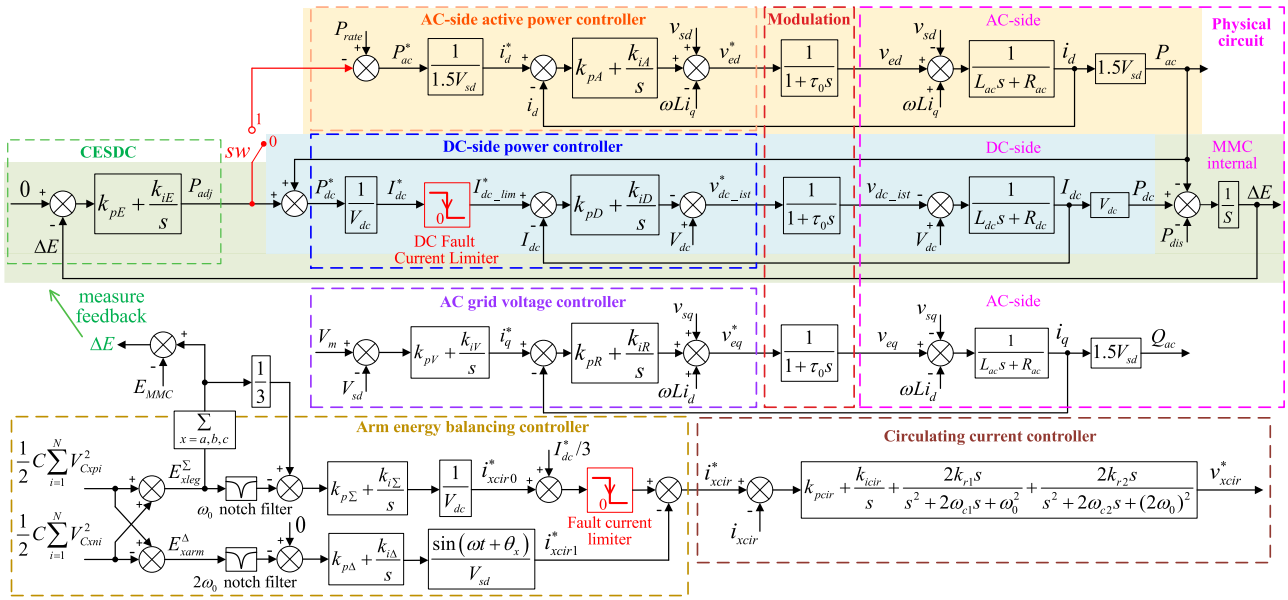

Fig. 2. Comprehensive control schematic based on FRT-CES strategy.

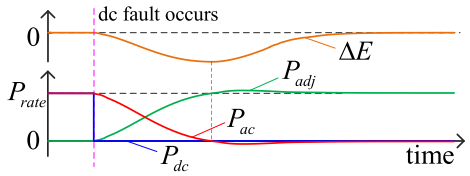

Fig. 3. Simple sketch of ac-side active power regulation after dc fault.

of the total stored energy in all SMs from its nominal value E_{MMC}. During power transmission, there is no low-frequency fluctuation in ΔE due to three-phase symmetry, so only a PI controller is used in CESDC. In normal operation, the output P_{adj} of CESDC equals to the value of power dissipation P_{dis} ($P_{\mathrm{adj}} = P_{\mathrm{MMC}} = P_{\mathrm{dis}}$).

When dc-side PTP fault occurs, dc power P_{dc} drops to zero instantly. In the effect of dc fault current limiter, dc-side fault current is cleared quickly by controlling MMC dc-side voltage to zero. And the red switch *sw* will be closed ($sw = 1$) once the fault is detected. In the new control pathway, the adjusting variable P_{adj} is utilized to regulate the ac-side active power reference ($P^*_{\mathrm{ac}} = P_{\mathrm{rate}} - P_{\mathrm{adj}}$). And then ac-side active power P_{ac} follows its reference instruction P^*_{ac}. In this situation, the actual power of MMC is changed to $P_{\mathrm{MMC}} = -P_{\mathrm{ac}}$. As P_{adj} increases gradually, ac-side active power P_{ac} will be gradually reduced to zero. Its transient change is attenuated, so the short-term frequency support will be provided. A simple sketch of power regulation is depicted in Fig. 3.

Therefore, with the proposed strategy, MMC does not shut down to be off-grid only for its self-protection after dc fault, but adjusts its operating mode to actively cope with the dc fault. Besides, ac grid voltage support is achieved by a reactive power/grid voltage (Q/V) closed-loop control, as depicted in Fig. 2. Interarm and interleg capacitor energy balancing and circulating current control can be referred to [27]–[29]. Inter-SM energy balancing each arm can be realized by the usual capacitor voltage sorting algorithm [30].

III. MMC Internal and AC-Side Transient Characteristics With FRT-CES Strategy

The dc-side fault current has been eliminated as mentioned above, and then both MMC internal and ac-side transient characteristics are taken into consideration in this section.

According to the postfault control pathway with the red switch closed ($sw = 1$) in Fig. 2, the closed-loop transfer function of MMC inner CES deviation ΔE can be derived.

$$\Delta E(s) = \frac{P_{\mathrm{dc}}(s) - G_{\mathrm{ac}}P_{\mathrm{rate}}(s) - P_{\mathrm{dis}}(s)}{s + G_{\mathrm{CESDC}}G_{\mathrm{ac}}} \tag{2}$$

where dc power P_{dc} is zero after dc fault and G_{ac} represents the closed-loop transfer function of ac-side active power, $G_{\mathrm{ac}} = P_{\mathrm{ac}}(s)/P^*_{\mathrm{ac}}(s)$. The transfer function of CESDC is given as

$$G_{\mathrm{CESDC}} = k_{pE} + k_{iE}/s. \tag{3}$$

Based on the ac-side plant, the parameters of the active power controller are usually selected as $k_{pA} = L_{\mathrm{ac}}/\tau_{\mathrm{ac}}$ and $k_{iA} = R_{\mathrm{ac}}/\tau_{\mathrm{ac}}$, so G_{ac} can be derived as

$$G_{\mathrm{ac}} = \frac{1}{(1+\tau_0 s)\,\tau_{\mathrm{ac}} s + 1} \tag{4}$$

where τ_{ac} is usually chosen as 1–5 ms [31] and τ_0 is much smaller. Also, the dynamic performance of ac-side power control is much faster than that of CESDC, so the impact of ac-side power control on the CES deviation $\Delta E(s)$ can be neglected. Hence, G_{ac} can be assumed as a unity gain link ($G_{\mathrm{ac}} = 1$), and the power dissipation $P_{\mathrm{dis}}(s)$ is also negligible. Based on (2)–(4), ΔE(s) can be deduced as

$$\Delta E(s) = \frac{s}{s^2 + k_{pE}\cdot s + k_{iE}}\left(P_{\mathrm{dc}}(s) - P_{\mathrm{rate}}(s)\right). \tag{5}$$

The CES deviation $\Delta E(s)$ reflects the MMC internal characteristic. The ac-side active power, reflecting ac-side transient characteristic, can also be derived easily from Fig. 2

$$P_{\rm ac}(s) = P_{\rm rate}(s) + \frac{k_{pE}\cdot s + k_{iE}}{s^2 + k_{pE}\cdot s + k_{iE}}\left(P_{\rm dc}(s) - P_{\rm rate}(s)\right). \tag{6}$$

From (5) and (6), it is clear that MMC inner CES can indeed be utilized to regulate ac-side active power with the proposed strategy. Therefore, ac-side transient characteristics can be improved by designing the parameter pair (k_{pE}, k_{iE}).

Taking inverse Laplace transformation of (5) and (6), their time-domain responses can be derived under three scenarios: $k_{iE} > k_{pE}^2/4$, $k_{iE} = k_{pE}^2/4$, and $k_{iE} < k_{pE}^2/4$, which are shown in (7) and (8) at the bottom of this page. Without loss of generality, the CES deviation $\Delta\tilde{E}(t)$ and ac-side active power $\tilde{P}_{\rm ac}(t)$ are given in per-unit values with respect to the base value of MMC capacity $P_{\rm rate}$. The following variable $\tilde{x}$ is defined as $\tilde{x} = x/P_{\rm rate}$.

In (7) and (8), $\Delta\tilde{P}_{\rm dc}$ indicates the instantaneous power outage after dc short-circuit fault. It is clearly demonstrated that MMC inner CES deviation $\Delta\tilde{E}(t)$ and ac-side active power $\tilde{P}_{\rm ac}(t)$ are only dependent on the controller parameter pair (k_{pE}, k_{iE}), whatever the capacity rating of MMC is

$$\Delta\tilde{P}_{\rm dc} = (P_{\rm dc} - P_{\rm rate})/P_{\rm rate} = -1 \text{ p.u.} \tag{9}$$

IV. Improvement of AC-Side Transient Characteristics

Since MMC inner CES is utilized to regulate ac-side active power, the inner CES must be sufficient to maintain terminal voltage characteristics during the regulating process. In this section, the prerequisite of inner CES utilization is derived first for guaranteeing CES sufficiency. And then universal design of improving ac-side transient characteristics is proposed, which can be applicable to other MMCs with different capacity ratings.

A. Prerequisite of Inner CES Utilization

When MMC inner CES provides short-term power output to ac grid after dc fault, the CES becomes discharging until ac-side active power is reduced to zero. However, the energy stored in SMs each arm should be large enough to sustain terminal voltages during the discharging process. Otherwise, arm voltages will be deteriorated, which causes dc fault current unextinguished and ac-side currents distorted.

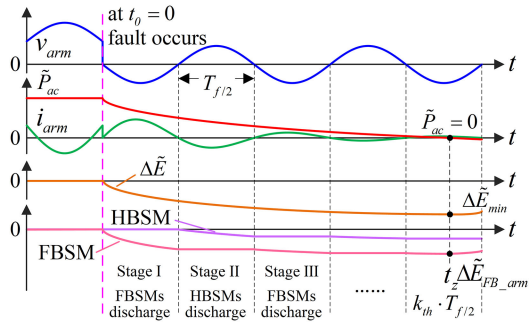

Fig. 4. General view of HBSMs and FBSMs discharging in one arm.

After the PTP fault occurs, MMC dc-side voltage and fault current are controlled to zero instantly, and ac-side active power decreases slowly with the proposed strategy. Arm voltages and arm currents will exclude dc components, and then every arm will discharge at the same rate due to three-phase symmetry. Therefore, the real-time energy deviation every arm is $\Delta\tilde{E}(t)/6$. The common operating principle of HBSMs and FBSMs is employed here for keeping voltage balance in normal operation [32]. Namely, HBSMs and FBSMs synthesize the positive arm voltage together, while only FBSMs synthesize the negative arm voltage. During the postfault transient process, the energy discharging will lead to larger voltage variation in FBSMs. Therefore, the energy deviation in FBSMs every arm should be critically analyzed.

It is assumed that the PTP fault occurs at an instant when arm voltage is about to enter a negative half-wave period, and the power factor is unity. The FBSMs will only discharge as soon as the dc fault occurs, so the energy discharging of FBSMs in this situation is the most serious. The discharging process is depicted in Fig. 4. During the first negative half-wave period (Stage I), FBSMs are negatively inserted and become discharging until arm voltage $v_{\rm arm}$ moves into Stage II, a positive half-wave period. Along with the decrease of ac-side active power $\tilde{P}_{\rm ac}$, the

$$\Delta\tilde{E}(t) = \begin{cases} \left(2\Delta\tilde{P}_{\rm dc}/\sqrt{4k_{iE} - k_{pE}^2}\right)\cdot e^{-k_{pE}\cdot t/2}\cdot\sin\left(\sqrt{4k_{iE} - k_{pE}^2}\cdot t/2\right), & k_{iE} > k_{pE}^2/4 \\ \Delta\tilde{P}_{\rm dc}\cdot t\cdot e^{-k_{pE}\cdot t/2}, & k_{iE} = k_{pE}^2/4 \\ \left(\Delta\tilde{P}_{\rm dc}/\sqrt{k_{pE}^2 - 4k_{iE}}\right)\cdot\left(e^{-(k_{pE} - \sqrt{k_{pE}^2 - 4k_{iE}})\cdot t/2} - e^{-(k_{pE} + \sqrt{k_{pE}^2 - 4k_{iE}})\cdot t/2}\right), & k_{iE} < k_{pE}^2/4 \end{cases} \tag{7}$$

$$\tilde{P}_{\rm ac}(t) = 1 + \Delta\tilde{P}_{\rm dc}\times$$

$$\begin{cases} 1 - e^{-k_{pE}\cdot t/2}\cdot\cos\left(\sqrt{4k_{iE} - k_{pE}^2}\cdot t/2\right) + \left(k_{pE}/\sqrt{4k_{iE} - k_{pE}^2}\right)\cdot e^{-k_{pE}\cdot t/2}\cdot\sin\left(\sqrt{4k_{iE} - k_{pE}^2}\cdot t/2\right), & k_{iE} > k_{pE}^2/4 \\ 1 - e^{-k_{pE}\cdot t/2} + (k_{pE}/2)\cdot t\cdot e^{-k_{pE}\cdot t/2}, & k_{iE} = k_{pE}^2/4 \\ 1 + \left(\left(k_{pE} - \sqrt{k_{pE}^2 - 4k_{iE}}\right)/2\sqrt{k_{pE}^2 - 4k_{iE}}\right)\cdot e^{-\left(k_{pE} - \sqrt{k_{pE}^2 - 4k_{iE}}\right)\cdot t/2} & \\ \quad - \left(\left(k_{pE} - \sqrt{k_{pE}^2 - 4k_{iE}}\right)/2\sqrt{k_{pE}^2 - 4k_{iE}}\right)\cdot e^{-\left(k_{pE} + \sqrt{k_{pE}^2 - 4k_{iE}}\right)\cdot t/2}, & k_{iE} < k_{pE}^2/4 \end{cases} \tag{8}$$

discharging rate in Stage II is slowed down. Therefore, HBSMs will discharge during the entire Stage II due to their larger capacitor voltages than FBSMs. The two stages mentioned above will be repeated until ac-side active power $\tilde{P}_{\rm ac}$ decreases to zero. As a result, FBSMs discharge during odd half-wave periods and HBSMs discharge during even half-wave periods within one arm. MMC inner CES deviation $\Delta\tilde{E}$ will reach its nadir $\Delta\tilde{E}_{\rm min}$ at the moment t_z when ac-side active power $\tilde{P}_{\rm ac}$ is reduced to zero, as depicted in Fig. 4. It is assumed that the dc short-circuit fault occurs at $t_0 = 0$, and the time t_z, called as transient time in this article, locates in the $k_{\rm th}$ half-wave period ($T_{f/2} = \pi/\omega_0$). During the transient process, the energy deviation of FBSMs in one arm will also reach its nadir, denoted as $\Delta\tilde{E}_{\rm FB\_arm}$. When k is even, $\Delta\tilde{E}_{\rm FB\_arm}$ remains unchanged during the current half-wave period because FBSMs are bypassed; when k is odd, $\Delta\tilde{E}_{\rm FB\_arm}$ is varied with t_z and $\Delta\tilde{E}_{\rm min}$ because FBSMs are discharging in the current half-wave period. In conclusion, when k is even, the energy deviation nadir $\Delta\tilde{E}_{\rm FB\_arm}$ is the sum of the discharged energy of FBSMs in the previous odd half-wave periods. When k is odd, $\Delta\tilde{E}_{\rm FB\_arm}$ is also determined by the discharged energy of FBSMs in the current $k_{\rm th}$ half-wave period in addition to the discharged energy in the previous odd half-wave periods. The discharged energy of FBSMs in the $k_{\rm th}$ (k is odd) half-wave period is calculated by subtracting the value $\Delta\tilde{E}((k_{\rm th}-1)T_{f/2})$ at the beginning of the $k_{\rm th}$ half-wave period from the value $\Delta\tilde{E}_{\rm min}$/6. As a result, the energy deviation nadir $\Delta\tilde{E}_{\rm FB\_arm}$ in one arm can be derived as

$$\Delta\tilde{E}_{\rm FB\_arm} = \begin{cases} \left(\Delta\tilde{E}_{\rm min} + \sum_{i=1}^{k}(-1)^i \cdot \Delta\tilde{E}\left((i-1)T_{f/2}\right)\right)/6, & k \text{ is odd} \\ \sum_{i=1}^{k}(-1)^i \cdot \Delta\tilde{E}\left((i-1)T_{f/2}\right)/6, & k \text{ is even.} \end{cases} \quad (10)$$

Besides, MMC inner CES deviation nadir $\Delta\tilde{E}_{\rm min}$ can be derived with letting the derivative of (7) equal to zero. First, the corresponding moment t_z can be solved out.

Substituting (11), shown at the bottom of this page, into (7), the CES deviation nadir $\Delta\tilde{E}_{\rm min}$ can be calculated out as

$$\Delta\tilde{E}_{\rm min} = \Delta\tilde{P}_{\rm dc}/\sqrt{k_{iE}} \cdot e^{-k_{pE}\cdot t_z/2}. \quad (12)$$

Because of only FBSMs generating the negative arm voltage after dc fault, the capacitor voltages of N/2 FBSMs each arm must be large enough to sustain the negative-level output of ac-side terminal voltage, which yields

$$-NV_{C\_\rm FB}(t)/2 \le -\sqrt{2/3}V_s \quad (13)$$

where $V_{C\_\rm FB}(t)$ is the capacitor voltage of an FBSM, assuming that the capacitor voltages of FBSMs each arm are equal. V_s is ac grid voltage (phase-to-phase rms). The actual energy deviation of FBSMs in one arm $\Delta E_{\rm FB\_arm}$ can be expressed as

$$\Delta E_{\rm FB\_arm} = N/2 \cdot CV_{C\_\rm FB}^2(t)/2 - E_{\rm FB\_arm} \quad (14)$$

where $E_{\rm FB\_arm} = CV_{\rm dc0}^2/(4N)$ is the rated energy of FBSMs within one arm. $V_{\rm dc\,0}$ is the rated dc voltage, which is divided equally by N SMs in one arm. Combining (13) with (14), the energy deviation $\Delta\tilde{E}_{\rm FB\_arm}$ derived in (10) must satisfy

$$\Delta\tilde{E}_{\rm FB\_arm} \ge -\left(1-M^2\right)\tilde{E}_{\rm FB\_arm} \triangleq \Delta\tilde{E}_{\rm lim} \quad (15)$$

where M is the ratio of rated ac voltage and dc voltage, given as $M = \sqrt{2/3}V_s(V_{\rm dc}/2)$. $\tilde{E}_{\rm FB\_arm} = E_{\rm FB\_arm}/P_{\rm rate}$ and $\Delta\tilde{E}_{\rm lim}$ is defined as the lowest limit.

Fig. 5(a) presents the 3-D graph of $\Delta\tilde{E}_{\rm FB\_arm}$ and the lowest limit $\Delta\tilde{E}_{\rm lim}$ along with the change of parameter pair (k_{pE}, k_{iE}). The main parameters of MMC are listed in Table II of Section VI. The condition (15) will be satisfied when surface $\Delta\tilde{E}_{\rm FB\_arm}$ is higher than plane $\Delta\tilde{E}_{\rm lim}$. The data points of their intersections are collected and then replotted in Fig. 5(b) with utilizing the curve-fitting method. The blue fitting curve is the borderline of the condition (15), and the corresponding parameter pair (k_{pE}, k_{iE}) should meet the relationship of

$$k_{iE} > 0.01579k_{pE}^3 - 0.6089k_{pE}^2 - 35.66k_{pE} + 1395. \quad (16)$$

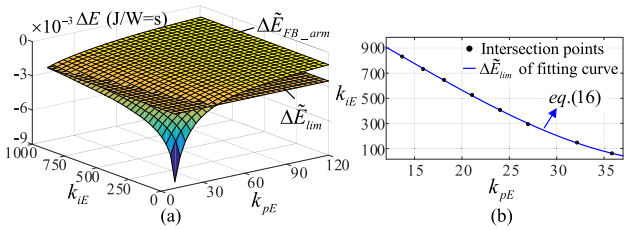

Fig. 5. (a) 3-D graph. (b) Intersecting line of $\Delta\tilde{E}_{\rm FB\_arm}$ and $\Delta\tilde{E}_{\rm lim}$.

TABLE II
SIMULATION PARAMETERS

Items	Values
Rated power $P_{\rm rate}$	1000 MVA
DC voltage $V_{\rm dc0}$	640 kV
AC grid voltage (phase-phase rms) V_s	310 kV
Short-circuit ratio *SCR*	7
Number of HBSMs N/2	10
Number of FBSMs N/2	10
Capacitor voltage V_{C0}	32 kV
SM capacitor C	1.3 mF
Arm inductance L	0.05 H, 1 Ω
AC-link impedance L_s	0.05 H, 1.6 Ω
Sampling period T_s	1e-4 s

$$t_z = \begin{cases} 2\arctan\left(\sqrt{4k_{iE}-k_{pE}^2}/k_{pE}\right)/\sqrt{4k_{iE}-k_{pE}^2}, & k_{iE} > k_{pE}^2/4 \\ 2/k_{pE}, & k_{iE} = k_{pE}^2/4 \\ \ln\left(\left(k_{pE}-\sqrt{k_{pE}^2-4k_{iE}}\right)/\left(k_{pE}+\sqrt{k_{pE}^2-4k_{iE}}\right)\right)/\sqrt{k_{pE}^2-4k_{iE}}, & k_{iE} < k_{pE}^2/4 \end{cases} \quad (11)$$

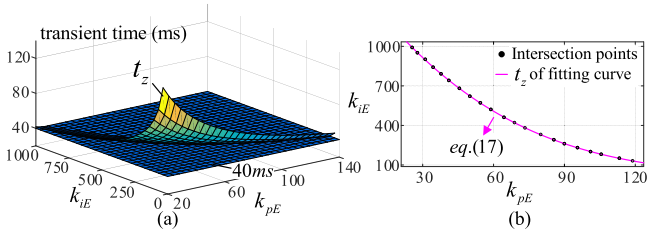

Fig. 6. (a) 3-D graph. (b) Intersecting line of t_z and 40 ms.

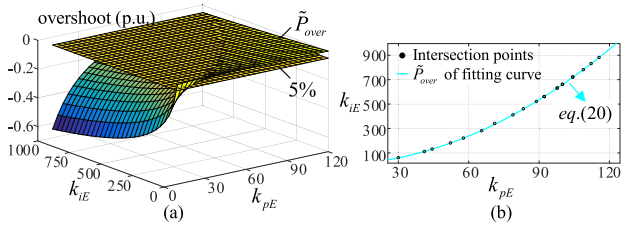

Fig. 7. (a) 3-D graph. (b) Intersecting line of $P_{\rm over}$ and 5%.

When (16) is satisfied, i.e., $\Delta\tilde{E}_{\rm FB\_arm} > \Delta\tilde{E}_{\rm lim}$, arm voltages are generated without distortion to safeguard MMC dc-side and ac-side terminal voltage characteristics, which is beneficial for eliminating dc fault current and improving ac-side transient characteristics with the proposed strategy. Therefore, the condition (16) is the prerequisite of MMC inner CES utilization. And $\Delta\tilde{E}_{\rm lim}$ indicates the available utilization of MMC inner CES. The larger the absolute value of $\Delta\tilde{E}_{\rm lim}$ is, the better the ac-side transient characteristics can be designed.

B. Universal Design of Improving Transient Characteristics

When the prerequisite is satisfied, MMC internal and dc-side characteristics will be controlled as expected. In order to improve ac-side transient characteristics, universal design based on FRT-CES strategy is proposed here to excavate the potential capability of MMC inner CES to achieve short-term frequency support after dc fault.

The moment t_z, zero-crossing point of $\tilde{P}_{\rm ac}$, reflects the transient response time of ac-side active power after dc fault. Different from usual control strategies, the transient time t_z should be longer possibly here so that the transient change of ac-side active power will be slower. Then, the threat of frequency oscillation and voltage instability caused by dc fault will be milder for ac grid.

According to (11), the 3-D graph of t_z can be plotted in Fig. 6(a). Supposing that the acceptable transient time is longer than two fundamental periods (40 ms) in terms of ac-grid security and stability, surface t_z needs to be designed higher than the plane 40 ms. Similarly, with the curve-fitting method, the intersecting line can be obtained, as drawn in Fig. 6(b). The boundary condition is derived as (17). Compared with the transient time in Table I, the transient change of ac-side active power is attenuated a lot with the proposed strategy. Therefore, the short-term frequency support will be achieved by MMC inner CES providing power regulation

$$k_{iE} < -0.0003089k_{pE}^3 + 0.1451k_{pE}^2 - 24.67k_{pE} + 1533. \tag{17}$$

Remarkably, the transient time t_z derived in (11) is just dependent on the parameter pair (k_{pE}, k_{iE}). On the prerequisite of (16), i.e., $\Delta\tilde{E}_{\rm FB\_arm} > \Delta\tilde{E}_{\rm lim}$, the boundary condition (17) is applicable to other MMCs with different capacity ratings when the transient time is desired longer than 40 ms. Therefore, the proposed design of transient time t_z is universal.

After MMC inner CES deviation arrives at the nadir $\Delta\tilde{E}_{\rm min}$, the CES becomes charged to its nominal value $\tilde{E}_{\rm MMC}$ gradually in the effect of CESDC, as depicted in Fig. 3, which is beneficial for postfault stable operation and fast recovery after dc fault cleared. However, the charging power of inner CES comes from ac grid, so there exists an overshoot in ac-side active power. The power overshoot $\tilde{P}_{\rm over}$ can be calculated by letting the derivative of (8) equal to zero, so the corresponding moment t_p can be derived

$$t_p = 2t_z. \tag{18}$$

Substituting (18) into (8), $\tilde{P}_{\rm over}$ will be calculated out

$$\tilde{P}_{\rm over} = 1 + \Delta\tilde{P}_{\rm dc} \cdot \left(1 + e^{-k_{pE}\cdot t_p/2}\right). \tag{19}$$

During the regulating process, the power overshoot should be small. Otherwise, ac-side dynamic characteristics may be deteriorated. When $\tilde{P}_{\rm over}$ is designed to be no more than 5%, the 3-D graph and intersecting line are depicted in Fig. 7. When the boundary condition (20) is satisfied, the overshoot $\tilde{P}_{\rm over}$ will be less than 5% so that the impact of the ac-side power overshoot on ac grid is suppressed

$$k_{iE} < 0.06546k_{pE}^2 + 0.07044k_{pE} - 1.169. \tag{20}$$

From (11), (18), and (19), the power overshoot $\tilde{P}_{\rm over}$ is only dependent on (k_{pE}, k_{iE}) as well, so the universal design of $\tilde{P}_{\rm over}$ is also applicable to other MMCs with different capacity ratings on the prerequisite of (16), i.e., $\Delta\tilde{E}_{\rm FB\_arm} > \Delta\tilde{E}_{\rm lim}$.

C. Optimized Value Region

Summing up the value range consistent with the quantified results in Figs. 5–7, an optimal region marked with underpainting is determined, as depicted in Fig. 8. When the parameter pair (k_{pE}, k_{iE}) locates within the optimal region, the desired transient characteristics, i.e., $\Delta\tilde{E}_{\rm FB\_arm} > \Delta\tilde{E}_{\rm lim}$, $t_z > 40$ ms, and $\tilde{P}_{\rm over} < 5\%$, are satisfied. Compared with the results in Table I, the transient time of ac-side active power is extended over ten times with limited overshoot.

Furthermore, if ac-side transient characteristics are required stricter for the security and stability of ac grid system, the parameter region can be optimized again with above-mentioned universal design. The boundary conditions of $t_z > 60$ ms and $\tilde{P}_{\rm over} < 3\%$ are also added in Fig. 8, which are marked with Curve ⑤ and ⑦, respectively. As a result, the optimized region is further divided into four regions. Region a represents the

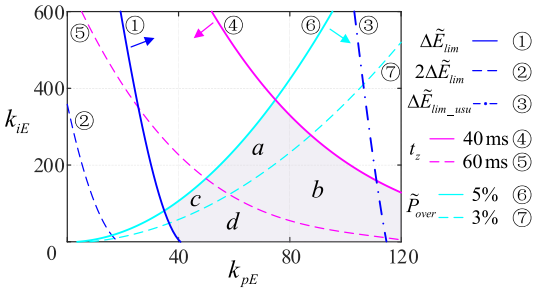

Fig. 8. Optimized value region based on the derived prerequisite and universal design of ac-side transient characteristics.

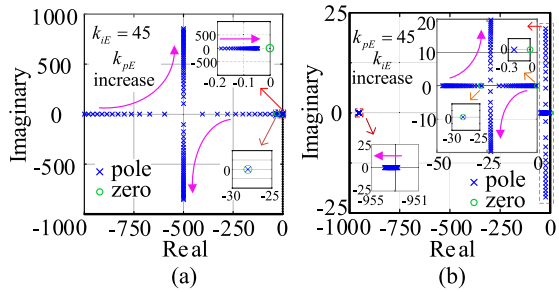

Fig. 9. Closed-loop eigenvalues of the small-signal state-space model with the change of (a) k_{pE} and (b) k_{iE}.

region that satisfies $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$, 40 ms $< t_z <$ 60 ms, and 3% $< \tilde{P}_{\mathrm{over}} <$ 5%, while Region d represents the region that satisfies $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$, $t_z >$ 60 ms, and $\tilde{P}_{\mathrm{over}} <$ 3%. Similarly, the meanings of other regions can also be known. The parameters (k_{pE}, k_{iE}) can be adjusted according to the desired transient characteristics. Besides, the boundary condition of $2\Delta\tilde{E}_{\mathrm{lim}}$ equipped in MMC is also provided in Fig. 8, which is denoted with Curve ②. Clearly, when MMC inner CES is larger, e.g., larger SM capacitance or MMC integrated with batteries, more energy can be utilized to provide short-term frequency support to ac grid. The threat of power and frequency oscillation can be suppressed further.

When inner CES is reduced to 35 kJ/MVA (35 ms) [33], the performance of the proposed strategy is also analyzed and evaluated. The corresponding energy lowest limit is $\Delta\tilde{E}_{\mathrm{lim\_usu}}$, which is depicted with Curve ③ in Fig. 8. Although MMC inner CES is reduced, there is still an optimized region that satisfies $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim\_usu}}$, $t_z >$ 60 ms, and $\tilde{P}_{\mathrm{over}} <$ 3%. And $\tilde{P}_{\mathrm{over}}$ will be further reduced. In this case, the short-term frequency support can also be provided with the proposed strategy after the dc fault.

V. Small-Signal Stability Analysis

Since the parameter pair (k_{pE}, k_{iE}) is adjusted based on the desired ac-side transient characteristics, the influence of the variation of (k_{pE}, k_{iE}) on the stability of the control system should be carefully evaluated.

The postfault control loop ($sw = 1$) is considered here. The state-space model of the control system can be established according to CESDC, active power controller, ac-side plant, the plant of CES, and their input–output relationships in Fig. 2. Two state variables of them are defined as follows:

$$\frac{dx_1}{dt} = 0 - \Delta E \tag{21}$$

$$\frac{dx_2}{dt} = \frac{P_{\mathrm{rare}} - P_{\mathrm{adj}}}{1.5V_{\mathrm{sd}}} - i_d. \tag{22}$$

Neglecting the impact of modulation process, a four-order state-space model of the control system is established and then linearized around a given steady-state operation point to obtain the small-signal model according to [34]

$$\Delta\dot{x} = A(x_0, u_0)\Delta x + B(x_0, u_0)\Delta u \tag{23}$$

where $\Delta x = [\Delta x_1, \Delta x_2, \Delta i_d, \Delta(\Delta E)]^{\mathrm{T}}$, $\Delta u = [\Delta P_{\mathrm{rate}}, \Delta P_{\mathrm{dc}}, \Delta P_{\mathrm{dis}}]^{\mathrm{T}}$, and $A(x_0,u_0)$ and $B(x_0,u_0)$ are given as

$$A(x_0,u_0) = \begin{bmatrix} 0 & 0 & 0 & -1 \\ -\frac{k_{iE}}{1.5V_{\mathrm{sd}}} & 0 & -1 & \frac{k_{pE}}{1.5V_{\mathrm{sd}}} \\ -\frac{k_{iE}k_{pA}}{1.5V_{\mathrm{sd}}L_{\mathrm{ac}}} & \frac{k_{iA}}{L_{\mathrm{ac}}} & -\frac{k_{pA}+R_{\mathrm{ac}}}{L_{\mathrm{ac}}} & \frac{k_{pE}k_{pA}}{1.5V_{\mathrm{sd}}L_{\mathrm{ac}}} \\ 0 & 0 & -1.5V_{\mathrm{sd}} & 0 \end{bmatrix} \tag{24}$$

$$B(x_0,u_0) = \begin{bmatrix} 0 & 0 & 0 \\ 1/(1.5V_{\mathrm{sd}}) & 0 & 0 \\ k_{pA}/(1.5V_{\mathrm{sd}}L_{\mathrm{ac}}) & 0 & 0 \\ 0 & 1 & -1 \end{bmatrix}. \tag{25}$$

Based on (23), the closed-loop eigenvalues of the small-signal state-space model with the change of controller parameters (k_{pE}, k_{iE}) can be obtained, as shown in Fig. 9. The parameters of the active power controller are selected as $k_{pA} = L_{\mathrm{ac}}/\tau_{\mathrm{ac}}$ and $k_{iA} = R_{\mathrm{ac}}/\tau_{\mathrm{ac}}$, so the order of the small-signal model will be reduced to three due to zero-pole cancelation. In Fig. 9, there are three trend lines of the closed-loop eigenvalues with the change of (k_{pE}, k_{iE}). When k_{pE} is increased gradually, two eigenvalues are approaching to the line with a real part of -500, and another one is approaching to the origin. All poles will be located in the left-half s-plane, so the control system is stable with the change of k_{pE}. Similarly, all poles are located in the left-half s-plane with the change of k_{iE}. Merely, one pole is close to the origin when the value of k_{iE} is very small, but the control system is still stable.

Considering the finite CES inside MMC, the prerequisite of inner CES utilization should be satisfied first. As a result, when (k_{pE}, k_{iE}) are adjusted based on the proposed quantified analysis in Section IV, the stability of the control system can be guaranteed.

VI. Simulation Results

In order to verify the validity of the proposed FRT-CES strategy, simulation is carried out by establishing a

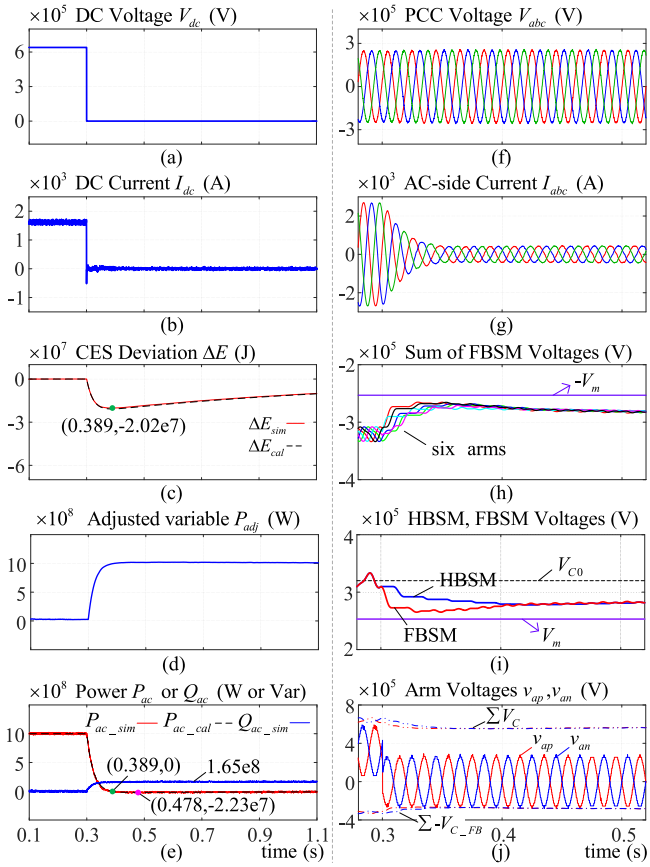

Fig. 10. Simulation results of Case I: $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$, $t_z > 60$ ms, $\tilde{P}_{\mathrm{over}} < 3\%$.

1000 MVA/640 kV three-phase hybrid SMs-based MMC model in MATLAB/imulink platform. The simulation diagram is depicted in Fig. 1, and the main parameters are listed in Table II. In order to enhance the simulation efficiency, 20 SMs per arm are used instead of hundreds of SMs, so the equivalent SM capacitor voltage is 32 kV. SM capacitance is chosen so that the capacitor voltage fluctuation is limited about 5% of its nominal voltage.

A. *Case I: (k_{pE}, k_{iE}) Locates in Region* d

First, the performance of the proposed FRT-CES strategy with ($k_{pE} = 45$, $k_{iE} = 45$) located in Region d of Fig. 8 during dc-side PTP fault is investigated. The corresponding transient characteristics are $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$, $t_z > 60$ ms, and $\tilde{P}_{\mathrm{over}} < 3\%$. The detailed simulation results are presented in Fig. 10. During normal operation, MMC delivers 1000 MW of active power to ac grid. At $t = 0.3$ s, dc-side PTP fault occurs and dc voltage drops to zero instantly, as shown in Fig. 10(a). Under the control of FRT-CES strategy, dc fault current is eliminated quickly by controlling the dc components of arm voltages to zero, as seen in Fig. 10(b) and (j). In Fig. 10(d), the output P_{adj} of CESDC gradually increases and is utilized to reduce the reference of ac-side active power P^*_{ac}, which will contribute to attenuating the transient change of P_{ac} after the dc fault. From Fig. 10(c) and (e), it is clearly shown that the simulation results of inner CES deviation ΔE_{sim} and ac-side active power

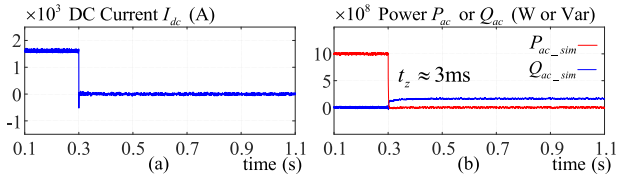

Fig. 11. (a) DC current. (b) AC-side active power and reactive power with conventional FRT strategy.

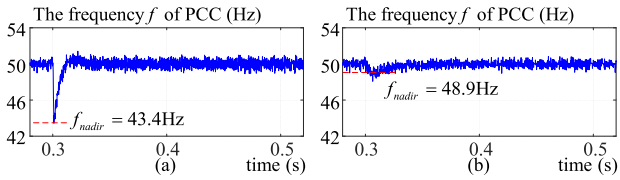

Fig. 12. Frequency of PCC with (a) conventional FRT strategy and (b) proposed FRT-CES strategy.

$P_{\mathrm{ac\_sim}}$ are highly consistent with the calculation results of ΔE_{cal} and $P_{\mathrm{ac\_cal}}$ based on (7) and (8), which proves the theoretical analysis and mathematical derivation in Section III. Besides, the transient time t_z of ac-side active power P_{ac} is extended to 89 ms, which is over 60 ms. The power overshoot $\tilde{P}_{\mathrm{over}}$ is 2.23% (<3%). Also, 165 MVar of reactive power is provided to support PCC voltages, as depicted in Fig. 10(e) and (f).

In order to present the waveforms clearly, Fig. 10(f)–(j) provide the results within the period of 0.3 ∼ 0.5 s. Fig. 10(i) shows that FBSMs and HBSMs (in phase A upper arm) discharge alternatively after the dc fault, and the sum of capacitor voltages in FBSMs is lower than that in HBSMs, but larger than the phase peak voltage V_m of PCC. From Fig. 10(h), the sum of FBSM capacitor voltages each arm is always larger than V_m, so the negative-level output capability of FBSMs is sufficient to meet the demand of negative arm voltage, which can also be proved in Fig. 10(j) with enough capacitor voltages $\Sigma - V_{C\_\mathrm{FB}}$ of FBSMs. This implies that the prerequisite $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$ is satisfied. The waveform quality of arm voltages is guaranteed, so the dc fault current is eliminated and ac-side currents in Fig. 10(g) are controlled well. Since the prerequisite has been satisfied, a little longer time of the CES deviation ΔE returning to zero after reaching its nadir ΔE_{min}, as seen in Fig. 10(c), will not bring any adverse influence. These simulation results coincide with the desired performance in Region *d*.

In comparison, the simulation results of conventional FRT strategy without utilizing MMC inner CES [15], [19], [20] are provided in Fig. 11. Similarly, dc fault current is eliminated quickly, but ac-side active power declines to zero sharply within 3 ms, which causes a severe drop in the grid frequency, as shown in Fig. 12(a). The grid frequency of PCC is detected by phase-locked loop [35], and the frequency nadir is 43.4 Hz. However, when the proposed FRT-CES strategy is employed, the short-term frequency support is provided so that the transient characteristic of grid frequency is greatly improved. The frequency nadir is increased to 48.9 Hz, as seen in Fig. 12(b).

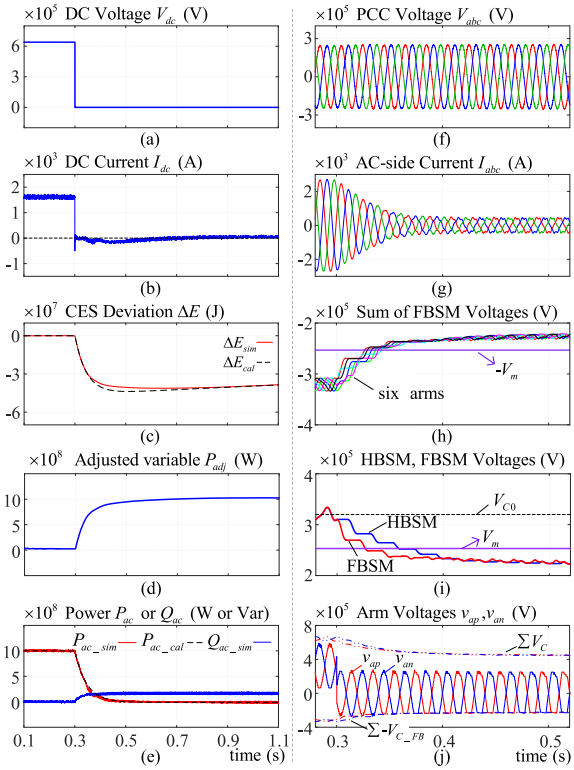

Fig. 13. Simulation results of Case II: $\Delta\tilde{E}_{\mathrm{FB\_arm}} < \Delta\tilde{E}_{\mathrm{lim}}$.

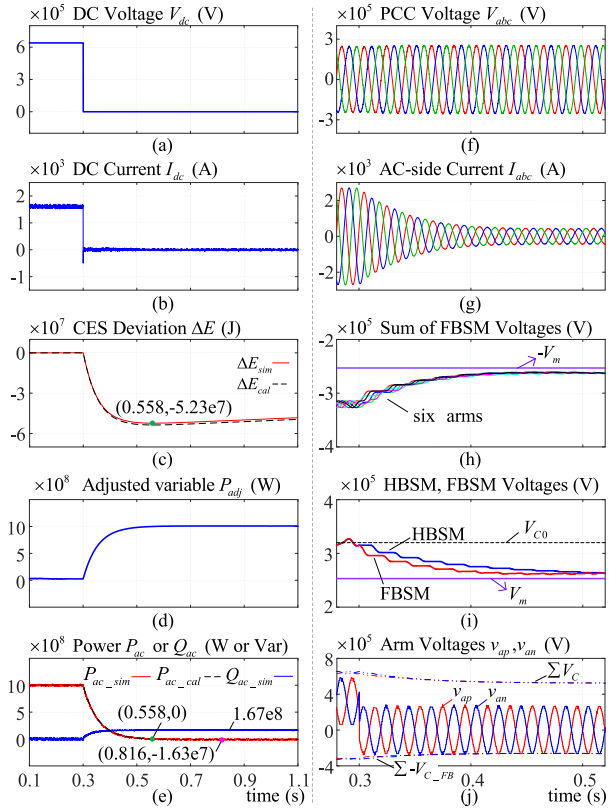

Fig. 14. Simulation results of Case III: $2\Delta\tilde{E}_{\mathrm{lim}}$ in MMC.

B. Case II: (k_{pE}, k_{iE}) Locates Where $\Delta\tilde{E}_{\mathrm{FB\_arm}} < \Delta\tilde{E}_{lim}$

Fig. 13 presents the simulation results of the proposed strategy with ($k_{pE} = 22,\ k_{iE} = 5$) located below the Curve ① in Fig. 8. Similarly, dc fault occurs at $t = 0.3$ s. More energy is released to attenuate the transient change of ac-side active power, as shown in Fig. 13(c) and (e). However, Fig. 13(h) clearly shows that the sum of FBSM capacitor voltages each arm is lower than the phase peak voltage V_m after dc fault, which means $\Delta\tilde{E}_{\mathrm{FB\_arm}} < \Delta\tilde{E}_{\mathrm{lim}}$. Therefore, the negative-level output capability of FBSMs will be insufficient to synthesize the desired negative arm voltages, which causes negative arm voltages flat-topped, as seen in Fig. 13(j). The distorted arm voltages cause dc fault current unextinguished and ac-side currents distorted, as presented in Fig. 13(b) and (g). Therefore, the dc fault is not ridden through. Notably, positive arm voltages are generated normally in Fig. 13(j). Although the sum of capacitor voltages in HBSMs is also lower than V_m in Fig. 13(i), both HBSMs and FBSMs can synthesize positive arm voltages together. This sufficiently declares that the capacitor voltages of FBSMs should be concerned first.

In consequence, the prerequisite $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$ should be satisfied first, and then the improvement of ac-side transient characteristics can be considered. Otherwise, dc fault current cannot be eliminated, and ac grid currents will be deteriorated.

C. Case III: $2\Delta\tilde{E}_{lim}$ in MMC

The performance of FRT-CES strategy with two times of CES inside MMC is also investigated during dc-side PTP fault. Double CES is achieved with SM capacitance doubled here ($C = 2.6$ mF). The lowest limit of CES deviation is increased to $2\Delta\tilde{E}_{\mathrm{lim}}$, so more energy can be utilized to provide short-term frequency support to ac grid. The parameter pair is selected as ($k_{pE} = 18,\ k_{iE} = 3$), and Fig. 14 presents the corresponding simulation results. Similarly, the dc fault current is eliminated quickly, and 167 MVar of reactive power is generated to support ac grid voltage after dc fault. Besides, the transient time t_z of ac-side active power is extended to 258 ms, and power overshoot $\tilde{P}_{\mathrm{over}}$ is limited to 1.63%, as shown in Fig. 14(e). Although more energy is released to attenuate the transient change of ac-side active power in Fig. 14(c) compared with the two cases above, Fig. 14(h) shows that the sum of FBSM capacitor voltages each arm is still larger than phase peak voltage V_m of ac grid due to $2\Delta\tilde{E}_{\mathrm{lim}}$ in MMC. Therefore, the waveform quality of arm voltages and ac-side currents can be guaranteed, as presented in Fig. 14(j) and (g).

The simulation results of conventional FRT strategy with $2\Delta\tilde{E}_{\mathrm{lim}}$ inside MMC are almost the same as those in Fig. 11 ($\Delta\tilde{E}_{\mathrm{lim}}$ in MMC). Fig. 15 presents the frequency responses with conventional FRT strategy and the proposed FRT-CES strategy under the condition of $2\Delta\tilde{E}_{\mathrm{lim}}$ equipped in MMC. Clearly, the amount of stored energy has little impact on the frequency response with conventional FRT strategy. However, when the proposed FRT-CES strategy is applied, the frequency is scarcely affected by the dc fault because more energy is utilized to attenuate the transient change of ac-side active power. The frequency nadir is 49.4 Hz.

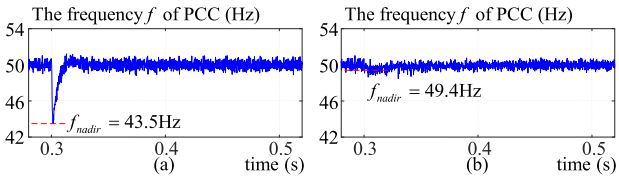

Fig. 15 Frequency of PCC with (a) conventional FRT strategy and (b) proposed FRT-CES strategy under $2\Delta\tilde{E}_{\rm lim}$ in MMC.

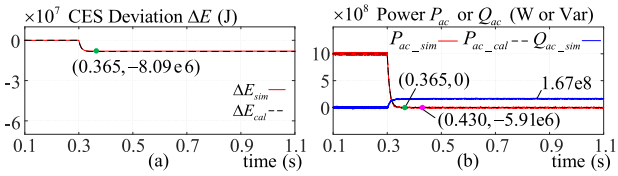

Fig. 16. Simulation results of Case IV: $\Delta\tilde{E}_{\rm usu}$ in MMC.

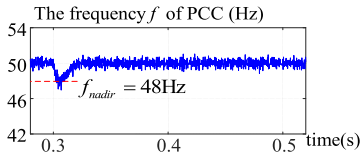

Fig. 17. Frequency of PCC with the proposed strategy in Case IV.

D. Case IV: $\Delta\tilde{E}_{\rm lim\_usu}$ in MMC

The performance of FRT-CES strategy under the condition of the CES reduced to 35 kJ/MVA [33] is also investigated. The corresponding SM capacitance is $C = 0.57$ mF, and the controller parameters are designed as ($k_{pE} = 120$, $k_{iE} = 1$). From Fig. 16, the transient time t_z is 65 ms and the power overshoot $\tilde{P}_{\rm over}$ is limited to 0.59%, which still satisfy $\Delta\tilde{E}_{\rm FB\_arm} > \Delta\tilde{E}_{\rm lim\_usu}$, $t_z > 60$ ms, and $\tilde{P}_{\rm over} < 3\%$. The optimized region in Fig. 8 is reduced along with the reduction of inner CES, and the power overshoot is greatly reduced. Because lesser active power is absorbed from ac grid to charge MMC inner CES, the time to obtain $\Delta E = 0$ again will be long. Since the prerequisite ($\Delta\tilde{E}_{\rm FB\_arm} > \Delta\tilde{E}_{\rm lim}$) has been satisfied to guarantee stable operation, the longer recovery time will not bring negative impacts.

Compared with conventional FRT strategy, the frequency characteristic has also improved a lot, and the frequency nadir has increased from 43.5 to 48 Hz, as depicted in Fig. 17. The short-term frequency support can also be provided with the proposed strategy.

VII. Experimental Results

The proposed strategy is also experimentally validated on a single-phase hybrid SMs-based MMC prototype, as shown in Fig. 18. And its layout is depicted in Fig. 19. In order to verify the universal design that is applicable to MMCs of different capacity ratings, $\Delta\tilde{E}_{\rm lim}$ of the MMC prototype is designed same as three-phase MMC in simulation. Therefore, the experiments under the same controller parameters (k_{pE}, k_{iE}) as Case I–III in simulation are carried out. The experimental parameters are

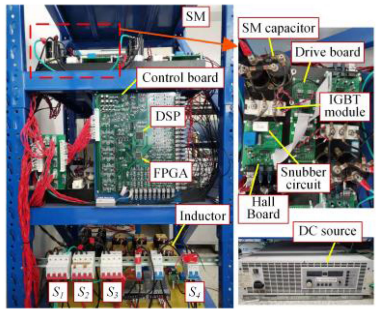

Fig. 18. Photograph of the experimental setup.

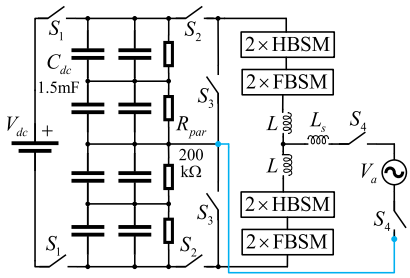

Fig. 19. Layout of the single-phase MMC prototype.

TABLE III
Single-Phase MMC Experimental Parameters

Items	Values
Rated power $P_{\rm rate}$	560 W
DC voltage $V_{\rm dc0}$	300 V
AC grid voltage (rms) V_s	84 V
Number of HBSMs $N/2$	2
Number of FBSMs $N/2$	2
Capacitor voltage $V_{\rm C0}$	75 V
SM capacitor C	2 mF
Arm inductance L	3 mH
AC-link impedance L_s	3 mH
Sampling frequency f	7500 Hz

provided in Table III. The control system is implemented with using a TMS320F28335 DSP and an EP4CE10E22C8 FPGA. Active and reactive power ($P_{\rm ac}$, $Q_{\rm ac}$), CES deviation (ΔE), and adjusting variable ($P_{\rm adj}$) are output by a 12-bit digital-to-analog chip MAX5742. The others are gathered by voltage or current probes, and all experimental waveforms are acquired by a scope recorder YOKOGAWA DL850E. Noticeably, the switch S_3 is closed to emulate dc line PTP fault, and switch S_2 is open subsequently for protecting dc source.

First, the experimental results with the same parameters as simulation in Case I, ($k_{pE} = 45$, $k_{iE} = 45$), are shown in Fig. 20. In normal operation, MMC delivers 550 W of active power to ac grid. It is clear that the dc-side fault current is eliminated immediately once dc-side PTP fault occurs. And 137 Var of reactive power is output to support ac grid voltage. Meanwhile, MMC inner CES is utilized to attenuate the change rate of ac-side active power. The transient time t_z is extended to 90 ms with power overshoot $\tilde{P}_{\rm over}$ limited to 2.14%. And the sum of capacitor voltages in FBSMs each arm is always larger

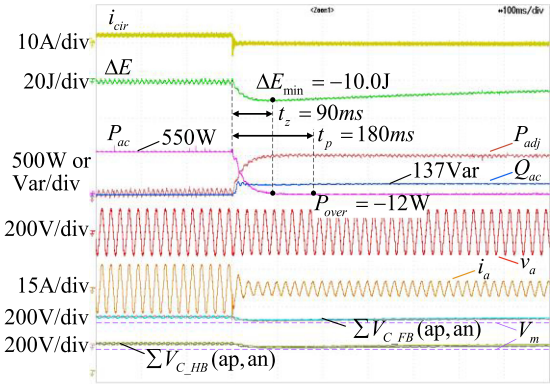

Fig. 20. Experimental results in Case I.

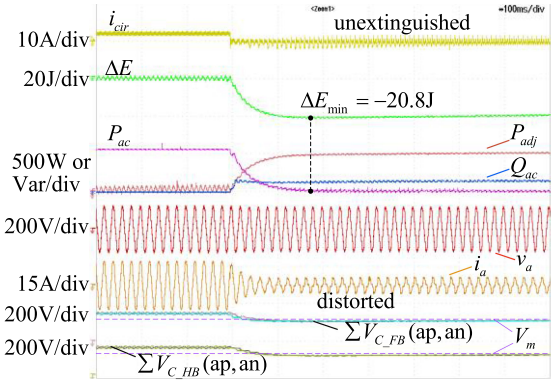

Fig. 21. Experimental results in Case II.

than the phase peak voltage, which indicates the prerequisite $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$ is satisfied.

In single-phase MMC, inner CES is just the total stored energy in the leg. There exists a second-order harmonic ripple in the CES deviation ΔE as analyzed in [36] and [37], which causes a second-order harmonic (2^{nd}_{ω}) component in the leg circulating current i_{cir}. In the effect of CESDC, its output P_{adj} will include 2^{nd}_{ω} component. Because P_{adj} is utilized to regulate ac-side active power reference P^*_{ac} after dc fault, the 2^{nd}_{ω} component will be introduced into P_{ac}. Furthermore, a third-order harmonic component will be introduced into ac-side current i_a. However, in three-phase MMC, the 2^{nd}_{ω} components of leg CES deviations cancel with each other. Therefore, the total CES deviation ΔE in MMC excludes harmonic components so that the proposed strategy will not introduce harmonic components into ac-side currents in three-phase MMC, which can be verified in the simulation results.

Fig. 21 presents the experimental results in Case II, $\Delta\tilde{E}_{\mathrm{FB\_arm}} < \Delta\tilde{E}_{\mathrm{lim}}$ with ($k_{pE} = 22$, $k_{iE} = 5$). After dc fault, the sum of capacitor voltages in FBSMs each arm is not sufficient to synthesize the negative arm voltage, which causes both dc-side and ac-side terminal voltages distorted. As a result, dc fault current i_{cir} cannot be extinguished, and ac-side current i_a is also distorted. Therefore, in order to acquire better MMC internal, dc-side, and ac-side transient characteristics, the prerequisite $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$ should be satisfied at first.

Fig. 22 presents the experimental results under Case III, $2\Delta\tilde{E}_{\mathrm{lim}}$ in MMC with ($k_{pE} = 18$, $k_{iE} = 3$). Similarly, the SM capacitance is doubled ($C = 4$ mF). Once PTP fault occurs,

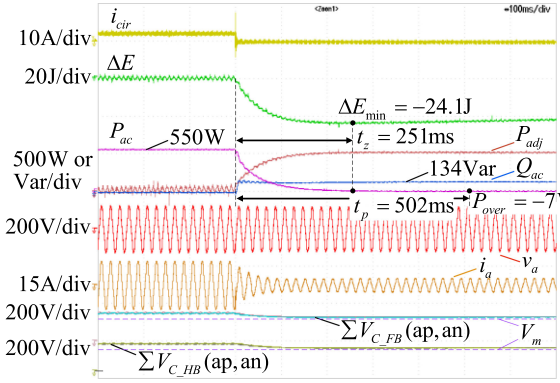

Fig. 22. Experimental results in Case III.

the dc-side fault current is eliminated quickly, and 134 Var of reactive power is provided to support ac grid voltage. The transient time t_z of P_{ac} is extended to 251 ms, and power overshoot $\tilde{P}_{\mathrm{over}}$ is limited to 1.25%. Meanwhile, the prerequisite $\Delta\tilde{E}_{\mathrm{FB\_arm}} > \Delta\tilde{E}_{\mathrm{lim}}$ is always satisfied during the regulating process.

These experimental results are highly consistent with the simulation results in Case I–III. The validity of the proposed FRT-CES strategy and universal design has been well verified.

VIII. Conclusion

A novel FRT-CES has been proposed in this article. With the proposed strategy, the clearance of dc fault current, ac-side grid support, and stable operation of the converter (MMC) can be accomplished simultaneously. After dc fault, MMC is not off-grid only for its self-protection, but actively adjusts its operation to cope with the dc fault. MMC inner CES is utilized to attenuate the transient change of ac-side active power after dc fault, as a result of which an additional function of the stored energy in MMC is developed to provide short-term frequency support to ac grid. Besides, the prerequisite of inner CES utilization and universal design of improving ac-side transient characteristics are also proposed and quantified through mathematical analysis, which can not only guide the design of controller parameters to acquire the desired ac-side transient characteristics, but also guide the design of the CES requirement in MMC. As long as the prerequisite is satisfied, the proposed universal design is applicable to other MMCs with different capacity ratings. Compared with conventional FRT strategy, the transient time of ac-side active power can be extended to tens to hundreds of milliseconds with the proposed strategy. Better ac-side transient characteristics can be acquired with larger CES in MMC. As a result, the threat of dc fault to the security and stability of MMC and ac grid system will be suppressed with the proposed strategy.

References

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[2] T. H. Nguyen, K. A. Hosani, M. S. E. Moursi, and F. Blaabjerg, "An overview of modular multilevel converters in HVDC transmission systems with STATCOM operation during pole-to-pole DC short circuits," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4137–4160, May 2019.

[3] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.
[4] M. Priya, P. Ponnambalam, and K. Muralikumar, "Modular-multilevel converter topologies and applications – A review," *IET Power Electron.*, vol. 12, no. 2, pp. 170–183, Feb. 2019.
[5] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.
[6] S. Cui and S. K. Sul, "A comprehensive DC short-circuit fault ride through strategy of hybrid modular multilevel converters (MMCs) for overhead line transmission," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7780–7796, Nov. 2016.
[7] J. Dorn, H. Gambach, J. Strauss, and T. Westerweller, "Trans bay cable—A breakthrough of VSC multilevel converters in HVDC transmission," in *CIGRE Colloq.*, San Francisco, CA, USA, Mar. 2012.
[8] G. Tang, Z. He, H. Pang, X. Huang, and X.-P. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE J. Power Energy Syst.*, vol. 1, no. 2, pp. 22–35, Jun. 2015.
[9] G. P. Adam and I. E. Davidson, "Robust and generic control of full-bridge modular multilevel converter high-voltage DC transmission systems," *IEEE Trans. Power Del.*, vol. 30, no. 6, pp. 2468–2476, Dec. 2015.
[10] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Full-bridge MMC converter optimal design to HVDC operational requirements," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1342–1350, Jun. 2016.
[11] X. Yu, Y. Wei, and Q. Jiang, "STATCOM operation scheme of the CDSM-MMC during a pole-to-pole DC fault," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1150–1159, Jun. 2016.
[12] W. Xiang, W. Lin, T. An, J. Wen, and Y. Wu, "Equivalent electromagnetic transient simulation model and fast recovery control of overhead VSC-HVDC based on SB-MMC," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 778–788, Apr. 2017.
[13] R. Zeng, L. Xu, and L. Yao, "An improved modular multilevel converter with DC fault blocking capability," in *Proc. IEEE PES General Meeting Conf. Expo.*, National Harbor, MD, USA, Jul. 2014, pp. 1–5.
[14] L. Huang *et al.*, "The evolution and variation of sub-module topologies with DC-fault current clearing capability in MMC-HVDC," in *Proc. IEEE 3rd Int. Future Energy Electron. Conf.*, Kaohsiung, Taiwan, Jun. 2017, pp. 1938–1943.
[15] S. Cui, S. Kim, J. Jung, and S. Sul, "Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 610–616.
[16] J. Hu, K. Xu, L. Lin, and R. Zeng, "Analysis and enhanced control of hybrid-MMC-based HVDC systems during asymmetrical DC voltage faults," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1394–1403, Jun. 2017.
[17] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.
[18] R. Li, J. E. Fletcher, L. Xu, D. Holliday, and B. W. Williams, "A hybrid modular multilevel converter with novel three-level cells for DC fault blocking capability," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 2017–2026, Aug. 2015.
[19] M. Lu, J. Hu, L. Lin, and K. Xu, "Zero DC voltage ride through of a hybrid modular multilevel converter in HVDC systems," *IET Renewable Power Gener.*, vol. 11, no. 1, pp. 35–43, Nov. 2017.
[20] Z. Suo, G. Li, L. Xu, R. Li, W. Wang, and Y. Chi, "Hybrid modular multilevel converter based multi-terminal DC/DC converter with minimised full-bridge submodules ratio considering DC fault isolation," *IET Renewable Power Gener.*, vol. 10, no. 10, pp. 1587–1596, Nov. 2016.
[21] M. Benini, S. Canevese, D. Cirio, and A. Gatti, "Battery energy storage systems for the provision of primary and secondary frequency regulation in Italy," in *Proc. IEEE 16th Int. Conf. Environ. Elect. Eng.*, Florence, Italy, Jun. 2016, pp. 1–6.
[22] F. M. Gonzalez-Longatt and S. M. Alhejaj, "Enabling inertial response in utility-scale battery energy storage system," in *Proc. IEEE Innov. Smart Grid Technol. Asia*, Nov. 2016, pp. 605–610.
[23] Y. J. A. Zhang, C. Zhao, W. Tang, and S. H. Low, "Profit-maximizing planning and control of battery energy storage systems for primary frequency control," *IEEE Trans. Smart Grid*, vol. 9, no. 2, pp. 712–723, Mar. 2018.
[24] X. Zhang, L. Yang, and X. Zhu, "Integrated control of photovoltaic-energy storage system for power oscillation damping enhancement," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, Hefei, China, May 2016, pp. 1571–1575.
[25] D. Wu and L. Peng, "Analysis and suppressing method for the output voltage harmonics of modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4755–4765, Jul. 2016.
[26] C. Dong, S. Yang, H. Jia, and P. Wang, "Padé-based stability analysis for a modular multilevel converter considering the time delay in the digital control system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5242–5253, Jul. 2019.
[27] S. Cui, S. Kim, J. Jung, and S. Sul, "A comprehensive cell capacitor energy control strategy of a modular multilevel converter (MMC) without a stiff DC bus voltage source," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 602–609.
[28] A. E. Leon and S. J. Amodeo, "Energy balancing improvement of modular multilevel converters under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6628–6637, Aug. 2017.
[29] D. Wu and L. Peng, "Characteristics of nearest level modulation method with circulating current control for modular multilevel converter," *IET Power Electron.*, vol. 9, no. 2, pp. 155–164, Oct. 2016.
[30] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.
[31] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4858–4867, Dec. 2012.
[32] J. Lee, J. Jung, and S. Sul, "Balancing of submodule capacitor voltage of hybrid modular multilevel converter (MMC) under DC bus voltage variation of HVDC system," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10458–10470, Nov. 2019.
[33] Z. Xu, H. Xiao, and Z. Zhang, "Selection methods of main circuit parameters for modular multilevel converters," *IET Renewable Power Gener.*, vol. 10, no. 6, pp. 788–797, Jul. 2016.
[34] P. S. Kundur, *Power System Stability and Control*. New York, NY, USA: McGraw-Hill, 1994.
[35] D. Zhu, S. Zhou, X. Zou, and Y. Kang, "Improved design of PLL controller for LCL-type grid-connected converter in weak grid," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2019.2943634.
[36] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 358–371, Jan. 2015.
[37] G. Bergna-Diaz, J. A. Suul, and S. D'Arco, "Energy-based state-space representation of modular multilevel converters with a constant equilibrium point in steady-state operation," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4832–4851, Jun. 2018.

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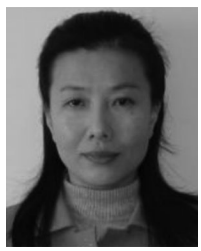

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