A Modular Multilevel Resonant DC–DC Converter

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***Abstract*—A modular multilevel resonant (MMR) dc–dc converter, its modulation, and control are proposed in this article. The MMR converter inherits the desirable features of both the modular multilevel converter and *LLC* resonant converter, such as high voltage capability, easy fault-tolerant operation, and soft switching. Besides, the MMR can regulate the output voltage over a wide input voltage range with much narrower frequency range compared to conventional resonant converters. By constantly inserting certain number of submodules into the arm according to the input voltage, the resonant tank voltage can be regulated with a relatively constant amplitude regardless of the wide input variation. This modulation technique is acted as a feedforward loop to roughly regulate the output according to the input voltage, and the feedback loop in the control system precisely regulates the output by varying the switching frequency. Simulations on a 200-kW MMR that converts 9–15 kV to 750 V are provided to verify the effectiveness of the proposed topology and control method. Experimental results on an MMR prototype are also given to demonstrate the feasibility.**

***Index Terms*—DC–DC converter, modular, multilevel, resonant, wide voltage range.**

I. Introduction

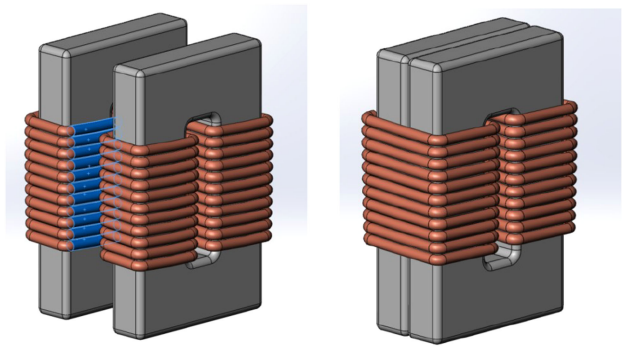
THE oceans in the world cover more than 70% of our planet and exploring the deep is critical to our ability to feed a booming human population, power our cities, and fathom the earth's climate [1], [2]. Undersea cabled observatories support a variety of science instrumentation such as conductivity/temperature/depth instrument, video, and autonomous undersea vehicles. They have become important data-acquisition platform for ocean scientific research [1], [3].

To power those science instruments in undersea cabled observatories, a step-down dc–dc converter is usually required to convert the medium dc voltage from the coast station to a low dc voltage (around 400 V) [3], [4]. The dc–dc converter can process up to 100 kW power and can be placed a few hundreds of kilometers away from the coast [3], [4]. The input voltage of the dc–dc converter may vary over a wide range due to the voltage drop on the cable resistance. Consider a 300-km cable with a parasitic resistance of 450 Ω, the voltage drop on the cable can change from 0 to 4.5 kV when the input current changes from 0 to 10 A. Therefore, it is essential that the dc–dc converter can regulate the output over a wide range of input voltage.

To support the medium voltage, input-series–output-parallel (ISOP) structure is usually used [5]. It consists of many identical dc–dc modules and their input sides are connected in series to support the high voltage and output sides are connected in parallel to support the high current [4], [6]. The dc–dc module can be a forward converter [4] or a phase shift full bridge [6]. The problem of this structure is low power density and low efficiency. In the 10-kW ISOP prototypes in both [4] and [6], there are 48 dc–dc modules and each module only outputs 208 W power; however, the transformer in each module has to withstand an insulation voltage more than 10 kV. In addition, it is hard to achieve high efficiency since forward converter is a hard switching converter and phase shift full bridge has circulating current [7].

For medium-/high-voltage applications, dc–dc converters with a single transformer can reduce the size and power losses compared to the ISOP structure. Fig. 1 can be used to explain this efficiency benefit. The transformers in Fig. 1(a) and (b) have the same magnetic cores, cables, and number of turns. The single transformer in Fig. 1(b) can output the same power as the two transformers in Fig. 1(a) with the same flux density B and cable current, but the single transformer case can save about one-fourth of the cables, hence can reduce the copper losses.

To achieve medium-to-low dc voltage conversion with a single transformer, the most straightforward way is to use the front-to-front (F2F) configuration (dc–ac–dc), and the modular multilevel converter (MMC) can be employed in the medium voltage



(a) (b)

Fig. 1. Diagram of transformers with identical magnetic cores, cables, and number of turns. (a) Two transformers. (b) Single transformer.

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side [8], [9]. When conventional pulsewidth modulation is used for F2F converter, the switching frequency is at least a few times higher than the fundamental ac frequency. The fundamental ac frequency cannot be too high due to the hard switching, and the transformer size is usually large. To circumvent this difficulty, a quasi-two-level (Q2L) modulation is proposed for the F2F converter, where the switching frequency is the same as the fundamental ac frequency and the output power is controlled by shifting the phase between primary- and secondary-side ac voltages [10]–[12]. With the Q2L modulation, the transformer size in the F2F converter can be reduced significantly, and power devices can achieve soft switching under certain conditions. The F2F converter with MMC on the medium voltage side actually operates similar to the dual active bridge (DAB), and hence can be called as modular multilevel DAB (M2DAB) [13]–[15]. The drawback of the M2DAB is high reactive current and loss of zero voltage switching (ZVS) when the voltage gain is not unity, similar to the conventional DAB converter [16], [17]. Therefore the M2DAB is not suitable for the step-down dc–dc converter in the undersea observatory where the input voltage varies over a wide range. In addition, the magnetic core of the transformer in M2DAB may have dc bias when the square voltage applied to the transformer is not symmetrical [18], [19].

Combining MMC with resonant converter opens another way to convert the medium dc to low dc voltage. A nonisolated resonant mode modular converter (RMMC) with high step-down ratio was proposed in [20]. A phase-shifted modulation is employed for the RMMC and in each resonant cycle only one of the submodules (SMs) is switching, whereas the rest of the SMs are constantly inserted into the arm. This modulation can inherently balance the SM capacitor voltages and can achieve a high step-down ratio. The problem of the RMMC is high conduction losses in the medium voltage side. With only one SM switching in each resonant cycle, the resonant tank voltage amplitude is equal to the SM capacitor voltage and is much lower than the medium dc voltage. As a result, the current stress in the medium side is high. An isolation transformer is added to alleviate this problem [21], still, the current in the isolated RMMC medium side is much higher than that of the M2DAB under the same voltage and power condition [20], [21].

This article proposes a modular multilevel resonant (MMR) dc–dc converter (see Fig. 2) and the corresponding modulation and control to achieve medium-to-low dc voltage conversion with wide input range. Derived from the MMC and *LLC* resonant dc–dc converter, the proposed MMR can easily achieve fault-tolerant operation with the modular structure and can achieve high power density with only a single medium frequency transformer. The fundamental ac frequency of the MMR is the same as the switching frequency, and the secondary rectifiers and half of the primary-side switches can achieve soft switching in the whole operating range. Compared to the RMMC [20], [21], the medium voltage side current stress of the MMR is lower. Besides, the MMR can regulate the output over a wide input voltage range with much narrower frequency range compared to conventional resonant converters. By constantly inserting certain number of SMs into the arm according to the input, the wide range of input voltage can be "folded" to a narrow range. For an

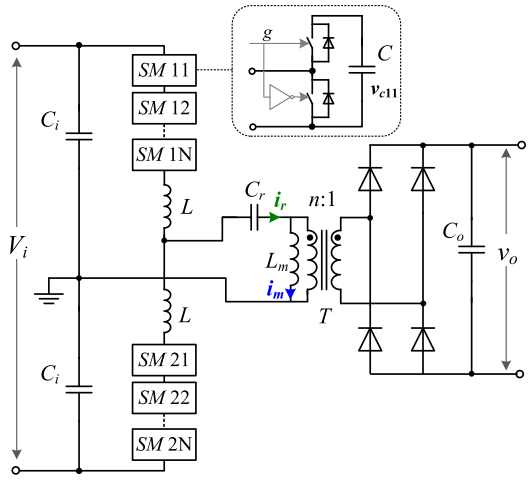

Fig. 2. Topology of the proposed MMR dc–dc converter.

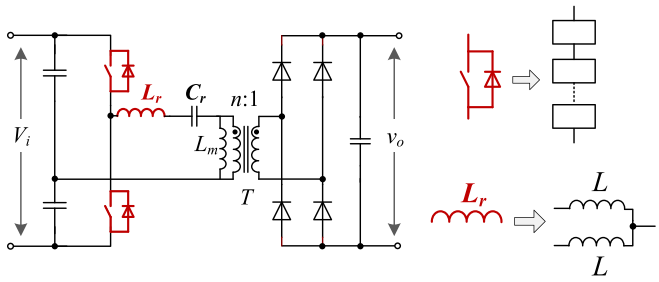

Fig. 3. Derivation of the MMR using an *LLC* converter.

MMR converting 9–15 kV to 750 V, the input voltage range is folded from 75%–125% to 94%–106%. This modulation technique is acted as a feedforward loop to roughly regulate the output according to the input voltage, and the feedback loop in the control system precisely regulates the output by varying the switching frequency. The above modulation can also reduce the required number of SMs compared to M2DAB [13], [14]. Simulations on a 200-kW MMR that converting 9–15 kV to 750 V are provided to verify the effectiveness of the proposed topology and control method. Experimental results on an MMR prototype are also given to demonstrate the feasibility.

II. MMR Topology and Modulation

As illustrated in Fig. 3, the proposed MMR converter can be derived from an *LLC* resonant converter by replacing its primary-side power device with series-connected SMs and by splitting the resonant inductor L_r into two inductors L. The series-connected SMs enable high voltage operation. The two inductors L are inserted into the arms to limit the dc loop circulating current when SMs switch in and out of the circuit. The SM capacitors almost have no influence on the resonance since its capacitance is much larger compared to the resonant capacitor C_r. The resonant tank can be treated the same as that of the conventional *LLC* converter and is only composed of L, C_r, and the magnetizing inductor L_m. The MMR inherits the desirable features of both the MMC and *LLC* such as high voltage capability, easy fault-tolerant operation, and soft switching.

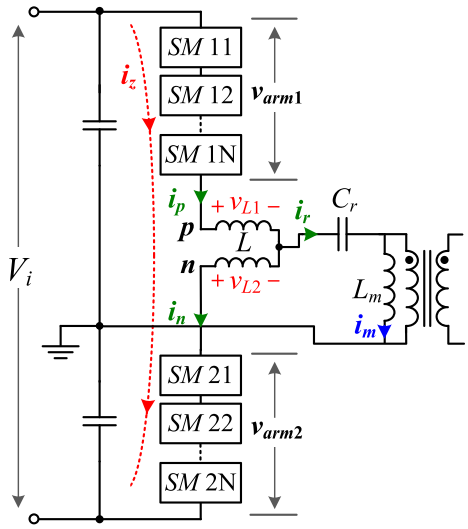

Fig. 4. Arm voltages and currents of the MMR.

A. Arm Current and Voltage

As shown in Fig. 4, the arm currents of the MMR are composed of a dc circulating current i_z, and an ac component equal to half of the resonant current i_r similar to an MMC [22], [23]; hence, arm currents i_p and i_n can be expressed as

$$\begin{cases} i_p = \dfrac{i_r}{2} + i_z \\ i_n = -\dfrac{i_r}{2} + i_z. \end{cases} \tag{1}$$

The voltage drop on the two arm inductors can be expressed as

$$v_{pn} = v_{L1} - v_{L2} = L\frac{d\,(i_p + i_n)}{dt} = 2L\frac{di_z}{dt}. \tag{2}$$

Since i_z is essentially a dc current, v_{pn} is approximately equal to 0, and the points p and n in Fig. 4 are virtually short circuited. Thus, the two arm inductors work in parallel from the perspective of the resonant tank, and the equivalent resonant inductance is

$$L_r = L/2. \tag{3}$$

Since the points p and n in Fig. 4 are virtually shorted, the input voltage V_i is equal to the sum of the arm voltages $v_{\rm arm1}$ and $v_{\rm arm2}$ (see Fig. 4)

$$V_i = v_{\rm arm1} + v_{\rm arm2} \tag{4}$$

and the voltage on the resonant tank v_p can be expressed as

$$v_p = v_{\rm arm2} - \frac{V_i}{2} = \frac{V_i}{2} - v_{\rm arm1}. \tag{5}$$

The resonant tank voltage v_p can be controlled by adjusting the arm voltages $v_{\rm arm1}$ and $v_{\rm arm2}$, which provides another degree of freedom to regulate the output voltage besides varying the switching frequency. Next, we will discuss how to adjust $v_{\rm arm1}$ and $v_{\rm arm2}$ to change v_p, and we first need to know how these arm voltages are generated.

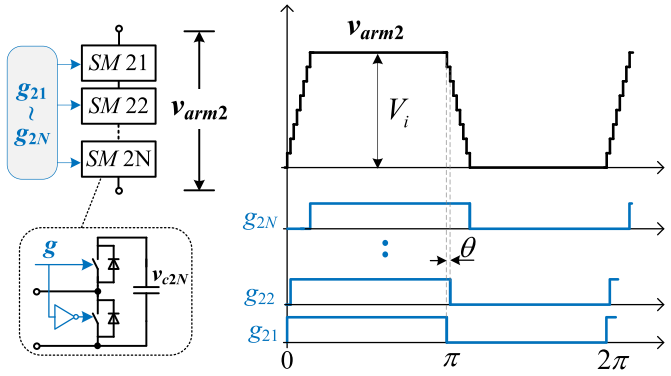

Fig. 5. Gate signals and arm voltage of the MMR.

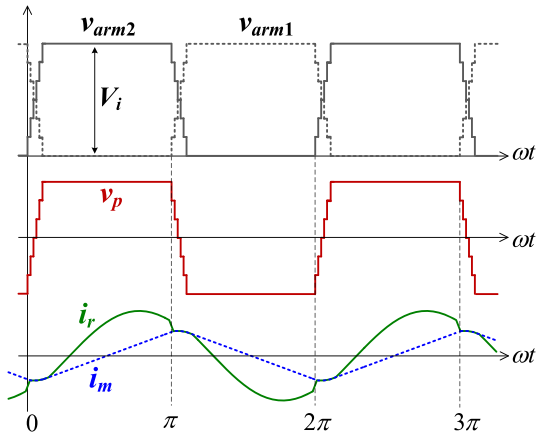

Fig. 6. Arm voltages, resonant tank voltage, resonant, and magnetizing current of the MMR.

B. Modulation

The gate signals and arm voltage of the lower arm are shown in Fig. 5. g_{21} to g_{2N} are the gate signals with 50% duty ratio, and between any two adjacent gate signals, there is a θ phase displacement. With these gate signals, the lower arm can generate a multilevel trapezoidal voltage $v_{\rm arm2}$ when the SM capacitor voltage is well balanced, and this $v_{\rm arm2}$ can be treated as a quasi-square voltage by choosing a fairly small θ.

Driving SMs in the upper arm using the gate signals complementary to those in Fig. 5, the primary side circuit can generate a multilevel trapezoidal voltage v_p as shown in Fig. 6, where v_p is the voltage applied on the resonant tank (see Fig. 4). Then, the MMR can operate similar to a conventional *LLC* converter as shown in Fig. 6, where i_r and i_m are the resonant and magnetizing currents, as indicated in Fig. 2. Nevertheless, if the output voltage of MMR is controlled only by varying the switching frequency, the voltage regulation range will still be limited just as the conventional resonant converters.

To widen the voltage range of the MMR, a modulation strategy shown in Fig. 7 that utilizing the control degree of freedom provided by the modular circuit is proposed. Different from Fig. 5, some of the gate signals in Fig. 7 are set as constantly high (g_{21} to g_{2K}), and the capacitors of these SMs are constantly inserted into the circuit. When both the upper and lower arms are

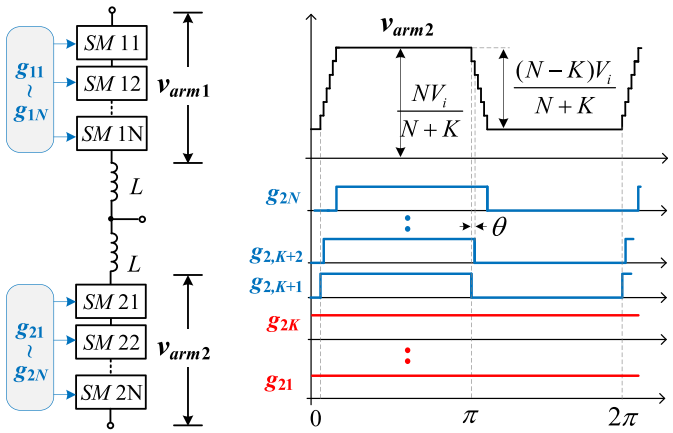

Fig. 7. Proposed modulation to change the amplitude of arm voltages.

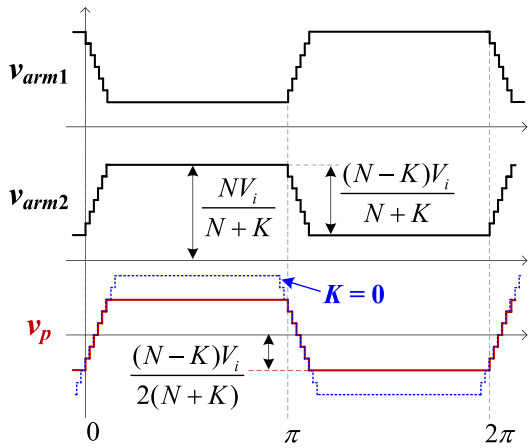

Fig. 8. Proposed modulation: the magnitude of arm voltages $v_{\rm arm1}$ and $v_{\rm arm2}$ and resonant voltage v_p with different K.

modulated in this way, there are totally $N+K$ SM capacitors inserted into the circuit at any instant

$$v_{\rm arm1}+v_{\rm arm2}=(N+K)v_c=V_i \tag{6}$$

then the nominal SM capacitor voltage becomes $v_c=V_i/(N+K)$. As a result, $v_{\rm arm2}$ has a dc offset and an ac component with amplitude: $(N-K)V_c=(N-K)V_i/(N+K)$, as illustrated in Fig. 7.

Applying the modulation scheme in Fig. 7 for both the upper and lower arms, the resonant tank voltage v_p can be controlled by adjusting the value K, as shown in Fig. 8. The amplitude of v_p can be expressed as

$$\|v_p\|=\frac{N-K}{N+K}\frac{V_i}{2}. \tag{7}$$

$\|v_p\|$ decreases with the increase of K. When $K=0$, $\|v_p\|$ has the largest amplitude.

With the control freedom introduced in Figs. 7 and 8, the voltage regulation range of the MMR can be expanded. Fig. 9 shows the MMR steady-state equivalent circuit, where v_{p1} is the fundamental component of v_p, R_e is equivalent resistance of the

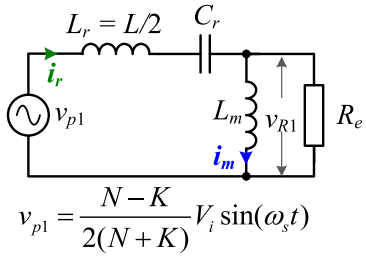

Fig. 9. Steady-state equivalent circuit of the MMR.

load, and v_{R1} is the voltage across R_e. Since

$$v_o\propto\|v_{R1}\|\propto\|v_{p1}\| \tag{8}$$

where $\|v_{R1}\|$ and $\|v_{p1}\|$ are the amplitudes of v_{R1} and v_{p1}, respectively. We can control $\|v_{p1}\|$ by adjusting K under different voltage gain conditions, such that v_o maintains at relatively constant value regardless of the wide input range, and the MMR can always operate near the resonant frequency and maintain high efficiency in the whole operating range.

Another desirable feature of the proposed modulation is the number of SMs can be reduced (hence less power devices and capacitors). With the proposed modulation in Figs. 7 and 8, when the input voltage V_i increases, the number K increases and V_i is supported by $N+K$ SMs, whereas in the conventional modulation (see Fig. 5) [13], [14], the input voltage is only supported by N SMs. Consider an MMR converting a 9–15 kV to 750 V, and a 1200-V SiC MOSFET is employed as the power devices for the primary side. The SM capacitor voltage is chosen as 750 V to allow some safety margin. The required number of SMs with different modulation are calculated as follows.

1) Conventional modulation (see Fig. 5): The number of SMs is chosen such that $V_c=750$ V when $V_i=15$ kV; therefore, the number of SM is $N=15\,000/750=20$.
2) Proposed modulation (see Figs. 7 and 8): Assume $K=4$ when $V_i=15$ kV, then $N+K=20$, the number of SM is $N=16$ in each arm and totally eight SMs can be reduced.

III. MMR Control

This section first presents a feedforward control scheme based on the proposed modulation in Figs. 8 and 9 to enable power conversion with a wide input voltage range, and then a feedforward plus feedback control scheme is proposed. The SM capacitor voltage balancing control is then presented. Finally, soft switching characteristics of the MMR are analyzed.

A. Feedforward Control

Consider an MMR converting 9–15 kV (V_i) to 750 V (v_o) with parameters listed in Table I. With conventional modulation in Fig. 5, $\|v_p\|$, the amplitude of the MMR resonant tank voltage v_p, varies between 75% and 125% when normalized to 12 kV (median voltage of V_i), as shown in Fig. 10. It is challenging to design the resonant tank with such a wide voltage range and the switching frequency has to vary over a wide range accordingly, especially under light load conditions.

TABLE I
MMR PARAMETERS FOR SIMULATION

Input voltage	V_i	$9 \sim 15$ kV
Output voltage	v_o	750 V
Rated power	P_o	200 kW
Number of SMs each arm	N	16
SM capacitance	C	20 μF
Arm inductor	L	704 μH
Resonant capacitor	C_r	180 nF
Magnetizing inductance	L_m	5 mH
Transformer turn ratio	$n:1$	6:1
Input capacitor	C_i	10 μF
Output capacitor	C_o	2 mF

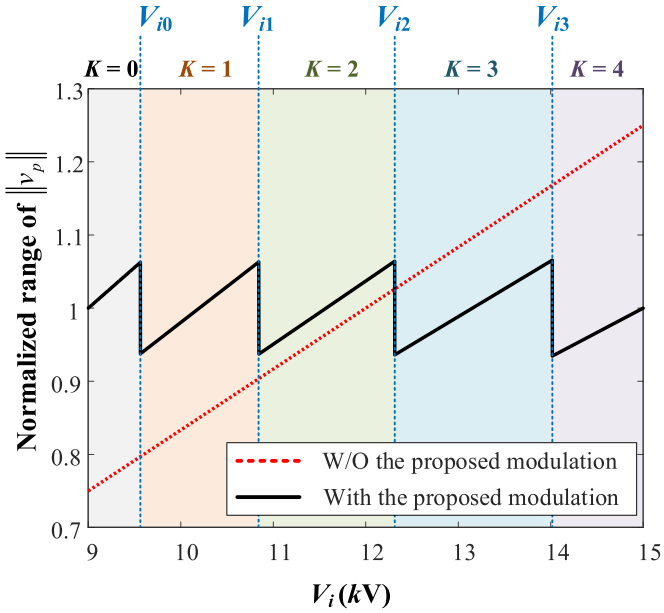

Fig. 10. Normalized variation range of the resonant tank voltage v_p.

The proposed modulation technique in Figs. 8 and 9 can regulate $\|v_p\|$ by changing K according to (7). K is adjusted such that $\|v_p\|$ does not vary with the change of input voltage V_i and maintains at a relatively constant value. With the above target, when $V_i = 9$ kV, let $K = 0$, then $\|v_p\| = 4.5$ kV and the MMR can output 750 V with parameters given in Table I. Under other values of V_i, K is chosen such that $\|v_p\|$ has the smallest variation compared to 4.5 k

$$\min \left| \frac{N-K}{N+K}\frac{V_i}{2} - 4.5 \right| \quad \text{subject to } K = 0, 1, 2, \ldots, N, \quad V_i = 9\text{–}15 \text{ (kV)}. \tag{9}$$

When V_i increases to a certain voltage V_{iK}, K will increase to $K+1$ to satisfy (9), and at the voltage V_{iK}, we must have

$$\frac{N-K}{N+K}\frac{V_{iK}}{2} - 4.5 = -\left(\frac{N-K-1}{N+K+1}\frac{V_{iK}}{2} - 4.5\right) \tag{10}$$

TABLE II
VOLTAGES THAT K CHANGES

	Voltage (kV)	K
V_{i0}	9.563	$0 \leftrightarrow 1$
V_{i1}	10.843	$1 \leftrightarrow 2$
V_{i2}	12.312	$2 \leftrightarrow 3$
V_{i3}	14.016	$3 \leftrightarrow 4$

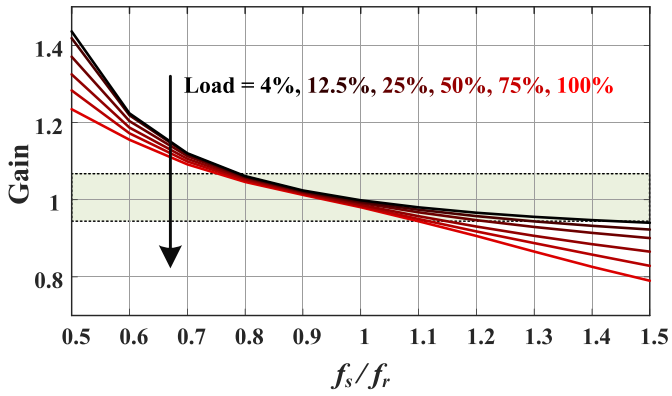

Fig. 11. Gain sweep of the MMR converter under different switching frequencies.

otherwise $|\frac{N-K}{N+K}\frac{V_i}{2} - 4.5|$ is not minimized. According to (10), we can derive

$$V_{iK} = \frac{18}{\frac{N-K}{N+K} + \frac{N-K-1}{N+K+1}}. \tag{11}$$

Substituting $K = 0, 1, 2, 3$ into (11), we can calculate the values of V_i when K should have a change and Table II lists these values. With the proposed modulation, the normalized range of $\|v_p\|$ is plotted as the black line in Fig. 10, where K changes to $K+1$ at the voltage V_{iK}. The range of $\|v_p\|$ looks like "folded" and is much narrower compared with that without the proposed modulation. In practice, when the input voltage is close to the values listed in Table II, K may frequently change due to voltage ripple or measurement noise, affecting the stability. Some hysteresis windows can be added to the threshold voltages in Table II to avoid this problem.

With the above modulation scheme, the range of v_p becomes -6% to 6% and it is easy to design the resonant tank to cover this voltage range. The design procedures are the same as that of a conventional *LLC* resonant converter [7], [24], and Table I lists the values of the resonant components. The gain of the MMR is swept using PLECS to obtain the switching frequency range and Fig. 11 shows the results, in which f_s is the switching frequency, $f_r = 1/(2\pi\sqrt{L_r C_r})$ is the resonant frequency, and the gain is $2nv_o/V_i$. The green shaded area is the $\pm 6\%$ gain variation region, and to regulate this $\pm 6\%$ error for 4%–100% load, the switching frequency changes between 15 and 29 kHz, which is a narrow range considering the input voltage changes from 9 to 15 kV. Under light load conditions, it is possible to further shrink the switching frequency range by changing K.

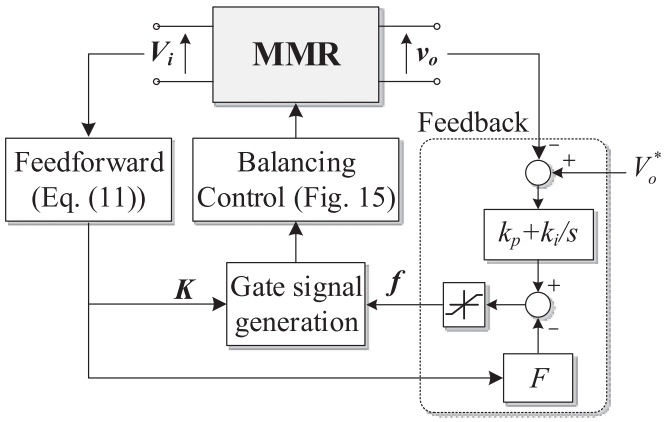

Fig. 12. Proposed feedforward plus feedback control to regulate the MMR output voltage.

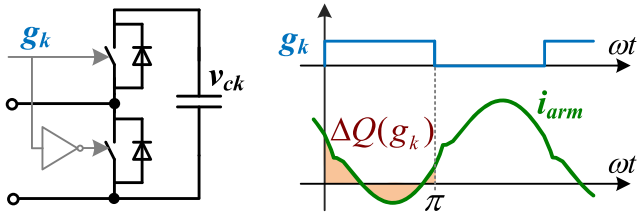

Fig. 13. When the upper device of an SM is ON, the arm current $i_{\rm arm}$ will charge/discharge the SM capacitor.

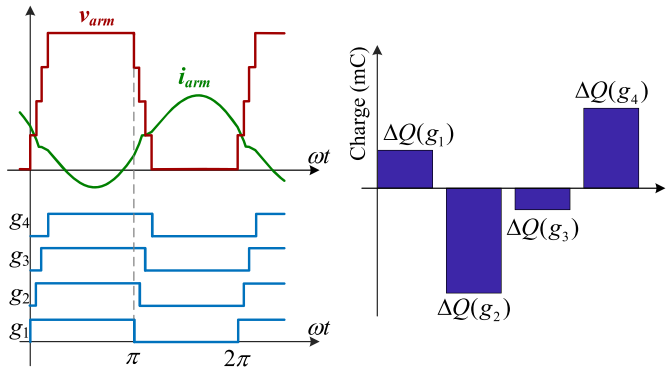

Fig. 14. $\Delta Q(g_1)$ to $\Delta Q(g_4)$ are different since each gate signal has different phase.

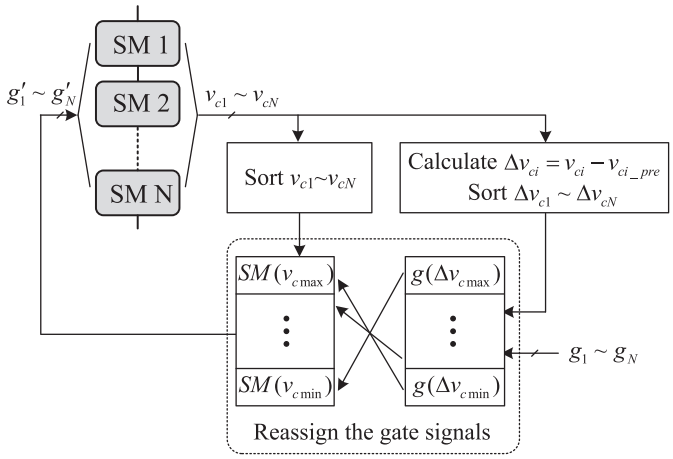

Fig. 15. Control block diagram to balance the SM capacitor voltages [14].

B. Output Voltage Control Scheme

Fig. 12 shows the block diagram of the proposed MMR output voltage control scheme. The feedforward loop samples the input voltage V_i to roughly regulate the output v_o by changing the value K according to (11), whereas the feedback loop finely control v_o by adjusting the switching frequency. In the feedback loop, v_o is compared with its reference V_o^*, and their error is sent to a proportional-integral (PI) compensator to adjust the switching frequency. The characteristics from the control variable f to v_o of the MMR are the same as that of the *LLC* converter, because their resonant tank structures are completely the same. The small-signal analysis and feedback control design can be found in [7]. The value K is also employed as a feedforward signal to the feedback loop to counterbalance the disturbance due to K changes. When K increases to $K+1$, the amplitude of the resonant tank voltage v_p will suddenly decrease according to Fig. 10, leading to the voltage sag on v_o. To suppress this sag, the switching frequency decreases by F at the moment when K changes to $K+1$ (see Fig. 12), which can increase the gain of the MMR according to Fig. 11 and hence counterbalance the voltage sag.

C. SM Capacitor Voltage Balancing

Balancing of the SM capacitor voltages is essential for stable operation, and the SM voltage balancing algorithm in [14] is used in this article. The basic idea of the balancing control can be explained using Figs. 13–15. As shown in Fig. 13, when the upper device of an SM is ON, the arm current $i_{\rm arm}$ will charge/discharge the SM capacitor and the net charge on the capacitor in a switching cycle is $\Delta Q(g_k) = \int_0^{\pi} i_{\rm arm} d(\omega t)$. Consider an arm with four SMs in Fig. 14, where g_1 to g_4 are the gate signals for SMs. These gate signals have different phases and thus $\Delta Q(g_1)$ to $\Delta Q(g_4)$ are different. These ΔQ will not change unless the operating condition changes, and the historical information ΔQ can be used to balance the SM capacitors.

The block diagram for the balancing control is illustrated in Fig. 15. Consider an arm with N SMs and $v_{c1} \sim v_{cN}$ are the SM capacitor voltages, these voltages are sorted to get the relative order the capacitor voltages. Meanwhile, the voltage variation $\Delta v_{ci} = v_{ci} - v_{ci\_\rm pre}$ is calculated for each SM, where $v_{ci\_\rm pre}$ is the capacitor voltage of the ith SM in the previous calculation cycle. The voltage variation Δv_{ci} is proportional to ΔQ_{ci} since $\Delta v_{ci} = \Delta Q_{ci}/C$. The voltage variations $\Delta v_{c1} \sim \Delta v_{cN}$ are sorted afterward. Then, we assign the gate signals with larger Δv to SMs with lower v_c and assign gate signals with smaller Δv to SMs with higher v_c. With the control method in Fig. 15, the SM capacitor voltages can be balanced under different voltage gain and load conditions [14].

D. Simulation Results

To verify the proposed topology and control, simulations of an MMR with parameters listed in Table I are conducted in PLECS.

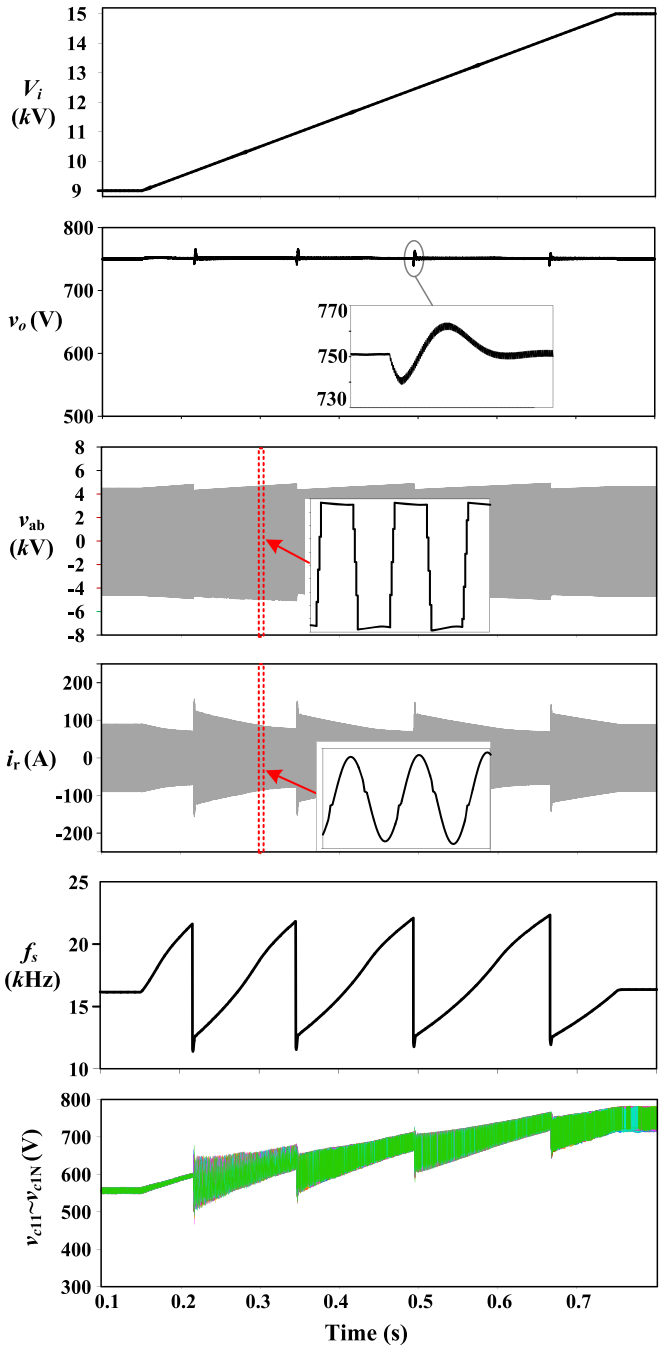

Fig. 16. Simulation results when V_i changes from 9 to 15 kV and $P_o = 200$ kW.

$k_p = 0.1$, $k_i = 500$, and $F = 10\,000$ (see Fig. 12) are used for simulations.

Fig. 16 shows simulation results when the input V_i changes from 9 to 15 kV within 0.6 s. The output power is full load $P_o = 200$ kW. With such a wide input voltage range, the output v_o is maintained at 750 V. The feedforward control roughly regulates the output voltage v_o by changing K according to (11) and Table II. The feedback control finely regulates v_o by adjusting the switching frequency according the error between v_o and its reference. The switching frequency changes between 11.5 and 22 kHz to regulate a 6% error. This frequency range

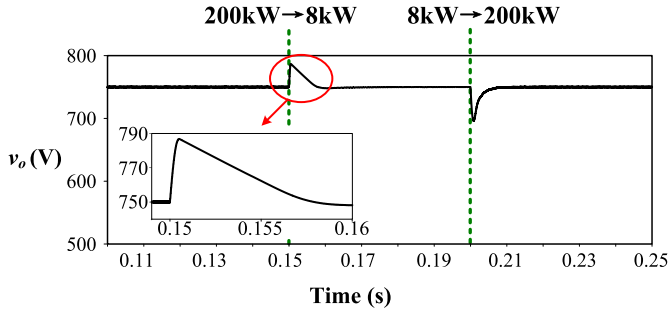

Fig. 17. Simulation results under step load change when $V_i = 9$ kV.

is wider than that in Fig. 11 because of the dynamic response. When K changes, the overshoots in v_o, v_{ab}, and i_r are small, particularly the overshoot of v_o is only 15 V. The small overshoot on v_o is achieved by decreasing f_s by 10 kHz when K changes to $K + 1$, which can counterbalance the sudden drop on v_o caused by the change of K.

Fig. 17 shows the simulation results when the load steps between full load and 4% load. The input voltage is $V_i = 9$ kV. The maximum voltage spike is less than 40 V and the recovery time is less than 10 ms. This 40-V spike is 5% of the nominal MMR output 750 V and this variation is acceptable for the undersea cabled observatory system, in which the 750 V is converted to low dc voltages to power those scientific instruments and the 5% variation has minor influence on the low dc voltages.

E. Soft Switching Analysis

With the same resonant tank and secondary-side rectifiers, the MMR and *LLC* resonant converters have the same resonant voltage/current. The diodes in the MMR rectifier can achieve zero current switching (ZCS), but the MMR primary-side switches have different soft switching characteristics compared to *LLC* because of the dc circulating current in the modular circuit. We will consider an MMR with one SM per arm (see Fig. 18) to analyze the soft switching conditions, and the calculated range is applicable to MMR with multiple SMs.

Fig. 19 shows the key waveforms of the MMR in Fig. 18. The resonant current i_r and resonant tank voltage v_p are exactly the same as that of the *LLC* converter. The arm currents i_p and i_n consist of an ac component equal to $i_r/2$ and a dc circulating current i_z, as explained in (1). Because of i_z, the currents through power devices are not symmetrical: i_{1a} and i_{2a} have a negative bias, and hence, S_{1a} and S_{2a} (the green devices in Fig. 18) can easily achieve ZVS-ON and ZCS-OFF, whereas i_{1b} and i_{2b} have a positive bias, and hence, S_{2b} and S_{1b} (the red devices in Fig. 18) have narrower soft switching ranges. Also because of i_z, the rms current through these red devices (SM lower side devices) is much higher than that of green devices (SM upper side devices).

To obtain the soft switching range, we need to calculate the current through the power devices at the switching instant. Consider the ZVS-ON range of the MMR primary-side switches. Table I lists the MMR parameters. The color surface in Fig. 20 represents the calculated currents when power devices are turned

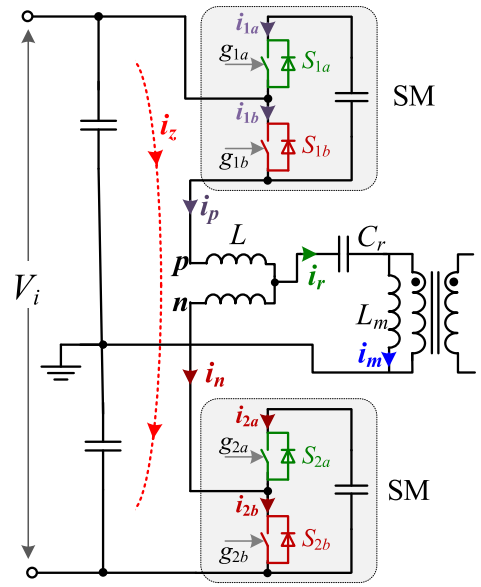

Fig. 18. MMR with one SM in each arm.

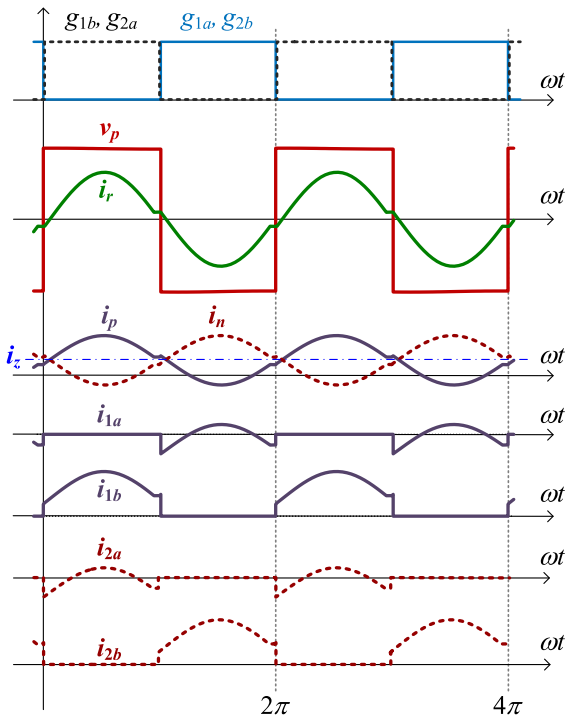

Fig. 19. Key waveforms of the MMR with one SM per arm.

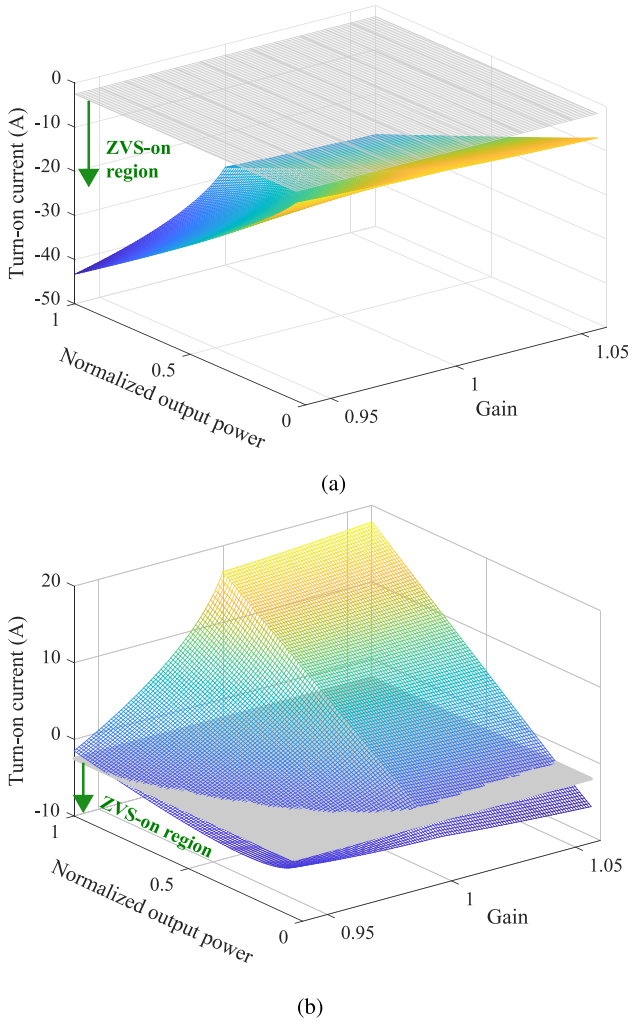

Fig. 20. ZVS-ON range of the MMR primary-side devices. (a) ZVS-ON range of S_{1a} and S_{2a}. (b) ZVS-ON range of S_{1b} and S_{2b}.

ON under different output power (normalized to 200 kW) and gain conditions. Without the dc circulating current i_z, the color surfaces of Fig. 20(a) and (b) should be the same. i_z brings a negative bias to the turn-ON currents of the SM upper devices S_{1a} and S_{2a} [see Fig. 20(a)], and a positive bias to the turn-ON currents of the SM lower devices S_{1b} and S_{2b} [see Fig. 20(b)]. The bias magnitude increases as the output power increases.

To achieve ZVS-ON, the turn-ON current of a power device should be negative to charge/discharge the parasitic capacitance. Assume SiC MOSFET Cree C3M0016120 K is employed as the power device, then at least -2.64 A is required to achieve ZVS-ON since the equivalent C_{ds} (capacitance between drain and source) from 0 to 750 V is about 1.32 nF and the dead time is assumed as 750 ns. This boundary current is plotted as the gray surface in Fig. 20. The SM upper devices S_{1a} and S_{2a} can always achieve ZVS-ON, whereas the SM lower devices S_{1b} and S_{2b} can only achieve ZVS-ON under light load conditions. Considering conduction losses, the total power losses of S_{1b} and S_{2b} (in red color) will be higher than that of S_{1a} and S_{2a} (in green color). Paralleled power semiconductor devices can be used for those SM lower devices to reduce the power losses and alleviate the thermal stress. The antiparallel diodes of the SM upper devices should have low reverse recovery to reduce the switching losses.

IV. Experimental Results

A nonisolated MMR prototype, with parameters listed in Table III, is used to demonstrate the proposed topology and control methods. A photograph of the prototype hardware is shown in Fig. 21. The SMs and passive components are put into the pluggable modules that can be easily inserted/removed from the converter cabinet. A photograph of a pluggable module with three SMs is shown in the top left of Fig. 21. Each SM has a DSP

TABLE III
MMR PARAMETERS FOR EXPERIMENTATION

Input voltage	V_i	$600 \sim 900$ V
Output voltage	v_o	250 V
Number of SMs each arm	N	15
SM capacitance	C	60 μF
SM voltage	V_c	50 μF
Arm inductor	L	1000 μH
Resonant capacitor	C_r	330 nF
Magnetizing inductance	L_m	3.3 mH
Transformer turn ratio		6:1
Input capacitor	C_i	170 μF
Output capacitor	C_o	2 mF

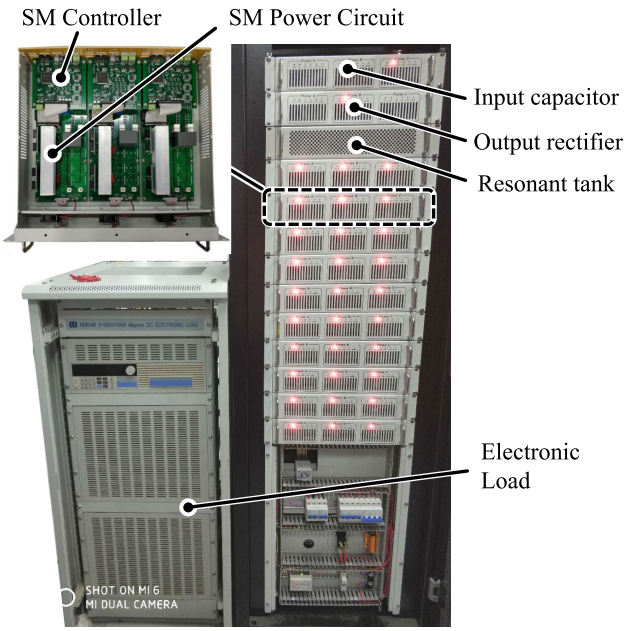

Fig. 21. Photograph of the MMR prototype.

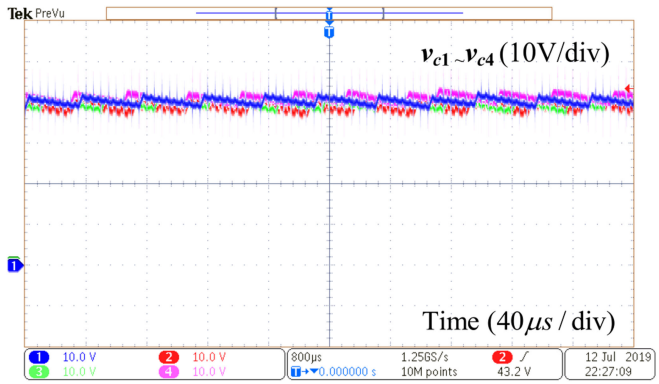

Fig. 22. Experimental waveforms: SM capacitor voltages are balanced at 40 V.

for local control and communication with central controller. The dead time of the primary-side switch is 1.5 μs.

The experimental results are shown in Figs. 22–25. Fig. 22 shows the capacitor voltages of SMs 1–4; these voltages are well balanced with the control algorithm in Fig. 15.

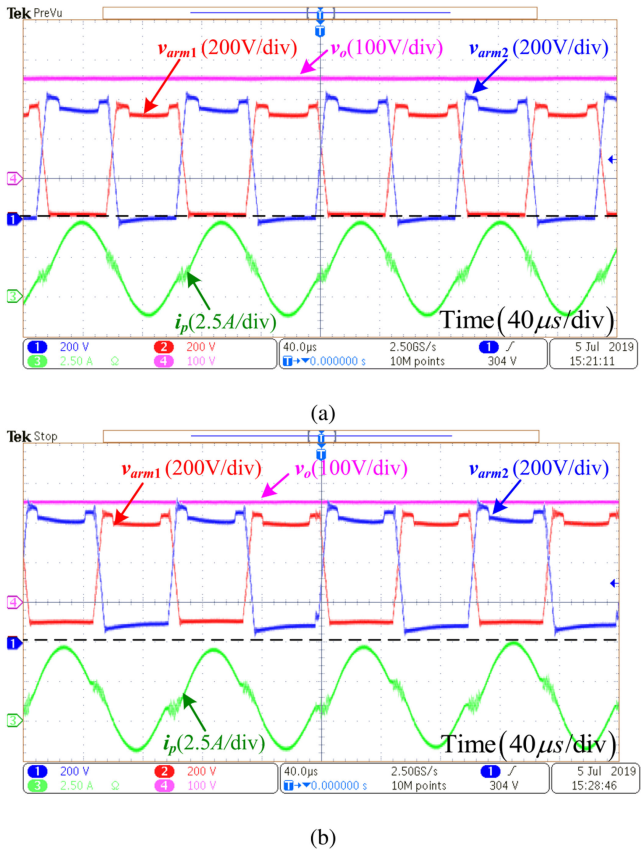

Fig. 23. Experimental waveforms with different K. (a) $K = 0$, $V_i = 700$ V. (b) $K = 1$, $V_i = 800$ V.

Fig. 23 shows the upper and lower arm voltages $v_{\rm arm1}$ and $v_{\rm arm2}$ under different K. In Fig. 23(a) where $K = 0$, all the SMs are driven by gate signals with 50% duty ratio, the minimum voltage of $v_{\rm arm1}$ or $v_{\rm arm2}$ is 0. In Fig. 23(b) where $K = 1$, one of the SMs is constantly inserted into the arm, and the minimum value of $v_{\rm arm1}$ or $v_{\rm arm2}$ is equal to the SM capacitor voltage, as explained in Figs. 5 and 8. In both the cases, the upper arm current i_p is in a sinusoidal shape and output voltage is maintained at 250 V. Note that the voltage sag in $v_{\rm arm1}$ and $v_{\rm arm2}$ is caused by the voltage drop on the power devices. Assume the equivalent resistance of an arm is $R_{\rm eq}$, the measured arm voltage is $v_{\rm arm} + i_{\rm arm}R_{\rm eq}$, thus $v_{\rm arm1}$ have a voltage sag when the upper arm current i_p becomes negative. In the prototype, the SM capacitor voltage is about 40 V and the voltage drop on the power devices is noticeable. This voltage sag will become insignificant in the practical medium-voltage applications, in which case the voltage drop on the power devices is still a few volts and is less than 0.5% of SM capacitor voltage (a few hundred volts).

Fig. 24 shows the waveforms of the output voltage v_o and upper arm current i_p under load step change, in which the input voltage is $V_i = 700$ V. When the load changes between 250 and 60 Ω, the output voltage maintains at 250 V with a maximum voltage ripple 15 V.

Fig. 25 shows the waveforms under variation of input voltage V_i. In Fig. 25(a) where V_i changes from 700 to 800 V,

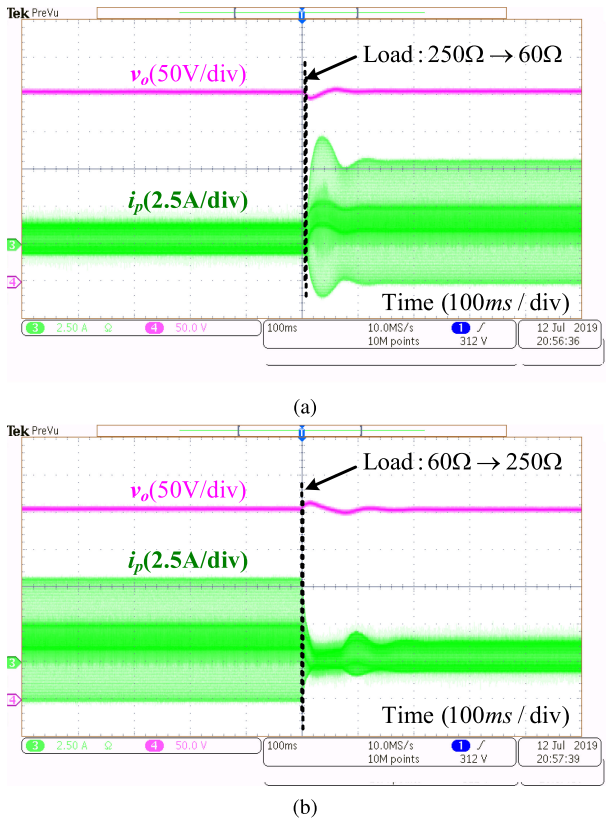

Fig. 24. Experimental waveforms with step load change. (a) 250 Ω → 60 Ω. (b) 60 Ω → 250 Ω.

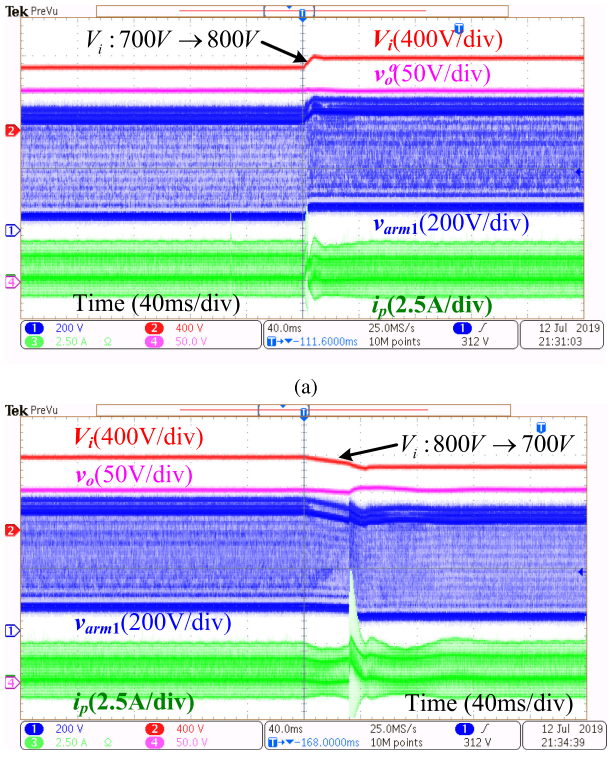

Fig. 25. Experimental waveforms with input voltage V_i change. (a) 700 V → 800 V. (b) 800 V → 700 V.

K changes from 0 to 1 such that the resonant tank voltage V_i has smallest variation. In Fig. 25(b) where V_i changes from 800 to 700 V, K changes from 1 to 0. The arm current i_p has a current spike when K changes, but the spike is small and will not affect the converter stability. This spike can be further suppressed using a coupled inductor to replace the arm inductors if needed [14]. The output voltage v_o is maintained at 250 V with insignificant voltage ripple.

V. Conclusion

An MMR dc–dc converter able to work over a wide input voltage range is proposed in this article. The proposed MMR inherits the desirable features of both the MMC and *LLC*, such as high voltage capability, easy fault-tolerant operation, and soft switching. Besides, the MMR can regulate the output voltage over a wide input voltage range with much narrower frequency range compared to conventional resonant converters. By constantly inserting certain number of SMs into the arm according to the input voltage, the wide range of input voltage can be "folded" to a narrow range. For an MMR converting 9–15 kV to 750 V, the input voltage range is folded from 75%–125% to 94%–106%. This modulation technique is acted as a feedforward loop to roughly regulate the output according to the input voltage, and the feedback loop in the control system precisely regulates the output by varying the switching frequency. The above modulation can also reduce the required number of SMs compared to M2DAB [13], [14].

Similar to other MMC-based dc–dc converter, the primary-side circuit of the MMR has a dc circulating current, and as a result, the SM upper devices can achieve ZVS-ON and ZCS-OFF, whereas ZVS-ON range of the SM lower devices is reduced. The antiparallel diodes of the SM upper devices should have low reverse recovery to reduce the switching loss. Advanced modulation may be introduced to expand ZVS-ON range of the SM lower devices. For high-power applications, multiple transformers and multiple secondary rectifiers in parallel can be used to reduce the transformer manufacturing difficulty and current stress of the rectifier diodes, similar to the converters in [25] and [26].

Simulations on a 200-kW MMR that converts 9–5 kV to 750 V are provided to verify the effectiveness of the proposed topology and control method. Experimental results on an MMR prototype are also given to demonstrate the feasibility. These results suggest MMR a promising candidate in applications with a wide input voltage range.

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