A Comprehensive Study of Common Mode Voltage Reduction and Neutral Point Potential Balance for a Back-to-Back Three-Level NPC Converter

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***Abstract*—A comprehensive study of common-mode voltage (CMV) reduction and neutral point (NP) potential balance for a back-to-back three-level NPC converter is proposed in this article. Based on phase-disposition PWM, a zero-sequence voltage (ZSV) injection method is adopted. The ZSV is divided into two parts: ZSV for CMV reduction, and ZSV for NP potential balance. The specific selection method is discussed in detail in this article. After using the proposed ZSV injection method, the CMV can be reduced to 1/6 of the dc bus voltage, and the NP potential fluctuations can also be suppressed. Simulation and experimental results verify the effectiveness of the proposed method.**

***Index Terms*—Back-to-back three-level (3L) NPC converter, common-mode voltage (CMV) reduction, neutral point (NP) potential balance, zero-sequence voltage (ZSV) injection.**

I. Introduction

With the development of variable-frequency technology, multilevel converters have been widely used in both industrial field and civil areas such as wind turbine system, mine hoist, electrified railway, and motor drive [1]–[6]. Many converters use uncontrolled diode rectifier to feed the dc voltage, which causes the harmonic pollution and low power efficiency. In this case, the back-to-back multilevel converters are researched for approximately sinusoidal wave of grid current and bidirectional power flow which can feedback the braking energy of ac motors [7], [8]. Back-to-back three-level (3L) neutral-point clamped (NPC) converter is the most used converter for medium and high-power applications for its superiority in decreased harmonics, lower EMI, and simple control [9], [10].

However, the back-to-back 3L NPC converter will generate common-mode voltage (CMV) between the input and output neutral point (NP), which affects the service life of the motor bearing [11]–[13] and the NP voltage fluctuations will cause low reliability of the converter system [14], [15]. These are two main problems that must be solved for better performance.

For the CMV reduction, a hardware solution of installing an active common-mode filter is proposed in [16], this solution can suppress CMV in a wide range of frequency, while the common-mode transformer has a big volume, increasing the complexity and cost of the converter. In [17], a PWM strategy is presented in a three-phase back-to-back two-level converter, which can eliminate the CMV to zero by synchronizing all the commutations of one converter with commutations of the other one in theory. But considering the NP potential balance control of multilevel converter, it's impossible to suppress the CMV to zero, so the strategy is infeasible for multilevel converters. Wang *et al*. [18] introduced a CMV reduction method for a back-to-back four-level hybrid-clamped converter by injecting zero-sequence voltage (ZSV). This method can suppress the CMV to 2/9 of the dc-link voltage at lowest, but the dc capacitor voltage ripples increase. If the dc capacitor voltage ripples are taken into consideration, the CMV cannot be suppressed to the lowest.

In order to balance the NP potential of NPC converters, the space vector PWM method is the most used in industrial applications [19], [20]. However, with the increase in level number, the number of vectors grows in an exponential way, which is complex to compute and analyze. Virtual-vector PWM method is also a good solution to balance the NP potential over all the modulation indexes and load power factors [21]–[23]. Nevertheless, this method causes a high number of switching transitions and complex control. To simply the control of NP potential balance for the multilevel converter, a ZSV injection method based on phase-disposition PWM (PDPWM) is proposed in [24]. The ZSV injection method can regulate the NP potential balance by modulating the NP current, which can also be used in other topologies or other PWM strategies, such as four-level hybrid-clamped converter [25] or carrier-overlapped PWM [26], [27]. So ZSV injection method is a good solution for both the CMV suppression and NP potential balance.

In this article, a novel control method of both CMV reduction and NP potential balance for a back-to-back 3L NPC converter is proposed. This method is made up of two algorithms: the CMV reduction algorithm, and the NP potential balance algorithm. This method is used for a back-to-back 3L NPC converter, as

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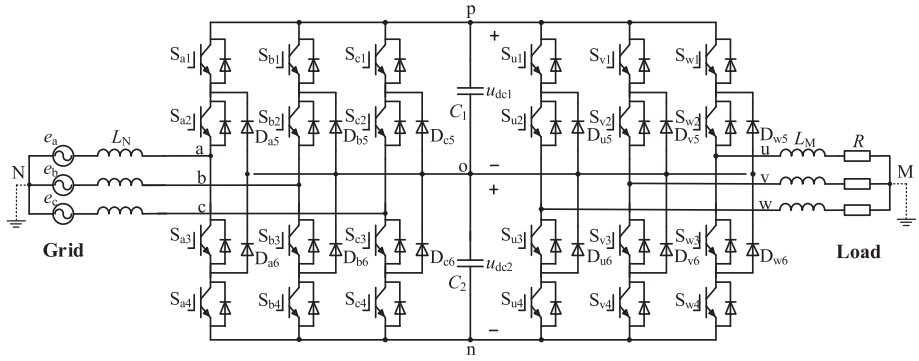

Fig. 1. Back-to-back 3L NPC converter.

shown in Fig. 1. It consists of a 3L rectifier connected with the input grid voltage source and a 3L inverter connected with the output load. Two dc bus capacitors connect the output of the 3L rectifier with the input of the 3L inverter. In this converter, N-point is the NP of the grid side, M-point is the NP of the load side, and o-point is the NP of the dc side. The following parts will introduce the back-to-back 3L NPC converter, analyze the principle of the CMV reduction and the NP potential balance control method, and verify the effectiveness of the proposed method by simulation and experimental results.

II. Analysis of CMV in the Back-to-Back 3L NPC Converter

A. Definition of CMV in the Back-to-Back 3L NPC Converter

For the 3L rectifier on the left side of Fig. 1, the CMV is the voltage between N-point and o-point, it can be expressed as

$$u_{\mathrm{No}} = (u_{\mathrm{ao}} + u_{\mathrm{bo}} + u_{\mathrm{co}})/3 \tag{1}$$

where u_{ao}, u_{bo}, and u_{co} are the instantaneous voltages between the input nodes a, b, and c of the rectifier and o-point, respectively.

For the 3L inverter on the right side of Fig. 1, the CMV is the voltage between M-point and o-point, it can be expressed as

$$u_{\mathrm{Mo}} = (u_{\mathrm{uo}} + u_{\mathrm{vo}} + u_{\mathrm{wo}})/3 \tag{2}$$

where u_{uo}, u_{vo}, and u_{wo} are the instantaneous voltages between the output nodes u, v, and w of the inverter and o-point, respectively.

For the back-to-back 3L NPC converter, the CMV is the voltage between N-point and M-point, it is equal to the difference of the rectifier CMV and the inverter CMV, meeting

$$\begin{aligned} u_{\mathrm{NM}} &= u_{\mathrm{No}} - u_{\mathrm{Mo}} \\ &= (u_{\mathrm{ao}} + u_{\mathrm{bo}} + u_{\mathrm{co}})/3 - (u_{\mathrm{uo}} + u_{\mathrm{vo}} + u_{\mathrm{wo}})/3. \end{aligned} \tag{3}$$

Define the normalized reference voltages of the rectifier side as u_{sa}, u_{sb}, and u_{sc}, they meet

$$\begin{cases} u_{\mathrm{sa}} = m_1 \sin(\omega_1 t + \theta_1) \\ u_{\mathrm{sb}} = m_1 \sin(\omega_1 t - 2\pi/3 + \theta_1) \\ u_{\mathrm{sc}} = m_1 \sin(\omega_1 t + 2\pi/3 + \theta_1) \end{cases} \tag{4}$$

where $u_{\mathrm{sa}} + u_{\mathrm{sb}} + u_{\mathrm{sc}} = 0$, m_1 is the modulation index, $m_1 \in [0, 1]$, ω_1 is the angular speed, and θ_1 is the initial phase angle. They are all the parameters of the rectifier side.

Define the normalized reference voltages of the inverter side as u_{su}, u_{sv}, and u_{sw}, they meet

$$\begin{cases} u_{\mathrm{su}} = m_2 \sin(\omega_2 t + \theta_2) \\ u_{\mathrm{sv}} = m_2 \sin(\omega_2 t - 2\pi/3 + \theta_2) \\ u_{\mathrm{sw}} = m_2 \sin(\omega_2 t + 2\pi/3 + \theta_2) \end{cases} \tag{5}$$

where $u_{\mathrm{su}} + u_{\mathrm{sv}} + u_{\mathrm{sw}} = 0$, m_2 is the modulation index, $m_2 \in [0, 1]$, ω_2 is the angular speed, and θ_2 is the initial phase angle. They are all the parameters of the inverter side.

The PDPWM method is adopted at both the rectifier side and the inverter side to control the switches on and off. In a carrier cycle, u_{max1}, u_{mid1}, and u_{min1} are defined as the maximum, median, and minimum of the reference voltages u_{sa}, u_{sb}, and u_{sc}, respectively. The sum of u_{max1}, u_{mid1}, and u_{min1} is equal to zero, so u_{max1} must be large than zero, u_{min1} must be less than zero, while u_{mid1} is not sure to be positive or negative.

To simplify the analysis, assuming that each dc capacitor voltage is E. Therefore, the output voltage u_{omax1} corresponding to u_{max1} may be E, 0, the output voltage u_{omin1} corresponding to u_{min1} may be $-E$, 0, and the output voltage u_{omid1} corresponding to u_{mid1} may be E, 0 or $-E$, 0.

Define u_{max2}, u_{mid2}, and u_{min2} as the maximum, median, and minimum of the reference voltages u_{su}, u_{sv}, and u_{sw}, respectively. The case is the same as the rectifier side. So the output voltage u_{omax2} corresponding to u_{max2} may be E, 0, the output voltage u_{omin2} corresponding to u_{min2} may be $-E$, 0, and the output voltage u_{omid2} corresponding to u_{mid2} may be E, 0 or $-E$, 0.

So formula (3) can be changed into

$$\begin{aligned} u_{\mathrm{NM}} &= (u_{\mathrm{omax1}} + u_{\mathrm{omid1}} + u_{\mathrm{omin1}})/3 \\ &\quad - (u_{\mathrm{omax2}} + u_{\mathrm{omid2}} + u_{\mathrm{omin2}})/3 \\ &= [(u_{\mathrm{omax1}} - u_{\mathrm{omax2}}) + (u_{\mathrm{omid1}} - u_{\mathrm{omid2}}) \\ &\quad + (u_{\mathrm{omin1}} - u_{\mathrm{omin2}})]/3. \end{aligned} \tag{6}$$

Therefore, the CMV of the back-to-back 3L NPC converter can be viewed as 1/3 of the sum of the output voltage difference

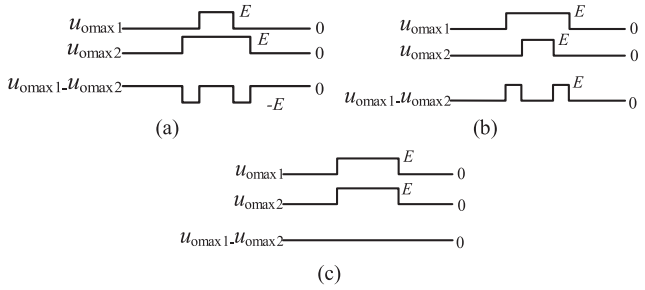

Fig. 2. Output voltages and output voltage difference of the maximum reference voltages. (a) Mode 1. (b) Mode 2. (c) Mode 3.

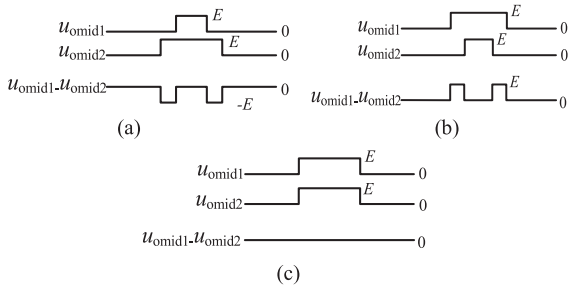

Fig. 3. Output voltages and output voltage difference of the median reference voltages (condition 1). (a) Mode 4. (b) Mode 5. (c) Mode 6.

corresponding to the maximum, median, and minimum on the rectifier side and the inverter side.

B. Analysis of CMV in Different Conditions

Define $\{u_{\max 1}\}$, $\{u_{\text{mid}1}\}$, and $\{u_{\min 1}\}$ as the duty ratio of the maximum, median, and minimum reference voltages of the rectifier side, respectively; $\{u_{\max 2}\}$, $\{u_{\text{mid}2}\}$, and $\{u_{\min 2}\}$ as the duty ratio of the maximum, median, and minimum reference voltages of the inverter side, respectively.

In a carrier cycle, the maximum reference voltages of the rectifier side and the inverter side correspond to three possible modes of the output voltages and the output voltage difference according to the duty ratio, as shown in Fig. 2. When $\{u_{\max 1}\} < \{u_{\max 2}\}$, the output voltages and the output voltage difference are denoted as mode 1, as shown in Fig. 2(a); when $\{u_{\max 1}\} > \{u_{\max 2}\}$, the output voltages and the output voltage difference are denoted as mode 2, as shown in Fig. 2(b); when $\{u_{\max 1}\} = \{u_{\max 2}\}$, the output voltages and the output voltage difference are denoted as mode 3, as shown in Fig. 2(c).

In a carrier cycle, the median reference voltages of the rectifier side and the inverter side can be divided into four conditions according to the positive and negative voltage.

1) $u_{mid1} > 0$, $u_{mid2} > 0$: The median reference voltages of the rectifier side and the inverter side correspond to three possible modes of the output voltages and the output voltage difference in the first condition according to the duty ratio. As shown in Fig. 3, they are denoted as mode 4, mode 5, and mode 6, respectively.

2) $u_{mif1} > 0, \text{u}_{\text{mid}2} < 0$: The median reference voltages of the rectifier side and the inverter side correspond to three possible modes of the output voltages and the output voltage difference in the second condition according to the duty ratio. As shown in Fig. 4, they are denoted as mode 7, mode 8, and mode 9, respectively.

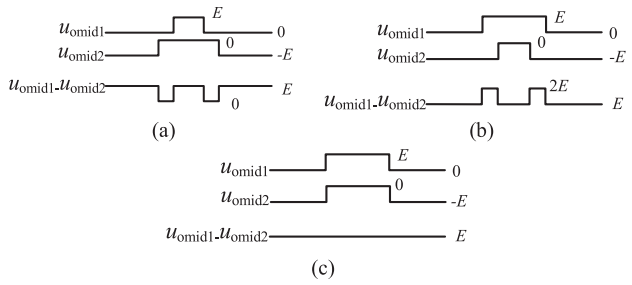

Fig. 4. Output voltages and output voltage difference of the median reference voltages (condition 2). (a) Mode 7. (b) Mode 8. (c) Mode 9.

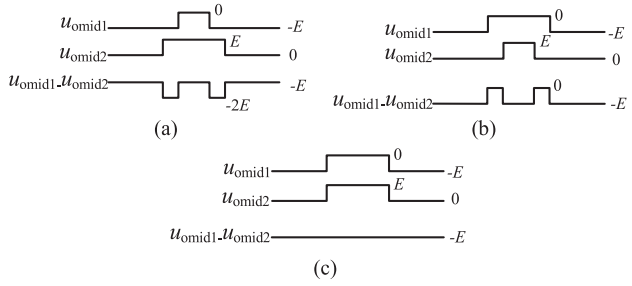

Fig. 5. Output voltages and output voltage difference of the median reference voltages (condition 3). (a) Mode 10. (b) Mode 11. (c) Mode 12.

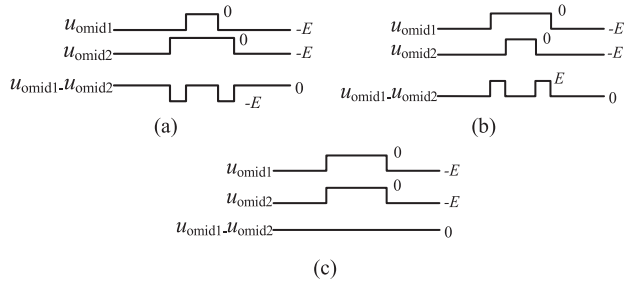

Fig. 6. Output voltages and output voltage difference of the median reference voltages (condition 4). (a) Mode 13. (b) Mode 14. (c) Mode 15.

3) $u_{mid1} < 0, \text{u}_{\text{mid}2} > 0$: The median reference voltages of the rectifier side and the inverter side correspond to three possible modes of the output voltages and the output voltage difference in the third condition according to the duty ratio. As shown in Fig. 5, they are denoted as mode 10, mode 11, and mode 12, respectively.

4) $u_{mid1} < 0, u_{mid2} < 0$: The median reference voltages of the rectifier side and the inverter side correspond to three possible modes of the output voltages and the output voltage difference in the fourth condition according to the duty ratio. As shown in Fig. 6, they are denoted as mode 13, mode 14, and mode 15, respectively.

In a carrier cycle, the minimum reference voltages of the rectifier side and the inverter side correspond to three possible

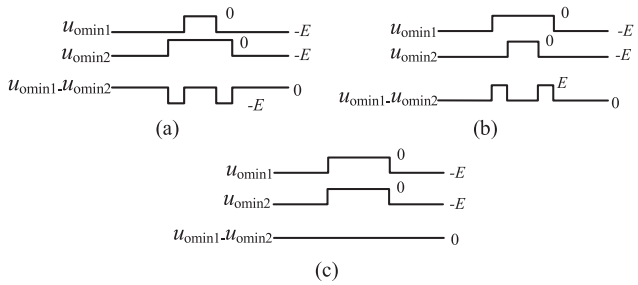

Fig. 7. Output voltages and output voltage difference of the minimum reference voltages. (a) Mode 16. (b) Mode 17. (c) Mode 18.

TABLE I
MODE GROUPS AND POSSIBLE CMVS ($u_{\mathrm{mid1}} > 0$, $u_{\mathrm{mid2}} > 0$)

Mode groups	Possible CMVs
{1, 4, 17}	**−2*E*/3**, -*E*/3, 0, *E*/3
{1, 5, 16}	**−2*E*/3**, -*E*/3, 0, *E*/3
{1, 5, 17}	−*E*/3, 0, *E*/3, **2*E*/3**
{1, 5, 18}	−*E*/3, 0, *E*/3
{1, 6, 17}	−*E*/3, 0, *E*/3
{2, 4, 16}	**−2*E*/3**, -*E*/3, 0, *E*/3
{2, 4, 17}	−*E*/3, 0, *E*/3, **2*E*/3**
{2, 4, 18}	−*E*/3, 0, *E*/3
{2, 5, 16}	−*E*/3, 0, *E*/3, **2*E*/3**
{2, 6, 16}	−*E*/3, 0, *E*/3
{3, 4, 17}	−*E*/3, 0, *E*/3
{3, 5, 16}	−*E*/3, 0, *E*/3
{3, 6, 18}	0

TABLE II
MODE GROUPS AND POSSIBLE CMVS ($u_{\mathrm{mid1}} > 0$, $u_{\mathrm{mid2}} < 0$)

Mode groups	Possible CMVs
{1, 7, 16}	**−2*E*/3**, −*E*/3, 0, *E*/3
{1, 7, 17}	−*E*/3, 0, *E*/3, **2*E*/3**
{1, 7, 18}	−*E*/3, 0, *E*/3
{2, 7, 16}	−*E*/3, 0, *E*/3, **2*E*/3**
{2, 9, 16}	0, *E*/3, **2*E*/3**
{3, 7, 16}	−*E*/3, 0, *E*/3

modes of the output voltages and the output voltage difference according to the duty ratio. As shown in Fig. 7, they are denoted as mode 16, mode 17, and mode 18, respectively.

Because the median reference voltages of the rectifier side and the inverter side have four possible combinations, the mode groups of the output voltages and the output voltage difference corresponding to the maximum, median, and minimum reference voltages can also be divided into four conditions.

When $u_{\mathrm{mid1}} > 0$, $u_{\mathrm{mid2}} > 0$, there are 13 possible mode groups by analyzing the relationship of the reference voltages. The mode groups and the possible CMVs are shown as Table I, and the amplitude of CMV is 2*E*/3.

When $u_{\mathrm{mid1}} > 0$, $u_{\mathrm{mid2}} < 0$, there are six possible mode groups by analyzing the relationship of the reference voltages. The mode groups and the possible CMVs are shown as Table II, and the amplitude of CMV is 2*E*/3.

TABLE III
MODE GROUPS AND POSSIBLE CMVS ($u_{\mathrm{mid1}} < 0$, $u_{\mathrm{mid2}} > 0$)

Mode groups	Possible CMVs
{1, 11, 17}	**−2*E*/3**, −*E*/3, 0, *E*/3
{1, 12, 17}	**−2*E*/3**, −*E*/3, 0
{2, 11, 16}	**−2*E*/3**, −*E*/3, 0, *E*/3
{2, 11, 17}	−*E*/3, 0, *E*/3, **2*E*/3**
{2, 11, 18}	-*E*/3, 0, *E*/3
{3, 11, 17}	-*E*/3, 0, *E*/3

TABLE IV
MODE GROUPS AND POSSIBLE CMVS ($u_{\mathrm{mid1}} < 0$, $u_{\mathrm{mid2}} < 0$)

Mode groups	Possible CMVs
{1, 13, 17}	**−2*E*/3**, −*E*/3, 0, *E*/3
{1, 14, 16}	**−2*E*/3**, −*E*/3, 0, *E*/3
{1, 14, 17}	−*E*/3, 0, *E*/3, **2*E*/3**
{1, 14, 18}	−*E*/3, 0, *E*/3
{1, 15, 17}	−*E*/3, 0, *E*/3
{2, 13, 16}	**−2*E*/3**, −*E*/3, 0, *E*/3
{2, 13, 17}	−*E*/3, 0, *E*/3, **2*E*/3**
{2, 13, 18}	−*E*/3, 0, *E*/3
{2, 14, 16}	−*E*/3, 0, *E*/3, **2*E*/3**
{2, 15, 16}	−*E*/3, 0, *E*/3
{3, 13, 17}	−*E*/3, 0, *E*/3
{3, 14, 16}	−*E*/3, 0, *E*/3
{3, 15, 18}	0

When $u_{\mathrm{mid1}} < 0$, $u_{\mathrm{mid2}} > 0$, there are six possible mode groups by analyzing the relationship of the reference voltages. The mode groups and the possible CMVs are shown as Table III, and the amplitude of CMV is 2*E*/3.

When $u_{\mathrm{mid1}} < 0$, $u_{\mathrm{mid2}} < 0$, there are 13 possible mode groups by analyzing the relationship of the reference voltages. The mode groups and the possible CMVs are shown as Table IV, and the amplitude of CMV is 2*E*/3.

Therefore, the CMV amplitude of back-to-back 3L NPC converter based on PDPWM method is 2*E*/3.

III. METHOD OF CMV REDUCTION AND NP POTENTIAL BALANCE

A. CMV Reduction Method

According to Figs. 2–7 and Tables I–IV, it can be found that the output voltage difference between the rectifier side and the inverter side may be $-E$, 0, E. And the output voltage difference is 0 while the reference voltage of the rectifier sides is equal to that of the inverter side. If the CMV of back-to-back 3L NPC converter is 2*E*/3, two groups output voltage difference must be E, 0, and the other is $-E$, 0, in the corresponding mode groups. Similarly, if the CMV is $-2E/3$, two groups output voltage difference must be $-E$, 0, and the other is 0, E, in the corresponding mode groups.

Based on the above analysis, a CMV suppression method using ZSV injection is proposed in this article. In a carrier cycle, when the CMV is equal to 2*E*/3, choose one of the two groups whose output voltage difference is E, 0, inject ZSV v_{zcmv} to

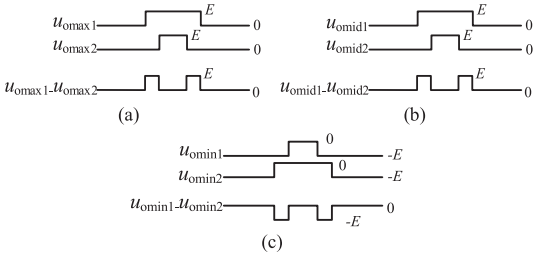

Fig. 8. Mode group {2, 5, 16}. (a) Mode 2. (b) Mode 5. (c) Mode 16.

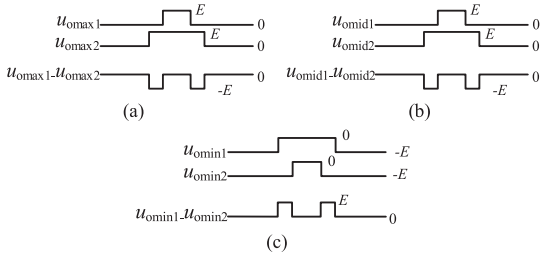

Fig. 9. Mode group {1, 4, 17}. (a) Mode 1. (b) Mode 4. (c) Mode 17.

the inverter side to make the reference voltage of the rectifier side equal to that of the inverter side, so that the output voltage difference will be 0, and the CMV amplitude will be reduced to *E*/3 after injecting ZSV. This is scheme I. When the CMV is equal to $-2E/3$, choose one of the two groups whose output voltage difference is $-E$, 0, inject ZSV $v_{\rm zcmv}$ to the inverter side to make the reference voltage of the rectifier side equal to that of the inverter side, so that the output voltage difference will be 0, and the CMV amplitude will be *E*/3 after injecting ZSV. This is scheme II.

The injected ZSV $v_{\rm zcmv}$ meets the following requirements in a carrier period.

1) After injecting ZSV, one-phase reference voltage of the rectifier side must be equal to that of the inverter side.
2) After injecting ZSV, the sign of $\{u_{\max 1}\} - \{u_{\max 2}\}$, $\{u_{\rm mid1}\} - \{u_{\rm mid2}\}$, and $\{u_{\min 1}\} - \{u_{\min 2}\}$ cannot be reversed. Otherwise, the sign of output voltage difference will be reversed, which lost the CMV reduction effect.
3) After injecting ZSV, the sign of original reference voltages cannot be changed. Otherwise, the output voltage difference may be $\pm 2E$ and the CMV cannot be suppressed.
4) After injecting ZSV, the range of reference voltages is still $[-1, 1]$, avoiding over-modulation.

Take mode group {2, 5, 16} as an example. As shown in Fig. 8, the output voltage differences of mode 2 and mode 5 are both *E*, 0, and the output voltage difference of mode 16 is –*E*, 0. Using scheme I, the ZSV $v_{\rm zcmv}$ met the previous requirements, is injected to the inverter side, it can be expressed as

$$\begin{cases} \{u_{\max 1}\} \geq \{u_{\max 2}\} + v_{\rm zcmv} \\ \{u_{\rm mid1}\} \geq \{u_{\rm mid2}\} + v_{\rm zcmv} \\ \{u_{\min 2}\} + v_{\rm zcmv} \leq 1. \end{cases} \tag{7}$$

Therefore, $v_{\rm zcmv}$ meets formula (8) in this case

$$v_{\rm zcmv} = \min\left\{\{u_{\max 1}\} - \{u_{\max 2}\}, \{u_{\rm mid1}\} - \{u_{\rm mid2}\}, 1 - \{u_{\min 2}\}\right\}. \tag{8}$$

Take mode group {1, 4, 17} as another example. As shown in Fig. 9, the output voltage differences of mode 1 and mode 4 are both –*E*, 0, and the output voltage difference of mode 17 is *E*, 0. Using scheme II, the ZSV $v_{\rm zcmv}$ met the previous requirements, is injected to the inverter side, it can be expressed as

$$\begin{cases} \{u_{\max 1}\} \leq \{u_{\max 2}\} + v_{\rm zcmv} \\ \{u_{\rm mid1}\} \leq \{u_{\rm mid2}\} + v_{\rm zcmv} \\ \{u_{\min 2}\} + v_{\rm zcmv} \geq 0. \end{cases} \tag{9}$$

Therefore, $v_{\rm zcmv}$ meets formula (10) in this case

$$v_{\rm zcmv} = \max\left\{\{u_{\max 1}\} - \{u_{\max 2}\}, \{u_{\rm mid1}\} - \{u_{\rm mid2}\}, -\{u_{\min 2}\}\right\}. \tag{10}$$

B. NP Potential Balance Method

The fluctuations of the NP potential produce the NP current, which needs to be compensated to balance the NP potential. Assuming that each dc capacitor is *C*, the voltage of the upper capacitor is $u_{\rm dc1}$, the voltage of the lower capacitor is $u_{\rm dc2}$, the NP current to be compensated is $i_{o\_\rm ref}$, and $i_{o\_\rm ref}$ is positive when it outflows from o-point. So $i_{o\_\rm ref}$ can be expressed as

$$i_{o\_\rm ref} = C\frac{\Delta u}{\Delta t} = C\frac{u_{\rm dc1} - u_{\rm dc2}}{\Delta t}. \tag{11}$$

In order to control the NP potential balancing, a ZSV injection method is introduced. Different from the previous research, this method will consider the effect of both the input currents of the rectifier side and the output currents of the inverter side on the NP average current, so as to call it an NP potential balance method based on six-phase load. The ZSV is injected to both the rectifier side and the inverter side to modulate the fluctuations of the NP potential. According to the relationship of the NP average current and the ZSV, it meets

$$i_o = -\sum_{x=a,b,c} |v_{x0} + v_z| \cdot i_x + \sum_{x=u,v,w} |v_{x0} + v_z| \cdot i_x. \tag{12}$$

The six-phase reference voltages of $u_{\rm sa}$, $u_{\rm sb}$, $u_{\rm sc}$, $u_{\rm su}$, $u_{\rm sv}$, and $u_{\rm sw}$ are sorted in order from small to large, and expressed as v_1, v_2, v_3, v_4, v_5, and v_6. The range of ZSV to be injected is

$$-1 - v_1 \leq v_z \leq 1 - v_6. \tag{13}$$

Among all the possible ZSVs, several key ZSVs are chosen to simplify the calculation. These several key ZSVs can keep one phase of the six-phase reference voltages an integer in a carrier cycle, which means one phase's switches keep unchanged in a carrier cycle, so the switching loss can be reduced in a certain degree. From the analysis, it can be known that formula (12) is a piecewise linear function, and the inflection points of the piecewise function are the key ZSVs. By analyzing, these ZSVs may be $-1 - v_1$, $-v_6$, $-v_5$, $-v_4$, $-v_3$, $-v_2$, $-v_1$, and $1 - v_6$, respectively. Fig. 10 is an example that includes all possible key ZSVs.

These possible key ZSVs are substituted into formula (12), respectively, and the corresponding NP average currents are

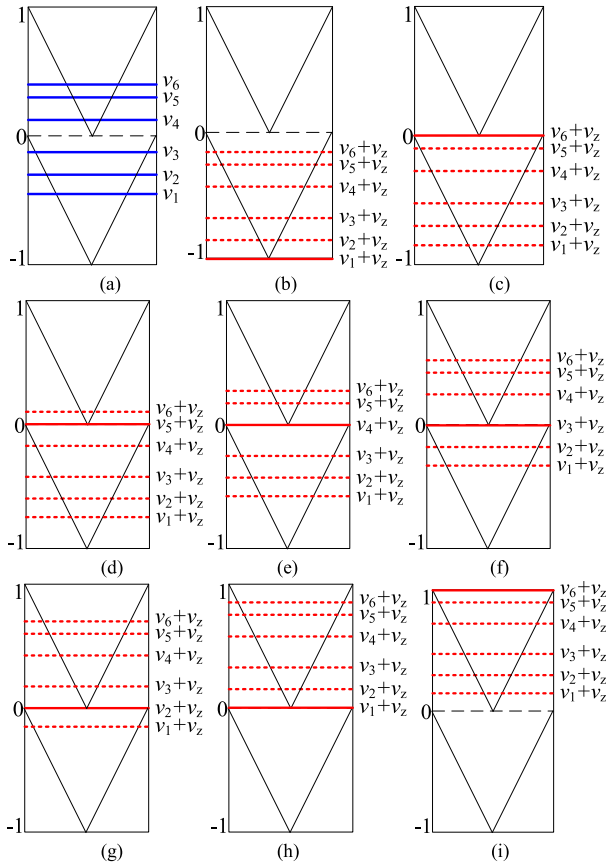

Fig. 10. Possible key ZSVs. (a) $v_z = 0$. (b) $v_z = -1 - v_1$. (c) $v_z = -v_6$. (d) $v_z = -v_5$. (e) $v_z = -v_4$. (f) $v_z = -v_3$. (g) $v_z = -v_2$. (h) $v_z = -v_1$. (i) $v_z = 1 - v_6$.

denoted as $i_{o1} - i_{o8}$, meeting

$$i_{o1} = -\sum_{x=a,b,c} |v_{x0} - 1 - v_1| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - 1 - v_1| \cdot i_x \quad (14)$$

$$i_{o2} = -\sum_{x=a,b,c} |v_{x0} - v_6| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - v_6| \cdot i_x \quad (15)$$

$$i_{o3} = -\sum_{x=a,b,c} |v_{x0} - v_5| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - v_5| \cdot i_x \quad (16)$$

$$i_{o4} = -\sum_{x=a,b,c} |v_{x0} - v_4| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - v_4| \cdot i_x \quad (17)$$

$$i_{o5} = -\sum_{x=a,b,c} |v_{x0} - v_3| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - v_3| \cdot i_x \quad (18)$$

$$i_{o6} = -\sum_{x=a,b,c} |v_{x0} - v_2| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - v_2| \cdot i_x \quad (19)$$

$$i_{o7} = -\sum_{x=a,b,c} |v_{x0} - v_1| \cdot i_x + \sum_{x=u,v,w} |v_{x0} - v_1| \cdot i_x \quad (20)$$

$$i_{o8} = -\sum_{x=a,b,c} |v_{x0} + 1 - v_6| \cdot i_x + \sum_{x=u,v,w} |v_{x0} + 1 - v_6| \cdot i_x. \quad (21)$$

TABLE V
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Value
Power	$P = 2$ kW
Grid line voltage (RMS)	$U_{ab} = 230$ V
DC bus voltage	$U_{dc} = 400$ V
Carrier frequency	$f_s = 4$ kHz
Upper and lower capacitor	$C_1 = C_2 = 2000\ \mu$F
Inductor of grid side	L_N=8mH
Inductor of load side	L_M=5mH
Load resistance	R=28Ω

In this NP potential balance method based on six-phase load, there are eight key ZSVs at most, which decreases the calculation of choosing ZSV. By calculating formula (14) to formula (21), the NP average currents i_{o1}–i_{o8} will be received. Compare i_{o1}–i_{o8} with the compensated NP current i_{o_ref}, respectively, and choose the key ZSV whose NP average current nearest to i_{o_ref} as the optimal ZSV. Then the NP potential balance will be controlled. Compared with ZSV injection at only one side, the calculation error is smaller injecting ZSV into both the rectifier side and the inverter side.

C. Total Scheme for Both CMV Reduction and NP Potential Balance

From the above analysis, both CMV reduction and NP potential balance are achieved by ZSV injection. So a ZSV injection method is proposed as a solution for both the CMV reduction and NP potential balance. The ZSV includes two parts: one part is v_{zcmv} for CMV reduction, injected to only the inverter side; the other part is v_z for NP potential balance, injected to both the rectifier side and the inverter side. And the specific selection strategies of v_{zcmv} and v_z are shown as the flow charts in Fig. 11, which have the same description as Part A and Part B, respectively. In theory, the ZSV v_{zcmv} will influence the NP current. Considering the requirements of injecting ZSV v_{zcmv} in Part A, v_{zcmv} will be limited to a small value. In addition, the NP potential balance is regulated with a closed-loop control, the small disturbance caused by v_{zcmv} can be regulated dynamically. Therefore, the NP potential can keep balance after injecting the ZSV v_z and v_{zcmv}.

Based on this scheme, the CMV amplitude of the back-to-back 3L NPC converter can be suppressed to $E/3$, reducing to 1/6 of the dc bus voltage. The NP potential fluctuations can also be suppressed in theory, which will be verified by simulation and experiments in the following analysis.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the correctness of the proposed CMV reduction and NP potential balance scheme, a 2-kW back-to-back 3L NPC converter model was designed in Simulink and a 2-kW physical platform was built in the laboratory. And the simulation and experimental parameters are shown as Table V. For the control strategy, a dual closed-loop vector control algorithm is adopted in the rectifier side, and the VVVF control algorithm

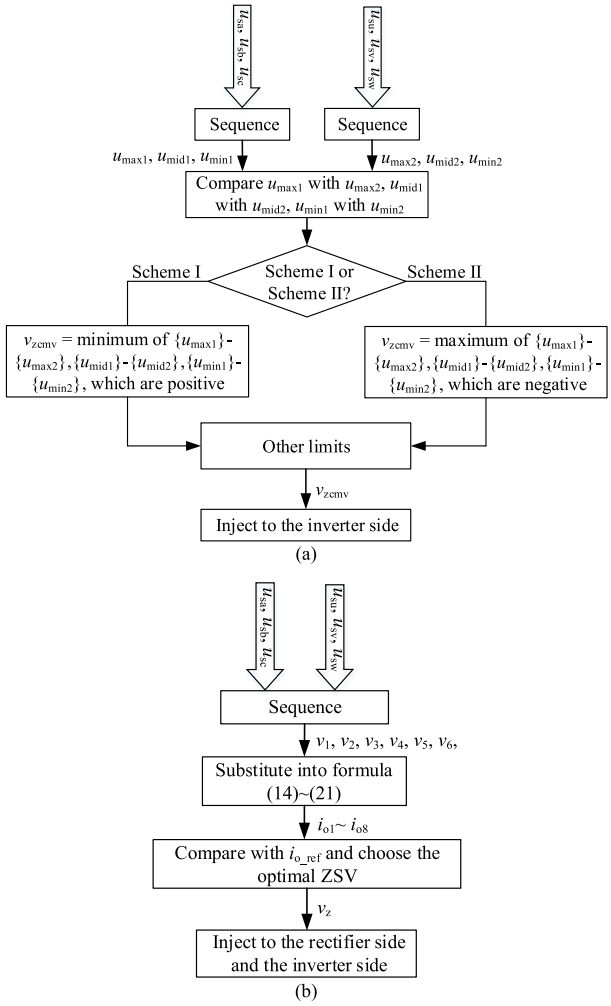

Fig. 11. Flow charts of the proposed ZSV injection strategy. (a) ZSV injection for CMV reduction. (b) ZSV injection for NP potential balance.

is used in the inverter side. Combining the proposed CMV reduction and NP potential balance method above, a diagram of the control system is given as Fig. 12.

A. Simulation Results

The following simulation results are produced at the inverter frequency of 50 Hz, that is, the modulation index of the inverter side is equal to 1.

Fig. 13 shows the three-phase currents and line voltages of the rectifier side after using the CMV reduction and NP potential balance method. The three-phase currents of the rectifier side are approximately sinusoidal, and the three-phase line voltages are five-level with the amplitude of 400 V. Similarly, in Fig. 14, the three-phase currents of the inverter side are sinusoidal with the frequency of 50 Hz, and the three-phase line voltages are five-level with the amplitude of 400 V, after using the CMV reduction and NP potential balance method.

Fig. 15 shows the voltages of the upper and lower capacitors before and after ZSV injection. From the enlarged picture, the triple frequency fluctuations are obvious before ZSV injection.

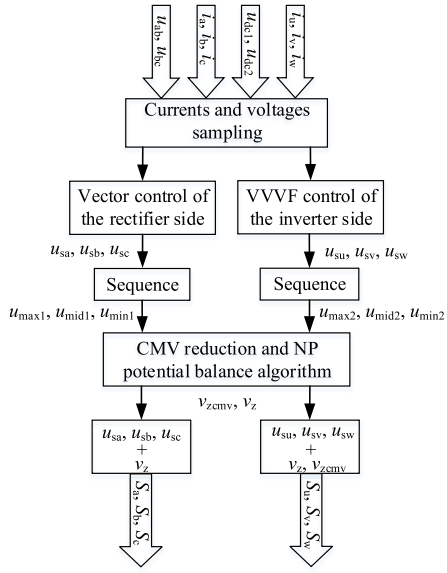

Fig. 12. Diagram of the control system of the back-to-back 3L NPC converter.

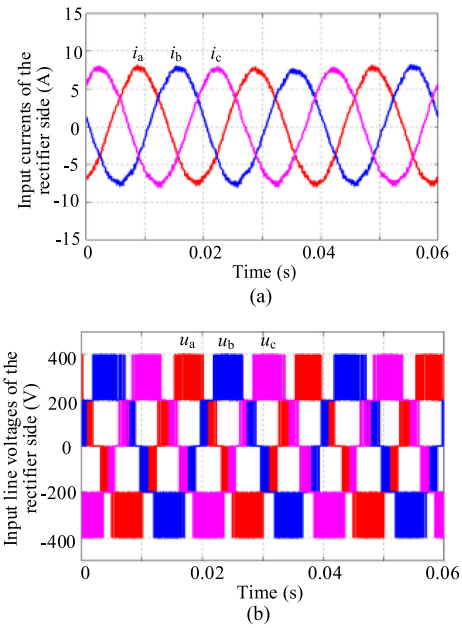

Fig. 13. Three-phase currents and line voltages of the rectifier side (simulation results). (a) Currents. (b) Line voltages.

After ZSV injection, the fluctuations are decreased, and the upper capacitor voltage is approximately equal to the lower capacitor voltage. Therefore, the suppression method of NP potential fluctuations is effective.

Fig. 16 shows the CMV of the back-to-back 3L NPC converter before and after ZSV injection. Before ZSV injection, the amplitude of CMV is about 133 V, 1/3 of the dc bus voltage. After ZSV injection, the amplitude of CMV is about 67 V, reducing half of the original CMV. So the simulation results agree well with the theoretical analysis, and the CMV reduction method is effective.

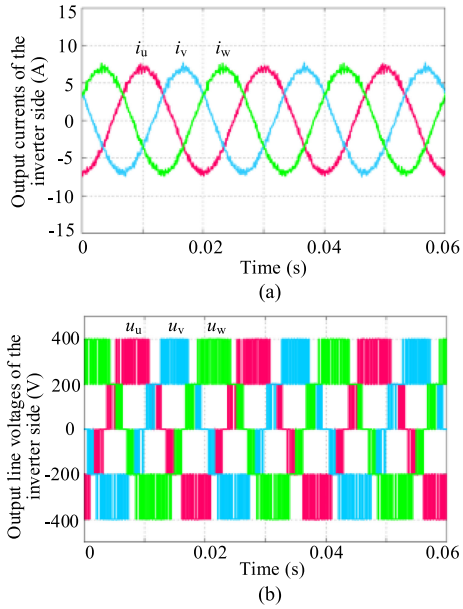

Fig. 14. Three-phase currents and line voltages of the inverter side (simulation results). (a) Currents. (b) Line voltages.

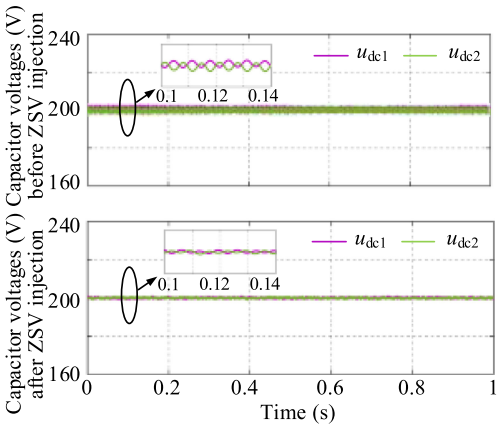

Fig. 15. Voltages of the upper and lower capacitors before and after ZSV injection (simulation results).

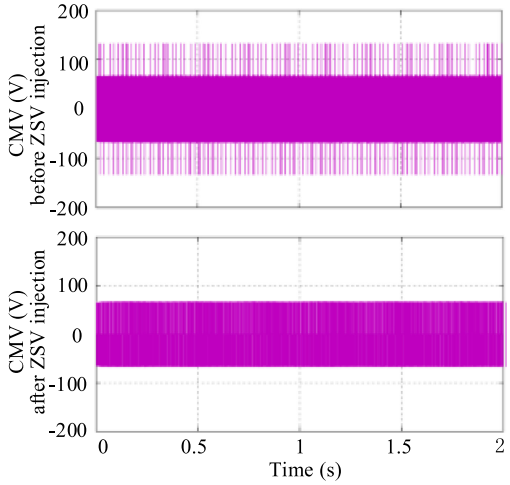

Fig. 16. CMV of back-to-back 3L NPC converter (simulation results).

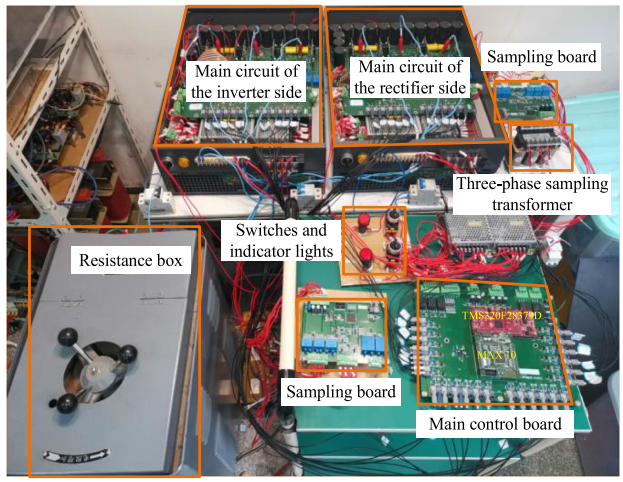

Fig. 17. Physical platform of back-to-back 3L NPC converter.

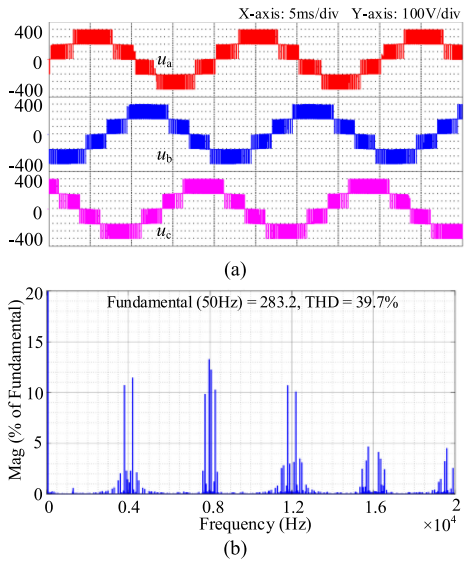

Fig. 18. Three-phase line voltages and its harmonic spectrum of the rectifier side before ZSV injection (experimental results). (a) Line voltages. (b) Harmonic spectrum.

B. Experimental Results

The physical platform of the back-to-back 3L NPC converter is shown as Fig. 17. The controller board uses a TMS320F38379D DSP chip and an Altera MAX 10 FPGA kit. This platform was run at the inverter frequency of 50, 40, 30, 20, and 10 Hz, respectively, to verify the effectiveness of the proposed CMV reduction and NP potential balance method. In other words, the modulation indexes of the inverter side are equal to 1, 0.8, 0.6, 0.4, and 0.2, respectively. Because the input grid voltages are unchanged, the modulation index of the rectifier side is equal to 0.94.

Figs. 18 and 19 show the three-phase line voltages and its harmonic spectrum of the rectifier side before and after ZSV injection, respectively. From Fig. 18(b) and Fig. 19(b), most of the harmonic components are concentrated on the carrier

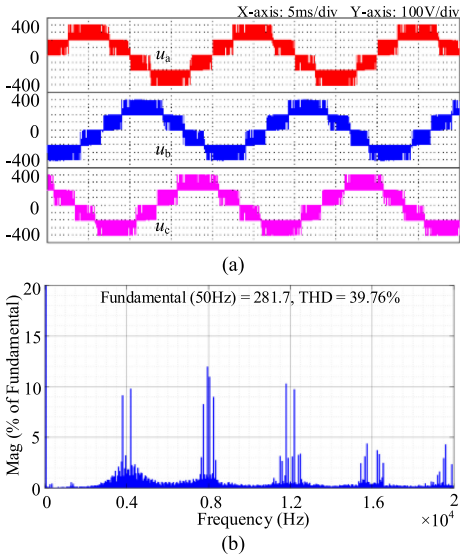

Fig. 19. Three-phase line voltages and its harmonic spectrum of the rectifier side after ZSV injection (experimental results). (a) Line voltages. (b) Harmonic spectrum.

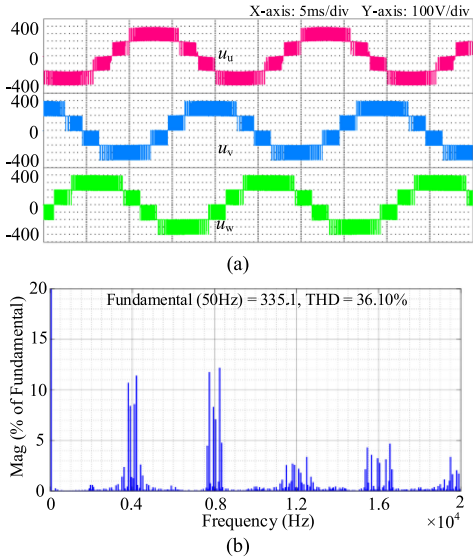

Fig. 20. Three-phase line voltages and its harmonic spectrum of the inverter side before ZSV injection (experimental results). (a) Line voltages. (b) Harmonic spectrum.

frequency and multiple carrier frequency. There is a slight change of harmonic spectrum before and after the ZSV injection for the rectifier side. Figs. 20 and 21 show the three-phase line voltages and its harmonic spectrum of the inverter side before and after ZSV injection, respectively. Compared Fig. 20(b) with Fig. 21(b), harmonics around the carrier-frequency are reduced, and the THD is somewhat improved after ZSV injection for the inverter side.

Fig. 22 shows the three-phase input currents and output currents of the back-to-back 3L NPC converter after ZSV injection. Both the input and output currents are approximately sinusoidal.

Fig. 23 shows the total dc bus voltage, the upper, and lower capacitor voltages after ZSV injection. The dc bus voltage is kept

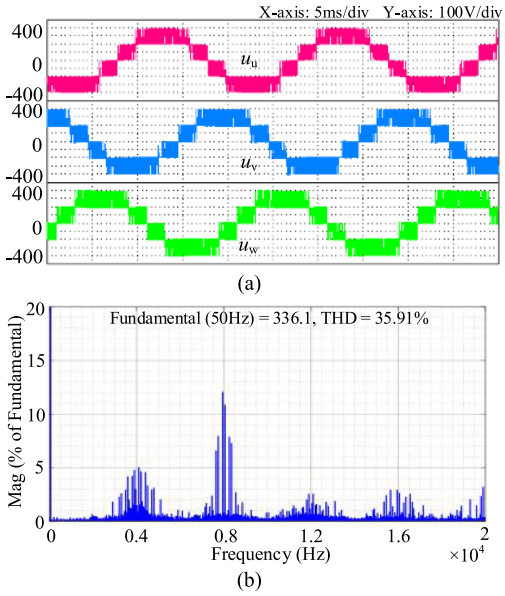

Fig. 21. Three-phase line voltages and its harmonic spectrum of the inverter side after ZSV injection (experimental results). (a) Line voltages. (b) Harmonic spectrum.

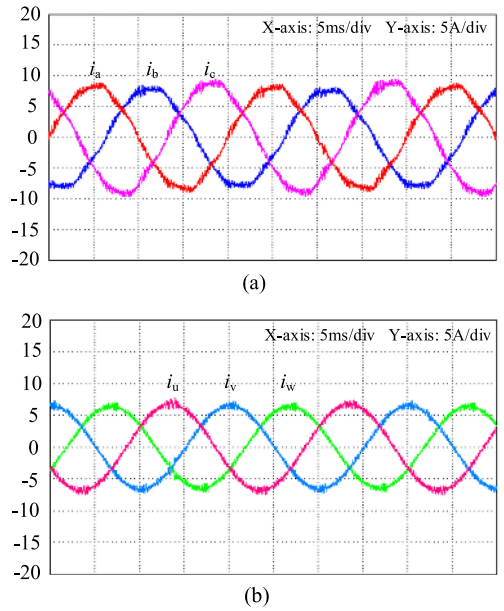

Fig. 22. Three-phase input currents and output currents of the back-to-back 3L NPC converter (experimental results). (a) Input currents. (b) Output currents.

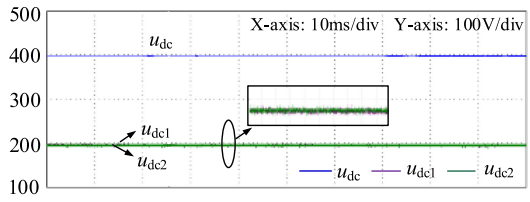

Fig. 23. Total dc bus voltage, the upper, and lower capacitors voltages after ZSV injection (experimental results).

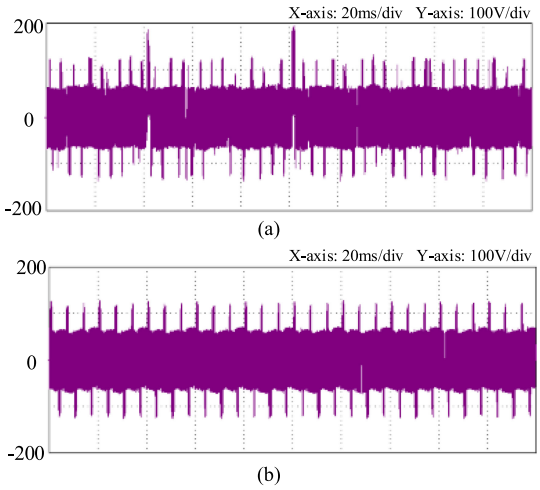

Fig. 24. CMV using NP potential balance algorithm at the rectifier side or at both the rectifier and inverter sides (experimental results). (a) At the rectifier side. (b) At both the rectifier and inverter sides.

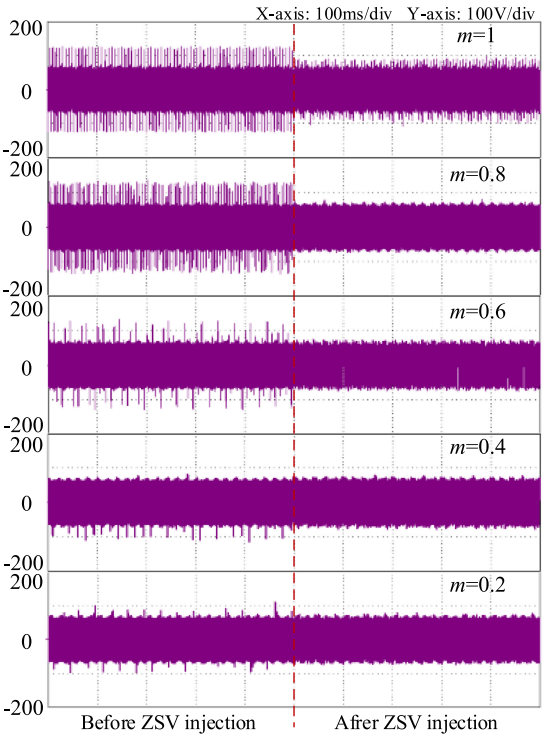

Fig. 25. CMV in different modulation indexes before and after ZSV injection (experimental results).

to 400 V, following the reference voltage. The voltages of the upper and lower capacitors are closed to 200 V, the fluctuations are small, and the waveforms are smooth after ZSV injection, which demonstrates the effectiveness of the NP potential balance method.

Fig. 24 shows the CMV of the back-to-back 3L NPC converter using the NP potential balance algorithm at only the rectifier side or at both the rectifier and inverter sides without the CMV reduction algorithm. As shown in Fig. 24, the CMV is larger using the NP potential balance algorithm at only the rectifier side, rising CMV up to 200 V, while the method using the NP potential balance algorithm at both the rectifier and inverter sides has no effect on CMV, which is beneficial to the CMV reduction further.

Fig. 25 shows the dynamic process of the CMV in different modulation indexes before and after ZSV injection. Before ZSV injection, the amplitude of CMV is about 133 V at all modulation indexes, and the proportion of 133 V amplitude is decreased with the reduction of the modulation index. After ZSV injection, the amplitude of CMV is reduced to 67 V, 1/6 of the dc bus voltage, which agrees well with the theoretical analysis and the simulation results.

V. Conclusion

A novel CMV reduction and NP potential balance method based on the PDPWM is proposed for a back-to-back 3L NPC converter in this article. Comprehensive consideration of the CMV reduction and the NP potential balance, a ZSV injection method is adopted. The ZSV is made up of two parts. For the CMV reduction, the ZSV is injected to the inverter side to make one phase reference voltage of the inverter side equal to that of the rectifier side, so that the output voltage difference of the corresponding phase is 0, and the CMV can be reduced to 1/6 of the dc bus voltage. This is the lowest CMV amplitude that can be reduced to in the back-to-back 3L NPC converter. For the NP potential balance, several key ZSVs are selected according to one phase still principle in a carrier period, which can reduce the switching loss to a certain degree. And the optimal ZSV is selected from the key ZSVs, which makes the NP average current closer to the compensated one. The optimal ZSV is injected to both the rectifier and inverter sides so that the NP potential fluctuations are decreased, and this strategy helps for the CMV reduction control. Simulation and experimental results verify the effectiveness of the proposed CMV reduction and NP potential balance method. The NP potential fluctuations are suppressed, and the CMV is reduced at all modulation indexes. This method is simple to implement. It is also beneficial for the industrial production to reduce the CMV of ac motor. It has wide application prospects.

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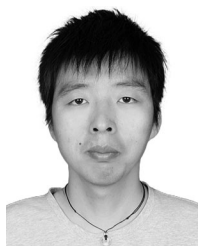

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