A Bidirectional Communicating Power Supply Circuit for Smart Gate Driver Boards

Julien Weckbrodt, Nicolas Ginot, Christophe Batard, Thanh Long Le, and Stéphane Azzopardi

***Abstract*—In power circuits, the gate drivers are required to provide an optimal and safe switching of power semiconductor devices. Nowadays, the gate driver boards include more and more features, such as short-circuit detection, soft-shutdown, temperature sensing, ON-state voltage monitoring. Research works are in progress on the integration of on-line monitoring features for a predictive maintenance. The instrumentation of the gate drive system supposes the integration of a communication system to transmit the monitoring data. In high-power designs, a galvanic isolation is mandatory on the gate driver board. The parasitic capacitance seen on the isolation barrier is critical in these designs as it can lead to the circulation of common mode currents during the switching. Adding extra optocouplers or transformers on the isolation barrier is, therefore, risky due to electromagnetic interference constraints. In this article, a new bidirectional data transmission method is proposed for gate drivers used for driving 1.2 kV silicon carbide (SiC) power metal oxide semiconductor field effect transistors (MOSFETs). The proposed method enables the energy transmission and a bidirectional data exchange on a single power supply transformer. The experimental results are provided demonstrating 1 Mb/s for TxD and 16 kb/s for RxD. The targeted application is the health monitoring of SiC power MOSFETs using the gate driver board.**

***Index Terms*—Communication channel, driver circuits, electrical isolation, isolated power supply, power system monitoring, SiC MOSFET.**

I. Introduction

SILICON carbide (SiC) power transistors, such as SiC power metal oxide semiconductor field effect transistor (MOSFETs) are more and more used in power converters. These components are excellent candidates to replace the silicon-based devices in power circuits. The interesting properties of the SiC power components enables operation at higher frequency and higher temperature. Indeed, compared with silicon devices, the fast switching of SiC MOSFET reduces considerably the switching losses. Their performances in high-temperature conditions also enable a higher power density for energy converters.

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Many research works on robustness have been carried out due the emergence of SiC-based power transistors. Recent studies have pointed out ageing indicators that could be used for health monitoring purposes, such as the evolution of the gate leakage current [1]–[5] or the on-state resistance [1]–[4], [6]. The on-line monitoring of these electrical parameters requires measurement circuits and a data exchange on the gate drive system. Implementing such methods could help to prevent damages by detecting ageing before failures. The targeted application is the predictive maintenance for high-reliability power circuits in aeronautical environments.

In power electronics designs, the gate driver provides an optimal command of the power semiconductor device using an electrically isolated circuit. For safety reasons, this electric isolation is mandatory in high-voltage circuits. As a result, the driver board is divided in two parts: the primary circuit connected to the control unit and the secondary circuit close to the power semiconductor device. The ground potential on the secondary circuit is fixed by the source/emitter voltage of the power component (Kelvin connection). The galvanic isolation represents a major constraint for the integration of intelligent circuits on the gate driver board. The new SiC power semiconductor devices can reduce the energy losses during the switching as it can switch faster than Silicon ones. As a result, electromagnetic interferences are even more restrictive in SiC gate driver designs due to high dv/dt during the turn-ON and the turn-OFF.

Although optocouplers or optical fibers can be used to transmit switching orders, transformers are always used in gate drive topologies, at least to provide supply voltage to the secondary circuit. In conventional gate driver boards, the only information transmitted across the isolation barrier is the switching orders (PWM) and an error signal, in the event of a fault detection [7]–[10]. Nowadays, new "smart gate drivers" enable data exchange by the addition of transformers dedicated to the communication across the electrical isolation [11]–[15]. Adding extra transformers across the isolation is quite cumbersome and it can lead to the circulation of parasitic common mode currents as they introduce extra capacitances between the primary and the secondary circuit. The common mode current is a well-known issue in the gate drive topologies. Several research works proposed optimizations to reduce this parasitic current [10], [11], [16]–[19]. In [16], a supply circuit is studied to reduce the coupling capacitance using a coupled filter inductor on the power circuit. The cascaded gate driver supply architectures were analyzed in [18] and [19]. Architectures were proposed in which the power supply circuits are pooled in order to reduce

the resulting common mode current under very high dv/dt. This solution treats the problem of EMI interference at the converter level considering several power transistors. As explained in [16]–[19], the electromagnetic perturbations are due to the high dv/dt applied between the primary and the secondary ground potentials during the switching of the power device.

The interest of communication on power circuitry is not new, and many works have been carried out in the field of power-line communication [20]–[22]. However, such methods of communication are not applicable for highly constrained isolated designs confronted to high dv/dt due to the proximity of the switching cells. In this context, the addition of communication features within the gate driver board with no significant impact on the common mode current represents a real challenge. Yang *et al.* [23] reported an isolated full-bridge dc-dc converter with a 1 MHz bidirectional communication channel. Unfortunately, no test was performed to check the dv/dt immunity since the operating principle and the targeted application are different from the presented method.

In this article, power supply structures based on the dc-dc push-pull operating principle are described in the following section. A method for DATA exchange using the power supply circuit is proposed in Section III. The operating principle and simulations using SPICE models are detailed. The experimental setup and waveforms are then provided in order to check the feasibility of the proposed solution. Finally, the designed circuit is confronted with high dv/dt to test the communication system in a severe environment. Experimental waveforms corresponding to a 400 V/200 A switching in a dc-dc Buck converter are also provided.

II. Conventional Power Supply Topologies Used in Gate Driver Boards

In the case of gate drivers used to drive Insulated gate bipolar transistors (IGBTs), a symmetrical supply voltage is often required (+15 V/–15 V). Since, the new SiC power MOSFETs generally require a +20 V/–5 V gate-source voltage for the optimal switching, a 25 V power supply voltage is required for driving such components. There are two main solutions for providing the supply voltage: a bootstrap circuit or an isolated dc/dc converter. Power supply circuit based on bootstrap circuit is generally chosen in the low-cost or low-voltage applications. In most cases, the isolated dc/dc converters are preferred, as an additional isolation is often required between the high-side (HS) transistor and low-side (LS) transistor in a half-bridge configuration. The isolated dc/dc converters used in gate drivers are generally realized by a Push–Pull converter or sometimes by a Flyback topology [7], [10], [24], [25]. The gate drivers using an optical power transfer have also been studied [26], [27]. Although these methods provide an optimal common-mode rejection, the low efficiency of the photoelectric transducers makes them inadequate for power modules command (power consumption >1 W). In this article, only the Push–Pull dc/dc converters used as a power supply circuit in driver boards will be considered.

The classical structure of Push–Pull converters is shown in Fig. 1. The transistors at primary side are alternately switched

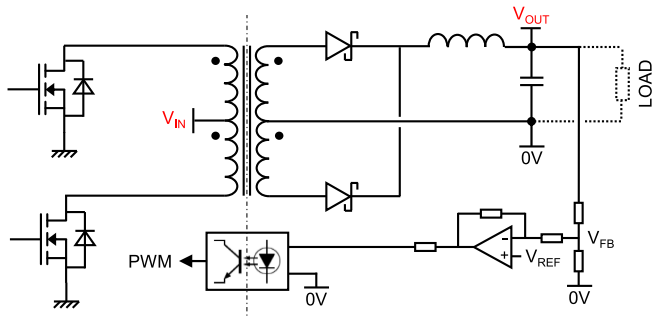

Fig. 1. Isolated Push-Pull dc-dc converter with regulation loop.

ON and OFF, a short deadtime is observed in order to avoid short circuits. The particularity of the Push–Pull converter is that the current is drawn from the line during both halves of the switching cycle. The stability of the output voltage is typically ensured by a feedback using an optocoupler. However, as explained before, the addition of elements over the isolation barrier is problematic in the gate drive boards. Consequently, open-loop strucutres are always preferred for power supplies in the gate drivers boards. The power consumption in gate driver boards is relatively low (<10 W) in comparison with the driven power circuit (several kW). In addition, this low-energy transfer allows circuit simplifications, as efficiency is not a critical parameter in these designs. In Fig. 2, a state-of-the-art of power supply circuits used in gate driver boards is presented. These low-power dc/dc converters in open-loop configuration are derived from the Push–Pull converter topology. The main characteristics of the driver boards mentioned in Fig. 2 are described in Table I. In the rest of the article, the circuit presented in Fig. 2(d) was chosen for demonstrating the communication principle. In this circuit, a square signal with fixed duty cycle is used to apply ±15 V on the primary windings. The secondary voltage V_{SEC} periodically varies from +30 V to −30 V. On the secondary side, the output voltage V_{OUT} corresponds to the double of the input voltage (transformer turns ratio 2:1) reduced by the diodes voltage drop.

III. Proposed Structure for Data Exchange Using the Isolated Power Supply Circuit

A. Operating Principle

Since the addition of extra transformers or optocouplers decreases the quality of the isolation barrier, the method proposed in the present article enables energy transfer and DATA exchange on the same transformer. As explained in Fig. 3, the isolated power supply circuit is used as a communication channel between the primary circuit and the secondary circuit. The operation can be divided in two steps: phase A and phase B.

During the first period of time T_A, the TxD signal is transmitted using a Manchester code applied to the command signal *Cmd* instead of the square signal described in Section II. The decoding of this signal can be realized at the secondary side using a XOR logic gate. During this period, the energy and the TxD signal are both transmitted through the transformer. An RC-series snubber circuit was implemented in order to optimize

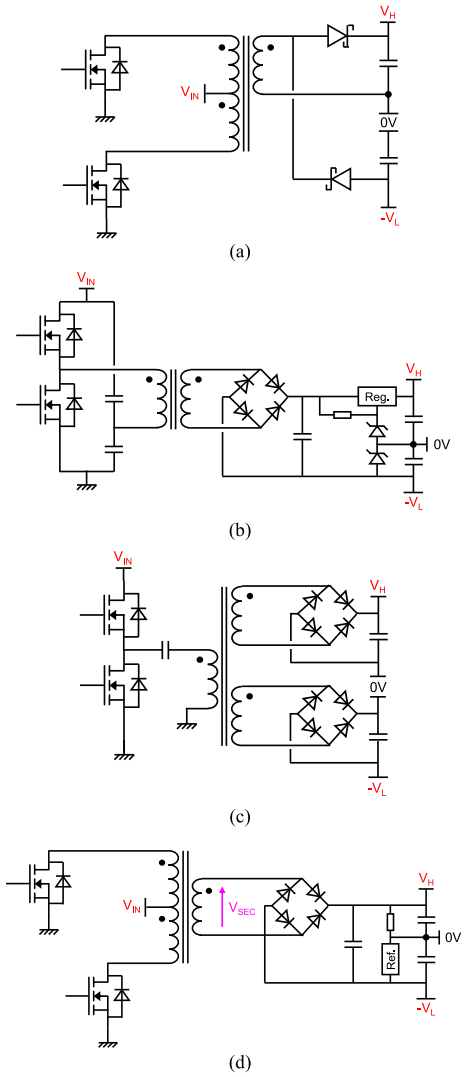

Fig. 2. Open loop Push-Pull converters with fixed duty cycle—State of the art on the power supply circuits in commercially available gate driver boards. (a) Infineon 2ED300C17. (b) Semikron SkyperPro32. (c) Cree PT62SCMD12. (d) Power Integration 2SC0650.

TABLE I
STATE-OF-THE-ART ON GATE DRIVER BOARDS

Fig.	Driver board reference	Supply circuit topology	Output power	Total parasitic capacitance
2 (a)	2ED300C17	Open loop push-pull	4 W	18 pF
2 (b)	SkyperPro32	Open loop push-pull	1.1 W	12 pF
2 (c)	PT62SCMD12	Open loop push-pull	3.5 W	-
2 (d)	2SC0650	Open loop push-pull	6 W	28 pF
-	CGD15HB6LP	Flyback circuit	-	17 pF
4	This work	Open loop push-pull	4 W	13 pF*

*8pF for the power supply and 5pF for the pulse transformer (@1MHz).

the switching of the transistors Q_1 and Q_3. Due to the Manchester coding, the operating frequency of the proposed dc/dc converter is not fixed. The frequency spectrum is spread between 500 kHz and 1 MHz.

During the phase B, the energy transfer through the transformer is stopped during a predetermined time (here $T_B =$ 11 μs). At this moment, the transformer is demagnetized by switching OFF the transistors Q_1 and Q_3 at the same time. Oscillations may occur during the demagnetizing process. These oscillations can be reduced by the addition of resistive loads connected to the primary windings, as shown in Fig. 5. These loads are disabled during the phase A (signal *En*). They also help to transmit pulses from the secondary winding to the primary ones. The transformer is then available for data transmission from the secondary side to the primary side (RxD). At this moment, the power supply transformer operates as a pulse transformer: a positive pulse corresponds to a high logic level request and a negative pulse corresponds to a low logic level request. The typical signals are described in Fig. 4. As shown in Fig. 6(b), the RxD pulses are generated by the transistors Q_5 to Q_8, which were added on the diode bridge circuit (phase B). The transistors Q_5 and Q_6 are P-channel MOSFETs so their commands require level shifter circuits. An example of level shifter topology is presented in Fig. 6(b).

Concerning the timing constraints, the pulses width was fixed at $t_{\text{pulse}} = 200$ ns considering the supply transformer design. A

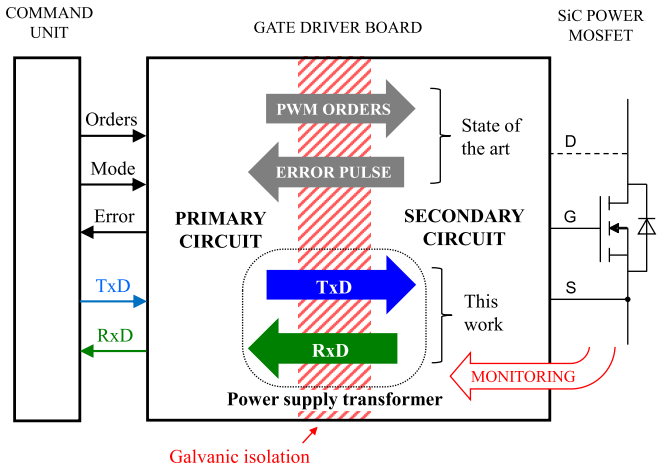

Fig. 3. Proposed strategy for online monitoring using a smart driver board.

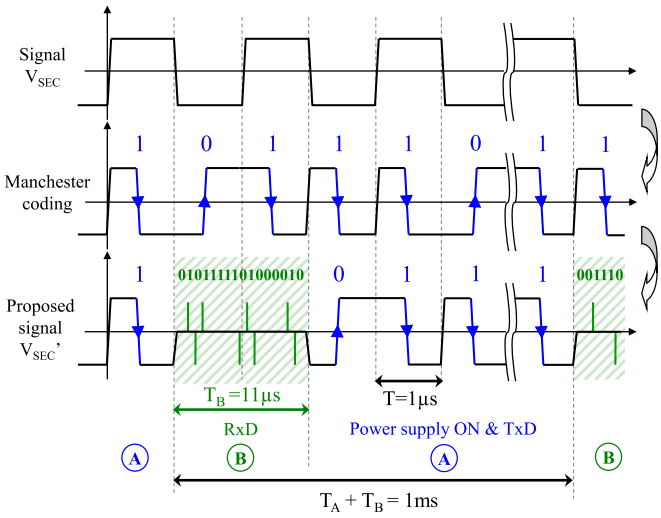

Fig. 4. Proposed principle based on the topology presented in Fig. 2(d).

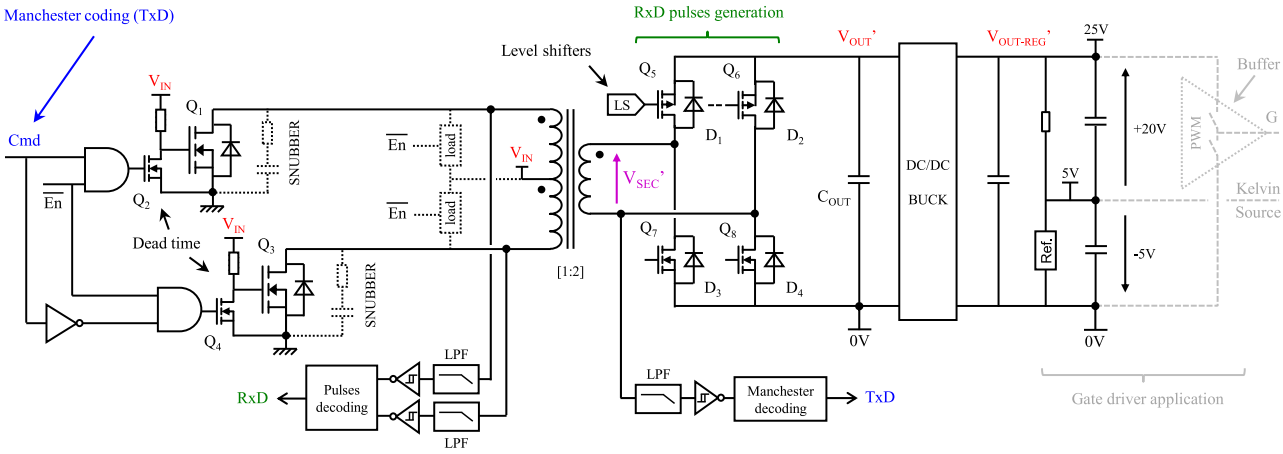

Fig. 5. Proposed communicating power supply circuit for gate driver application.

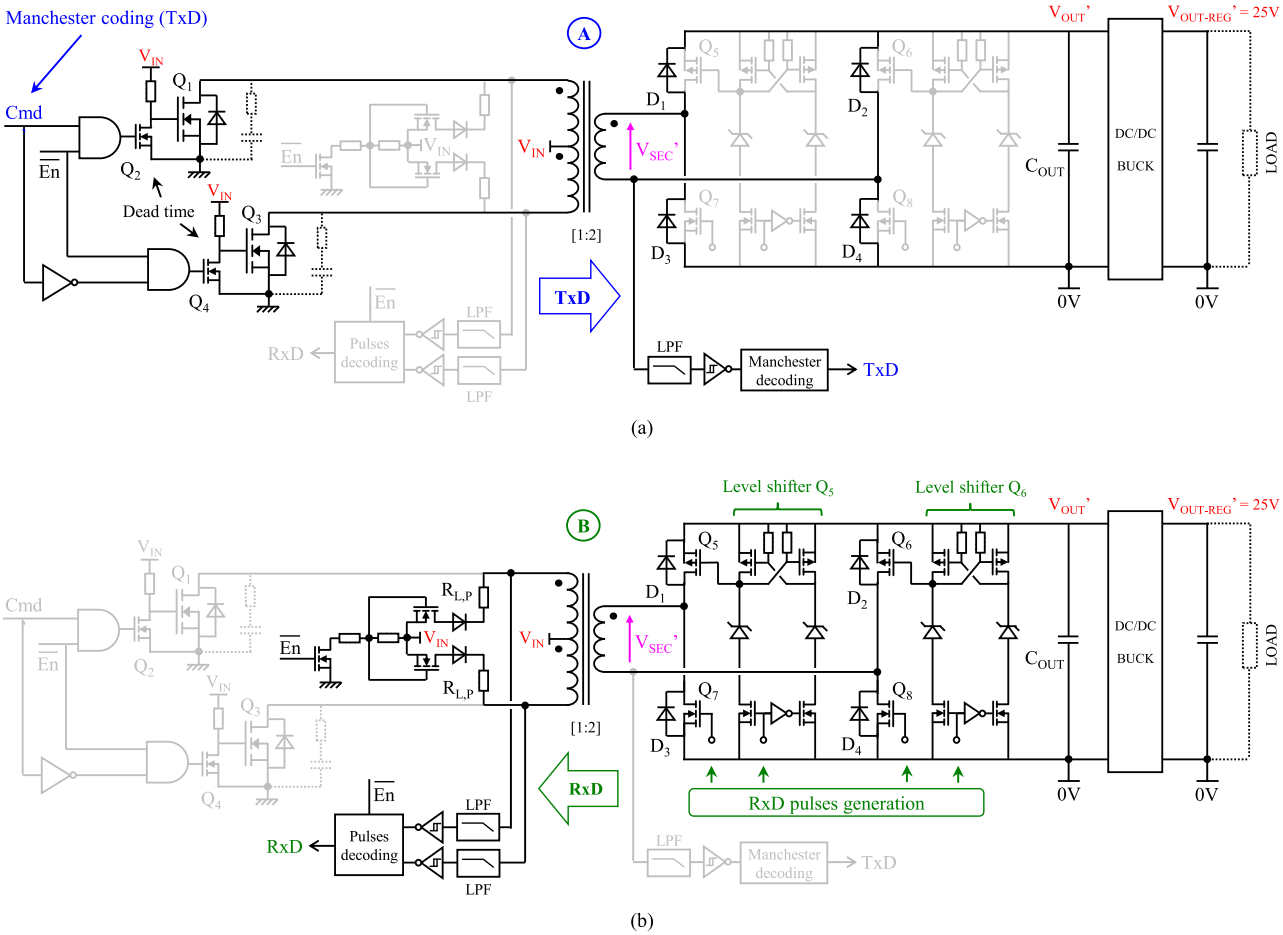

Fig. 6. Proposed communicating power supply circuit: (a) phase A, and (b) phase B.

bit time of $t_{\text{bit}} = 500$ ns was, therefore, implemented for RxD DATA in order to preserve the integrity of the pulses. Based on simulations, a 2 μs timeout was implemented in order to avoid transmission errors before the beginning of the RxD pulses generation. An additional timeout of 1 μs was observed at the end of the phase B in order to disconnect the primary load before the starting of the power converter. The cycle (A+B) is then repeated every $T_A + T_B = 1$ ms in our example. Regarding the timing constraints presented in Fig. 4, a bit rate of maximum 1 Mb/s for TxD and 16 kb/s for RxD can be achieved. Indeed, the Manchester code was designed to transmit 1 bit/μs, which correspond to a theoretical bit rate of 1 Mb/s when $T_B << T_A$. The RxD bit rate is dependent on the T_B value, as described in Fig. 9. In the case of $T_B = 11\,\mu$s, the RxD bit rate is 16

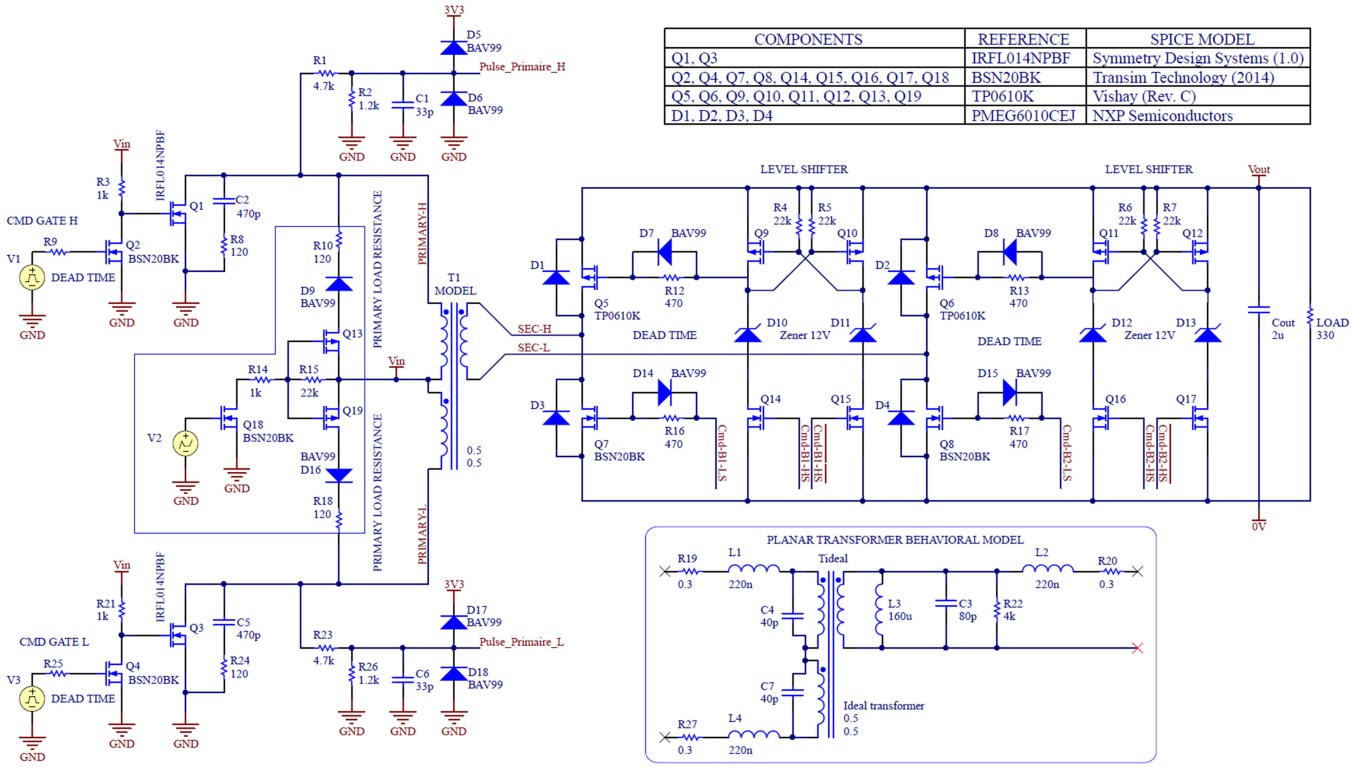

Fig. 7. Simulated circuit using Altium Designer.

kbit/s corresponding to 16 bits/cycle with a $2 + 1$ μs timeout between each phase. The health monitoring is a long process, so monitoring data does not require a high-speed transmission as measurements are not performed at every cycle.

The proposed method supposes the integration of programmable circuits on the gate driver, such as FPGA circuits for data management. Considering the timing constraints, a minimal clock frequency of 10 MHz is required for FPGA implementation. A universal asynchronous receiver transmitter (UART) protocol should be implemented for complex DATA exchange between the primary circuit and the secondary circuit of the gate driver.

B. Simulation Using SPICE Models

The circuit presented in Fig. 7 was simulated using SPICE models for active components and a transformer behavioral model. The references of the components used and the associated SPICE models are given in the table presented in Fig. 7. The supply transformer was realized by a planar transformer integrated in a six-layered board.

The simulations presented in Fig. 8 suggest an extra consumption due to the RxD pulses during the demagnetizing period. This effect is due to the ± 15 V applied on the primary load resistances. The energy consumed by a single pulse $E_{1\ \mathrm{pulse}}$ can be calculated using

$$E_{1\ \mathrm{pulse}} = \frac{{V_{\mathrm{IN}}}^2}{R_{L,\ P}} \cdot t_{\mathrm{pulse}} \tag{1}$$

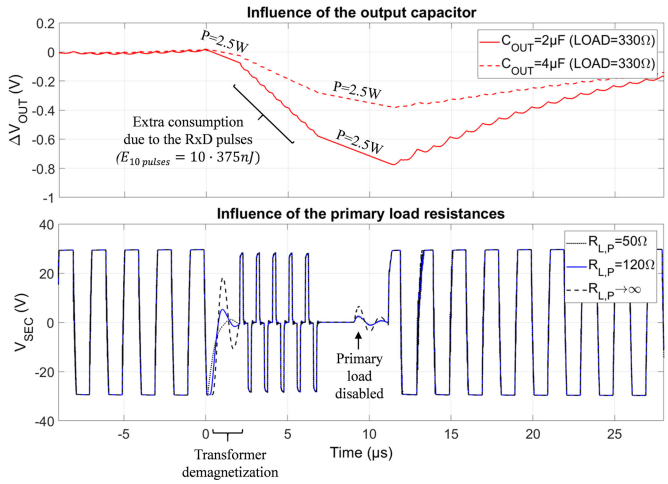

Fig. 8. Simulations using SPICE models ($V_{\mathrm{OUT}} = 28.8$ V).

where $R_{L,P}$ is the primary load resistance. Since, the positive pulses are dissipated in the upper load resistance and the negative ones are dissipated in the lower load resistance, the resulting extra power consumption P_{RXD} during T_B can be expressed as follows:

$$P_{\mathrm{RXD}} = n \cdot \frac{{V_{\mathrm{IN}}}^2}{R_{L,\ P}} \cdot \frac{t_{\mathrm{pulse}}}{T_B} \tag{2}$$

where n is the number of RxD pulses, corresponding to the number of changes in the logic levels ($0 \rightarrow 1$ or $1 \rightarrow 0$). In the worst case, $n = (T_B - 3\,\mu\mathrm{s})/t_{\mathrm{bit}} = 16$, which leads to an additional

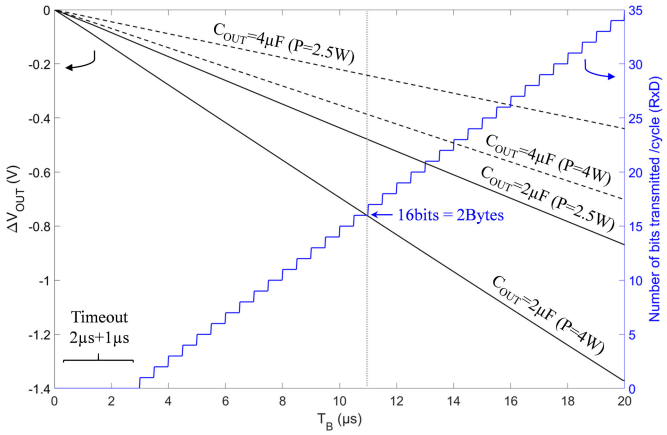

Fig. 9. Influence of T_B on the performances of the proposed circuit.

power consumption during T_B of 545 mW considering the timing constraints proposed in Section II-A.

As explained before, the demagnetizing oscillations can be reduced depending on the primary load resistance seen by the primary windings of the transformer. The influence of the primary load resistance value on the demagnetizing is also presented in Fig. 8. A low $R_{L,P}$ resistance can reduce the demagnetizing oscillations but it would increase the power consumption due to the RxD pulses. Based on the simulations, the primary load resistance was chosen $R_{L,P} = 120\ \Omega$.

The main inconvenient of the proposed method is the output voltage drop during the phase B due to the complete demagnetization of the supply transformer. The duration of this period is critical and should be reduced as much as possible. Fortunately, the voltage drop can be compensated by adding extra output capacitors C_{OUT}, as shown in Fig. 9. As expressed in (3), the observed variation ΔV_{OUT} on the output voltage V_{OUT} is also dependant from the total power consumption P as

$$\Delta V_{\mathrm{OUT}} = V_{\mathrm{OUT}} \left(e^{-\frac{T_B}{R_{\mathrm{LOAD}} \cdot C_{\mathrm{OUT}}}} - 1 \right) \approx -\frac{P \cdot T_B}{V_{\mathrm{OUT}} \cdot C_{\mathrm{OUT}}} \tag{3}$$

where R_{LOAD} is the equivalent resistance seen at the output. Fig. 9 illustrates the compromise between the RxD bit rate and the dropout voltage at the output.

IV. Experimental Results

A. DATA Exchange

A 6-layered printed circuit board (PCB) was designed to check the viability of the proposed method. The duration of the phase B was fixed at $T_B = 11\ \mu$s in order to transmit 2 Bytes using a 500 ns bit time (=8 μs) after the 2 μs-deadtime. Once the transmission is complete, another 1 μs-deadtime was observed in order to prevent any conflict.

The transformer used is a planar transformer with five turns in the primary windings and ten turns in the secondary winding. As shown in Fig. 10, two planar transformers were integrated in a six-layered board (high side and low side) corresponding to a half-bridge application. The planar transformer is a shell form

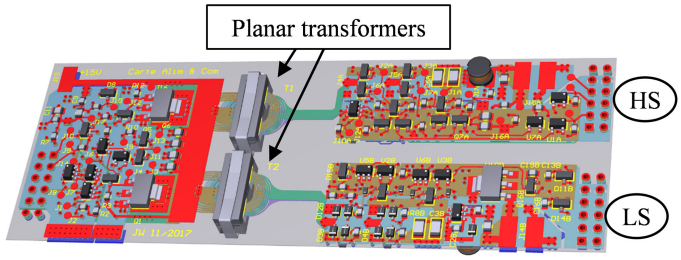

Fig. 10. Six-layered board design using Altium designer.

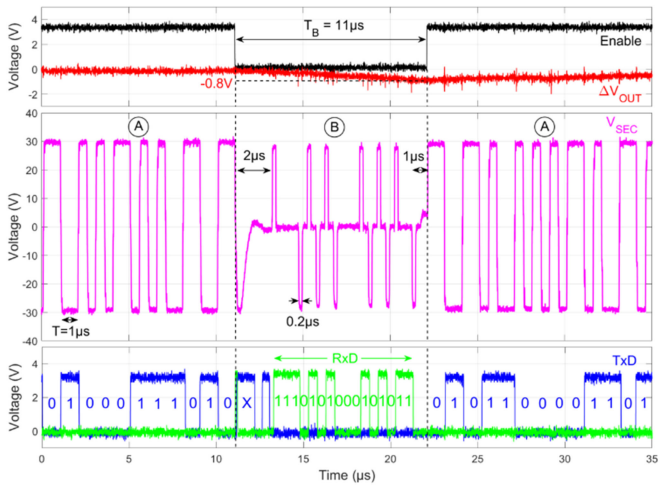

Fig. 11. Experimental waveforms.

in which the magnetic core is realized by a E-shaped ferrite core associated to a 3F3 ferromagnetic material. The windings of the transformer are located on the internal layers of the PCB. The electric isolation is realized by a 500 μm epoxy-layer, which guarantees a reliable isolation between primary and secondary circuits. The resulting parasitic common mode current is relatively low since the coupling capacitor of the power transformer is only 8 pF (characterization at 1 MHz using a vector network analyzer). The design of the planar transformer used will not be more detailed in the present article because any type of transformer can be used for the proposed method.

For experimental needs, data frames were implemented on two FPGA boards using VHDL programming. Due to the FPGA board, the logic levels are in CMOS 3.3 V compatibility. The experimental waveforms are shown in Fig. 11 demonstrating the data exchange using the proposed circuit. A low logic level is applied during 11 μs on the "Enable" signal every 1 ms ($f = 1$ kHz), which opens Q_1 and Q_3 and enables the primary load resistance. V_{SEC} represents the differential voltage at the secondary winding of the transformer, as described in Figs. 5 and 6. On Fig. 11, the TxD and RxD signals represent the data after decoding at the primary side (RxD) and at the secondary side (TxD). A maximum bit rate of 1 Mb/s for TxD and 16 kb/s for RxD was observed. These characteristics can be optimized depending on the static consumption of the circuit, the pulsewidth and the bit time. The transformer demagnetization can be seen on the $V_{\mathrm{SEC}}{}'$ waveform during the 2 μs delay before

the RxD pulses generation. The TxD signal is decoded at the primary side by a XOR logic function between a synthetized clock signal and the drain-source voltage of Q_8. The same result could be obtained with Q_7 and a logic inverter. The synthetized clock signal is obtained by synchronization with the first rising edge of the TxD signal (phase A).

An output voltage dropout of $\Delta V_{\mathrm{OUT}} = -0.8$ V can be observed on Fig. 11, which corresponds to $V_{\mathrm{OUT}} = 27.5$ V at the end of the phase B. This value is highly dependent on the circuit consumption. In this case, a 330 Ω-load resistance (R_{LOAD}) was used to simulate a static power consumption of 2.5 W. The output voltage drop depends on four parameters: the duration of the demagnetized period, the power consumption of the circuit, the value of the capacitor C_{OUT} and the number of changes in the RxD logic levels as explained in the previous section. The circuit was tested with a nominal capacitance of 14.1 μF for the output capacitor. However, a voltage derating behavior was observed on this capacitor. In the board presented in Fig. 10, the output capacitor consists of three ceramic capacitors of 4.7 μF (=14.1 μF) in X7R material *(MC1206B475K500CT)*. Considering that the capacitance depends on the voltage applied, the equivalent capacitor at $V_{\mathrm{OUT}} = 28.8$ V was about 2 μF and the observed ΔV_{OUT} was much more than expected with the nominal value (14.1 μF). The voltage drop could be reduced by the use of NP0/C0G capacitors or the increase of the nominal voltage. In this design, a 1206 package with 50 V rated voltage has been chosen in order to reduce the bank capacitors size.

A postregulation is then realized by a Buck converter which can regulate the supply voltage at 25 V as long as V_{OUT} is greater than 25.7 V. The demagnetized duration and the capacitor C_{OUT} must be chosen considering the worst case scenario. In the experimental setup, Artix-7 FPGA boards were used to manage the communicating power supply circuit (FPGA board: *Nexys4 DDR*).

B. High dv/dt Susceptibility Tests

The gate driver boards are always implemented as close as possible to the power modules in order to guarantee a correct switching of the power device. Indeed, the parasitic inductances of wires are sensitive to the common-mode currents. The power circuit is often composed of several power devices in series or parallel. In a half-bridge configuration, two power devices are associated in series (HS and LS). During a fast switching of the power component, a high dv/dt can be observed in the switch node. In the gate driver boards, the secondary ground potential is imposed by the source voltage that is a floating potential as the source voltage of the HS component varies when the LS power device is used. As a result, the gate drivers are submitted to a severe environment with high-EMI constraints.

In order to test the dv/dt susceptibility, high voltage pulsed signals were applied between the primary ground and the floating secondary ground [11], as shown in Fig. 12. In this experiment, a battery-powered oscilloscope was used with caution as high-voltage transients were applied on the secondary ground potential. The TxD signal was monitored during this process in order to detect the perturbations on the internal signals. The monitored signal is taken at the input of a Schmitt triggered

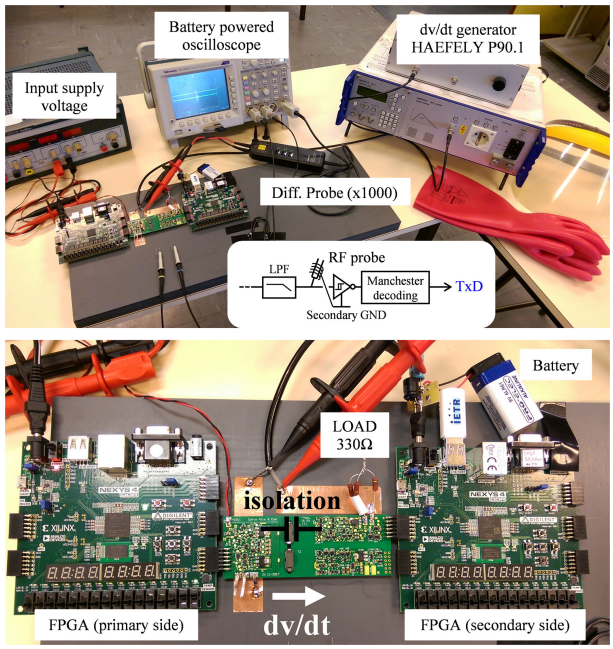

Fig. 12. Experimental setup for high dv/dt susceptibility tests.

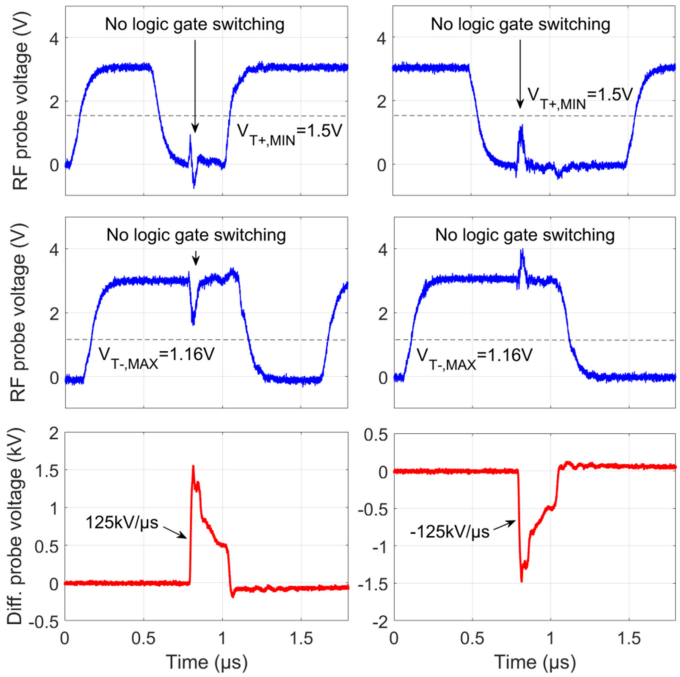

Fig. 13. Monitoring of the TxD signal during a high dv/dt switching.

logic gate. The Schmitt triggers are very important in this design as it can provide a reliable digital signal at the output using the hysteresis principle. The tests were performed up to ±125 kV/μs applied across the isolation barrier. The signals presented in Fig. 13 were taken at the secondary side using an RF probe to minimize the noises due to the ground loop. In this configuration, the oscilloscope must be referred at a floating potential due to the fast pulses of 1.5 kV applied on the isolation barrier. The results presented in Fig. 13 demonstrate the reliability of the proposed DATA communication system in the worst case.

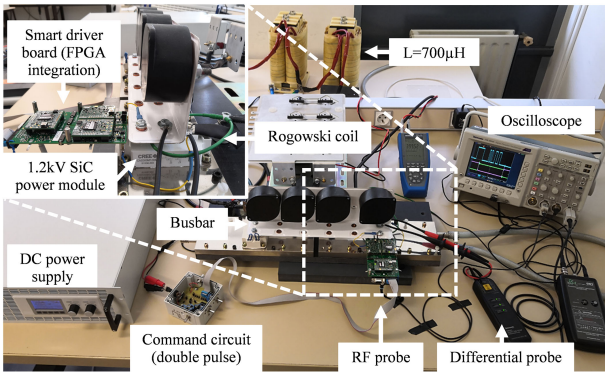

Fig. 14. Experimental setup for evaluation under real-switching conditions.

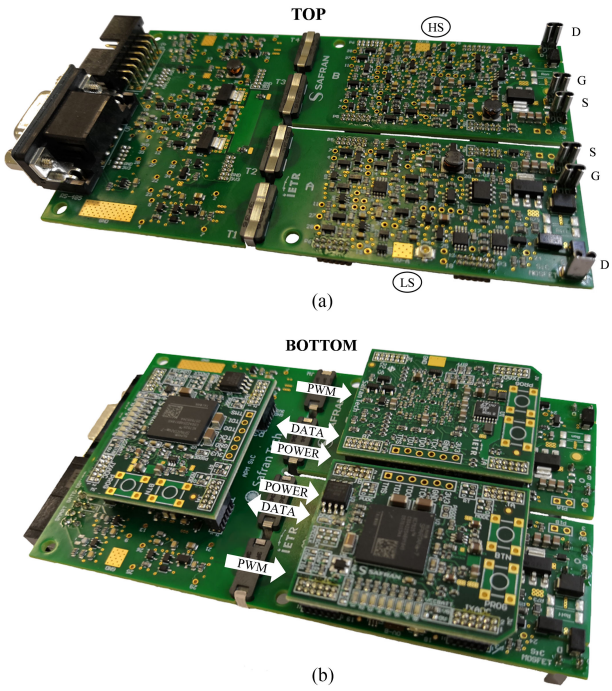

Fig. 15. Smart driver board for health monitoring with embedded communication features. (a) Top view. (b) Bottom view.

The observed noise on the signals is the addition of the real perturbation and the noise due to the probe. Since the EMI noises are monitored in the worst case of study, the threshold voltages of the Schmitt-triggered logic gates were used to verify the integrity of the TxD signal when the EMI noise occurs.

C. Implementation in a Driver Board Design Under Real-Switching Conditions

As described in Fig. 14, a gate driver board was connected to a 1.2 kV SiC MOSFET module (Cree CAS300M12BM2) in a double pulse test bench. The proposed solution was implemented in a smart driver board that integrates Spartan-7 FPGA boards on the primary and secondary circuits, as shown in Fig. 15(b). This circuit was tested in a dc–dc buck configuration using an inductance of 700 μH connected to the busbar. An external gate resistance of 2.4 Ω was implemented on the gate driver board presented in Fig. 15. This board was specifically designed

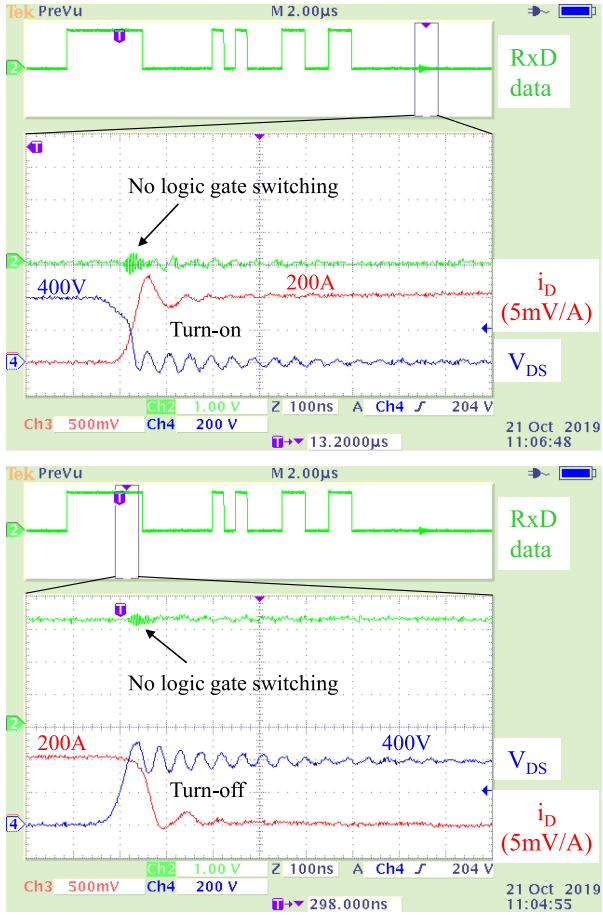

Fig. 16. Experimental results using a 400 V/200 A switching cell.

for health monitoring and integrates the proposed method as a communication channel in addition to conventional features (galvanic isolation, short-circuit detection, soft shut-down …). The design of this board will not be more detailed in the present article.

In the experimental setup, a differential probe and a Rogowski coil were used to monitor the drain-source voltage and the drain current of the power SiC MOSFET. As shown in Fig. 16, a 400 V/200 A switching did not affect the RxD signal at the primary side as no undesirable logic level change occurred during the switching. The resulting dv/dt is about 15 kV/μs, which correspond to an optimal switching at 400 V considering the switching characteristics provided in the CAS300M12BM2 datasheet (rise time of 68 ns and fall time of 43 ns).

V. Discussion and Perspectives

As mentioned in the introduction, the targeted application is health monitoring for power SiC MOSFET transistors. In this case, the RxD data are monitoring parameters that can be measured using the secondary circuit of a smart driver board, such as the on-state voltage, the gate leakage currents, temperature values or others ageing indicators. The RxD data could also be used for fault transmission by sending a more detailed error message to the primary side. It could even replace the traditional error pulse transmission, but this solution is not recommended as the latency of the proposed communication method is not

guaranteed. Another application is the reparametrizing of the gate driver in real time, which could be achieved by exploiting the TxD flux. For example, switching slope control, blanking time setting, or gate-source voltage variation could be realized using the proposed method. Other applications, such as the implementation of sensors on high-voltage lines could also be addressed.

Nowadays, gate drivers integrate more and more features and FPGA/CPLD are already integrated on the primary circuit in some designs. The addition of measurement and communicating features on the gate drivers increases the complexity, the cost and the size of the board that could be a major constraint to the development of such technology. However, Fig. 15 demonstrates that it is possible to integrate the proposed solution in a 120 $\times$ 70 mm² design for driving a 62 mm power module. Moreover, the FPGA integration is the first step in the prototyping process as most of the circuitry presented in Fig. 6 could be integrated in the mixed analog/digital chip designs.

VI. Conclusion

A new structure for the bidirectional data communication using a low-power supply circuit was proposed and investigated. The presented results show the relevance of the proposed method in highly constraints gate driver designs. The proposed structure was simulated and the experimental results are provided. Careful consideration should be given to the choice of the output capacitors throughout the implementation of this topology. In the implemented solution, bit rates of 1 Mb/s for TxD and 16 kb/s for RxD were demonstrated. Fast transient voltages were also applied on the designed board in order to verify its dv/dt immunity up to 125 kV/μs. The method was also implemented in a smart gate driver board and confronted to a 400 V/200 A switching using a 1.2 kV SiC module. The proposed solution requires the integration of digital circuits on the gate driver board but offers new perspectives for on-line monitoring using the gate drivers in power electronics. A specific serial protocol based on UART can be implemented for complex data communication across the isolation barrier of the gate driver boards. Due to the complexity and the cost of the health monitoring using the gate driver, this technology might make sense only for high-power converters (>50 kW) in which the reliability is the priority.

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