Review of Loss Distribution, Analysis, and Measurement Techniques for GaN HEMTs

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***Abstract*—In recent years, there has been a trend for improved performance in semiconductor switches, allowing power electronic systems to achieve higher efficiency and higher power density. This desired improvement has led to the adoption of wide-bandgap devices-based switches due to the fact that silicon (Si) has been reaching its material limit. Si carbide and gallium nitride (GaN) offer faster switching speeds. Therefore, they require higher level measurement technologies to analyze them. In this article, the theoretical loss breakdown of a GaN-based power electronic system is presented including an analysis of its dynamic behavior. Several methods of measurement are presented to quantify the behavior of fast switching.**

***Index Terms*—Dynamic R_{dson}, gallium nitride (GaN), loss analysis, loss measurement, loss modeling, wide bandgap (WBG).**

I. Introduction

THE SILICON (Si)-based switches, like MOSFET and insulated-gate bipolar transistor (IGBT), are the legacy switch devices that have been used in various power converters designs. The methods to estimate the losses introduced from the MOSFET and IGBT have been well developed [1], [2]. Si switch devices have seen repeated technological improvements throughout their lifetime. However, it has now become apparent that this improvement cannot continue indefinitely as the device performance is limited by the material properties. The inclusion of wide bandgap (WBG) semiconductors in power converters is a necessary step to secure continued performance enhancement in power electronic systems [3]–[5]. Gallium nitride (GaN) power switch devices recently have gained great popularity in both academia and industry, due to their better figures of merit versus conventional MOSFETs. So far, vertical GaN devices have not yet been produced on a commercial level. The commercially available GaN devices are most likely to be a lateral structure [5]. The device structure comparison between vertical Si MOSFET and lateral GaN high electron mobility transistor (HEMT) is shown in Fig. 1.

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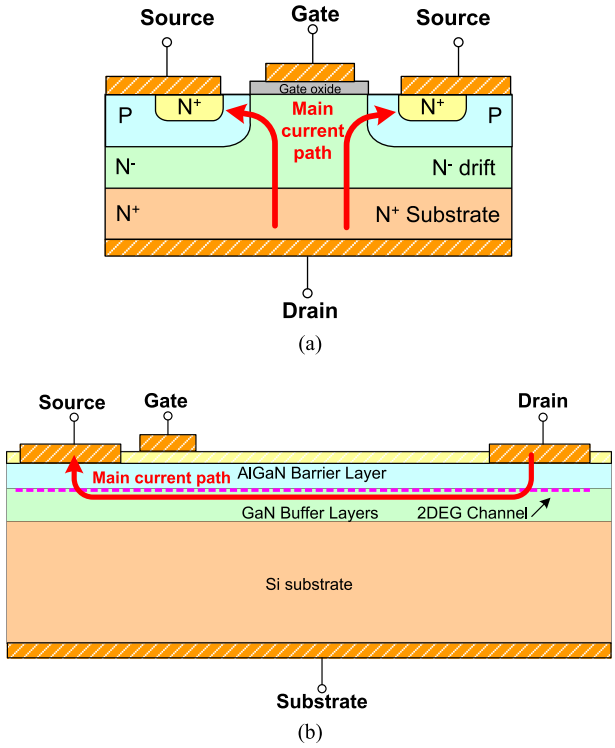

Fig. 1. Transistor structure. (a) Vertical Si MOSFET. (b) Lateral GaN HEMT.

GaN enhancement-mode HEMTs have excellent performance and relatively high charge density and mobility. GaN differs from other transistors because of its 2-dimensional electron gas (2DEG). The 2DEG is a byproduct of the heterointerface between the GaN layer and AlGaN layer. Due to the performance of GaN HEMTs, its incorporation into both soft-switching and hard-switching applications leads to many potential benefits. Using GaN HEMTs is beneficial when operating the switches with the zero-voltage switching (ZVS) technique; this is due to their much smaller parasitic capacitance compared to a conventional Si MOSFET. As the device capacitance is decreased, the required inductance needed to charge and discharge this capacitance is also reduced, resulting in a more compact converter. Small gate charge makes GaN devices suitable for hard-switched converters as the duration of the *I*/*V* overlap is much shorter than Si, in addition to the gate drive losses being reduced as well. GaN devices also do not contain a physical body diode which results in zero reverse-recovery losses. Therefore, GaN devices introduce lower switch-ON/switch-OFF losses in hard-switched converters [6]–[8]. In fact, GaN HEMTs are being incorporated

into many power converter topologies and applications. These applications include consumer adapter, wireless charger, light detection and ranging, onboard charger, isolated dc/dc auxiliary power module, and traction inverter [9]–[15].

With the increased usage of GaN devices, it becomes important for both researchers and engineers to understand how GaN devices differ from Si devices in terms of losses and how to appropriately measure these losses. However, there are not many papers that discuss and review the comprehensive loss distribution, loss analysis, and measurement techniques for GaN-based applications. In this article, the detailed $E_{\rm on}/E_{\rm off}$ switching loss composition and percentage for GaN and the quantitively advantages of GaN compare to Si MOSFET in terms of loss are presented. A step-by-step case study on PLECS-based GaN loss modeling is also provided. Moreover, this article also provides a review on the dynamic $R_{d\rm son}$ and its measurement technique.

This article is organized as follows. Section II introduces the GaN device loss mechanisms, which includes switching loss, conduction loss, deadtime loss, dynamic $R_{d\rm son}$ loss, and $C_{\rm oss}$ capacitance hysteresis loss. Section III discusses the different state-of-the-art analytical models. In Section IV, as a case study, the PLECS-based GaN modeling is introduced and presented in detail. The simulation verification are also given to verify the accuracy of the device loss model. In Section V, the loss measurement techniques are introduced, so that different types of losses can be captured.

II. GaN Power Loss Mechanisms

In general, similar to Si devices, the losses for GaN can be mainly divided into conduction loss and switching loss while the detailed loss composition for GaN device differs to Si's. Therefore, care should be taken when analyzing a converter developed with GaN such that the losses are accurately estimated. For GaN, the conduction loss includes the $R_{d\rm son}$ loss at 25 °C, $R_{d\rm son}$ loss from heating effect, $R_{d\rm son}$ loss from trapping effect (also known as dynamic $R_{d\rm son}$ loss), and deadtime loss; the switching loss includes turn-ON/turn-OFF *V–I* overlap loss, $E_{q\rm oss}$ and $E_{\rm oss}$ losses. It is also noticed that under very high frequency, there is another type of loss called $C_{\rm oss}$ capacitance hysteresis loss which has drawn some attention, but most likely, for radio frequency (RF) applications.

A. V–I *Overlap Loss*

Power loss is defined as the area of overlap between voltage and current waveforms. For semiconductor devices, the ideal operation is to have zero current through the switch in the OFF state and zero voltage across the switch in the ON state. Both of these requirements are achieved instantaneously when a device transition is required. In practice, there is some *V–I* overlap as the devices transition from OFF to ON and vice versa.

For turn ON, each switching transition can be broken down into four segments. The stages for an ON transition are detailed next and summarized by Fig. 2 and its loss breakdown is shown in Fig. 3.

1) Period 1 turn-ON delay (t_0–t_1): the device begins to transition into the ON state when a positive gate voltage is applied. During this stage, the device remains OFF until the gate reaches the threshold voltage.
2) Period 2 current rise (t_1–t_2): once the gate voltage has reached the threshold, it continues to rise, with the channel current directly related to the gate voltage.
3) Period 3 voltage fall time (t_2–t_3): once the current has reached its full load value, the voltage begins to fall to its ON-state value. The equivalent circuit is shown in Fig. 4.
4) Period 4 oscillations (t_3–t_4): once the voltage has reached its ON-state value, there may be some oscillations due to resonance. The gate voltage also rises from the plateau value to the steady-state value.

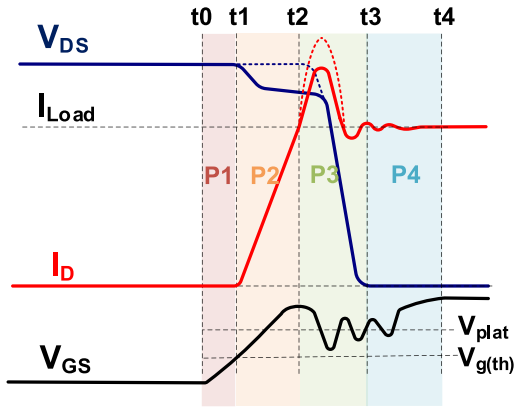

Fig. 2. Switch turn-ON transition.

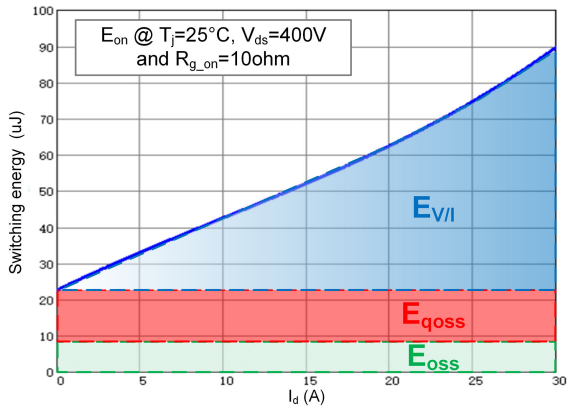

Fig. 3. Turn-ON loss breakdown of GaN.

B. *Capacitance Loss* $\rm E_{oss}$

$E_{\rm oss}$ loss is the energy lost in charging the parasitic capacitance of the switch. This energy is lost during turn ON as the capacitance is discharged through the channel of the switch. The equation for $E_{\rm oss}$ is described in

$$E_{\rm oss} = \int_0^{V_{\rm dc}} V_{\rm ds} \times C_{{\rm oss}(V{\rm ds})} dV_{\rm ds}. \tag{1}$$

C. *Capacitance Loss* $E_{q\rm oss}$

$E_{q\rm oss}$ is defined as the loss introduced from the capacitor charging current of the opposite switch in a half-bridge configuration [8]. In a conventional Si MOSFET half-bridge, during the

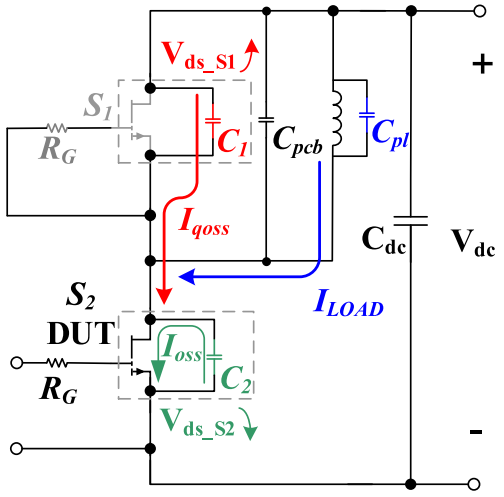

Fig. 4. Equivalent circuit during the switching-ON voltage commutation transition.

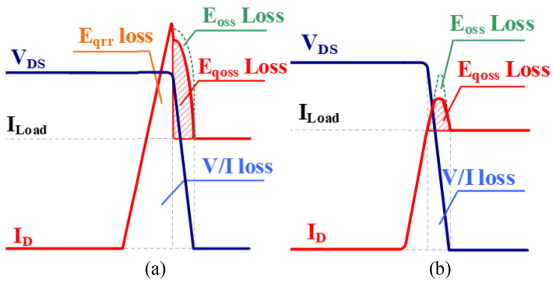

Fig. 5. Hard-switch turn-ON losses distribution. (a) Si MOSFET. (b) GaN HEMT.

turn-ON transition, the current bump includes E_{qrr}, E_{oss}, and $E_{q\text{oss}}$ losses, as shown in Fig. 5(a) [2]. With the lack of reverse recovery loss, $E_{q\text{oss}}$ becomes more obvious for GaN HEMT, as shown in Fig. 5(b). The equation for $E_{q\text{oss}}$ is as follows:

$$E_{q\text{oss}} = \int_0^{V_{\text{dc}}} (V_{\text{dc}} - V_{\text{ds}}) \times C_{\text{oss}(V\text{ds})} dV_{\text{ds}}. \tag{2}$$

The mechanism for this $E_{q\text{oss}}$ loss is that when the upper switch turns OFF, its output parasitic capacitance C_{oss} needs to be charged. This charging current has to travel through the low-side switch which will generate additional losses. $E_{q\text{oss}}$ and E_{oss} both deal with the same capacitive component of the switch; thus, the total charge of each is the same. However, they contribute different amount of losses due to the different conditions surrounding them. For E_{oss} loss, the initial V_{ds} voltage is equivalent to the dc-link voltage and is discharging to zero. For $E_{q\text{oss}}$, the initial drain source voltage is close to zero and the switch is charging to the dc link. Thus, the total energy dissipated is different as described by (1) and (2). It is important to note that the parasitic capacitances from the printed circuit board (PCB) and power inductor will also contribute to this loss, which will be discussed later.

In fact, the C_{oss} comparison among Si MOSFET C7 and CFD and GaN HEMT is shown in Fig. 6. It is clear that the total C_{oss}

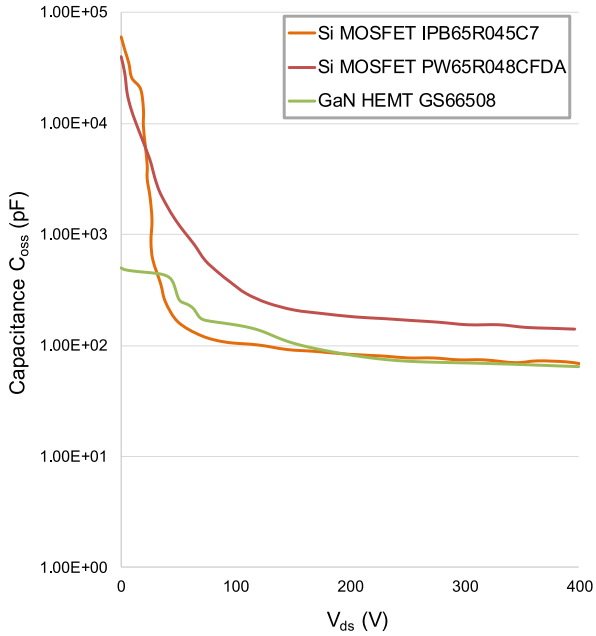

Fig. 6. C_{oss} comparison between Si MOSFET and GaN HEMT.

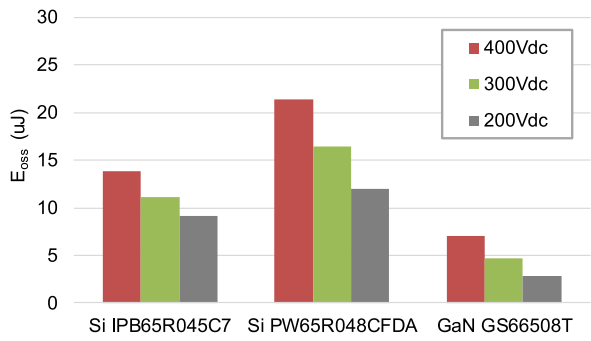

Fig. 7. E_{oss} comparison between Si MOSFET and GaN HEMT under different voltages.

of GaN is lower compared to Si MOSFET. This indicates a lower E_{oss} energy loss from GaN compare to Si MOSFET. Moreover, the Si MOSFETs obtain high nonlinearity. This will make the $E_{q\text{oss}}$ loss even larger. The comparisons for E_{oss} and $E_{q\text{oss}}$ between Si MOSFET and GaN HEMT at different voltages are also shown in Figs. 7 and 8, respectively.

D. Dynamic ON-State Resistance Loss

Dynamic ON-state resistance loss is a byproduct of the so-called dynamic $R_{d\text{son}}$. It is due to charge trapping effect of electrons and results in a decrease of the 2DEG density. This change in resistance will cause additional loss for the GaN-based power electronic applications. Typical on-state resistance for most Si devices is affected by device channel current and temperature; however, a recent research has shown that the increase in resistance for GaN devices exceeds what would be expected when accounting for temperature and current. This resistance increase is associated with charges becoming trapped due to material defects. The traps are a byproduct of manufacturing

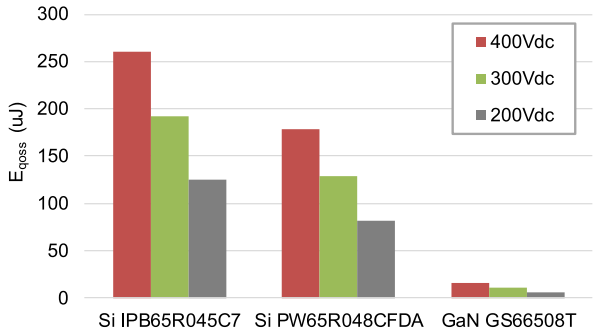

Fig. 8. E_{qoss} comparison between Si MOSFET and GaN HEMT under different voltages.

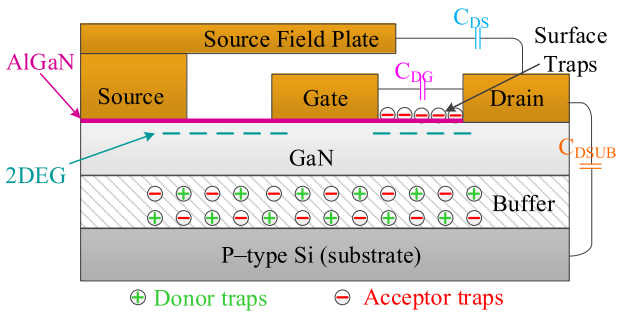

Fig. 9. Lateral GaN device with traps.

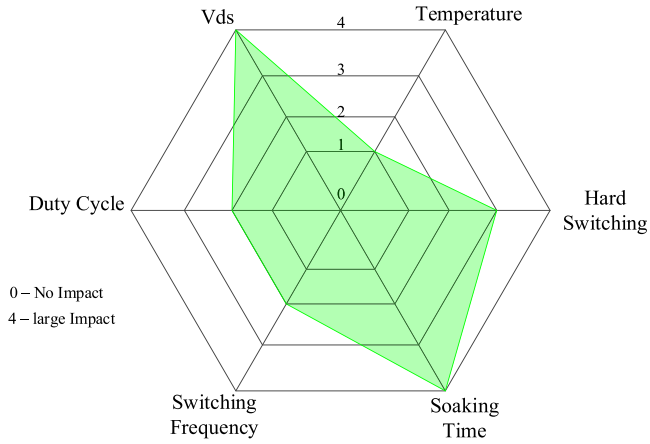

Fig. 10. Impact factors of dynamic R_{dson}.

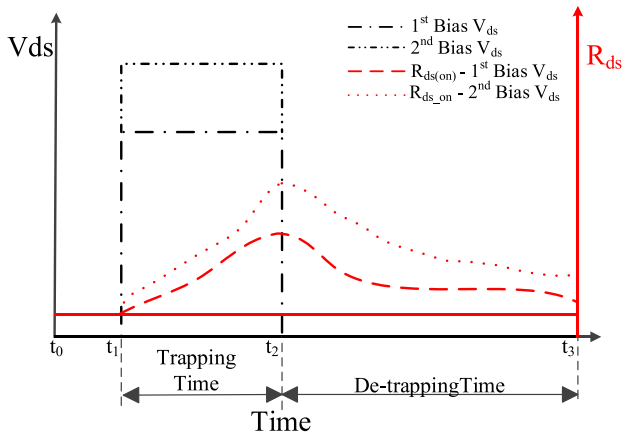

Fig. 11. Effect of trapping and detrapping process on dynamic ON-state resistance.

lateral type GaN which has a buffer layer between the substrate and GaN. The buffer layer needs to have a large resistance to prevent leakage currents [16]. Thus, manufacturers use iron and carbon inside the buffer to increase this resistance, but these impurities lead to the aforementioned traps that reduce the flow of current through the channel. Dynamic R_{dson} is not provided in manufacturers' data sheets but cannot be neglected by researchers and engineers as it represents additional losses and will cause a decrease in efficiency. These aspects are important as they can lead to extra junction temperature increase if not accounted for appropriately such as when considering the cooling system for a converter. Fig. 9 shows the layers of the GaN device and the space charges that can arise due to the traps. It also illustrates that there have been two types of traps reported: surface and buffer. Several impacting factors have been investigated by researchers to examine effects on the R_{dson}, and a summary of these impacting factors is presented in Fig. 10. The low impact of temperature on dynamic R_{dson} is due to the fact that temperature only has a noticeable effect with a relatively long-time scale. In other words, under a real switching condition, the impact of temperature on the trapping effect is almost negligible [17], [18]. Hard/soft switching has been investigated as well and appears to be an outlier factor for Panasonic devices which contain a slightly different structure utilizing a second drain. An important distinction in the impacting factors is that while frequency and duty have been shown to affect dynamic on-state resistance [19], this effect is only noteworthy in cases where the resistance has been increased beyond its nominal value. In other words, duty cycle and frequency do not contribute to the trapping of charges that causes the resistance to increase. Fig. 11 gives an overview of dynamic on state resistance in a switching cycle. Its interval can be divided into a trapping phase in the OFF state and a detrapping phase in the ON state. When under a large voltage stress, charges flowing into the buffer become trapped during the OFF state. Once the device switches ON, detrapping occurs and the electrons are able to be freed. This effect can be observed as a change in the channel resistance.

E. Deadtime Losses

Deadtime is necessary for proper current commutation of switches and to avoid accidental shorting of phase legs. Deadtime also has the additional function that allows some converters to operate in a zero-voltage or zero-current switching state by allowing the parasitic elements of the circuit to discharge. GaN devices do not have a parasitic body diode to conduct reverse current; thus, they have no reverse recovery losses. However, they are still capable of conducting current reversely through the same channel when its gate is OFF and the behavior for this is similar to a body diode. In order to prevent accidental

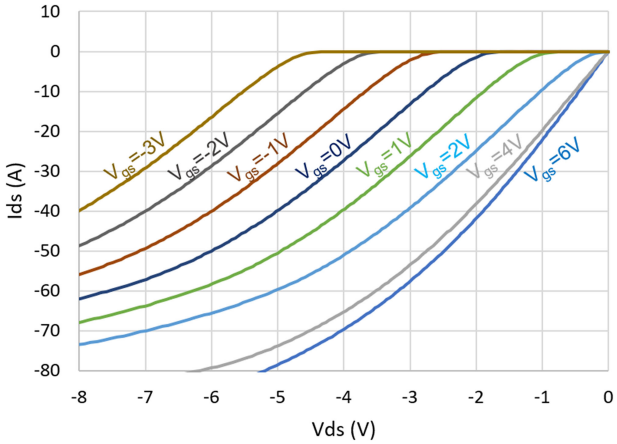

Fig. 12. GaN reverse conduction characteristics.

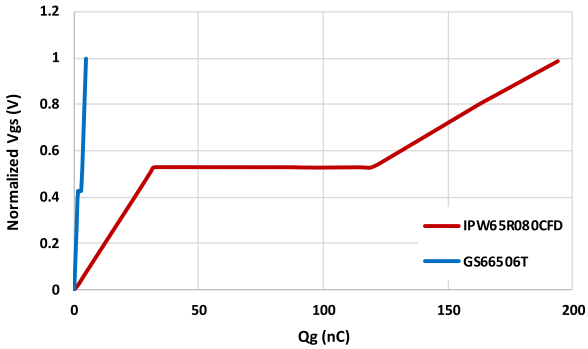

Fig. 13. Q_g comparison between Si MOSFET and GaN HEMT.

turn-ON, GaN devices are often recommended to use a negative gate voltage for the OFF state. This negative gate voltage is added to the voltage drop across the channel resistance leading to more losses with a more negative $V_{\rm gs}$. As shown in Fig. 12, the *IV* curves in the third quadrant also present the voltage drop under different negative turn-OFF gate voltages. Compared to the parasitic body diodes found in Si, the voltage drop of a GaN device during reverse conduction is much higher which is the cause of the increased losses [20], [21]. Adding a Schottky diode in parallel can improve the reverse recovery losses by fixing the forward voltage drop. Another solution to this problem is a method requiring the overlap of the gate signals such that they have a cross over point that is lower than the threshold voltage; this will ensure ZVS and minimize reverse conduction [22]. It should be noted that the test setup has an input voltage of 25 to 50 V and power ranging from 50 to 200 W. This method is not suitable for higher operating conditions with the 650 V GaN devices as d*v*/d*t* and d*i*/d*t* may be much higher and overlapping gate signals may lead to shoot through.

F. Gate Driver Loss

GaN has similar gate driver loss mechanism as for Si's. However, due to the relatively small gate charge Q_g, the gate driver loss from GaN is relatively smaller than Si's. Q_g comparison between Si MOSFET and GaN HEMT is shown in Fig. 13. GaN

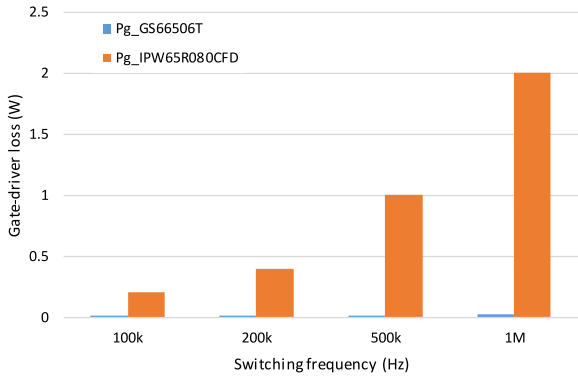

Fig. 14. Gate driver loss comparison under different switching frequencies.

HEMT obtains 40 times smaller Q_g compared to a Si MOSFET with a similar $R_{d\rm son}$ value. The gate driver loss can be estimated with the equation

$$P_{\rm driver} = V_g \times Q_g \times f_s. \tag{3}$$

As a result, the gate driver loss comparison under different switching frequency can be obtained in Fig. 14. Under 1 MHz, the loss difference is about 2 W. This can be a large loss difference for low-power applications, such as high frequency adaptors, etc.

G. Capacitance Hysteresis Loss at Higher Frequency

The losses associated with the output capacitance of the device also appear to show some sort of dynamics as researchers have reported in several works [23]–[27]. The importance of these findings is that a larger device die with smaller $R_{d\rm son}$ may not lead to a more efficient converter as the $C_{\rm oss}$ losses can begin to dominate at high-frequency operation. The losses were first noticed when GaN switches were used in an RF rectifier circuit with their source tied to gate such that it acted as a diode. The measured performance was much lower than simulation results, leading to the hypothesis that the increase in losses is a result of the output capacitance of the device or the dynamic $R_{d\rm son}$ [26]. In order to isolate the effects from dynamic $R_{d\rm son}$, several experiments have been performed using the GaN device as a capacitor by tying the gate to source and connecting it in parallel with a switching device. These tests have noted significant heating on the OFF device even when considering the possibility of thermal cross coupling [23]–[25]. In order to quantify the losses, a sawyer tower circuit is used. The premise of this circuit is that a capacitor with linear characteristics is connected in series to the device held in the OFF position. Capacitors connected in series must have equal charges which means that a voltage measurement on the reference capacitor can be used to deduce the charge and therefore the losses of the switch. It is hypothesized that the *dv/dt* is responsible for the increase in losses; this is tested at a constant frequency with different wave shapes (sine, square, class-Φ2 waveform). The results show that the waves with larger *dv/dt* results in larger energy dissipated per cycle which agrees with the previous notion of higher frequencies resulting in larger losses. In a continuation of these efforts to reduce the losses, the

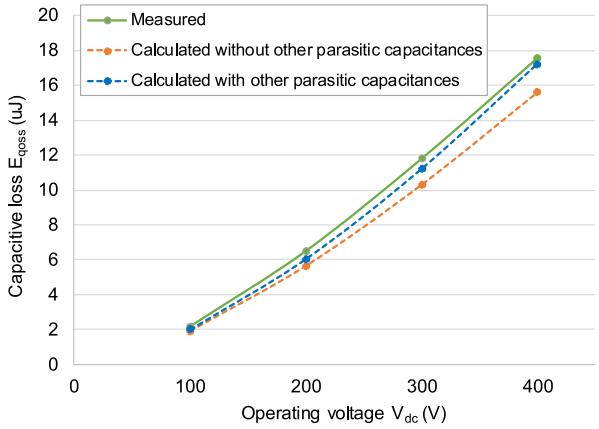

Fig. 15. $E_{q\mathrm{oss}}$ loss with/without other parasitic capacitances from circuit.

trapping effects in the buffer layer must be alleviated. In order to achieve this goal, a negative voltage bias is applied to the substrate; however, this mainly reduces the capacitance between the drain and substrate. The substrate capacitance is a part of the C_{oss}, and thus any reduction in that value will reduce the total E_{oss}. The results show that despite decreasing the losses, the *dv/dt* trend is not removed [25].

H. Parasitics Effects on Losses

The parasitic inductances from package and system circuit do not directly affect losses. However, with a relatively bad PCB layout design with large parasitic inductance, it might create some noise on the signals and impact the system efficiency indirectly. For example, the gate loop inductance might affect the V_{gs} signal and therefore a lower V_{gs} has to be applied. This leads to a higher $R_{\mathrm{DS(on)}}$ value and a higher conduction loss; the power loop inductance might create a larger V_{ds} overshoot and therefore a lower operating voltage has to be applied to the system. In other words, by applying a relatively good layout with minimized parasitic inductance, the advantages of GaN in the power electronics system can be fully utilized.

In the meanwhile, the parasitic capacitances from the PCB and the load inductor can directly affect the losses of the converter. These parasitic capacitances can contribute additional $E_{\mathrm{oss}}/E_{q\mathrm{oss}}$ losses, which is part of the switching loss. As they are voltage independent, the capacitive loss $E_{\mathrm{oss}}/E_{q\mathrm{oss}}$ considering the other parasitics from the circuit is given as follows:

$$E_{\mathrm{oss}} = \int_0^{V_{\mathrm{dc}}} V_{\mathrm{ds}} \cdot C_{\mathrm{oss}(V_{\mathrm{ds}})} dV_{\mathrm{ds}} + \frac{1}{2}\left(C_{\mathrm{pl}} + C_{\mathrm{pcb}}\right) V_{\mathrm{dc}}^2 \quad (4)$$

$$E_{q\mathrm{oss}} = \int_0^{V_{\mathrm{dc}}} \left(V_{\mathrm{dc}} - V_{\mathrm{ds}}\right) \cdot C_{\mathrm{oss}(V_{\mathrm{ds}})} dV_{\mathrm{ds}} + \frac{1}{2}\left(C_{\mathrm{pl}} + C_{\mathrm{pcb}}\right) V_{\mathrm{dc}}^2 \quad (5)$$

where C_{pl} is the parasitic capacitance from inductor and C_{pcb} is the parasitic capacitance from the PCB. The $E_{q\mathrm{oss}}$ measurement and calculation are also compared to verify the parasitic capacitances effect on the loss, which is shown in Fig. 15.

III. Analytical Models

A. Piecewise Linear Model

The piecewise linear model is one of the most popular and traditional methods for analyzing and estimating the losses of a transistor, due to the simplicity of the model [3]. The model considers the circuit only in terms of the input capacitance and external gate resistor and thus the current and voltage overlap are determined through the charging time of these capacitors. The piecewise linear model does not provide accurate results due to its exclusion of parasitic parameters and temperature dependency. For example, the transconductance in GaN devices depends on the junction temperature. The transconductance affects the plateau voltage of the device and the current through the channel which results in a non-negligible impact on the current rise time of the switch and contributes to larger turn-ON losses.

B. Improved Models

Several researchers have tried to account for the shortcomings of the piecewise linear model by increasing the complexity of the model by accounting for more dynamics. The more complicated analytical models are similar to the piecewise model in the analysis of the device transition, but they do not make the same simplifying assumptions. Thus, the end result is a more complicated model that accounts for more of the real dynamics that are present in the physical circuit. In order to better model the switching losses, the piecewise linear model has been modified to include parasitic elements and the effects of the synchronous transistor [28]. The transfer characteristics are linearized, and then differential equations are developed to describe the switching process. The model performs quite well when predicting the voltage and current waveforms; however, there is still a 10–20% error between the measured and actual losses. Similar models for Cascode devices have been developed and report relatively high accuracy with $<1\%$ difference between the measured efficiency and predicted efficiency of a buck converter [29]. The discrepancy in accuracy between the Cascode and E-mode models reinforces the notion that additional losses are not accounted for in the E-mode GaN device. Comparisons of the dynamic $R_{d\mathrm{son}}$ of Cascode and E-mode devices have been performed and show that the increase in resistance for E-mode devices is higher [19]. One advantage of the previous models' simplification is that the developed equations are far simpler and relatively easy to solve. By using a more realistic approximation for the switching characteristic curves, the experimental dynamics can be approached. The model shown in [30] also considers the V_{gs} dependence of the C_{iss} which is not provided by the manufacturer and has to be derived. This model however still cannot match experimental losses despite mimicking the switching waveforms accurately, with the authors citing the error to be within 20%. Transconductance of the GaN device is often neglected in the modeling process as it increases complexity. A good method for maintaining a simple model but allowing it to be useful at all operating points is to use a scaling method. The temperature coefficient for the transconductance of GaN devices

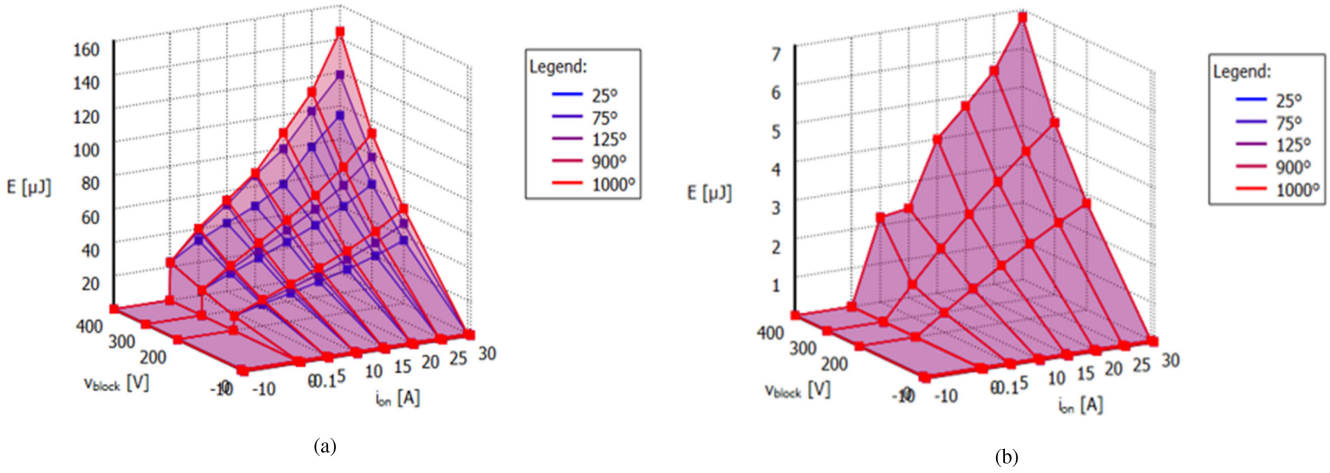

Fig. 16. Switching loss 3-D lookup table. (a) $E_{\rm on}$. (b) $E_{\rm off}$.

is negative which is the opposite of Si and SiC. $E_{\rm on}$ can be scaled accurately using the transconductance value. Extraction of the transconductance values along with scaling methods are provided in [6] and [7].

C. Circuit Simulation Models

Another approach to modeling GaN devices is to build a circuit model that tries to capture the behavior of the device during switching transitions. A GaN model has been developed in [31] that accounts for the reverse conduction characteristics of GaN. The results presented show that the simulated waveforms closely match those of the experimental ones. However, this model is resource intensive as circuit simulations are usually more computationally heavy and require more time to solve. This flaw is coupled with the fact that this model requires significant parameter extraction from the device data sheet. While the authors do present promising results, the lack of any loss estimates makes this method suspect. Other researchers, such as in [28], have presented similarly accurate simulation waveforms but still had 10–20% error when estimating the losses.

IV. PLECS Modeling

PLECS offers relatively quicker simulation than SPICE models as PLECS uses lookup tables to approximate switching losses; this makes it suitable for system loss analysis of power electronic converters. In this article, PLECS modeling is discussed in detail as a case study to present the step-by-step loss modeling for GaN-based applications.

A. Loss Model

The PLECS device modeling mainly includes three parts. They are the switching loss $E_{\rm on}/E_{\rm off}$, conduction loss, and thermal impedance. Unlike the SPICE device model, which determines the semiconductor losses from current and voltage transients, PLECS records the semiconductor's operating condition before and after each switch operation. The critical parameters used to determine the losses are drain current, blocking voltage, and junction temperature. PLECS then uses these parameters to read the resulting dissipated energy from a 3-D lookup table.

By applying the aforementioned intrinsic $E_{\rm on}/E_{\rm off}$ loss, the switching loss modeling in PLECS can be built as shown in Fig. 16. However, $E_{\rm on}/E_{\rm off}$ is determined not only by the drain current, blocking voltage, and junction temperature. The external gate resistance $R_{g\_{\rm on}}/R_{g\_{\rm off}}$ also affects the $E_{\rm on}/E_{\rm off}$ values. In fact, the gate resistance affects the *V–I* overlapping loss, while the capacitive losses $E_{\rm oss}$ and $E_{q\rm oss}$ are independent of the gate resistance. A scaling equation can be used to scale the $E_{\rm on}/E_{\rm off}$ value from one gate resistance to another. This creates a relatively straightforward and accurate way to generate the R_g-dependent $E_{\rm on}/E_{\rm off}$ value in the PLECS software.

The *V–I* overlapping loss equation for both turn-ON and turn-OFF can be written as

$$E_{VI\rm on} = \frac{\frac{V_{\rm ds}\cdot I_d}{2}\cdot[(Q_{gd}+Q_{\rm gs\_sw})\cdot(R_{\rm g\_int}+R_{g\_\rm on})]}{V_{g\_\rm on}-V_{\rm plat}} \tag{6}$$

$$E_{VI\rm off} = \frac{\frac{V_{\rm ds}\cdot I_d}{2}\cdot[(Q_{gd}+Q_{\rm gs\_sw})\cdot(R_{g\_\rm int}+R_{g\_\rm off})]}{|V_{g\_\rm off}|+V_{\rm plat}} \tag{7}$$

where $R_{g\_\rm int}$ is the internal gate resistance of the GaN device, $V_{g\_\rm on}/V_{g\_\rm off}$ is the turn-ON/turn-OFF gate voltage, and $Q_{\rm gs\_sw}$ can be obtained by (5)

$$Q_{\rm gs\_sw} = Q_{\rm gs}\cdot\left(\frac{\frac{I_d}{g_m}}{\frac{I_d}{g_m}+V_{\rm th}}\right). \tag{8}$$

Therefore, the $E_{\rm on}/E_{\rm off}$ scaling equation on different R_g can be written as (9) and (10), shown at the bottom of next page.

The conduction loss can be extracted by using the *VI* curves of the device. The simulated VI curves are shown in Fig. 17. The conduction loss can be separated as $R_{d\rm son}$ losses from heating effect and trapping effect. The heating effect can be modeled with different *IV* curves under different junction temperatures. The extreme high temperature can be applied as a simulation boundary to avoid extreme thermal runaway and thus lead to the

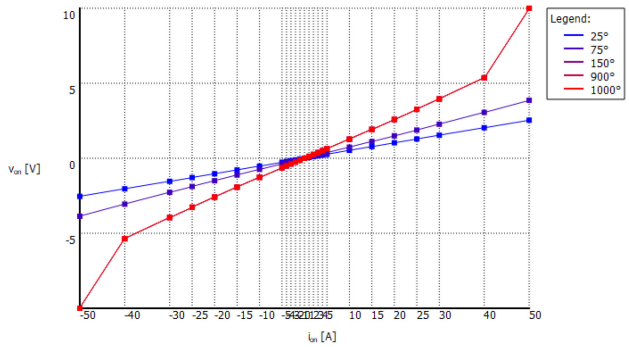

Fig. 17. *IV* curve modeling under different T_j.

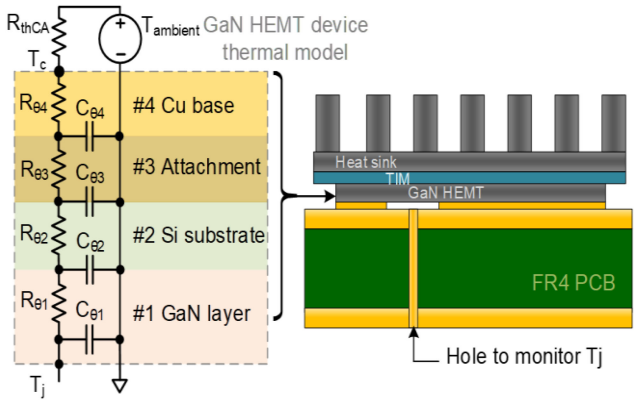

Fig. 18. GaN HEMT device thermal model.

computer system breakdown. For trapping effect, as explained in the previous section, there are many different impact factors, but it is mainly affected by the operating voltage $V_{\rm ds}$ for continuous running applications. Therefore, an equation can be drawn to simulate this part of loss as follows:

$$V_{\mathrm{on}(Vds)} = V \cdot \left(1 + k_{Tj} + k_{dR(Vds)}\right) \tag{11}$$

where k_{Tj} is defined as the increased $R_{d\rm son}$ ratio due to the heating effect and k_{dR} is defined as the increased $R_{d\rm son}$ ratio due to the trapping effect [18]. The k_{dR} factor also varies with the vendors of GaN devices. In fact, this is still an ongoing research topic on the exact values of dynamic $R_{d\rm son}$ [16], [18], [19], [32], [33].

The deadtime loss can be modeled by using the following equation in PLECS:

$$V_{\rm on} = v - (i < 0) \cdot (1 - g) \cdot (V_{\rm th} - V_{\rm gs\_off}). \tag{12}$$

This equation means that once the drain current is in reverse direction and the gate is turned OFF, there will be an additional ON-state voltage drop which is equal to the term $(V_{\rm th} - V_{\rm gs\_off})$ applied onto the total on-state voltage of the device to represent the diode behavior of GaN HEMT.

Regarding the capacitive hysteresis loss, for most power electronic converters operating below 5 MHz, the impact from this capacitance loss is neglectable. While for RF or wireless applications operating with a switching frequency above 5 MHz, the loss will be gradually noticed with the switching frequency increasing. For GaN devices, the loss estimation can be approximated with a Steinmetz fit according to [23]

$$E_{\rm oss\_hy} = K f_s^{\alpha} V_{\rm ds}^{\beta} \tag{13}$$

where *K*, α, and β are Steinmetz parameters and will vary according to the device used. Zulauf *et al.* [23] provide a list of parameters for several commercially available GaN devices.

In fact, for the application scope with very high switching frequency, the PLECS simulation might no longer be a good way to simulate the overall system. Other simulation approaches should be considered.

B. Thermal Modeling

The last part of the PLECS device modeling is the thermal impedance. The detailed thermal model of GaN HEMT can be found in [34]. The model is based on Cauer *RC* thermal network and includes four stages. As shown in Fig. 18, each stage of the *RC* parameter is assigned to the corresponding package layers, which are copper base, attachment, Si substrate, and GaN layer. In addition, curve fitting is applied to tune and improve the accuracy of the thermal model.

C. System Simulation Based on PLECS

A GaN-based synchronous buck converter is built to verify the PLECS device model. The applied GaN device is GS66508T. The converter is operating under 200-kHz switching frequency, input voltage is 400 V, and output voltage is around 193 V. As a top-cooled GaN device is applied, the GaN layer of the device is relatively close to the PCB, as shown in Fig. 18. Therefore, the monitored temperature through the thermal hole can be considered as the junction temperature. In this test, the temperature on the active switch is monitored. The thermal resistance of the device has been measured on the PCB. The overall junction-to-ambient thermal resistance is 5 °C/W. By knowing the thermal resistance of the switch device, the overall loss can be calculated. Finally, the junction temperature and the power loss on the active switch are compared, as shown in Fig. 19. It is clear that under heavy load, the simulation results

$$E_{\mathrm{on}(x\Omega)} = \left(R_{g\_\mathrm{on}(x)} - R_{g\_\mathrm{on}(a)}\right) \cdot \frac{\frac{V_{\rm ds} \cdot I_d}{2} \cdot (Q_{gd} + Q_{\rm gs\_sw})}{V_{g\_\rm on} - \left(V_{\rm th} + \frac{I_d}{g_m}\right)} + E_{\mathrm{on}(a\Omega)} \tag{9}$$

$$E_{\mathrm{off}(x\Omega)} = \left(R_{g\_\mathrm{off}(x)} - R_{g\_\mathrm{off}(a)}\right) \cdot \frac{\frac{V_{\rm ds} \cdot I_d}{2} \cdot (Q_{gd} + Q_{\rm gs\_sw})}{|V_{g\_\rm off}| + \left(V_{\rm th} + \frac{I_d}{g_m}\right)} + E_{\mathrm{off}(a\Omega)} \tag{10}$$

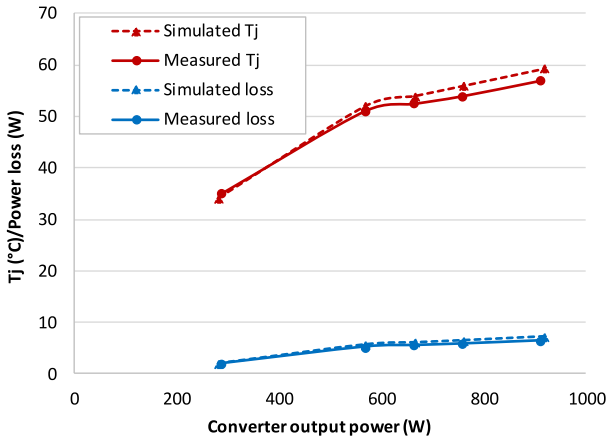

Fig. 19. Comparison of simulation and measurement results on a GaN-based buck converter.

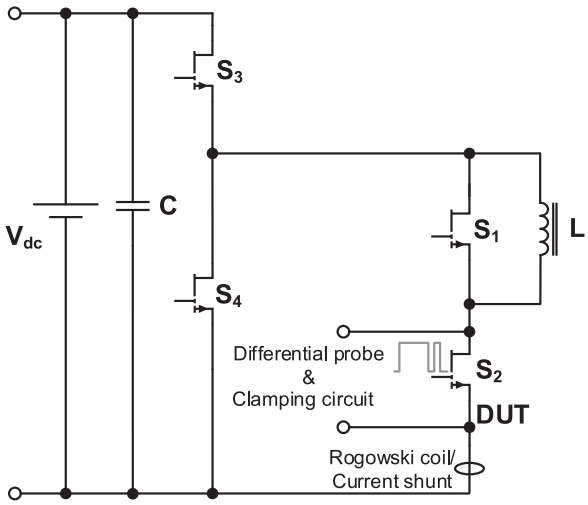

Fig. 20. DPT circuit with soak time control.

are slightly larger than the measurement results. This can be explained by the fact that the measured temperature should be slightly lower than the real junction temperature, as it is measured outside the package.

As a short summary, the PLECS-based device model is relatively accurate which could help engineers and researchers on the converter-level simulation. It can be a helpful tool for users to select the most suitable switch device and also to determine the number of paralleled devices for their specific GaN-based power converter designs.

V. Loss Measurement Techniques

Experimental testing is usually paired with theoretical analysis of losses to validate the modeling or simulation. Special care needs to be taken when extracting data from an experimental test setup, as devices like GaN have relatively high *di/dt* and *dv/dt* while the parasitic inductance and capacitance in the circuit are very small. Intrusive probes can greatly impact measurement results by introducing large amounts of stray inductance making high-fidelity equipment necessary to sample the data.

A. Double Pulse Test (DPT)

The DPT is a relatively straightforward and easy test to perform on switching devices to accurately determine losses. The DPT is also useful at determining the dynamic on-state resistance and can be modified with a clamping circuit for this purpose. Fig. 20 shows a traditional DPT circuit that has been modified to include S_3 and S_4 which act as voltage-soaking time control.

Most literature extracts the dynamic ON-state resistance through a similar approach by measuring the ON-state voltage and drain current of the device during test. For the ON-state voltage measurement, it is possible to use equipment to take a direct measurement such as in [35]. This direct measurement technique requires relatively specific and sophisticated equipment, thus is not as popular. Typically, the on-state voltage requires a clamping circuit to block the OFF-state high voltage and therefore allows the oscilloscope to measure the on-state voltage with a large degree of accuracy. Typically, a GaN device may have voltage swings of 600 V to few millivolts when comparing the OFF-state voltage spike to the ON state. The $V_{\rm ds}$ voltage is only important during the ON state where the measurement range is relatively small. Thus, the voltage can be clamped during the OFF state to allow a larger resolution during the ON state. Several clamping circuits have been proposed and developed in the literature [32], [33], [36]–[44]. The clamping circuit topologies and their specification are summarized in Fig. 21 and Table I.

Circuits 1 and 2 are very basic clamping circuits and not suitable for the application of measuring fast transients; they have only been included for completeness. Circuit 3 is a combination of Circuits 1 and 2 utilizing both a switching device and a diode. The diode is used to clamp the voltage to reduce spikes that result from switching transients. More recently, another circuit similar to Circuit 3 has been presented in [37]. This proposed circuit also requires a FET and clamping diodes but differs from Circuit 3 due to the FET being a GaN and it is actively controlled. These small modifications result in much greater complexity but offer more control and performance improvement. The resistance measurement is stable with less than 50 ns settling time under various conditions.

Circuit 4 is the current mirror circuit. It is unique in that it does not require any adjustment to the measured voltage based on the diode forward voltage drop which is presented in other clamping circuits. The design of the current mirror is presented in detail in [38]. It should be noted that due to the presence of common mode noise, a differential probe is required. The current mirror is also used and compared with the SiC clamping circuit (Circuit 5) in [39]. The results show that even with a differential probe, there remains some common mode noise in the measurement which skews the results. In [40], the current mirror is used as the clamping circuit; the tests are performed on Cascode devices which exhibit significantly less dynamic $R_{d\rm son}$. However, the authors present the measured clamped drain–source voltage and it is shown to have significant noise and ringing. In [41], the authors propose a new circuit that is similar to Circuit 5 except that an external source and filter are included for

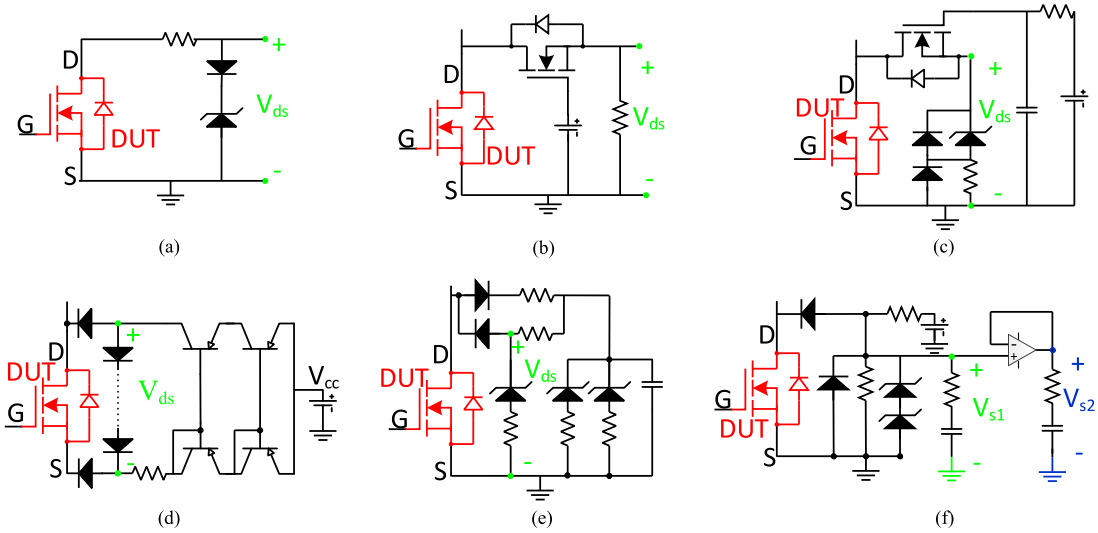

Fig. 21. Clamping circuits. (a) Circuit 1. (b) Circuit 2. (c) Circuit 3. (d) Circuit 4. (e) Circuit 5. (f) Circuit 6.

TABLE I
CLAMPING CIRCUITS PRESENTED IN LITERATURE

	Circuit 1	Circuit 2 [43]	Circuit 3 [37,44]	Circuit 4 [38]--[40]	Circuit 5 [32],[33],[36],[39],[42]	Circuit 6 [41]
Based on	Zener Diode	MOSFET	MOSFET	P-n Diode	SIC - SBD	Schottky diode, Op-Amp
Propagation delay	> 3000 ns	< 300 ns	<300 ns	<100 ns	<100 ns	<100 ns
Clamped Voltage	No limit	600V	600V	300V	600V	Limited to D1 blocking value
External source voltage	Passive	8V	8V	5V	Self-feeding	V_{cc}, Op-Amp power
V_{dson} Measurement	Ground	Ground	Ground	Differential	Ground	Ground
Voltage offset	Subtracted	Subtracted	Subtracted	Not introduced	Subtracted	Subtracted

better performance. Overall the circuit in [41] looks to provide a good solution to clamping with a low-settling time <100 ns. One uncertainty of this circuit is that the authors do not clearly define the benefits of the proposed circuit over the simpler Circuit 5, Circuit 5 does not include any additional sources or filter circuits making the design and implementation much easier.

When characterizing dynamic ON-state resistance, the most important time period is right after the device is switched ON. Therefore, a faster settling time will enable an accurate measurement. The settling time is related to the capacitance of the diodes used in the clamping circuit which is the reason that low-voltage Schottky diodes and high-voltage SiC diodes are applied. As can be seen from Table I, most experiments favor a circuit based on the SiC diode which is introduced in [36]. Circuit 5 and the updated Circuit 3 proposed in [37] are the most robust options.

When trying to determine the R_{dson} profile for a device, two different test setups can be performed. The first is the DPT and the second is continuous test. The DPT is widely applied for switching loss analysis and is prevalent in many tests as the first method to see the impact of switching state transitions on dynamic ON-state resistance. However, some researchers have noticed an accumulation of charge trapping which further increases the dynamic ON-state resistance in subsequent switching events. Thus, it becomes necessary to use a continuous test. Continuous tests best represent the device used in a power electronic system and would provide the most accurate loss analysis. One issue with the continuous test is that the increased R_{dson} contains both the heating effect and trapping effect. Fortunately, separating out the heating effect is not an issue for the DPT due to the time frame the test is run in. In [42], the authors separate the temperature effect by measuring the switching losses in the DPT and using these losses in a continuous dc test without switching. Thus, the change in resistance that would be caused by the same power loss can be quantified and then this can be contrasted with the continuous switching test to see how the resistance is affected.

Soft and hard switching have been investigated in several papers to see what effect they play in the role of dynamic ON-state resistance. Li *et al.* [32] propose a circuit that can be switched between soft- and hard-switching modulation. They also perform the DPT and multiple pulse test. The tests are performed on several devices from different GaN manufacturers; one of the devices is from Panasonic and has an additional p-n junction. The results show that soft switching reduces the dynamic ON-state resistance except in the device with the additional p-n junction. A similar experiment is conducted in [44], where the tests show similar results. Soft switching reduces the level of dynamic ON-state resistance with the conclusion that additional trapping is taking place during hard switching. One criticism of the tests performed is the lack of consideration for the heating effect which will be different for hard and soft switching because of the different loss levels. The heating effect was assumed to be negligible during multipulse test. The underlying assumption was that the duration is small enough that heating would not take place. Contrary to this, research in [42] shows that even a very small amount of heating can create a noticeable temperature rise in a DPT. The inclusion of a dc test similar to [42] that gives the baseline for temperature rise would provide more conclusive evidence to the comparison between soft switching and hard switching.

When considering the test setups, one important distinction is the blocking time. This is the time the switch is in the OFF state while the operating high voltage is applied on it. Typically, this is not accounted and can drastically affect test results. Some tests have accommodated for the blocking time and created test setups that can vary this stress applied to the switch during the OFF state through the use of additional power switches. One such setup where they show that the longer the device is blocking, the higher the measured dynamic ON-state resistance [33].

Modeling dynamic $R_{d\mathrm{son}}$ poses a challenge as can be seen from the various works presented. The exact dynamics are heavily influenced by the manufacturing of the device and related to material defects. Thus, researchers who have attempted to model dynamic $R_{d\mathrm{son}}$ have first performed tests and measured the dynamic $R_{d\mathrm{son}}$. In [43], researchers attempt to model the effects of dynamic $R_{d\mathrm{son}}$ through the use of seven RC networks for a total of 28 parameters. The result is mediocre at best, with the author reporting it is between 17%. Another paper is presented by the same author and presents similar data and claims the model results in an average difference of 6% and a maximal difference of 23% [45]. However, the model is taking into account very large detrapping times which are not practical. Most converters using GaN will be operating at high frequencies so modeling the resistance after detrapping time that is on the scale of 1 ms is not useful in real applications.

B. V–I *Alignment*

V–I alignment is important when determining losses as the $E_{\mathrm{on}}/E_{\mathrm{off}}$ is determined by the overlapping area between the current and voltage. By shifting these signals, the overlapping area and thus the measured loss will change. Properly aligning the probes can greatly impact the measurement as even a small delay can have a large negative impact on the measured losses [46]. Fig. 22 shows how the current and voltage can be aligned to acquire the loss measurement. Typically, during the switching-ON transient, the *di/dt* and the stray inductance will cause a voltage drop on the V_{ds}. Therefore, the beginning and end of the *di/dt* shall be aligned with the V_{ds} voltage drop.

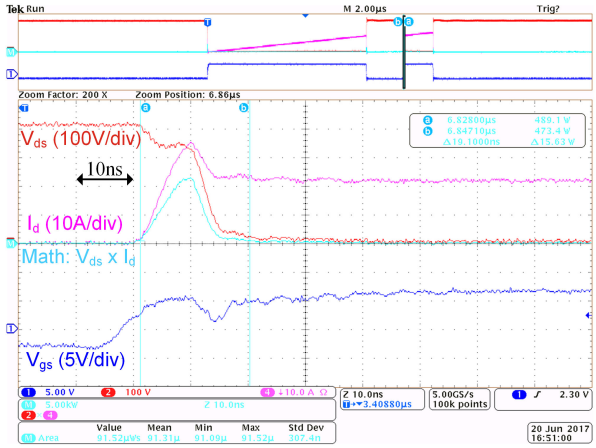

Fig. 22. *VI* alignment—E_{on} (teal), I_d (magenta), V_{ds} (red), and V_{gs} (blue).

There are three methods to deskewing probes discussed in [46]: 1) use of calibration fixture; 2) probe compensation output of scope; and 3) resistive load.

The steps for using the Tektronix calibration fixture can be found in [47]. The main drawback of this fixture is the requirement of the calibration fixture and the probe compatibility. This method is only compatible with Tektronix probes which are unsuitable for measuring high frequency transients of WBG devices due to their comparatively lower bandwidths (around 100 MHz) and unwanted added impedance.

Probe deskewing can be done without the fixture used in the first method. Utilizing the square-wave method, two probes can be connected to the probe compensation output of the scope. Each probe can be used to measure the same square wave, and then be adjusted using the deskew option such that they are aligned. For this method one probe is selected as the baseline and all other probes will be aligned with the chosen probe. This method is much more desirable as it does not have probe requirements or additional hardware [48].

The third method is suggested by Cree for their SiC double pulse tester. This method involves removing the freewheeling diode and replacing it with a low-inductance 100-Ω resistor. The load inductor is also removed. This method will allow the current and voltage probes to be aligned because the load is entirely resistive resulting in zero phase shift between the signals. In practice, there will exist a small delay due to tiny parasitics, but this delay should be negligible due to the total amount of impedance it contributes compared to the 100-Ω load [49].

C. Current/Voltage Probe Selection

When selecting voltage probes, designers have an option of passive or differential probes. Passive probes have much higher bandwidth and dynamic range when compared with differential

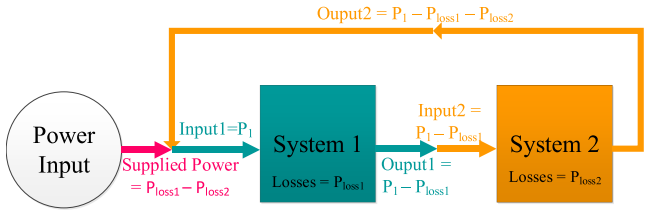

Fig. 23. Opposition method.

probes, but they suffer from capacitive loading of the circuit at high frequencies which makes them undesirable when measuring the fast transitions of GaN [50]. The capacitive load of the probes reduces the rise time of other signal points in the system.

When selecting a current probe, there are several popular options: coaxial shunt, split core probe current transformer, and Rogowski coil. Rogowski coil has the lowest bandwidth, making it unsuitable for DPT. It is reported in [51] that a Rogowski coil and amplifier is sufficient for measuring the current of GaN. However, this is not what is reported by Zhang *et al.* [46]. Among the three methods, the coaxial shunt has the highest bandwidth and provides the best accuracy. As with small die GaN devices, the small stray inductance from the probe could be a large portion of the total stray inductance in the power loop, thus making any measurements nonindicative of the actual switch performance.

D. Probe Grounding

When utilizing measurement devices, there are two more main concerns: probe lead inductance and common mode noise. Lead inductance results from using a long lead for the ground clip. This inductance is problematic, as it forms a resonant network with the input capacitance and can drastically alter measurements at high frequencies. The ideal solution is to use a spring clip for the probe tip, as the total loop length in much smaller when compared to the traditional alligator clip. However, active probes are immune to the introduction of lead inductance.

Common mode chokes can be employed to reduce the common mode noise that is capacitively coupled through the earth ground due to the copper foil layer of the power supply transformer. This noise can make measurements difficult but can be reduced via a common mode choke, which is a transformer connected between the positive and negative of the power supply. The common mode choke works by cancelling flux of differential signals which are desired in this configuration and the flux is added for any common mode signals. When the flux adds, it creates impedance that reduces the common mode current.

E. Opposition Method

The opposition method is a technique for determining losses in a converter. An in-depth explanation of the method as well as examples is presented in [52]. The opposition method requires two identical converters that can operate in the reverse direction. The converters are connected in such a fashion that there is no resistive load, with the power circulating between the two converters as in Fig. 23. This setup is useful for testing the power losses at full load and offers more accuracy than using a power analyzer for the input and output. However, it may not be feasible as it requires two identical converters. An alternative is to use a different converter, provided it is compatible rating wise and its losses are already known.

In [53], authors propose using the opposition method to nonintrusively measure the switching losses from GaN devices. This method makes use of two GaN half bridges with a load inductor connected between their switching nodes. The researchers apply the opposition method as it is described in [52] but vary the converter parameters to isolate various losses. Frequency-dependent losses can be identified by varying the switching frequency, while the turn-ON losses can be removed from the system with a purely ac through the inductor. One important note is that the inductor losses are minimized. To achieve this minimization, the researchers used two different inductors for the various tests such that they could minimize the conduction losses for one test and ac for another. This test looks promising for measuring GaN losses and provides significant advantages over the DPT in terms of being nonintrusive. Another advantage of this method is that state of the art probes are not required to measure fast transitions. The disadvantage of this test is the requirement of two inductors for minimizing losses in addition to temperature being an uncontrolled variable.

F. Calorimetric

One method to determine losses is to use a calorimeter to measure the total change in heat of the system via the air temperature. Typically, traditional calorimeters require several hours to reach thermal balance, which is not practical. The proposed method in [54] utilizes the converter itself as the calorimetric chamber which can reach thermal equilibrium more quickly. This is because the converter has a lower thermal capacitance compared to a calorimetric chamber. One drawback of this method is the inability to separate out the individual losses. The authors also cite that the method cannot measure the losses in the passive components but for the consideration of GaN losses this is irrelevant. However, similar to the opposition method presented in Section V-E, it may be possible to separate out losses with multiple tests by varying the switching frequency and load type.

G. Water Flow Exchanger

Similar to the calorimetric approach, this method is concerned with the change in temperature to determine the losses. The inlet temperature is compared against the outlet temperature to determine how much heat was injected into the coolant path. This method is applied in [55] in conjunction with the opposition method to determine the exact contributions of the loss. It should be noted that at low power the temperature difference may be extremely small; thus, this method is largely suited to higher power testing.

VI. Conclusion

Loss mechanisms for GaN power devices have been presented and loss measurement techniques were summarized. GaN is a promising technology, with very low switching and conduction losses. However, there are some uncertainties existing on some

factors contributing to small portion losses, such as the dynamic $R_{d\mathrm{son}}$. Manufacturers will need to work to improve these areas and to provide this information to engineers as currently modeling this behavior is difficult due to between-device variation. Measurement equipment also needs some improvements as the bandwidth, stray capacitance, and inductance introduce significant errors when performing a standard test, such as the DPT. Thus, improvements are needed to keep up with demands of new GaN technology.

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