Output Impedance Modeling and High-Frequency Impedance Shaping Method for Distributed Bidirectional DC–DC Converters in DC Microgrids

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***Abstract*—Output impedance characteristics of interfaced converters of energy sources are the important indicators to assess the anti-interference ability of the dc microgrids. However, the output impedance is often approximately modeled by neglecting the impacts of delay units. In order to accurately study the anti-interference ability, the output impedance of an energy storage system is modeled with the consideration of the coupling characteristics of the current control gains and the delays caused by digital control and switching. The constraint mechanism of the coupling factors to impact the effective bandwidth of current loop in a load current feedforward system is also revealed. Then, an impedance shaping method is proposed to improve the anti-interference ability by optimally shaping the high-frequency output impedance, and also to improve system performances in terms of increasing the bandwidth of inner loop and the stable margin of outer loop. The simulation and experimental results both clearly validate the correctness and feasibility of the proposed impedance shaping method.**

***Index Terms*—Bidirectional converter, current feedforward, dc microgrid (MG), output impedance optimization.**

I. Introduction

IN THE recent decades, microgrid (MG) technology is a continuously hot topic due to the dramatical development of the renewable generations. The photovoltaic (PV) storage-based dc MG is a typical dc MG scenario, as shown in Fig. 1. The interfaced converters of PV and storage system generally have different electrical and control parameters, leading to unexpected interaction among the converters and also resonant issues. On the other hand, the stable operation of the dc MG is challenged by the intermittent behavior of PV and the random operation of the loads. Impedance-based methods are often used to analyze such complex systems, and the criterions, e.g., Middlebrook impedance criterion [1] and its derived criterions [2], [3], provide specific index criteria to assess system stability. Based on a precise impedance model, the stable margin of the over system can be correctly shown by these criterions.

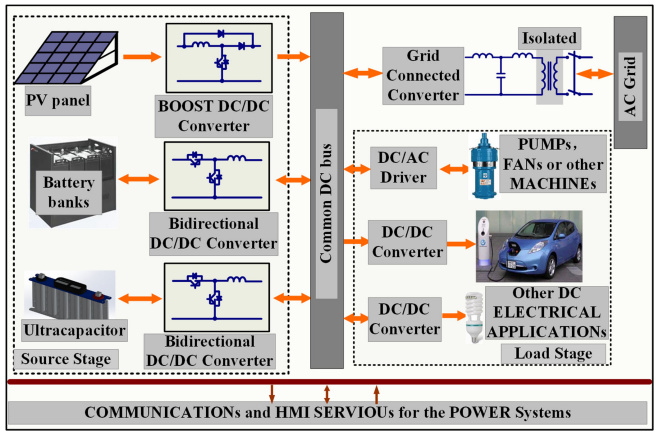

Fig. 1. Typical structure of PV-storage based dc MG.

The interfaced converter in the dc MG can be roughly classified into a source-stage converter (SSC) and a load-stage converter (LSC) [4]. Dependent on the operation and control mode of renewable sources, when controlled as current sources, the output impedance will be modeled as a Norton equivalent circuit and in contrast when controlled as voltage source, the output impedance is modeled as a Thevenin equivalent circuit. In comparison, the Norton equivalent circuits cannot control the dc MG voltage directly [5], while the Thevenin equivalent circuit can establish the dc-bus voltage, reducing the complexity of the stability analysis [6].

In order to meet the requirements of plug-and-play and distributed control, the energy-storage-system (ESS) usually adopts a droop control, where the equivalent output impedance usually has a linear behavior such as a virtual resistor (VR) for the

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steady-state power sharing [4]–[7]. In addition, in order to obtain different time scale of power sharing for ESS [8], the droop control has been extended from the conventional VR to proportional, derivative, and integral droops in [9]–[11], where the output impedance of each droop had been analyzed. However, the delay caused by digital control, sampling and switching is not considered in those modeling approaches, leading to that these models are only effective in low-frequency energy management analysis, but not applicable to analyze the higher frequency behavior [6], [7], [12]. Moreover, these models can not reflect the equivalent circuit structure characteristics of different controllers.

For LSCs, the tightly regulated point-of-load converters behave as a constant power load (CPL) [4], [6], [13]–[25], resulting in negative incremental impedances in the dc MG. Therefore, the operation of CPLs with a large proportional gain will degrade the system stabile margin, which may cause unacceptable dc MG voltage oscillation or collapse. In order to change the CPL characteristic, the impedance shaping methods are implemented, which can improve the dc MG system stable margin and suppress the common dc-bus voltage oscillation [13]–[25]. Various virtual impedance approaches, e.g., VR [14]–[16] or virtual capacitor [11], [17], [18], are implemented inside the LSC to shape the CPLs' input impedances, but result in the harsh compromise between the system stable margin and the load performance.

To overcome aforementioned defects, various output impedance shaping techniques were developed in the SSC [19]–[24] instead of LSCs. A VR connected in series with the output of the SSC to compensate the CPLs' negative resistance was proposed in [19]–[20], and a frequency-dependent virtual impedance to shape the SSCs' output impedance in the selected frequency range was proposed in [21]. However, aforementioned methods may lead to poor regulation capability of the dc MG voltage under heavy load changes. To improve the voltage regulation capability, a frequency-dependent virtual impedance comprising of a parallel RL branch was proposed in [22]. Furthermore, the load current feed-forward scheme is often implemented, because it is an effective method to achieve better dynamic performance during load transient [12], [19], [23], [24], and the output impedance structure with load current feedforward was presented in [24]. However, the inner current-loop controller and digital delay significantly limit the bandwidth of the impedance shaping approaches, rarely discussed so far.

The main contribution of this article includes the following three points.

1) A precise impedance model including the delay of SSC system is constructed. The control structure and parameters as well as distributed source characteristics are all involved in the model. This model accurately reveals the effect of controller structure and parameters on the system high frequency (HF) equivalent impedance characteristics.
2) By improving the inner current controller, an impedance shaping method is proposed to shape the HF characteristics of the ESS equivalent output impedance.
3) The proposed method also increases the current-loop bandwidth and improves the load current feedforward control performance. Thereby, the system voltage loop stability margin is improved, and the value range of VR is expanded as well.

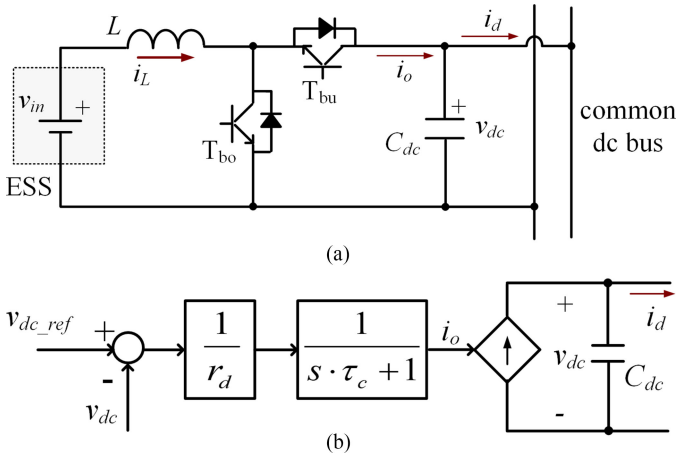

Fig. 2. Traditional bidirectional dc–dc topology based ESS branch and its droop-based control scheme. (a) Traditional bidirectional dc–dc topology. (b) Droop-based control scheme.

This article is organized as follows. In Section II, the equivalent output impedance of ESS is modeled and studied. In Section III, the system equivalent output impedance is reconstructed and analyzed based on the load current feedforward. In Section IV, an impedance shaping method is proposed and analyzed. Experimental results, which verify the effectiveness of the proposed method, are shown in Section V. Finally, Section VI concludes this article.

II. Impedance Model Analysis for ESS Branch Under Traditional Control

A. Conventional Control Structure of a Bidirectional DC–DC Converter in ESS

The detailed topology of the traditional bidirectional dc–dc converter in Fig. 1 is shown in Fig. 2(a), where ESS is connected to the common dc bus; $v_{\rm in}$ and $v_{\rm dc}$ are the ESS terminal voltage and the common dc-bus voltage, respectively; T_{bo} and T_{bu} are the power switches, which are driven in complementary mode to ensure the inductor current continuity; i_d is the load current; i_o is the output current to the dc capacitor; and i_L is the inductor current. By presenting their average values in a unit switching period as $\langle i_o \rangle$ and $\langle i_L \rangle$, the linear relationship can be expressed as

$$\langle i_o \rangle = (v_{\rm in}/v_{\rm dc}) \langle i_L \rangle . \tag{1}$$

VR often exhibits a proportional behavior when focus on dynamic power flow regulation, which can be placed in the voltage controller [8], [9]. And the droop control loop with a droop resistance r_d can be derived as shown in Fig. 2(b) [7], [8], where the given dc-bus voltage reference is $v_{\rm dc\_ref}$. Owning to i_L has better continuity, i_L is always used to replace i_o as the inner-loop control variable. The inner loop can be simplified as a first-order system with the time constant τ_c. Such control

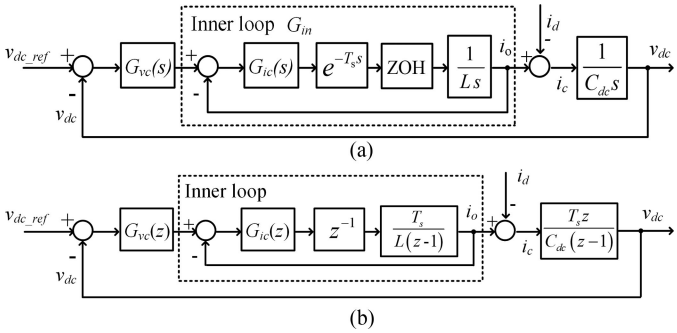

Fig. 3. Typical control block diagram for the ESS branch. (a) *s*-domain control structure. (b) *z*-domain control structure.

structure is derived without considering the delay, leading to that the real converter equivalent impedance is different from the desired impedance.

To consider the effects of delay, the typical control structure of the ESS branch in *s*-domain is reconfigured as shown in Fig. 3(a). The control period is consistent with the switching period T_s, the digital control delay is e^{-Tss}, and the switching delay can be equivalent as $e^{-0.5\ Tss}$ or a zero-order holder [25]. $G_{vc}(s)$ and $G_{ic}(s)$ are the voltage and current-loop controller, respectively.

Based on the *s*-domain model, the *z*-domain model of the system can be obtained as shown in Fig. 3(b). In order to increase the system operating bandwidth, the inner loop usually adopts proportional (P) control or state feedback control. When P control is used with the parameter k_{pi}, the current open-loop transfer function is obtained as

$$G_{\text{in\_op}}(z) = \frac{k_{pi} \cdot T_s}{L \cdot (z^2 - z)} = \frac{\beta}{z^2 - z} \tag{2}$$

where $\beta = (k_{pi}T_s)/L$ is the standardization coefficient of the inner-loop gain. In addition, β can also characterize the inner-loop time constant τ_c, and their relationship can be expressed as (3) without considering the delay

$$\tau_c = \frac{T_s}{\beta}. \tag{3}$$

Thereby, the closed-loop transfer function of the current loop is

$$G_{\text{in}}(z) = \frac{G_{\text{in\_op}}(z)}{1 + G_{\text{in\_}op}(z)} = \frac{\beta}{z^2 - z + \beta}. \tag{4}$$

Based on the well-known Jury's criterion, the necessary and sufficient conditions for the stability of the current loop can be derived as (5). Based on (5), it can be derived the value range of β is (0, 1) in order to stabilize the inner loop

$$\begin{cases} \Delta_{\text{in}}(z) = z^2 - z + \beta \\ 1.\ \Delta_{\text{in}}(1) = \beta > 0 \\ 2.\ (-1)^2 \Delta_{\text{in}}(-1) = 2 + \beta > 0 \\ 3.\ |\beta| < 1. \end{cases} \tag{5}$$

Owing to that the droop control is implemented to match the distributed source electrical capacity, it often shows the P control characteristics as shown in Fig. 2(b), where the droop resistance

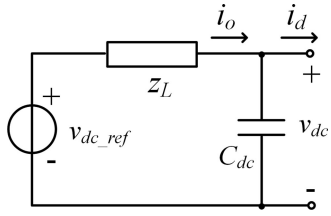

Fig. 4. Equivalent circuit model of the bidirectional converter system.

is embodied in the equivalent circuit structure. Assuming that k_{pv} is the P parameter, the voltage controller is

$$G_{\text{vc}}(z) = k_{\text{pv}} = \frac{1}{r_d}. \tag{6}$$

It shows the physical relationship between the droop resistance and the voltage-loop controller in (6).

B. Impedance Model of ESS Branch Under Traditional Control

According to Fig. 3, the system equivalent circuit model can be obtained, as shown in Fig. 4. z_L is the equivalent output impedance, which is

$$z_L(z) = r_d G_{\text{in}}{}^{-1}(z). \tag{7}$$

The system equivalent output impedance z_o can be expressed as (8), where z_{c_dc} is the impedance of capacitor C_{dc}. It can be seen that when the source and C_{dc} value are constant, the output impedance z_o is determined by the inner current-loop characteristic

$$z_o(z) = \frac{z_L \cdot z_{c\_\text{dc}}}{z_L + z_{c\_\text{dc}}}. \tag{8}$$

Fig. 5(a) shows the *s*-domain characteristics of z_L. It shows that the phase curve always intersects with –180° at $f_s/6$ ($f_s = 1/T_s$), and z_L exhibits negative impedance near this frequency domain. By increasing β from 0.3 to 0.5 and then to 0.8, the resistive band of z_L becomes wider, but its negative impedance characteristics are more severe. As shown in Fig. 5(a), with the increasing frequency bands, the impedance model error without considering delay effect increases, so that the negative impedance characteristics do not occur. From the analysis of (5), when β is larger than one, the current loop is unstable. In addition, the voltage closed-loop transfer function $G_{\text{Loop}}(z)$ is

$$G_{\text{Loop}}(z) = \frac{\alpha \cdot \beta \cdot z}{z^3 - 2z^2 + (1 + \beta + \alpha \cdot \beta) \cdot z - \beta} \tag{9}$$

where $\alpha = (k_{\text{pv}}T_s)/C_{\text{dc}}$ is the standardization coefficient of the outer-loop gain.

Thus, v_{dc} can be obtained from the control block diagram in Fig. 3 and the equivalent circuit in Fig. 4

$$v_{\text{dc}} = G_{\text{Loop}}(z) \cdot v_{\text{dc\_ref}} + z_o(z) \cdot (-i_d). \tag{10}$$

According to the aforementioned definition, α and β are written as

$$\alpha = k_{\text{pv}}T_s/C_{\text{dc}}, \text{and } \beta = k_{pi}T/L. \tag{11}$$

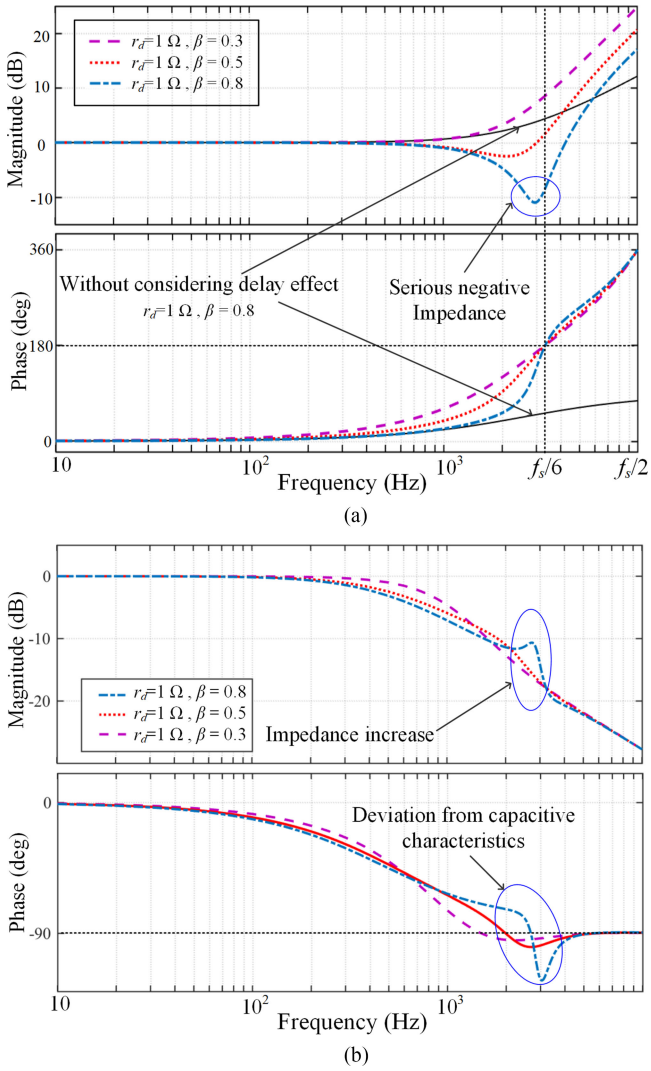

Fig. 5. Characteristics analysis of Gin coupled impedance under traditional control. (a) z_L characteristics ($\alpha = 0.128$, $T_s = 50$ μS). (b) z_o characteristics ($\alpha = 0.128$, $T_s = 50$ μS).

It standardizes the outer-loop gain $k_{\rm pv}$ and inner-loop gain k_{pi}, respectively. The larger value ranges of them indicate the larger stable margin, and the larger value of them means the better dynamic performances. However, their value ranges are limited by the system stability conditions, which can be also obtained from Jury's criterion. Accordingly, (12) shows necessary and sufficient conditions for the stable operation of $G_{\rm loop}(z)$

$$\begin{cases} \Delta_{\rm Loop}(z) = z^3 - 2z^2 + (1+\beta+\alpha\cdot\beta)\cdot z - \beta \\ 1.\ \Delta_{\rm Loop}(1) = \alpha\cdot\beta > 0 \\ 2.\ (-1)^3\Delta_{\rm Loop}(-1) = 4 + 2\beta + \alpha\cdot\beta > 0 \\ 3.\ |\beta| < 1, \text{and } \left|1-\beta^2\right| > |1+\alpha\cdot\beta-\beta|. \end{cases} \tag{12}$$

From (12), it is deduced that α and β must follow the relationship shown in (13). Combining (11) and (13), (14) can be obtained, which shows the mutually restrictive relationship between k_{pi} and $k_{\rm pv}$, i.e., the larger value of k_{pi}, the smaller value range of $k_{\rm pv}$

$$0 < \alpha < 1-\beta, \text{and } 0 < \beta < 1 \tag{13}$$

$$k_{pi} < \left(1 - k_{\rm pv}\cdot\frac{T_s}{C_{\rm dc}}\right)\cdot\frac{L}{T_s}. \tag{14}$$

Based on this constraint, the s-domain characteristics of z_o derived from (7) are shown in Fig. 5(b). With the increase of β, the amplitude of z_o decreases in a certain frequency range, which is beneficial to the anti-interference capability of the system to some extent, as shown in Fig. 5. However, when β is close to the critical value, the negative impedance characteristic of z_L causes the amplitude of z_o increase, and also results in z_o deviating from its capacitive characteristic near this frequency domain, thereby reducing the HF anti-disturbance capability of the system. Thus, there is also a mutual constraint relationship between the inner-loop response speed τ_c and the droop coefficient r_d by the same reason.

In [26], a critical frequency, at which the phase of the forward-path transfer function crosses –180° downward, is used to distinguish the high- and low-frequency resonance. Similar to [26], the frequency higher than the critical frequency is called as HF region in this article. Moreover, due to the limit of the control frequency, the upper limit of the higher frequency region is half of the control frequency, $f_s/2$. Based on the system control diagram, as shown in Fig. 3(b), the bode diagrams of the system open-loop transfer function with different parameters can be drawn in Fig. 6. The impacts of β and r_d on the critical frequency are shown in Fig. 6(a) and (b), respectively. With the increase of β, the critical frequency is increased as well, while r_d does not change the critical frequency. Considering the tolerances of system parameters, the minimum value of $\beta = 0.2$ is used to define the critical frequency. When $\beta = 0.2$, the critical frequency of the system is about 1 kHz. Thus, the high-frequency region is within the range from 1 kHz to $f_s/2$.

III. Impedance Model Analysis for ESS Branch With Load Current Feedforward Control

A. Construction of System Impedance With Feedforward Control

In order to improve the antidisturbance performance of the system, the disturbance current feedforward control is often introduced [12], [19], [23], [24], as shown in Fig. 7(a). i_d is fed forward into the current reference through the feedforward channel transfer function G_f in order to suppress the influence of the disturbance current on the voltage. This structure can be physically equivalent as two parts, as shown by the equivalent structure model I (dotted line) in the Fig. 7(a), where i_o and i_c are fed forward to the current inner loop by G_f, respectively.

The feedforward current of i_c can be evolved into $v_{\rm dc}$ feedforward based on the capacitive reactance relationship between i_c and $v_{\rm dc}$. In which, the feedforward loop of i_o and the inner current loop are regarded as a whole transfer function $G_{\rm inf}$

$$G_{\rm inf} = \frac{G_{\rm in}}{1 - G_f\cdot G_{\rm in}}. \tag{15}$$

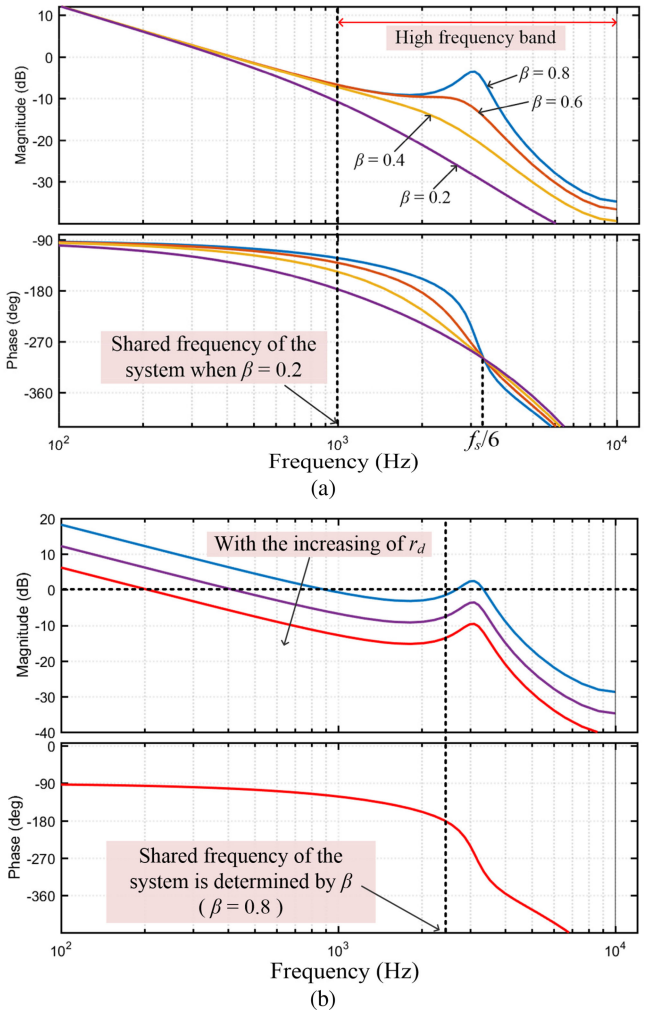

Fig. 6. Bode diagrams of system open-loop transfer function with (a) different values of β and (b) different values of r_d.

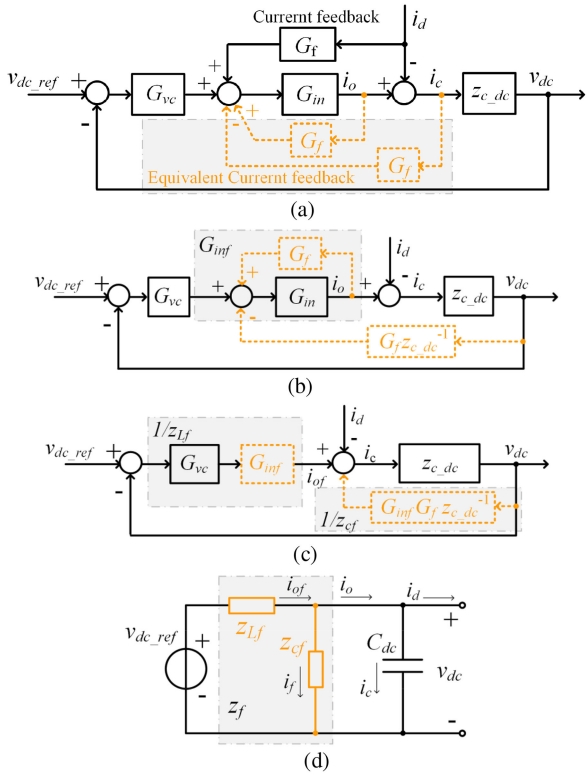

Fig. 7. Evolution of control block diagram and equivalent circuit structure diagram under current feedforward control. (a) Control structure under disturbance current feedforward control and its equivalent model structure I. (b) System's equivalent model structure II. (c) System's equivalent model structure III. (d) Equivalent circuit model with current feedforward control.

Based on the abovementioned analysis, the control structure can be further evolved as shown in Fig. 7(c). From the evolved control structure, an equivalent impedance z_{Lf} is constructed by G_{vc} and $G_{\rm inf}$, which is connected in series between the voltage source $v_{\rm dc\_ref}$ and $C_{\rm dc}$. Meanwhile, an equivalent impedance z_{cf} is constructed, which is connected in parallel with $C_{\rm dc}$. Therefore, the equivalent circuit structure is derived, as shown in Fig. 7(d). In which, both z_{Lf} and z_{cf} determine the system impedance characteristics, and they can be, respectively, expressed as

$$z_{Lf} = {G_{vc}}^{-1} \cdot {G_{\rm inf}}^{-1} \tag{16}$$

$$z_{cf} = {G_{\rm inf}}^{-1} \cdot {G_f}^{-1} \cdot z_{\rm c\_dc}. \tag{17}$$

B. Impedance Analysis for ESS Branch With Feedforward of i_d

Obviously, due to the effect of disturbance current feedforward, the system output impedance z_{of} is formed by $z_{\rm c\_dc}$ and z_f in parallel, where z_f depends on the characteristics of the digital controller, and z_f and z_{of} are, respectively, described as

$$z_f = z_{Lf} \parallel z_{cf} = \frac{z_{Lf} \cdot z_{Cf}}{z_{Lf} + z_{Cf}} = \left({G_{\rm in}}^{-1} - G_f\right) \cdot \frac{r_d \cdot z_{\rm c\_dc}}{r_d \cdot G_f + z_{\rm c\_dc}} \tag{18}$$

$$z_{of} = z_f \parallel z_{\rm c\_dc} = \frac{z_f \cdot z_{\rm c\_dc}}{z_f + z_{\rm c\_dc}} = (1 - G_f G_{\rm in})\, z_o. \tag{19}$$

Combining (9) and (16)–(19), (20) can be obtained

$$\frac{(z_{\rm c\_dc} \parallel z_{Cf})}{z_{Lf} + (z_{\rm c\_dc} \parallel z_{Cf})} = G_{\rm Loop}. \tag{20}$$

The expressions of (9) and (20) are essentially the same, and $G_{\rm Loop}(z)$ is the instruction tracking transfer function. Therefore, the current feedforward does not change the system forward channel closed-loop transfer function.

The s-domain shapes of z_f and z_L are compared, as shown in Fig. 8(a). When unit feedforward control, $G_f = 1$, is used, the amplitude of z_f is significantly reduced over the entire frequency range, and in particular, a strong antidisturbance capability is obtained in the low-frequency range. However, this reduction of impedance amplitude in the low-frequency range leads to the system loss of droop function. Since distributed power supplies

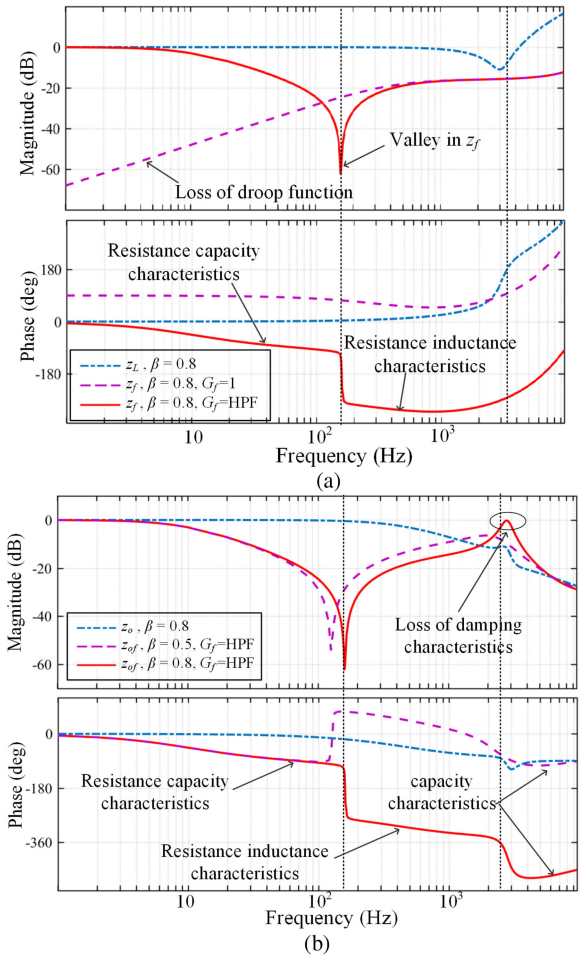

Fig. 8. Characteristics analysis of the system equivalent impedance under disturbance current feedforward control. (a) z_f characteristics ($\alpha = 0.128$, $T_s = 50\ \mu$S). (b) z_{of} characteristics ($\alpha = 0.128$, $T_s = 50\ \mu$S).

are usually connected in parallel with capacitive materials, especially supercapacitors, which have capacitive characteristics and have good HF energy absorption capability, the high-pass filter (HPF) is usually introduced into G_f to improve the HF antidisturbance capability of the system meanwhile ensuring the low-frequency energy management quality. G_f is expressed as

$$G_f(z) = \text{HPF} = \frac{1 - z^{-1}}{1 - \xi z^{-1}} \tag{21}$$

where $\xi \approx \frac{2-2\pi f_{cu} T_s}{2+2\pi f_{cu} T_s}$ is the high-pass filter coefficient, and f_{cu} is the corresponding cutoff frequency.

The s-domain shape of z_f with HPF is also seen in Fig. 8(a). There is a resonant valley in the amplitude-frequency curve of z_f, and it is also known from the analysis of (18) that the valley frequency is determined by the values of f_{cu} and k_{pi}. The amplitude of z_f in the medium- and high-frequency ranges is generally lower than the amplitude of z_L. Before the valley frequency, z_f exhibits resistance-capacitance characteristics, and after the resonant valley frequency, z_f exhibits resistance inductance.

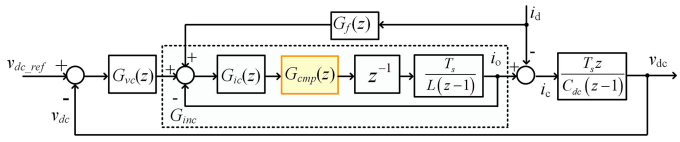

Fig. 9. Inner current control diagram with the proposed method.

The frequency characteristic of the system output impedance z_{of} is shown in Fig. 8(b). It can be known from (18) and (19) that a valley in the frequency characteristics of z_{of} is caused by the pole in the frequency domain of z_f, as shown in (18). In addition, based on (9) and (20), the feedforward control will not affect the transfer function of forward-path, and thus, does not affect its stability. The system has optimal antidisturbance characteristics at the valley frequency of z_{of}. According to the main disturbance band in the system, the frequency band in which the valley is located can be determined, thereby improving the antidisturbance capability of the system. Therefore, when the inner-loop control gain is fixed, the frequency domain model of z_f can be obtained by (18), and the valley of z_f is placed close to the main disturbance band by tuning f_{cu}. As shown in Fig. 8(a), a high-pass filter with $f_{cu} = 20$ Hz is used to place the valley close to 150 Hz, and thus, the system has better antidisturbance capability at 150 Hz disturbances.

Due to the feedforward, the overall output impedance of the system is significantly improved in a wide-frequency range, and appropriately increasing the inner-loop gain (β changes from 0.5 to 0.8) will increase the response bandwidth of the feedforward-based control. However, this will aggravate the HF negative impedance of z_f, which in turn results in the amplitude of z_{of} significantly higher than that of z_o in the HF range, and even damages the system HF damping characteristics.

As a result, excessive pursuit of the inner-loop response speed will affect the system equivalent output impedance. In addition, the system parameters variation, especially inductance variation, directly affects the value of β, which may reduce the system stability margin according to (13) and (14). In order to suppress this effect, enhance the system's antidisturbance capability and improve impedance characteristics, an HF output impedance shaping method for ESS is proposed in the following section.

IV. Proposed Output Impedance HF Shaping Method

Generally, the inner-loop dynamic response ability determines the bandwidth of the system, so it is an effective way to improve the system equivalent impedance characteristics by improving the inner-loop performance. This article proposes an HF output impedance shaping method (HF shaping method) for the SSC, as shown in Fig. 9, $G_{\text{cmp}}(z)$ expressed as (22) is connected into the inner current loop, aiming to improve the response characteristics of the disturbance current feedforward control at the HF range

$$G_{\text{cmp}}(z) = \frac{1 + \delta}{(1 + \delta z^{-1})}. \tag{22}$$

A. Current-Loop Characteristics With HF Shaping Method

In the proposed control, the open-loop and closed-loop transfer function of inner current loop, $G_{\mathrm{inc\_op}}(z)$ and $G_{\mathrm{inc}}(z)$, are expressed, respectively

$$G_{\mathrm{inc\_op}}(z) = G_{ic}(z)\cdot G_{\mathrm{cmp}}(z)\cdot \frac{T_s}{L}\frac{1}{z(z-1)} = \frac{\beta(1+\delta)}{z^2+(\delta-1)z-\delta} \tag{23}$$

$$G_{\mathrm{inc}}(z) = \frac{G_{\mathrm{inc\_op}}(z)}{1+G_{\mathrm{inc\_op}}(z)} = \frac{\beta(1+\delta)}{z^2+(\delta-1)z+(\beta+\beta\delta-\delta)}. \tag{24}$$

Jury' criterion is also used to evaluate the constraints for the stability of $G_{\mathrm{inc}}(z)$, and the inequality group shown in the following equation is deduced:

$$\begin{cases} \Delta_{\mathrm{inc}}(1) = z^2+(\delta-1)z+(\beta+\beta\delta-\delta) \\ 1.\ \Delta_{\mathrm{inc}}(1) = \beta(\delta+1) > 0 \\ 2.\ (-1)^2\Delta_{\mathrm{in}}(-1) = 2(1-\delta)+\beta(1+\delta) > 0 \\ 3.\ |\beta(1+\delta)-\delta| < 1. \end{cases} \tag{25}$$

The following equation is derived from (25):

$$0 < \beta < 1. \tag{26}$$

Based on (23) and (24), the root locus of the proposed control is shown in Fig. 10(a). It shows the effect of the proposed transfer function, $G_{\mathrm{cmp}}(z)$, on the inner current loop. Since the inner-loop gain $k_{pi} = \beta\cdot L/T_s$ and the starting point of the root locus is the system open-loop poles, with the increasing of β, the poles gradually move outward from the unit circle. When $G_{\mathrm{cmp}}(z)$ is not implemented, it can be seen that the root locus of the closed-loop transfer function of current, $G_{\mathrm{in}}(z)$, intersects the unit circle at $f_s/6$ when $\beta = 1$, which means that the allowable range of β is (0, 1), and it is consistent with the previous analysis in (5). Furthermore, the open-loop poles locate at the positive real axis when β (proportional to k_{pi}) is small, the current-loop exhibits monotonic convergence.

After the implementation of $G_{\mathrm{cmp}}(z)$ and with the increasing of δ from 0 to 1, it can be seen that the root locus of $G_{\mathrm{inc}}(z)$ gradually shifts to the left, and it intersects with the unit circle at $f_s/4$ when $\beta = 1$ and $\delta = 1$. It can be seen from (26) and Fig. 9(a) that the current gain margin is not enlarged, but the inner-loop bandwidth is expanded owing to that the left shift of the root locus. However, a root trajectory curve starts from negative real axis, especially when $\delta = 1$, one open-loop pole locates at (–1, 0), which means that the smaller the gain, the closer the pole is to –1. When the negative pole occurs, it is known that the current is prone to oscillate at $f_s/2$ under dynamic conditions.

In order to reduce the influence caused by such negative real-axis pole, the value of δ is provided as (27), which establishes a functional link between δ and β, and k_c is the operating

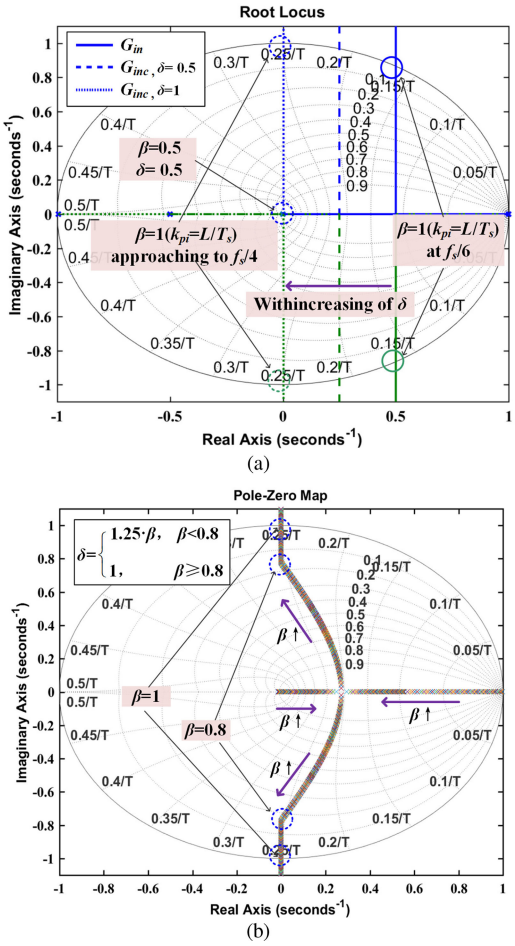

Fig. 10. Root trajectory analysis diagram with HF shaping method. (a) Root trajectory comparison analysis of inner current loop. (b) Current closed-loop poles distribution characteristics with proposed HF shaping method.

coefficient

$$\delta = \begin{cases} k_c\cdot\beta, & k_c\cdot\beta < 1 \\ 1, & k_c\cdot\beta \geq 1. \end{cases} \tag{27}$$

It unifies the characteristics of control gain and bandwidth in (27), showing that δ is determined by k_c and β. There are two objectives to select the value of δ. First, the inner-loop root locus should be shifted to the left in order to expand the bandwidth. Second, it is necessary to prevent the poles on the left-hand plane moving out the unit circle. Based on (26) and (28), the range of k_c can be obtained as [1] and [2]

$$k_c = \begin{cases} 1/\beta, & \beta \geq 0.5 \\ 2, & \beta < 0.5. \end{cases} \tag{28}$$

When $k_c = 1.25$, Fig. 10(b) shows the trajectory of the current closed-loop poles with the increasing of β. It is seen from Fig. 10(b) that the negative real-axis pole characteristics at low gain are greatly weakened, and the root locus is still near imaginary axis with the increasing of β. After $\beta \geq 0.8$, $\delta = 1$, the root locus moves along the imaginary axis, and it also intersects

with the unit circle at $f_s/4$ when $\beta = 1$. Apparently, by adjusting k_c, the tendency of the root trajectory moving to the imaginary axis can be changed. Therefore, compared with the conventional control method, the proposed method expands the control bandwidth of the current loop, but does not improve the gain margin of the current loop.

B. Voltage-Loop Characteristics With HF Shaping Method

In the proposed control, the open-loop and closed-loop transfer functions of the outer voltage loop are computed as, (29) and (30) shown at the bottom of this page.

The eigen polynomial of (30) is

$$\Delta_{\text{outc}}(z) = a3 \cdot z^3 + a2 \cdot z^2 + a1 \cdot z + a0 \tag{31}$$

where

$$\begin{cases} a0 = \delta - \beta(1+\delta) \\ a1 = \beta(1+\alpha)(1+\delta) - 2\delta + 1 \\ a2 = \delta - 2 \\ a3 = 1. \end{cases} \tag{32}$$

Combing Jury's criterion with (31), the sufficient and necessary conditions for system stability is

$$\begin{cases} 1.\ \Delta_{\text{outc}}(1) = \beta(1+\delta) > 0 \\ 2.\ (-1)^3 \Delta_{\text{outc}}(-1) = \beta(\alpha+2)(1+\delta) + 4(1-\delta) > 0 \\ 3.\ |a0| < |a3|, |b0| > |b2| \end{cases} \tag{33}$$

where

$$b0 = a0 \cdot a0 - a3 \cdot a3, b1 = a0 \cdot a2 - a3 \cdot a1. \tag{34}$$

The stability conditions in (33) are sequentially derived as follows. It can be known from (27) that $1 \geq \delta \geq 0$. Based on the first inequation in (33), the following equation can be derived as follows:

$$\left.\begin{array}{l} 1 \geq \delta \geq 0 \\ \Delta_{\text{outc}}(1) = \beta(1+\delta) > 0 \end{array}\right\} \Rightarrow \beta > 0. \tag{35}$$

Similarly, from the second inequation in (33), the following equation can be derived:

$$\left.\begin{array}{l} (-1)^3 \Delta_{\text{outc}}(-1) > 0 \\ 1 \geq \delta \geq 0 \end{array}\right\} \Rightarrow \beta(\alpha+2) > 0. \tag{36}$$

From $|a0| < |a3|$ as shown in the third inequation in (33), the following equation can be derived:

$$\left.\begin{array}{l} |a0| = |\delta - \beta(1+\delta)| \\ |a3| = 1 \\ |a0| < |a3| \end{array}\right\} \Rightarrow 1 > \beta > 0. \tag{37}$$

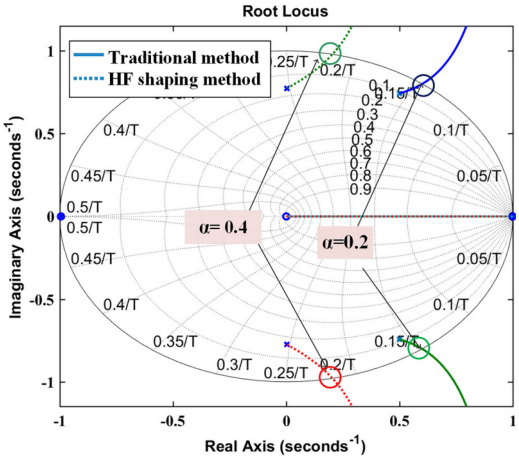

Fig. 11. Root trajectory comparison analysis of outer voltage loop.

Furthermore, from (34), the following equation can be derived:

$$\begin{cases} b0 < 0, b2 < 0 \\ |b0| = 1 - [\delta - \beta(1+\delta)]^2 \\ |b2| = 1 - \delta^2 - \beta(1+\delta)(1-\delta-\alpha). \end{cases} \tag{38}$$

Accordingly, $|b0| < |b2|$ as shown in the third inequation in (33), the following equation can be derived:

$$\left.\begin{array}{l} |b0| > |b2| \\ |b0| = 1 - [\delta - \beta(1+\delta)]^2 \\ |b2| = 1 - \delta^2 - \beta(1+\delta)(1-\delta-\alpha) \end{array}\right\} \Rightarrow \beta + \frac{\alpha}{1+\delta} < 1. \tag{39}$$

Combining (35)–(37) and (39), the necessary constraints for system stability is

$$\beta + \frac{\alpha}{1+\delta} < 1, \text{ and } 0 < \beta < 1. \tag{40}$$

By comparing (13) with (40), it can be seen that the proposed HF shaping method can increase the value range of α while it does not affect the value range of β. Therefore, the controller has significantly improved the adaptability of C_{dc}, but the adaptability of L does not change. In comparison, since L in each converter is relatively fixed when operating within the rated power, its parameters generally do not vary in a wide range and, thus, it does not have a serious impact on the system stable operation.

Under the conventional control method, when the larger inner control gain is used ($\beta = 0.8$), it is known from (13) that the allowable range of α is (0, 0.2), as shown in Fig. 11 that the root locus of the traditional method intersects with the unit circle when $\alpha = 0.2$. After the implementation of $G_{\text{cmp}}(z)$, $k_c = 1.25$,

$$G_{\text{outc\_op}}(z) = G_{vc}(z) \cdot G_{\text{inc}}(z) \cdot \frac{T_s}{C_{\text{dc}}} \frac{z}{z-1} = \frac{\alpha\beta(1+\delta)z}{z^3 + (\delta-2)z^2 + [\beta(1+\delta) - 2\delta + 1]z + [\delta - \beta(1+\delta)]} \tag{29}$$

$$G_{\text{outc}}(z) = \frac{G_{\text{outc\_open}}(z)}{1 + G_{i\text{outc\_open}}(z)} = \frac{\alpha\beta(1+\delta)z}{z^3 + (\delta-2)z^2 + [\beta(1+\alpha)(1+\delta) - 2\delta + 1]z + [\delta - \beta(1+\delta)]} \tag{30}$$

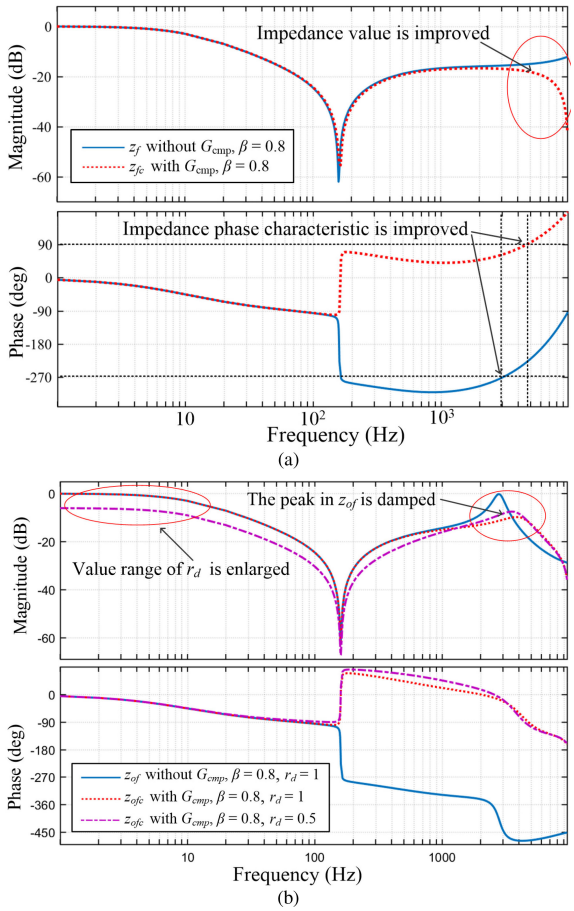

Fig. 12. Frequency domain characteristics analysis of system output impedance with proposed method. (a) z_f characteristics ($\alpha = 0.128$, $T_s = 50\ \mu$S). (b) z_{of} characteristics (Ts $= 50\ \mu$S).

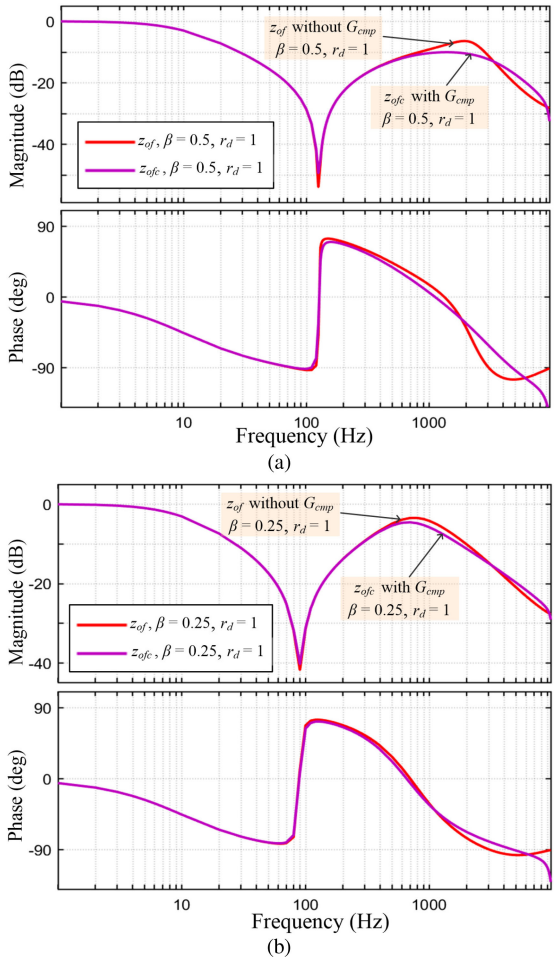

Fig. 13. Bode diagrams of the system output impedance z_{of} and z_{ofc} when (a) $\beta = 0.5$ and (b) $\beta = 0.25$.

and $\beta = 0.8$, it can be obtained from (40) that the range of α is (0, 0.4), which can be also seen from Fig. 11 that the root locus of the proposed method intersects with the unit circle when $\alpha = 0.4$. Furthermore, it is seen that the system's multiple open-loop poles are distributed more to the left, and the bandwidth of the outer voltage loop is increased. Therefore, the gain range of the outer loop is improved (the value range of α is expanded as well), which shows that the system stability margin is improved under the same gain conditions, and also means that the value range of r_d has been increased.

C. System Impedance Performance With HF Shaping Method

Due to the implementation of $G_{\rm cmp}(z)$ and current feedforward control, the system output impedance z_{ofc} is formed by $z_{\rm c\_dc}$ and z_{fc} connected in parallel, where z_{fc} depends on the characteristics of the digital controller, and z_{fc} and z_{ofc} are, respectively, described as

$$z_{fc} = \left(G_{\rm inc}{}^{-1} - G_f\right) \cdot \frac{r_d \cdot z_{\rm c\_dc}}{r_d \cdot G_f + z_{\rm c\_dc}} \tag{41}$$

$$z_{ofc} = z_{fc} \parallel z_{\rm c\_dc} = \left(1 - G_f G_{\rm inc}\right) z_o. \tag{42}$$

Fig. 12(a) shows the improvement effect of $G_{\rm cmp}(z)$ on the digital equivalent output impedance z_{fc} with the current feedforward loop. It can be seen that the frequency domain range occupied by the resistive characteristics at the HF band is increased (the crossing point at –90° has been increased from 3 to 5 kHz, approximately), and the equivalent impedance amplitude is also significantly attenuated, which makes the peak of the system's equivalent output impedance z_{of}, caused by higher loop gain, significantly attenuated as shown from Fig. 12(b). The proposed output impedance shaping solution can mainly reshape the output impedance at the HF range. Moreover, as the proposed method allows to increase the value range of r_d, as analyzed in Fig. 11, when $r_{\rm d}$ is reduced to 0.5, the impedance in medium and low frequency range can be reshaped, as shown in Fig. 12(b). Consequently, the overall equivalent output impedance of the system is reshaped.

When the inner-loop control gain is small, the frequency characteristics of the system output impedance are shown in Fig. 13. When $\beta = 0.5$, it can be seen from Fig. 13(a) that the proposed HF shaping method can still optimize the HF impedance. However, with the decrease of β, the HF amplitude peak of z_{of} is naturally damped, and the proposed method can still reshape the impedance but the contribution is not obvious, as shown in Fig. 13(b). Therefore, the effect of the proposed

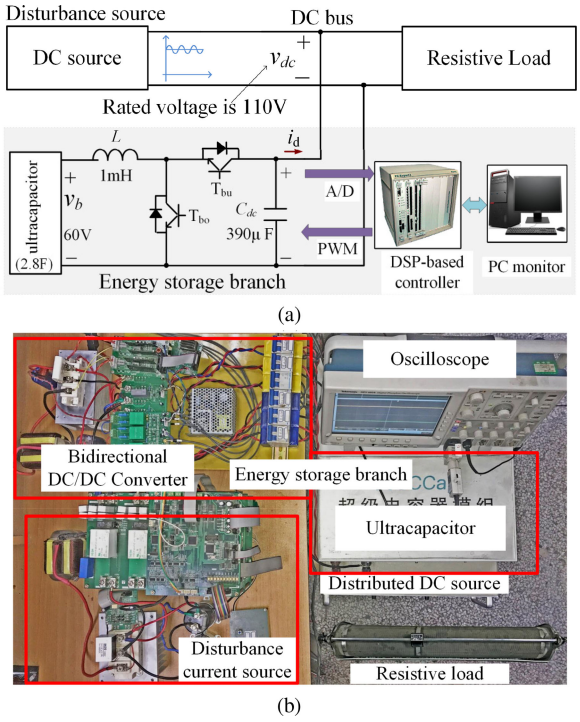

Fig. 14. Experimental platform. (a) Configuration of the experimental platform. (b) Photograph of the experimental platform.

TABLE I
ELECTRICAL PARAMETERS OF EXPERIMENTAL SETUP

Parameters	*Symbols*	*Values*
Capacitance of Ultracapacitor (μF)	C_{uc}	2.8e6
Capacitance in dc link (μF)	C_{dc}	390
Terminal voltage of Ultracapacitor (V)	v_b	60
DC link voltage (V)	v_{dc}	110
Filter inductance (mH)	L	1

TABLE II
CONTROL PARAMETERS OF EXPERIMENTAL SETUP

Parameters	*Symbols*	*Values*
Droop resistance (Ω)	r_d=1/k_{pv}	1, 0.5
Outer-loop control gain	k_{pv}	1, 2
Equivalent outer-loop gain	α=k_{pv}·T_s/C_{dc}	0.125, 0.25
Inner-loop control gain	k_{pi}	12, 16
Equivalent inner loop gain	β=k_{pi}·T_s/L	0.6, 0.8
Coefficient of $G_{cmp}(z)$	k_c	1.25
Cutoff frequency *of* $G_f(z)$ (Hz)	f_{cu}	20

method on system HF impedance optimization is reduced with the reduction of the inner-loop control gain.

V. EXPERIMENTAL ANALYSIS AND VERIFICATION

In order to verify the proposed method, a dc MG setup was built in laboratory, with the configuration and photograph, as shown in Fig. 14(a) and (b). The electrical and control parameters are summarized in Tables I and II, respectively. Disturbance current is generated by a self-designed, controllable current source, as shown in Fig. 14(b). In addition, a resistive load is used to perform the sudden load change to evaluate the step response capability of the system. The bidirectional

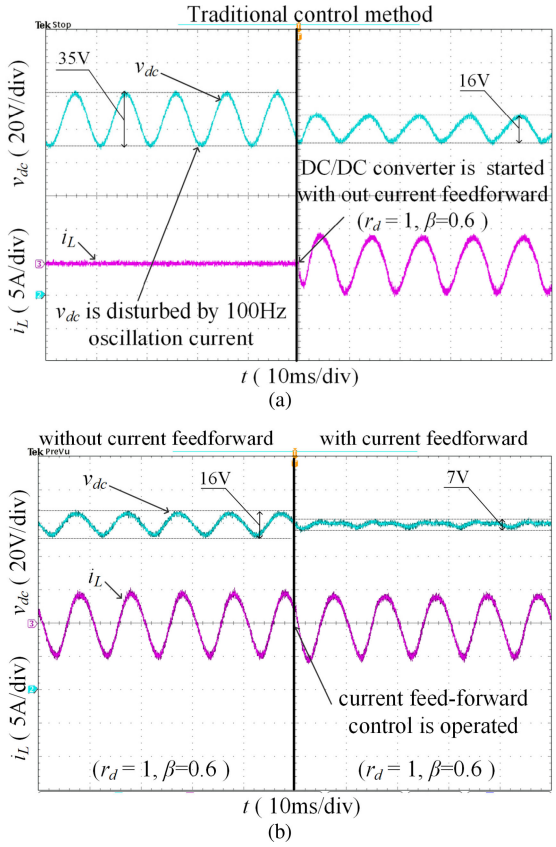

Fig. 15. Experimental results of the common dc-link voltage oscillation rejection capability with and without the disturbance current feedforward control under 100 Hz disturbance current injection. (a) Disabled and enabled dc/dc converter without feedforward control ($r_d = 1$, $\beta = 0.6$). (b) Without and with feedforward control in dc/dc converter ($r_d = 1$, $\beta = 0.6$).

converter is controlled by the DSP with 20 kHz control and switching frequency. The experimental waveforms are shown in Figs. 15–20.

A. System Performances With Traditional Control

The low frequency disturbance rejection capability in the dc MG voltage is compared in Fig. 15, where a 100 Hz disturbance current is injected to the common dc bus by the disturbance source. When the dc–dc converter in the ESS is disabled, the common dc bus has high oscillation of 35 V (31.8%) at 100 Hz, while the voltage oscillation in common dc bus is reduced to 16 V (14.5%) when the dc–dc converter is enabled due to the controller of r_d, as shown in Fig. 15(a). Moreover, the disturbance current feedforward can further reduce the common dc-bus voltage oscillation to 7 V (9%), as shown in Fig. 15(b), because the equivalent output impedance is greatly reduced by the disturbance current feedforward, as analyzed in Fig. 8(b).

B. Current Tracking Performance With HF Shaping Method

Since $\beta = k_{pi} \cdot T_s / L$, the value of L affects the value of β, and L generally has a certain error or variation range in practice. On the other hand, the larger k_{pi} can improve the current-loop bandwidth, as seen in Fig. 5(a) and Fig. 10(a). So, the variation

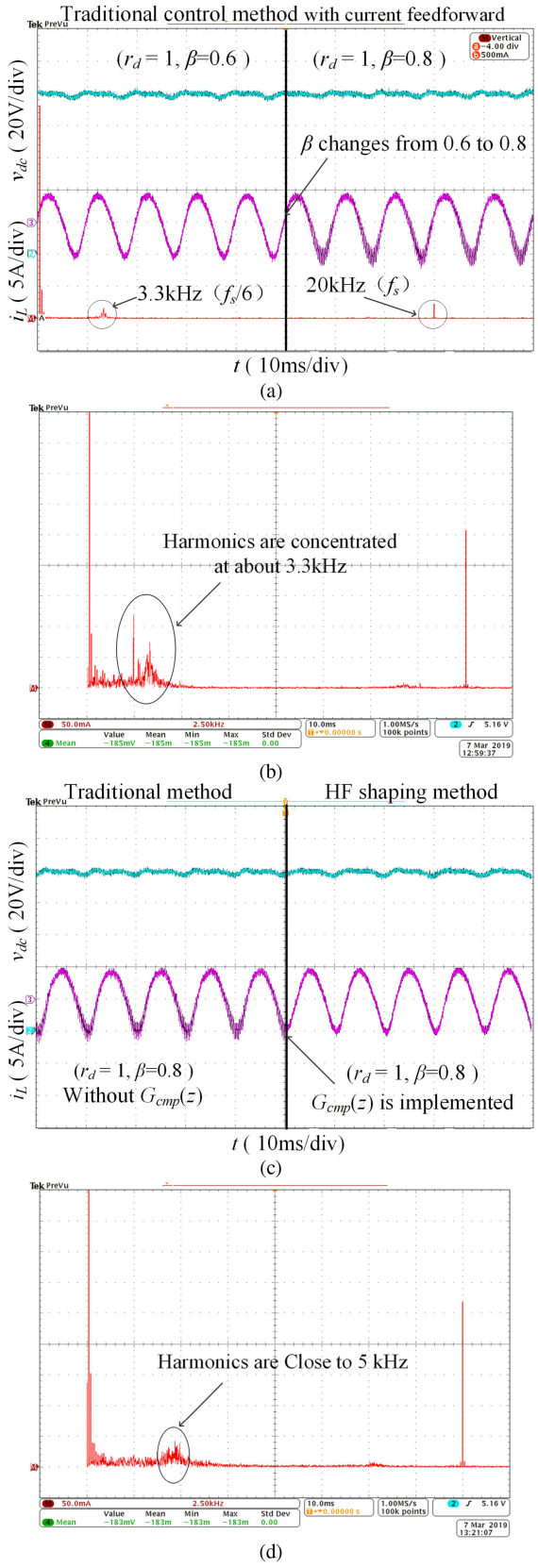

Fig. 16. System response waveforms when β approaches to critical value. (a) $v_{\rm dc}$ and i_L waveforms when the inner-loop gain step increase from $\beta = 0.6$ to $\beta = 0.8$ without the implementation of $G_{\rm cmp}(z)$. (b) FFT analysis for i_L without $G_{\rm cmp}(z)$ and $\beta = 0.8$. (c) System response waveforms with $G_{\rm cmp}(z)$ and $\beta = 0.8$. (d) FFT analysis for i_L with $G_{\rm cmp}(z)$ and $\beta = 0.8$.

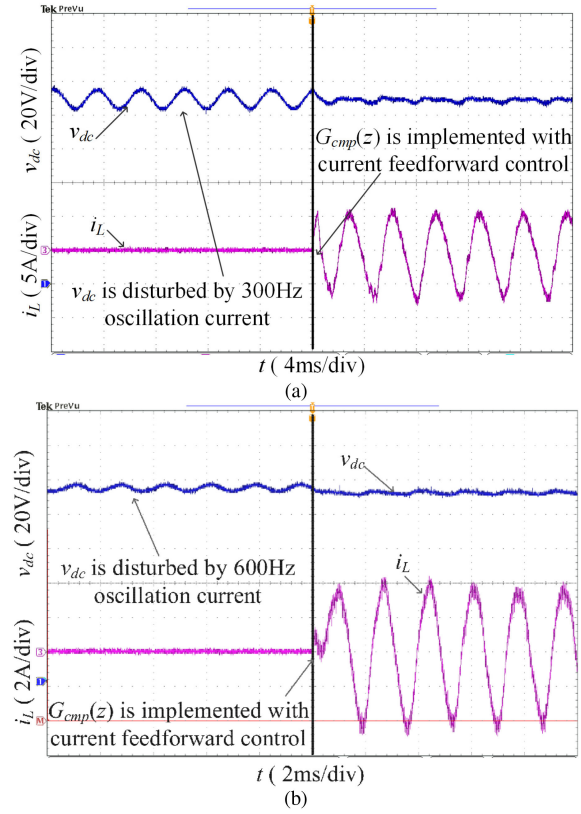

Fig. 17. Disturbance rejection capability of the proposed solution at (a) 300 Hz and (b) 600 Hz disturbance.

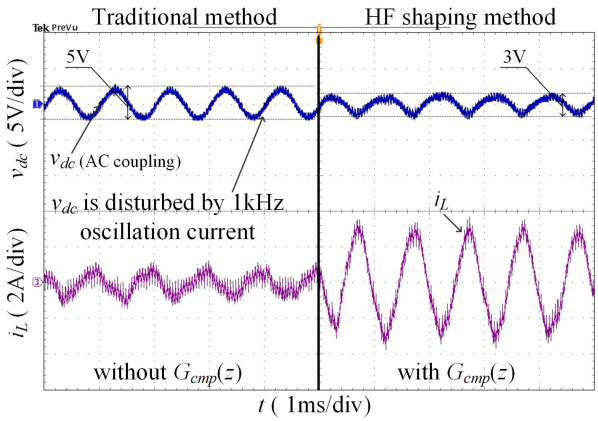

Fig. 18. Comparison of the disturbance rejection capability at 1 kHz.

of L may affect the system stable margin due to that the margin is reduced with the increasing of β. When the proportional gain of equivalent inner current loop, β, steps increase from 0.6 to 0.8, the waveforms of $v_{\rm dc}$ and i_L are as shown in Fig. 16. As analyzed previously, since the system equivalent output impedance with conventional disturbance current feedforward has a peak amplitude in the HF range (near $f_s/6$) and the system stability margin is small, the current oscillation in this frequency range occurs, which is clearly shown in Fig. 16(a), and the corresponding fast fourier transform (FFT) analysis of the current in Fig. 16(b) also shows that the current harmonics are concentrated at about 3.3 kHz (near $f_s/6$).

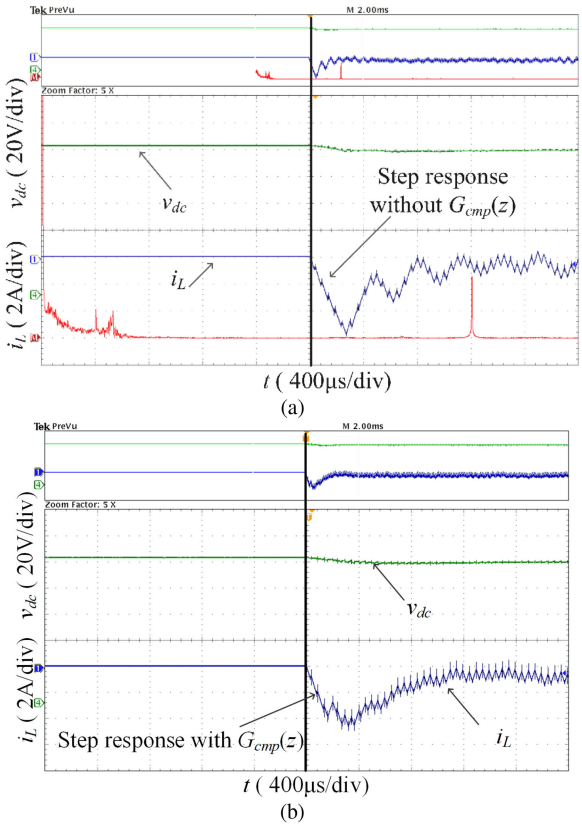

Fig. 19. Experimental results under step response. (a) Without $G_{\rm cmp}(z)$ ($\beta = 0.8$). (b) With $G_{\rm cmp}(z)$, ($\beta = 0.8$).

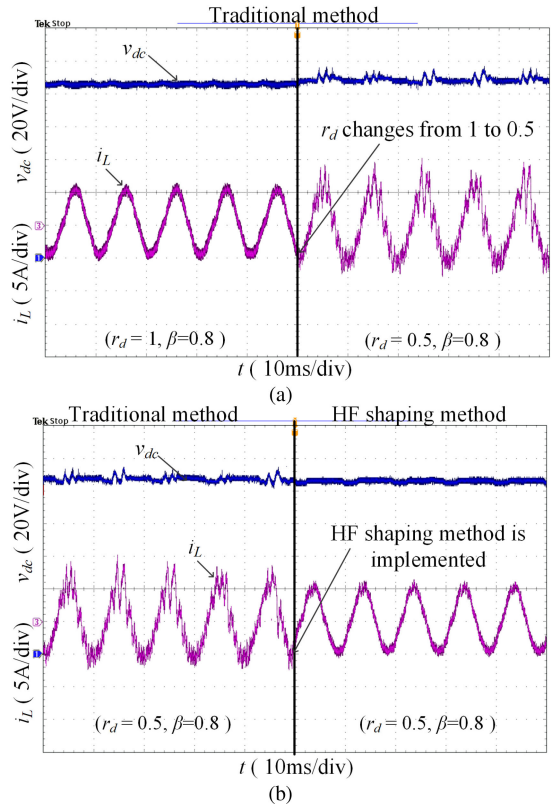

Fig. 20. $v_{\rm dc}$ and i_L waveforms when r_d changes from 1 to 0.5. (a) System response waveforms with traditional control. (b) System response waveforms with HF shaping method.

After the implementation of HF shaping method, such HF harmonic is significantly attenuated, as shown in Fig. 16(c), and the current spectrum is also provided, as shown in Fig. 16(d). As compared to Fig. 16(b), without the proposed $G_{\rm cmp}(z)$, the harmonic content is significantly reduced at $f_s/6$ and the main harmonic component is shifted to about 5 kHz, (near $f_s/4$), which is consistent with the theoretical analysis in Fig. 10(a).

C. HF Disturbance Response Performance of the System With HF Shaping Method

The dc-bus voltage performances on HF disturbance currents rejection are shown in Figs. 17 and 18. In this article, a controllable current source, used to disturb the dc-bus voltage, has limited bandwidth and with the increase of the frequency, the output current capability is gradually reduced. When the disturbance frequency is smaller than 300 Hz, the controllable current source has sufficient output capability, and 5 A current is generated, as shown in Fig. 17(a). When the disturbance current frequency is 600 Hz, the current amplitude is reduced to 4 A, as shown in Fig. 17(b). When the disturbance current frequency is 1 kHz, the current amplitude is further reduced to 3 A, as shown in Fig. 18.

When 300 Hz and 600 Hz disturbance currents are injected into the dc MG, the proposed solution can effectively suppress the voltage oscillation at such frequencies, as shown in Fig. 17(a) and (b), respectively.

When the disturbance current frequency is increased to 1 kHz, the comparison of the proposed solution and conventional disturbance current feedforward solution is shown in Fig. 18. With the conventional solution, the system almost loses the disturbance rejection capability. In contrast, the proposed solution can significantly suppress the disturbance after the implementation of $G_{\rm cmp}(z)$, as shown in Fig. 18. Therefore, the proposed solution can expand system's antidisturbance bandwidth.

Fig. 19 shows the system performances under the step change of the resistive load. There is a significant fluctuation in the mid-high frequency band under the step change of the resistive load without $G_{\rm cmp}(z)$, as shown in Fig. 19(a). This fluctuation is due to the increase of the equivalent output impedance amplitude and the negative impedance characteristics in such frequency range. In contrast, when $G_{\rm cmp}(z)$ is implemented, the negative characteristics is pushed to the higher frequency range and the equivalent impedance amplitude is lower. Consequently, the system has sufficient antihigh-frequency disturbance capability, and the mid-high frequency range fluctuation in the step response is effectively suppressed, as shown in Fig. 19(b).

D. Stability Margin Improvement Performance With HF Shaping Method

Similarly, in the case of large inner-loop gain ($\beta = 0.8$), the value of VR also affects system stability, which is expressed from (13) and (35). Fig. 20 shows the system response under

100 Hz disturbance when r_d changes from 1 to 0.5, which means α changes from 0.128 to 0.256. According to Fig. 11, with the implementation of $G_{\rm cmp}(z)$, the value range of α is theoretically expanded by about two times (from 0.2 to about 0.4), which means that allowable minimum value of r_d is changed from about 0.64 to 0.32 [$r_d = T_s/(\alpha \cdot C_{\rm dc})$, derived from (6) and (11)]. So, the system is unstable when r_d changes from 1 to 0.5 with traditional control method, which is clearly seen in Fig. 20(a) that the system becomes instable, the current oscillates with a large amplitude and this oscillation is coupled to the dc-bus voltage. In contrast, the proposed solution, can stabilize the system due to that $r_d = 0.5$ is still in the stable range, and the oscillation is well damped as well, as shown in Fig. 20(b).

VI. Conclusion

Including the delay of the digital control, sampling, and power converter, the equivalent impedance of the energy storage system under different control methods is modeled in this article. The coupling mechanism of the system controller structure, parameters, and delay links in the equivalent output impedance of the system is studied as well. In addition, the quantitative relationship between the current-loop controller parameters and the value range of virtual resistance is obtained. Accordingly, the performance of the system is improved in terms of inner current-loop bandwidth, voltage loop stability margin, and output impedance optimization, by the proposed HF shaping method implemented in the inner current loop. The proposed method can shift the root locus of the current loop to the left without any impacts on the system stability margin, the bandwidth of the current loop is expanded (the crossing frequency increases from $f_s/6$ to about $f_s/4$). Furthermore, the stability margin of the outer voltage loop is improved (the vale range of r_d is almost expanded by about two times). And the system equivalent output impedance characteristics in the HF range are optimized (antidisturbance frequency ability exceeds 1 kHz). The method is convenient for digital implementation, and the parameter adaptability is enhanced because the stability margin of the system is improved. The theoretical and experimental results clearly verify the correctness and feasibility of the proposed method, and prove that it can suppress the fluctuation of the dc MG voltage in a wide-frequency range.

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