Letters

New Insights on Output Capacitance Losses in Wide-Band-Gap Transistors

Mohammad Samizadeh Nikoo, *Member, IEEE*, Armin Jafari, Nirmana Perera, *Student Member, IEEE*, and Elison Matioli, *Member, IEEE*

***Abstract*—The low ON-resistance of wide-band-gap (WBG) transistors is a key feature for efficient power converters; however, the anomalous loss in their output capacitance ($C_{\rm OSS}$) severely limits their performance at high switching frequencies. Characterizing $C_{\rm OSS}$ losses based on the large-signal measurement methods requires an extensive effort, as separate measurements are needed at different operation points, including voltage swing, frequency, and *dv/dt*. Furthermore, there is a practical tradeoff in the maximum voltage and frequency applied to the device. Here, we introduce a new circuit model, including an effective $C_{\rm OSS}$ and a frequency-dependent series resistance, along with a simple small-signal method to fully characterize $C_{\rm OSS}$ losses in WBG transistors. The method accurately predicts $C_{\rm OSS}$ losses at any voltage swing or frequency. Contrary to other methods, this technique directly leads to a general identification of $C_{\rm OSS}$ losses at different operation points, revealing new insights on $C_{\rm OSS}$ losses in WBG transistors, especially the dependence of $E_{\rm DISS}$ on voltage and frequency. Based on the proposed approach, the issue of $C_{\rm OSS}$ losses in enhancement-mode GaN and SiC transistors was assigned to the limited quality factor of $C_{\rm OSS}$. The precise characterization of $C_{\rm OSS}$ losses proposed in this letter is essential for designing efficient high-frequency power converters.**

***Index Terms*—Cascode, $C_{\rm OSS}$, $E_{\rm DISS}$, energy loss, GaN, nonlinear resonance, output capacitance, SiC, superjunction (SJ).**

I. Introduction

THE nonrecoverable energy loss associated with resonantly charging and discharging the output capacitance ($C_{\rm OSS}$) of some of the advanced transistors and diodes considerably limit their performance in the power converters, especially those operating at high frequencies [1]–[11]. An unexpected power loss in soft-switched power converters based on Si superjunction (SJ) MOSFETs, especially those with low specific $R_{\rm ON}$, initiated studies on their large-signal $C_{\rm OSS}$, where the nonsymmetric charging and discharging processes were observed. Measurements with Sawyer–Tower (ST) method showed a frequency-independent $C_{\rm OSS}$-loss due to the charge trapping in SJ devices [8]–[11].

The lower-than-expected efficiencies in soft-switching power converters based on the wide-band-gap (WBG) transistors again initiated investigations on $C_{\rm OSS}$ losses [12]. Zulauf *et al.* [2] characterized the $C_{\rm OSS}$ charging/discharging energy dissipation ($E_{\rm DISS}$) in GaN transistors using an ST method, where the results showed frequency-dependent losses. Guacci *et al.* [3] used a thermal approach to study $C_{\rm OSS}$ losses in GaN transistors and observed *dv/dt*-dependent energy dissipation. The ST-based $E_{\rm DISS}$ measurement of some of the commercial SiC transistors, however, presented a weak dependence on frequency and *dv/dt* [1].

Although several measurements showed an effect from voltage swing, frequency, and *dv/dt* on $C_{\rm OSS}$ losses in SiC and enhancement-mode GaN transistors, the dependence of $E_{\rm DISS}$ on these parameters is still not clear [3]. Zulauf *et al.* [1] used the empirical relation

$$E_{\rm DISS}^{\rm Ref[1]} = k \cdot f^{\alpha} \cdot V^{\beta} \quad (1)$$

to fit the experimental data, where *f* is the frequency, *V* is the charging voltage, and *k*, α, and β are constants. For some of the evaluated transistors, the values of $\alpha < 1$ and $\beta < 2$ were obtained [13]. Although curve fitting from large-signal measurements shows the behavior of $C_{\rm OSS}$ losses, it requires excessive experiments with the high-voltage and high-frequency power amplifiers (PAs) at several operation points at different voltages and frequencies. Moreover, the need for a high-voltage RF PA can severely limit the maximum voltage and frequency applied to the device under test.

In this letter, we propose a small-signal modeling approach to extract the large-signal $C_{\rm OSS}$ losses of WBG transistors on a wide range of operation points. The device is simply modeled by a nonlinear capacitance $C_{\rm OSS}$ in series with a frequency-dependent resistance R_S. This modeling decouples the frequency and voltage dependence of losses, enabling to solve a large-signal problem with a small-signal approach. Using an impedance measurement to measure the values of R_S at different frequencies, together with the presented output capacitance versus voltage from the datasheets, we present a general relationship for $C_{\rm OSS}$ losses in different voltages and frequencies. As a result, just one simple small-signal measurement (instead of several different measurements in large-signal

Manuscript received October 25, 2019; revised November 19, 2019; accepted November 25, 2019. Date of publication December 3, 2019; date of current version March 13, 2020. This work was supported in part by the Swiss Office of Energy under Grant SI/501887-01 (MEPCO). *(Corresponding author: Mohammad Samizadeh Nikoo.)*

The authors are with the Power and Wide-Band-Gap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne CH-1015, Switzerland (e-mail: mohammad.samizadeh@epfl.ch; armin.jafari@epfl.ch; nirmana.perera@epfl.ch; elison.matioli@epfl.ch).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2958000

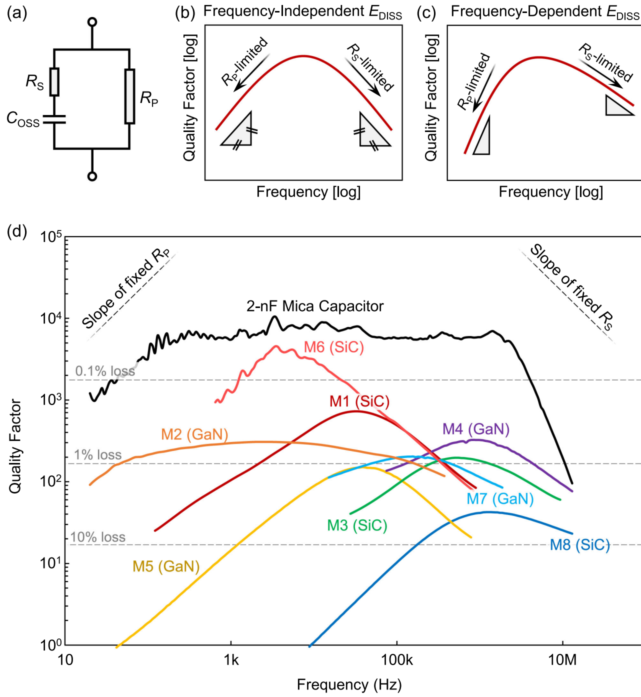

Fig. 1. (a) Circuit model for the output capacitance of transistors. Quality factor versus frequency for transistors with (b) fixed and (c) frequency-dependent R_S and R_P. (d) Measured quality factor of the C_{OSS} of different commercial WBG transistors versus frequency at $V_{DS} = 40$ V. The gate and source of transistors were shorted ($C_{OSS} = C_{DS} + C_{GD}$).

methods) leads to a general view of the C_{OSS} losses. The method does not suffer from some of the shortcomings of large-signal measurements, such as limitation in applied voltage/frequency (e.g., due to PA) or signal distortion at high frequencies. The proposed method gives insights into the dependence of E_{DISS} on frequency, voltage, and *dv*/*dt* value.

II. Model

Fig. 1(a) shows a model for the output capacitance of transistors, including a nonlinear capacitance C_{OSS} in series with resistance R_S and in parallel with resistance R_P, a representative for losses at high and low frequencies, respectively. The quality factor (*Q*-factor) of output capacitance can be defined as [see Fig. 1(b) and (c)]

$$Q = \frac{1}{R_S C_{OSS}\omega + (R_P C_{OSS}\omega)^{-1}}. \quad (2)$$

The effect of R_P (mainly corresponding to the leakage current) is dominant at dc, while R_S significantly contributes to the switching dynamics and C_{OSS} losses. As illustrated in Fig. 1(d), small-signal measurements show a considerable lossy behavior for the C_{OSS} of WBG transistors. For instance, the levels of losses are considerably higher than a reference low-loss mica capacitor. The small-signal extracted values of losses for frequencies higher than 1 MHz are in the range of 1%–10%, which is in agreement with the previously measured large-signal losses [1], [2]. This indicates the possibility of evaluating large-signal

TABLE I
Specifications of Evaluated WBG Transistors

No.	Voltage and current rating		C_{OSS}**
	Voltage (V)	Current* (A)	(pF)
M1	1200	36	80
M2	650	30	65
M3	650	93	118
M4	600	31	72
M5	100	90	840
M6	1700	4	16
M7	600	13	28
M8	1200	55	76

*Continuous current at 25 °C.
**Reported capacitance at two-third of voltage rating, measured at 1 MHz.

losses with proper small-signal modeling. Fig. 1(d) also shows that for frequencies higher than 1 MHz (which covers the switching bandwidth of WBG transistors), the *Q*-factor of all the considered transistors is limited by R_S.

For a linear capacitor with frequency-independent R_S and R_P, (2) fully describes the charging/discharging energy dissipation as

$$E_{DISS} = \frac{\pi}{2Q} E_{OSS} \quad (3)$$

where E_{OSS} is the total energy stored in C_{OSS}. In practice, however, C_{OSS} is nonlinear and R_S and R_P can change with frequency [see Fig. 1(b) and (c)]. The nonunity slope of the *Q*-factor versus frequency for several different WBG transistors (see Table I), as shown in Fig. 1(d) (measured with Keysight E4990A impedance analyzer with a very high accuracy), confirms the frequency-dependent nature of R_S and R_P.

We use the model presented in Fig. 1(a) to extract C_{OSS} charging /discharging energy dissipation. As mentioned, R_S is the origin of C_{OSS} losses in switching dynamics, as R_P just limits the *Q*-factor at low frequencies. By applying voltage $v(t)$ to the output capacitance and considering R_S as a perturbation element, the power loss in R_S can be written as

$$P_{\text{loss}} = R_S\left(C_{OSS}\tfrac{dv}{dt}\right)^2. \quad (4)$$

Assuming $v(t)$ represents a switching transient from 0 to V, the total energy loss during a single switching transient time t_{SW} is

$$E_{\text{loss}} = \int_0^{t_{SW}} R_S\left(C_{OSS}\tfrac{dv}{dt}\right)^2 dt. \quad (5)$$

In a charging and discharging process, however, E_{loss} is dissipated two times ($E_{DISS} = 2E_{\text{loss}}$). Considering a constant switching speed $dv/dt \cong V/t_{SW}$, which is very accurate for trapezoidal waveforms and also can be used for sinusoidal waveforms, we write

$$E_{DISS} = 2R_S\left(\tfrac{dv}{dt}\right)\int_0^V C_{OSS}^2\, dv \quad (6)$$

which clearly shows *dv*/*dt* dependence of C_{OSS} losses [2]–[4]. Equation (6) can be rewritten as

$$E_{DISS} = 2R_S\left(\tfrac{dv}{dt}\right)V C_{OSS}^{\text{eff}\,2} \quad (7)$$

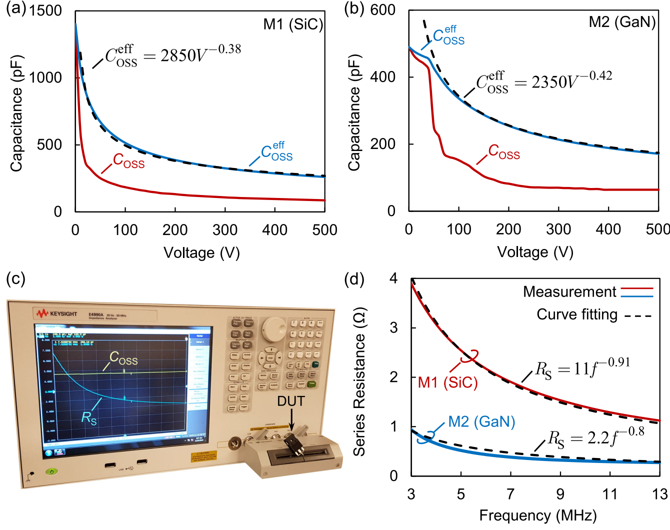

Fig. 2. C_{OSS} (at 1 MHz, reported in datasheet) and extracted effective C_{OSS} for (a) M1 (SiC) and (b) M2 (GaN). (c) Photograph of the experimental setup for measuring R_S (the gate and drain of the transistor are shorted) using Keysight E4990A impedance analyzer. (d) R_S as a function of frequency for M1 and M2 ($V_{DS} = 40$ V). Measurement (solid line) and curve fitting (dashed line).

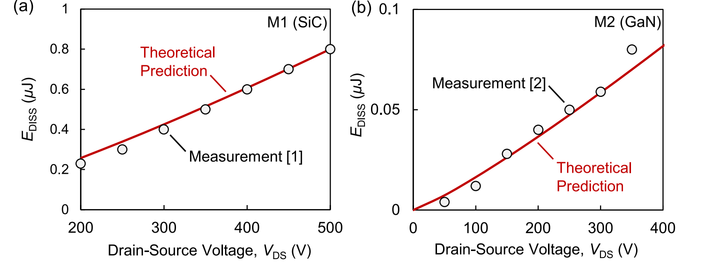

Fig. 3. Theoretical prediction of C_{OSS} energy dissipation (solid lines) compared with measurement results with the ST method [1], [2] for (a) M1 (at 1 MHz) and (b) M2 (at 10 MHz).

in which we introduced the new term C_{OSS}^{eff}, which is the root-mean-square (rms) of C_{OSS} from 0 to V, representing the average C_{OSS} value that contributes to the power dissipation in the device output capacitance

$$C_{OSS}^{eff} = \sqrt{\frac{1}{V}\int_0^V C_{OSS}^2\, dv}. \tag{8}$$

One can use $f = 1/(2t_{SW})$ to rewrite (6) as

$$E_{DISS} = 4R_S f V^2 C_{OSS}^{eff2}. \tag{9}$$

Comparing (9) with the experimental model (1) reveals two main points.

1) $\alpha = 1$ for a fixed and frequency-independent R_S; however, nonunity values of α have been reported in [2] and [13]. This agrees with the measurement results presented in Fig. 1(d), showing frequency-dependent R_S.
2) The obtained values of β, extracted by curve fitting in [13], were always less than 2. This is in agreement with (9) since when rising the voltage V, the rms value of C_{OSS} decreases. As a result, although the square of V is seen in (9), the C_{OSS}-related term leads to a $\beta < 2$.

III. C_{OSS}-Loss Evaluation

Here, we show how large-signal C_{OSS} losses can be extracted from the small-signal model. This section also validates the applicability of the proposed method to evaluate C_{OSS} losses by comparing the extracted E_{DISS} values with the ST method [1], [2]. The first step to extract the general relation of (9) is to obtain the effective C_{OSS}. This can be done by using the data reported in datasheets. Fig. 2(a) and (b) shows the reported C_{OSS} in the datasheet of transistors M1 (36-A-rated SiC FET with $R_{ON} = 80$ mΩ) and M2 (30-A-rated e-mode GaN HEMT with $R_{ON} = 50$ mΩ), respectively. The effective C_{OSS} values were obtained using (8) [see Fig. 2(a) and (b)]. One can directly use these values; however, here we applied a curve fitting to obtain the closed-form relations [dashed lines in Fig. 2(a) and (b)]

$$C_{OSS}^{eff} = (2850 \text{ pF}) \times (V[\text{V}])^{-0.38} \tag{10}$$

and

$$C_{OSS}^{eff} = (2350 \text{ pF}) \times (V[\text{V}])^{-0.42} \tag{11}$$

for M1 and M2, respectively.

After extraction of the effective C_{OSS}, the series resistance R_S was measured using a Keysight E4990A impedance analyzer [see Fig. 2(c)]. The R_S, as a key element in C_{OSS} losses, as a function of frequency is not typically reported by the manufacturers in datasheets. Fig. 2(d) illustrates the R_S for transistors M1 and M2 (solid lines). Unlike C_{OSS}, which is a strong function of voltage, R_S is almost constant with voltage, and therefore, it can be assumed as a linear parameter. On the other hand, C_{OSS} is not a function of frequency, while R_S is highly frequency dependent [see Fig. 2(d)]. For M1 and M2, we have

$$R_S = (11\ \Omega) \times (f\ [\text{MHz}])^{-0.91} \tag{12}$$

and

$$R_S = (2.2\ \Omega) \times (f\ [\text{MHz}])^{-0.8} \tag{13}$$

respectively. It should be noted that the level of R_S, as the effective series resistance of C_{OSS}, is significantly higher than the device ON-resistance (e.g., in GaN devices it includes the buffer and Si substrate instead of the two-dimensional electron gas [14]). Substituting (10)–(13) into (9) results in

$$E_{DISS} = 0.357 \times f^{0.09} \times V^{1.24} [\text{nJ}], \quad \text{for M1 (SiC)} \tag{14}$$

and

$$E_{DISS} = 0.049 \times f^{0.2} \times V^{1.16} [\text{nJ}], \quad \text{for M2 (GaN)} \tag{15}$$

where f and V are in MHz and Volts, respectively, showing losses at different operation points just by performing two measurements. The obtained relations were verified with measurement results using the ST method with sinusoidal waveforms performed at 1 MHz for M1 [1] and at 10 MHz for M2 [2]. As shown in Fig. 3, good agreements were obtained for both transistors. It should be noted that the level of losses in these transistors is

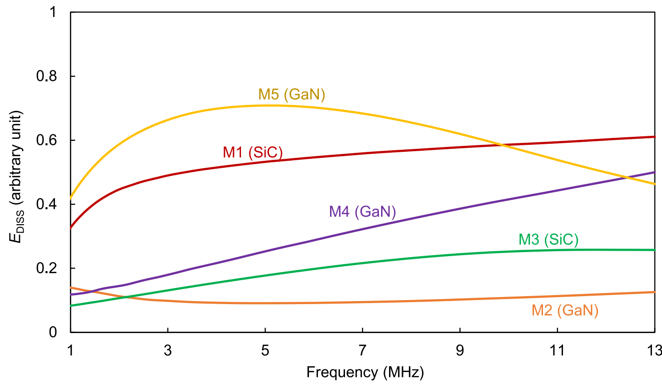

Fig. 4. Frequency dependence of E_{DISS} obtained from the proposed model versus frequency for five SiC and GaN transistors.

considerably different, showing the applicability of the proposed approach to extract C_{OSS} losses for a wide range of E_{DISS} values.

IV. Discussion

Despite several experimental works on C_{OSS} losses in WBG transistors, the dependence of E_{DISS} on frequency is not completely clear. Some transistors showed a strong dependence of E_{DISS} on frequency, while for some other transistors it was very weak. The same observations can be seen for *dv*/*dt* dependence. For some transistors, even lower E_{DISS} values were obtained for higher *dv*/*dt* values [1]. The proposed approach, however, clears the dependence of E_{DISS} on the frequency and d*v*/d*t*.

Based on (9), $E_{\mathrm{DISS}} \propto R_S(f) \times f$, which shows the frequency dependence of C_{OSS} losses. Fig. 4 presents the E_{DISS} dependence on frequency for several different transistors extracted using this model. R_S values were measured at 40 V. Since R_S shows negligible variation with voltage, the obtained results can be generalized to device performance at different voltages. Transistor M1 (SiC) shows a saturation in E_{DISS} versus frequency, in agreement with the measurement results in [1], which showed an almost frequency-independent E_{DISS}. Transistors M2 (GaN) and M3 (SiC) show almost constant E_{DISS} for frequencies higher than 5 MHz. The experimental results in [2] also present almost equal losses at 5 and 10 MHz for M2. Transistor M4, however, shows a significant increase in E_{DISS} at higher frequencies (>1 MHz). This is similar to most typical cases in the reported experimental results [2], [13]. Interestingly, for transistor M5, there is an initial increase in E_{DISS}; however, after $f = 5$ MHz, the losses even decrease with increasing the frequency. A similar behavior has been reported for some of the SiC transistors, showing lower E_{DISS} at higher frequencies or higher *dv*/*dt* values. As a conclusion, different frequency-dependence types can be observed in E_{DISS} in WBG transistors, and the present method allows us to investigate such effects using a small-signal modeling.

The proposed method gives a complete view of C_{OSS} losses due to a limited *Q*-factor in SiC and enhancement-mode GaN transistors. Here, we separately discuss about the applicability of the method for two other types of devices.

1) SJ devices: The dominant part of C_{OSS} loss in SJ transistors is due to the charge trapping that causes the frequency-independent energy dissipation. SJ devices, however, can potentially have a limited *Q*-factor. In this case, a frequency-dependent loss is added to the total energy dissipation. This might be the reason for previously observed frequency-dependent losses in some of the SJ transistors [16]. In this case, a low-frequency ST measurement (frequency-independent losses) together with the proposed method (frequency-dependent losses) gives a complete view of C_{OSS} energy dissipation.
2) Cascode devices: A type of frequency-independent losses, different from that is happening for SJ devices, was observed in cascode transistors [4], [15]. Some of the commercial cascode GaN (integrated with a low-voltage Si device) devices showed a considerably higher loss for voltages larger than ~200 V [2], [4]. As a result, one can separately characterize frequency-independent (using the ST method at the frequency corresponding to peak of *Q*-factor) and frequency-dependent (using the proposed method) C_{OSS} losses. Adding these different components give the general behavior of energy dissipation in the output capacitance.

Based on the proposed model, it is suggested to manufacturers to present R_S-versus frequency (at least for frequencies above 1 MHz) for WBG transistors. This curve, together with $C_{\mathrm{OSS}}^{\mathrm{eff}}$, gives a general view on C_{OSS} losses.

V. Conclusion

We proposed a new method to extract C_{OSS} losses for WBG transistors at different voltages and time/frequency frames, just by performing one small-signal measurement R_S versus frequency. This measurement together with the reported C_{OSS} versus V_{DS} reveals the general C_{OSS}-loss behavior of the device. The method helps to clear the voltage and frequency dependence of E_{DISS} and can be used to compare and benchmark different semiconductor devices. The results also led to a categorization of C_{OSS} loss in different types of transistors. The E_{DISS} in e-mode GaN and SiC transistors is mainly caused by the limited *Q*-factor of C_{OSS}, which was not observed in SJ and cascode devices. The generality and robustness of this method made it possible to quantify the C_{OSS} losses of WBG transistors as a crucial source of losses in the soft-switched power converters, especially those operating at high frequencies.

References

[1] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019.

[2] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. M. Rivas-Davila, "C_{OSS} losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018.

[3] M. Guacci *et al.*, "On the origin of the C_{OSS}-losses in soft switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679–694, Jun. 2019.

[4] M. S. Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal C_{OSS} and C_{OSS} losses of transistors based on nonlinear resonance," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2242–2246, Mar. 2020.

[5] D. Bura, T. Plum, J. Baringhaus, and R. W. de Doncker, "Hysteresis losses in the output capacitance of wide bandgap and superjunction transistors," in *Proc. 20th Eur. Conf. Power Electron. Appl.*, Sep. 2018, pp. P.1–P.9.

[6] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10-kV SiC MOSFETS and diodes," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5240–5250, Jun. 2018.

[7] Z. Tong, G. Zulauf, J. Xu, J. D. Plummer, and J. M. Rivas-Davila, "Output capacitance loss characterization of silicon carbide Schottky diodes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 856–878, Jun. 2019.

[8] G. D. Zulauf, J. Roig-Guitart, J. D. Plummer, and J. M. Rivas-Davila, "C_{OSS} measurements for superjunction MOSFETs: Limitations and opportunities," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 578–584, Jan. 2019.

[9] J. B. Fedison and M. J. Harrison, "C_{OSS} hysteresis in advanced superjunction MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 247–252.

[10] J. B. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, "$\mathrm{C_{OSS}}$ related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 150–156.

[11] J. Roig and F. Bauwens, "Origin of anomalous C_{OSS} hysteresis in resonant converters with superjunction FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3092–3094, Sep. 2015.

[12] K. Surakitbovorn and J. M. Rivas-Davila, "Evaluation of GaN transistor losses at MHz frequencies in soft switching converters," in *Proc. IEEE 18th Workshop Control Model. Power Electron.*, 2017, pp. 1–6.

[13] K. Surakitbovorn and J. M. Rivas-Davila, "On the optimization of a class-E power amplifier with GaN HEMTs at MHz operation," *IEEE Trans. Power Electron.*, to be published.

[14] J. Zhuang, G. Zulauf, J. Roig, J. D. Plummer, and J. M. Rivas-Davila, "An investigation into the causes of $\mathrm{C_{OSS}}$ Losses in GaN-on-Si HEMTs," in *Proc. 20th Workshop Control Model. Power Electron.*, Jun. 2019, pp. 1–7.

[15] J. Xu, L. Gu, S. Kargarrazi, Z. Ye, and J. M. Rivas-Davila, "Cascode GaN/SiC power device for MHz switching," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2780–2785.

[16] G. Zulauf and J. M. Rivas-Davila, "Coss losses in silicon superjunction MOSFETs across constructions and generations," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs*, May 2018, pp. 136–139.