Interleaved Current-Fed Switched Inverter

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***Abstract*—Current-fed switched inverter (CFSI) is a high-gain inverter topology suitable for applications which have limited input dc source voltage, e.g., roof-top solar applications. A very high step-up ratio between ac output and dc input along with inherent shoot-through protection makes it suitable for low-power stand-alone inverter applications. In this article, a novel interleaved topology for CFSI (ICFSI) is proposed to augment its power rating. A pulsewidth modulation (PWM) scheme is also proposed to drive the interleaved topology. Various modes of operation of ICFSI, along with the steady-state model and dynamic analysis, with the proposed PWM scheme, are reported. ICFSI, with the PWM scheme, results in a 33% increase in maximum ac gain as compared to CFSI. In this article, the small-signal model of ICFSI is also derived and verified. An analysis comparing the losses in CFSI and ICFSI is carried out. It is observed that interleaved operation improves the efficiency by 4% at 600 W. The proposed topology and analysis are verified with the experimental results obtained from a 600-W laboratory-developed prototype.**

***Index Terms*—Current-fed switched inverter (CFSI), high gain, impedance-source inverter (ZSI), interleaving.**

I. Introduction

CURRENT trend in renewable integration has seen a significant rise in installation of roof-top photovoltaic (PV) systems. These systems are lower in power rating as they are intended to power a single or few household loads. Fig. 1(a) shows the roof-top integration in various countries around the world. In India, roof-top integration is expected to ramp up very soon with an additional 40 GW installation by 2022 [1]. Typically, roof-top PV systems have lower output voltage, as the available space for solar installation is relatively smaller. This demands for a new direction of thought to design the power electronics interface for smaller PV installations to achieve high ac voltage. Typically, the power interface for these applications should have high conversion gain and scalable power output as shown in Fig. 1(b).

The most popular method to obtain a high ac output voltage from a smaller dc supply is to connect a transformer (T/F) at the output of a voltage-source inverter (VSI), as shown in Table I(a) [2]–[4]. In order to eliminate the line frequency transformer, boost stage can be used as an interface between the dc source and the VSI input, as shown in Table I(b) [5], [6]. This increases the power density and efficiency of the system. However, in this case, the interfacing is through a dc-link capacitor. Thus, this architecture is prone to failure due to shoot through (ST) when the operating switching frequency is very high.

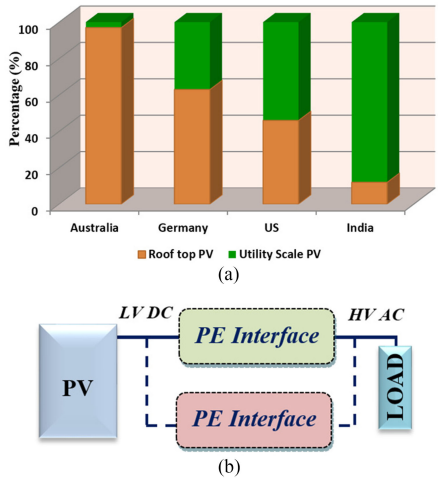

Fig. 1. (a) Share of roof-top PV in various countries. (b) Block diagram of power electronics (PE) interface suitable for a roof-top PV system.

A third method is to use a high-gain inverter, as shown in Table I(c), which has a very high step-up ratio between the output ac and input dc voltages. This is typically categorized as microinverter. These single-stage inverters have power rating in range of few hundred watts to about a kilowatt, constrained by the very high input current above this rating. Impedance-source inverters (ZSI) are explored as a potential solution under this category. High gain ZSIs can be classified into three broad categories, as shown in Fig. 2. The classification is based on the configuration of the front-end boost stage (FBS). Table II lists examples of these three categories with their dc gains (M). Various passive front-end boost stage-based ZSIs are reported in [7]–[10]. These topologies are capable of achieving high gain. However, higher passive component count makes the converters bulky in size. To deal with the difficulty, various active front-end boost stage-based (AFBS) ZSI topologies have been proposed in [11]–[14]. To further increase the gain, some of the topologies based on coupled inductors are also reported in the literature [15]–[18].

Current-fed switched inverter (CFSI), a type of active impedance-source inverters, was proposed in [14]. Some of its special properties, which make it suitable for roof-top PV applications, are high-voltage conversion ratio, ST protection, and continuous input current. In converters like CFSI, with high

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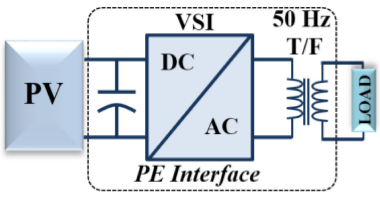
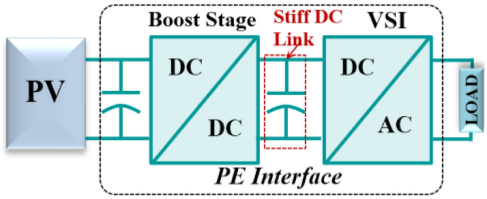
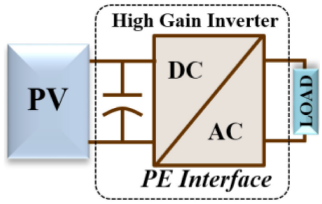
TABLE I
COMPARISON OF POWER ELECTRONICS INTERFACE FOR ROOF-TOP INSTALLATION

		
(a) Transformer based interface.	(b) Two stage interface.	(c) Single stage interface.
▪ Bulky ▪ Poor Efficiency ▪ Heavy ▪ Costly	▪ Lighter in weight and compact ▪ Better Efficiency ▪ Cost Effective	▪ Inherent boost stage ▪ ST protected ▪ More reliable

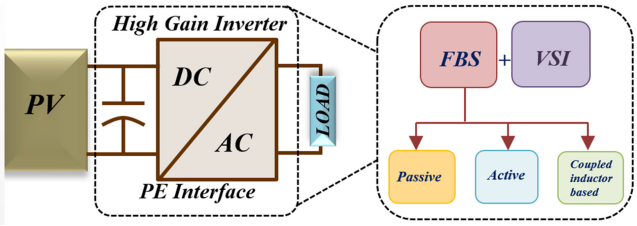


Fig. 2. Classification of high-gain ZSI.

step-up ratio, as power rating goes up, the input current drawn from the PV source also goes up [19]–[20].

High input current leads to significant conduction loss in the converter as depicted in Fig. 3(a). This is analogous to the high current at the output of voltage regulator modules (VRMs), which are essentially step-down converters used to power communication and computation ICs [21]–[22]. As depicted in Fig. 3(b), the high output current leads to considerable conduction loss.

Paralleling multiple phases and interleaving them is a feasible solution to improve efficiency of a converter at higher power level. This philosophy has been implemented in VRMs, as shown in Fig. 3(c), and helps to reduce the current stress of each phase. Thus, better performance in terms of efficiency is achieved [23], [24]. The ideology of paralleling is also discussed in [25]. It identifies the benefits of modularizing a single active bridge dc–dc converter in terms of improved efficiency at higher power rating. Paralleling has also been implemented in [26] for a series-resonant dc–dc converter for improving the power handling capability. In [27] and [28], multiple inverter modules are paralleled to deal with higher power rating. In this article, a similar approach is explored to achieve improved efficiency in case of CFSI. However, interleaving the parallel phases of CFSI alters its steady-state characteristics, boost factor, and dynamic model.

The overall objective of the article is to propose an optimized interleaved topology for CFSI and characterize its performance. A novel pulsewidth modulation (PWM) scheme is proposed, which incorporates ST to achieve higher gain while ensuring reliability of the interleaved topology. The interleaving of CFSI is verified with two modules, which results in 4% increase in efficiency at 600 W, and 33% increase in maximum achievable ac gain as compared to CFSI.

The contributions of the article are divided into various sections. Section II discusses different methods to parallel CFSIs in order to achieve modular design. In Section III, PWM scheme to interleave the parallel modules is discussed. The operating modes and steady-state performance analysis of the proposed interleaved topology (interleaved CFSI (ICFSI)) are also reported in this section. It is shown that the ICFSI achieves higher gain compared to the conventional CFSI. Small-signal model of ICFSI is derived and it is verified with PLEXIM simulation software as well as with experiment in Section IV. Loss analysis and comparative analysis between the efficiency, switch stress, and total harmonic distortion (THD) of CFSI and ICFSI are presented in Section V and VI. In Section VII, the proposed topology and analysis are verified with the experimental results obtained from a 600-W laboratory prototype. Finally, Section VIII concludes this article.

II. MODULAR IMPLEMENTATION

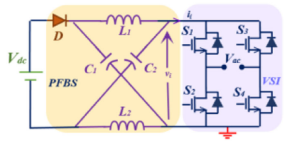
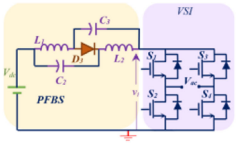
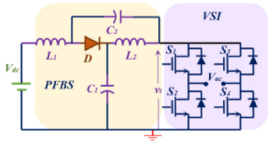
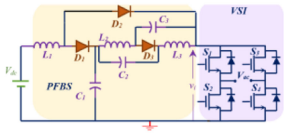
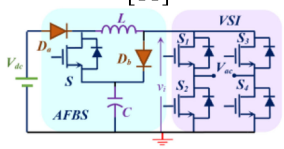
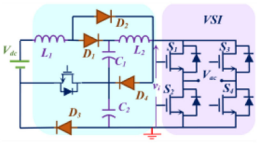
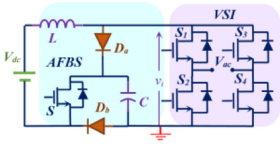
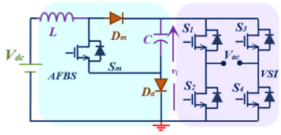
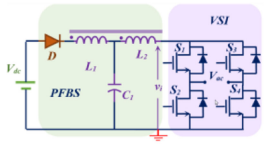
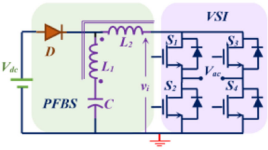
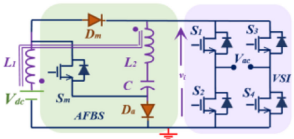
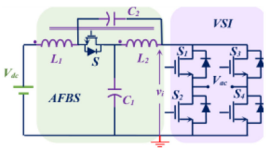
Schematic of CFSI, given in Fig. 4(a), has two stages: 1) AFBS; and 2) inverter stage. AFBS steps up the low-input dc ($V_{\rm dc}$) to a high dc voltage and this dc voltage is converted to ac by using the inverter stage. In this inverter stage, ST is inherently inserted and it is synchronized with the AFBS to boost up $V_{\rm dc}$ and thereby the ac output voltage. PWM scheme of CFSI which includes the ST interval is discussed in more detail in [14]. Due to high boost factor, input current drawn by CFSI is high for a particular power level. Thus, as power rating goes up, increase in conduction loss lowers the overall efficiency of the converter.

As discussed in Section I, interleaving is a preferable approach to increase the power handling capability of the converter. Several strategies can be used to modularize a CFSI for interleaved operation, as discussed next.

A. Strategy 1

As shown in Fig. 4(b), only one AFBS stage can be used and several inverter stages in parallel can be cascaded to this stage [29], [30]. This is not a good strategy as an increase in power rating forces the AFBS to cater to more load owing

TABLE II
CLASSIFICATION OF HIGH-GAIN ZSI

Passive FBS based ZSI			
ZSI [7]  $M = \frac{1}{(1-D)(1-2D)}$	Q ZSI [8]  $M = \frac{1}{1-3D}$	Voltage Fed Q ZSI [9]  $M = \frac{1+D}{1-3D}$	Capacitor Assisted QZSI [10]  $M = \frac{1+D}{1-2D-D^2}$
Active FBS based ZSI			
Switched Boost Inverter [11]  $M = \frac{1-D}{1-2D}$	Switched ZSI [12]  $M = \frac{1}{D^2-3D+1}$	Q SBI [13]  $M = \frac{1}{1-2D}$	CFSI [14]  $M = \frac{1}{1-2D}$
ZSI with coupled inductors in FBS			
Trans-ZSI [15]  $M = \frac{1}{1-(1+n)D}$	T ZSI [16]  $M = \frac{1}{1-\frac{D}{1-n}}$	Coupled Inductor Based CFSI [17]  $M = \frac{1}{1-\frac{2D}{1-n}}$	Q ZSI with Coupled Inductors [18]  $M = \frac{1}{1-2D}$

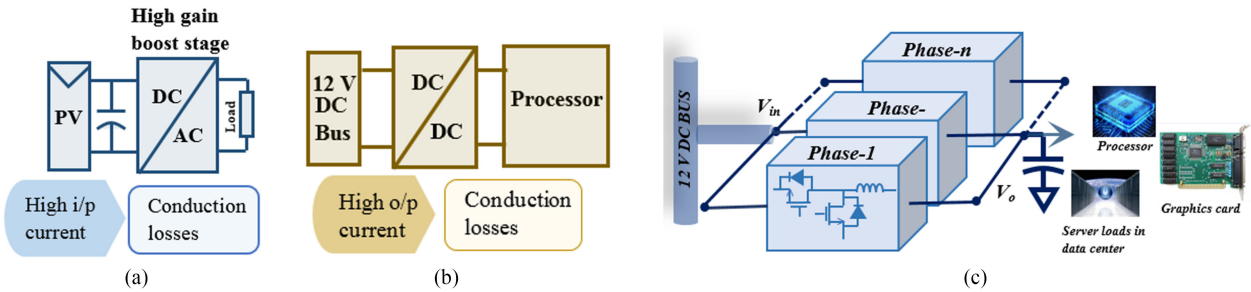


Fig. 3. (a) Issues with high-gain inverters. (b) Analogous challenges faced in processor power supply (VRM). (c) Interleaving of VRM phases to achieve better efficiency.

to its high step-up ratio. This increases the current stress and hence the conduction loss in AFBS significantly as compared to the inverter stage. Also, paralleling of inverters leads to circulating current which will further increase the conduction losses [26].

B. Strategy 2

In Strategy 2, as depicted in Fig. 4(c), multiple input stages (AFBS) are connected in parallel [31]. This facilitates sharing of input current and reduces the current stress in the modules. So, interleaving of AFBS is a preferable approach.

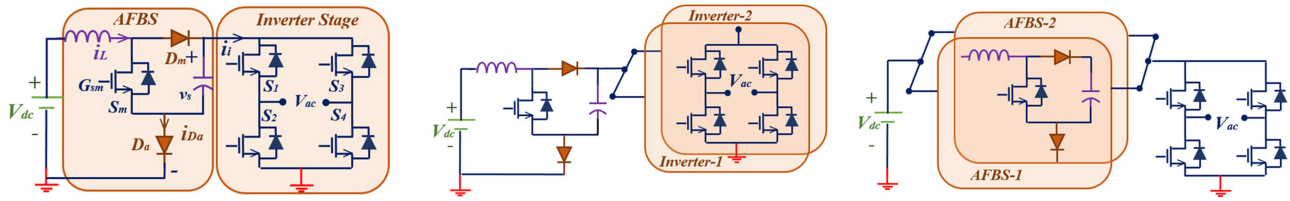


Fig. 4. (a) Schematic of CFSI. (b) Strategy 1: interleaving of inverter stage. (c) Strategy 2: interleaving of AFBS.

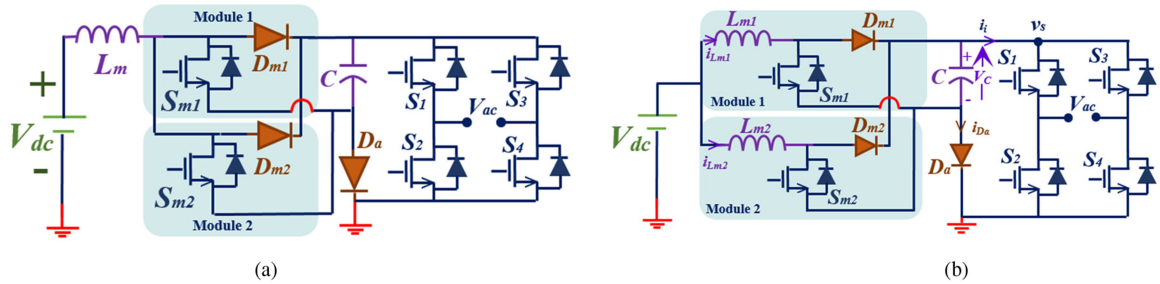


Fig. 5. Variations of strategy 2. (a) Single inductor topology. (b) ICFSI.

There are two possible schemes to implement Strategy 2 as given in Fig. 5. Scheme 1 adopts a single inductor approach. In this topology, switch (S_m) and the diode (D_m) are taken as a module and several such modules can be connected in parallel, as shown in Fig. 5(a). However, during some operating condition of this scheme, diodes (D_{m1} and D_{m2}) conduct in parallel. Because of negative temperature coefficient of diodes, paralleling will lead to thermal run away. Thus, this scheme is not feasible.

In Scheme 2, inductor (L_m), switch (S_m), and the diode (D_m) are connected to form a module, as shown in Fig. 5(b). They are connected to the common dc capacitor (C), diode (D_a), and the input source ($V_{\rm DC}$). This scheme facilitates sharing of input current among the two modules leading to improved efficiency and gain characteristics and hence of particular interest. Thus, in this article, different operating modes and the steady-state behavior of the topology along with its small signal modeling are discussed.

III. ICFSI

The realization of two-module ICFSI is shown in Fig. 5(b). In this scheme, both the modules share the input current and boost $V_{\rm dc}$ to obtain a higher dc-link voltage (V_C).

PWM intervals for ICFSI for a half-cycle of the modulating sinusoidal signal ($T_p/2$) is depicted in Fig. 6(a). As shown in the figure, PWM scheme typically has two modulated intervals: 1) power and zero intervals decided by sine PWM; and 2) ST interval decided by dc signals ($\pm V_{\rm ST}$). In CFSI, ST in the inverter legs is synchronized with the single switch (S_m) of AFBS [14].

As conveyed before, this article deals with the interleaving of CFSI, by implementing it in the AFBS. Hence, consequently, the synchronization of ST with the interleaved AFBS becomes essential. In the proposed PWM scheme, the ST signal ($G_{\rm ST}$) is alternately given to the two interleaved switches (S_{m1} and S_{m2}), as given in Fig. 6(b). For higher order modular interleaved topology, multiple dc or phased shifted carrier signals can be used to decide the synchronization. The proposed PWM scheme of ICFSI is such that, during the power interval of the inverter, diode D_a conducts and dc-link voltage appears at the input of inverter.

Fig. 6(b) shows the PWM scheme for ICFSI. Gate pulses for the inverter switches S_1–S_4 are generated by comparing $m(t)$ and $-m(t)$ with the high frequency carrier signal $V_{\rm tri}(t)$. ST in inverter legs is inserted to obtain higher gain. This ST is divided in each inverter leg to share the switching stress equally. S_2 and S_3 contribute to the ST interval in positive half cycle ($m(t) > 0$), while S_1 and S_4 contribute in negative half-cycle ($m(t) < 0$), as shown in Fig. 6(b). ST in inverter legs ($G_{\rm ST}$) is generated by comparing the dc signal $\pm V_{\rm ST}$ with $V_{\rm tri}$. Logic circuits to implement the PWM scheme are shown in Fig. 6(c) and (d).

A phase shift of 180° between the gate signals G_{sm1} and G_{sm2} are generated by comparing $V_{\rm ST}$ and $-V_{\rm ST}$ with $V_{\rm tri}$ (t), respectively. $+V_{\rm ST}$ is used to generate the gate signal (G_{sm1}) for the switch (S_{m1}) of Module 1 and insert ST in one of the inverter legs. Similarly, $-V_{\rm ST}$ is used to generate the gate signal (G_{sm2}) to turn ON the switch (S_{m2}) of Module 2 and to turn ON the switches of another inverter leg. ST in inverter legs is synchronized with the gate pulses of switch S_{m1} and S_{m2}. In case of two module interleaving, the ST signal ($G_{\rm ST}$) is alternately given to interleaved modules. For higher order modular interleaved topology, multiple dc and phase-shifted carrier signals can be used to decide the ST interval.

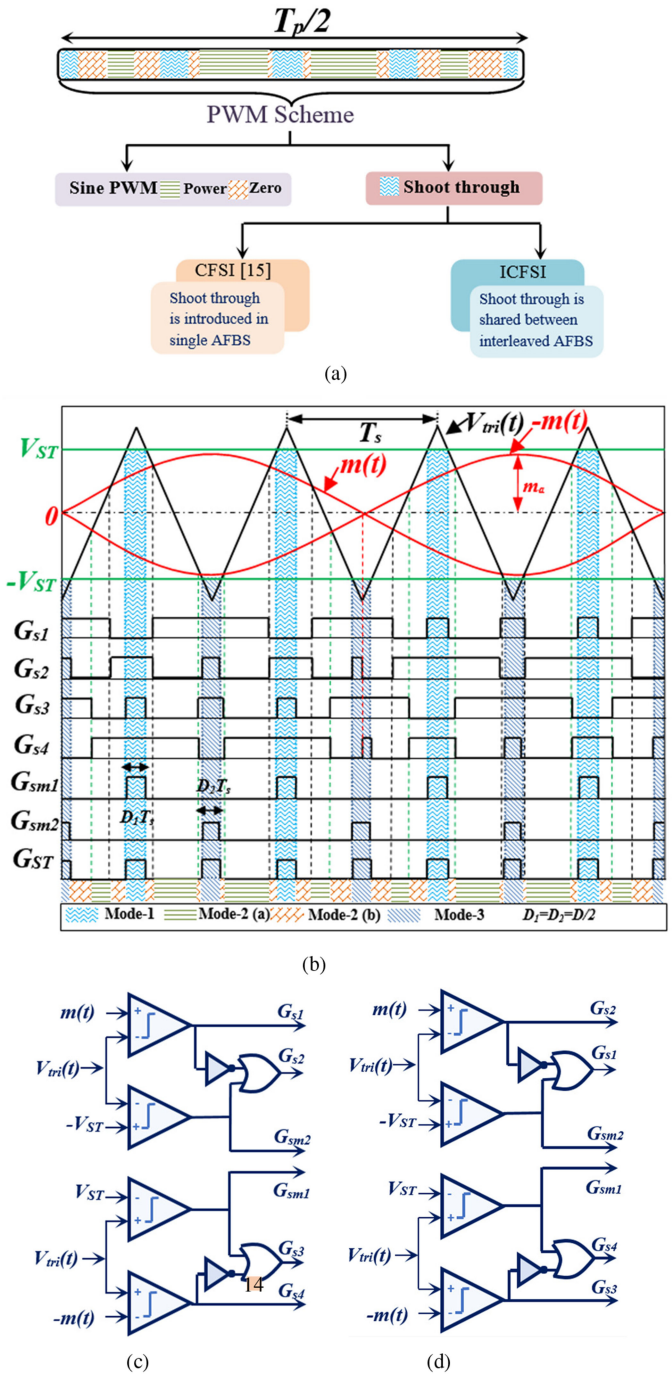


Fig. 6. (a) PWM intervals in ICFSI. (b) Proposed PWM scheme for ICFSI. (c) PWM logic circuit for $m(t) > 0$. (d) PWM logic circuit for $m(t) < 0$.

Due to the 180° phase shift between G_{sm1} and G_{sm2}, in ICFSI, ST interval (DT_s) is equally shared between two intervals (D_1T_s) and (D_2T_s). So, the switching frequency of the interleaved switches is the same as that of the carrier signal $(V_{\text{tri}}(t))$. On the contrary, switching frequency of the main switch (S_m) is twice that of $V_{\text{tri}}(t)$ in CFSI [14]. Since ST is an allowable state in ICFSI, the modulation index (m_a) of the inverter is limited by

$$D + m_a \leq 1. \tag{1}$$

TABLE III
OPERATING MODES OF ICFSI

Modes		Operating State		Conducting Devices	Figures
Mode-1 (D_1T_s)		Shoot-Through	Zero	S_{m1}, D_{m2}, S_3, S_4	Fig.7 (a)
Mode-2 ($(1-D)T_s$)	Mode 2 (a)	Non Shoot-Through	Power	D_{m1}, D_{m2}, D_a, S_1, S_4	Fig.7 (b)
	Mode 2 (b)		Zero	D_{m1}, D_{m2}, D_a, S_2, S_4	Fig.7 (c)
Mode-3 (D_2T_s)		Shoot-Through	Zero	S_{m2}, D_{m1}, S_1, S_2	Fig.7 (d)

This constraint is due to the fact that active power drawn by the inverter during ST interval is zero. The input of the inverter stage is a soft dc link which is zero during the ST interval.

A. Steady-State Analysis

1) Modes of Operation: Depending on the proposed PWM scheme, the converter operation is divided into three modes. The operating modes over a switching period of T_s, given in Table III, are depicted in Fig. 7. The steady-state analysis is done for $D_1 = D_2 = D/2$. Nonidealities, other than dc resistance (DCRs) of the inductors (L_{m1}, and L_{m2}), are considered to be zero in this analysis.

a) Mode 1 (ST Interval): The equivalent schematic of ICFSI during Mode 1 ((D_1T_s) interval) is shown in Fig. 7(a). In this interval, switches S_{m1}, S_3, and S_4 are turned ON, simultaneously. Turning ON of switch S_{m1} reverse biases the diode D_{m1} by dc-link voltage V_C and turns it OFF. Similarly, turning ON of S_3 and S_4 reverse biases the diode D_a and turns it OFF. However, diode D_{m2} is turned ON and forced to carry the inductor current i_{Lm2}. Thus, a voltage of $V_{\text{dc}} + V_C$ appears across L_{m1}, whereas a voltage of V_{dc} across L_{m2}, ideally. This explains the difference in the rising slopes of i_{Lm1} and i_{Lm2}, as depicted in Fig. 8(a) and (b).

Proposed PWM scheme, as shown in Fig. 6(b), is such that the inverter is operated in zero state during the ST interval. Thus, the input voltage of the inverter (v_s) is zero, as shown in Fig. 8(a) and (b). Inductor voltages (v_{Lm1} and v_{Lm2}) and the capacitor current (i_C) during this mode are given as follows:

$$\left.\begin{aligned} v_{Lm1}(t) &= V_{dc} + v_C - r_{L1} i_{Lm1}(t) \\ i_C(t) &= -i_{Lm1} \\ v_{Lm2}(t) &= V_{\text{dc}} - r_{L2} i_{Lm2}(t) \end{aligned}\right\}. \tag{2}$$

b) Mode 2 (Non-ST Interval): In this mode, both the boost stage switches S_{m1} and S_{m2} are turned OFF. Depending on the comparison of m(t) and $V_{\text{tri}}(t)$, Mode 2 is divided into power state and zero state as shown in Fig. 7(b) and (c), respectively. During power state, diagonal switches (S_1–S_4 or S_3–S_2) of the inverter are turned ON, as shown in Fig. 7(b). During zero state, either top (S_1–S_3) or bottom (S_2–S_4) switches of the inverter are turned ON as shown in Fig. 7(c).

In the boost stage, diodes D_{m1} and D_{m2} are forward biased and forced to carry the inductor currents i_{Lm1} and i_{Lm2}, respectively. However, diode D_a is turned ON by $(i_{Lm1} + i_{Lm2} – i_i)$ amount of current. The diode current is given in Fig. 8(c). Since

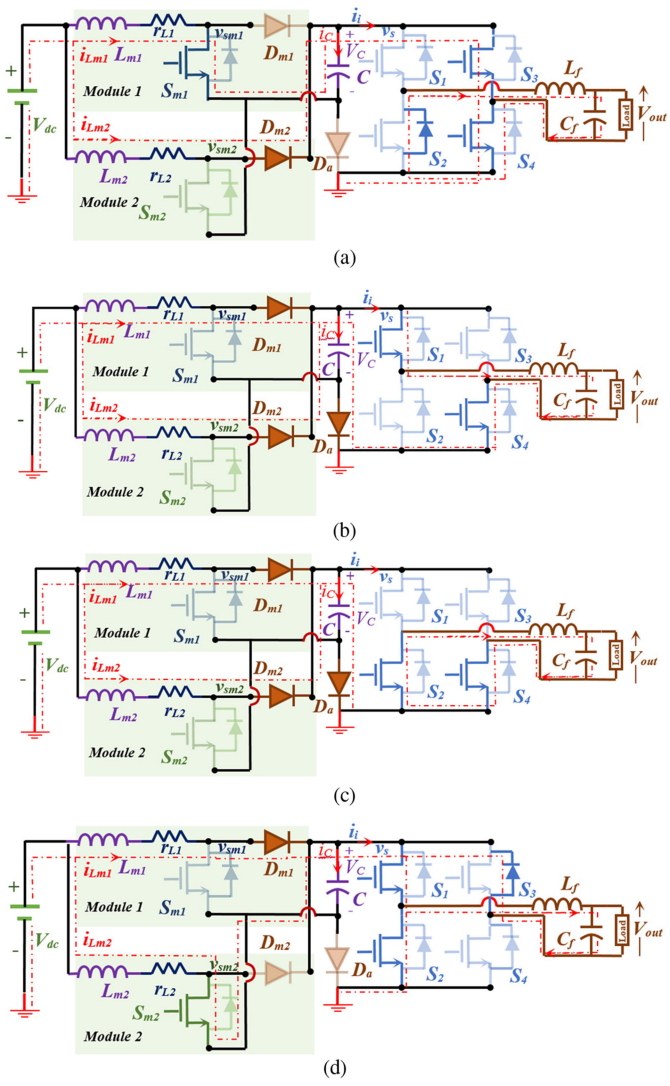


Fig. 7. Equivalent circuit diagram of the proposed ICFSI in: (a) Mode 1, (b) power state of Mode 2, (c) zero state of Mode 2, and (d) Mode 3.

diode D_a is in conduction during this mode, the input of the inverter (v_s) becomes equal to V_C, as depicted in Fig. 8(a) and (b). Inductor voltages (v_{Lm1} and v_{Lm2}) and the capacitor current (i_C) during this mode are given in (3). In this, i_i is the current drawn by the inverter stage

$$\left.\begin{aligned} v_{Lm1}(t) &= V_{\rm dc} - v_C(t) - r_{L1} i_{Lm1}(t) \\ i_C(t) &= i_{Lm1}(t) + i_{Lm2}(t) - i_i(t) \\ v_{Lm2}(t) &= V_{\rm dc} - v_C(t) - r_{L2} i_{Lm2}(t) \end{aligned}\right\}. \tag{3}$$

C) Mode 3 (ST Interval): The equivalent schematic of ICFSI during Mode 3 ((D_2T_s) interval) is shown in Fig. 7(d). It is similar to that of ST interval of Mode 1. Instead of turning ON S_{m1} in this mode, switch S_{m2} of Module 2 is turned ON along with inverter switches S_1 and S_2.

Turning ON of switch S_{m2} and one of the inverter legs reverse biases the diodes D_{m2} and D_a, respectively, and turns them OFF. However, D_{m1} is turned ON and forced to carry i_{Lm1}. Similar to Mode 1, the inverter is in zero state in this interval too. Inductor voltages (v_{Lm1} and v_{Lm2}) and the capacitor current (i_C) during this mode are given as follows:

$$\left.\begin{aligned} v_{Lm2}(t) &= V_{\rm dc} + v_C - r_{L2} i_{Lm2}(t) \\ i_C(t) &= -i_{Lm2} \\ v_{Lm1}(t) &= V_{\rm dc} - r_{L1} i_{Lm1}(t) \end{aligned}\right\}. \tag{4}$$

If the PWM scheme presented in [14] is modified, as reported in [32], conventional CFSI can be operated at an operating point, $D + m_a > 1$. On the similar lines, if the PWM scheme is altered, for ICFSI also, it is possible that $D + m_a$ is greater than 1. However, if the PWM scheme, presented in Fig. 6(b), is implemented for ICFSI operation and the inequality, $D + m_a > 1$, is imposed, then it will lead to a nonsinusoidal ac output voltage ($V_{\rm out}$). Fig. 9 gives the PLEXIM simulation results for ac output voltage ($V_{\rm out}$) and voltage before the filter circuit ($V_{\rm ac}$) for an ac gain of 3.24 with the same operating points for $D + m_a \leq 1$ as well as $D + m_a > 1$. For $D + m_a > 1$, as shown in Fig. 9, the ac output ($V_{\rm out}$) is flat topped instead of a sinusoidal signal and $V_{\rm ST} < m_a$. This results in wider ST intervals (D_1T_s and D_2T_s) by effectively reducing the actual power intervals. Consequently, the variation in the pulsewidth of $V_{\rm ac}$ is not a function of sine, thereby resulting in a flat topped signal ($V_{\rm out}$) at the output.

2) Gain Characteristics: In order to establish a relationship between V_C and $V_{\rm dc}$, (2)–(4) are averaged over a switching cycle of time period T_s. The averaging yields the following equations:

$$\langle v_{Lm1}\rangle_{T_s} = V_{\rm dc} - (1 - 2D_1 - D_2)\langle v_C\rangle_{T_s} - r_{L1}\langle i_{Lm1}\rangle_{T_s} \tag{5}$$

$$\langle v_{Lm2}\rangle_{T_s} = V_{\rm dc} - (1 - 2D_2 - D_1)\langle v_C\rangle_{T_s} - r_{L2}\langle i_{Lm2}\rangle_{T_s} \tag{6}$$

$$\begin{aligned} \langle i_C\rangle_{T_s} = {} & (1 - 2D_1 - D_2)\langle i_{Lm1}\rangle_{T_s} \\ & + (1 - 2D_2 - D_1)\langle i_{Lm2}\rangle_{T_s} - (1 - D)\langle i_i\rangle_{T_s}. \end{aligned} \tag{7}$$

Using (5)–(7), the average equivalent model is drawn in Fig. 10(a). This model is used to obtain a dc transformer model as shown in Fig. 10(b). In this model, the average value of the variables x is replaced by X. Using the dc transformer model, dc-link voltage (V_C) can be written as follows:

$$V_C = \frac{V_{\rm dc}\left[r_{L2}(1 - D_1 - D) + r_{L1}(1 - D_2 - D)\right] - I_i r_{L1} r_{L2} D'}{\left[r_{L2}(1 - D_1 - D)^2 + r_{L1}(1 - D_2 - D)^2\right]}. \tag{8}$$

Here, I_i is the average value of the inverter current (i_i). For a lossless H-bridge inverter, the average current (I_i) drawn by the inverter can be obtained by applying power balance for a unity power factor load $(R_{\rm ac})$

$$V_i I_i = \frac{{V_m}^2}{2R_{\rm ac}} = \frac{m_a^2 {V_C}^2}{2R_{\rm ac}} \Rightarrow I_i = \frac{m_a^2 V_C}{2R_{\rm ac}(1 - D)} \tag{9}$$

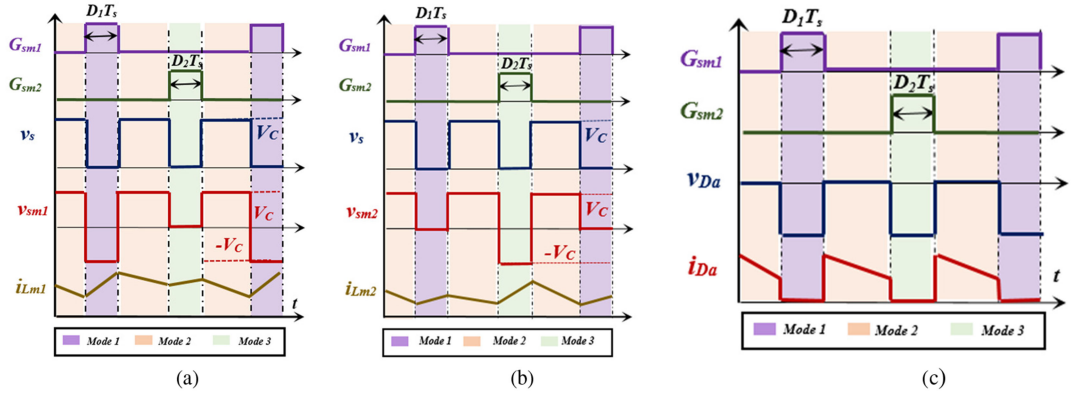


Fig. 8. (a) Steady-state waveforms of Module 1. (b) Steady-state waveforms of Module 2. (c) Switch node voltage (v_{Da}) and the current through diode (D_a).

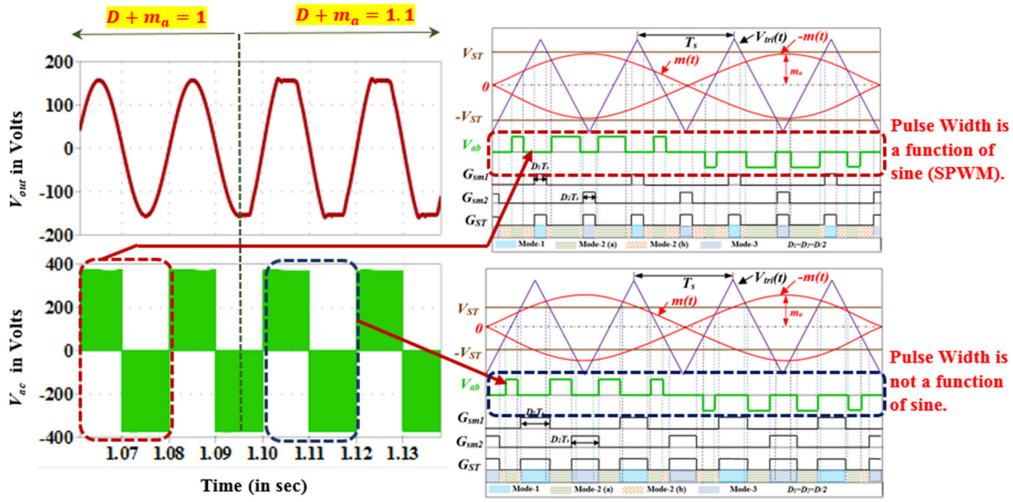


Fig. 9. PLEXIM simulation carried out for $D + m_a \leq 1$ and $D + m_a > 1$.

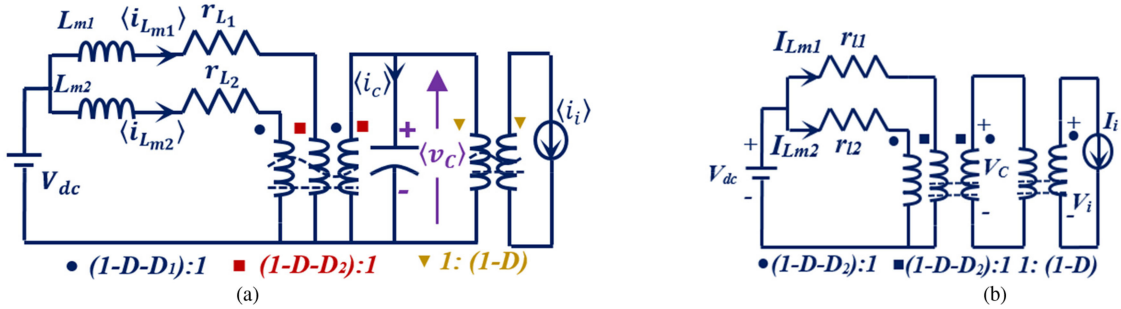


Fig. 10. (a) Average circuit model. (b) Equivalent dc transformer model of ICFSI.

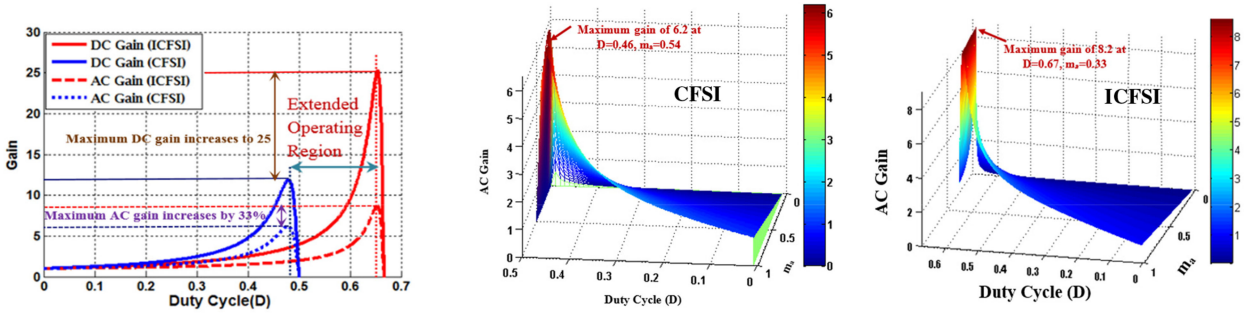
where $V_m(= m_a V_C))$ is the peak of ac output voltage. After eliminating I_i from (8), V_C can be written as follows:

$$V_C = \frac{V_{\rm dc}\left[r_{L2}\left(1-D_1-D\right)+r_{L1}\left(1-D_2-D\right)\right]}{\left[r_{L2}(1-D_1-D)^2+r_{L1}(1-D_2-D)^2\right]+\frac{r_{L1}r_{L2}m_a^2}{2R_{\rm ac}}}. \tag{10}$$

When $D_1 = D_2 = D/2$ and $r_{L1} = r_{L2} = r_L$, dc gain and ac gain $(V_m/V_{\rm dC})$ can be given as follows:

$$\text{DC gain}: \frac{V_C}{V_{\rm dc}} = \frac{1}{(1-1.5D)+\frac{m_a^2}{4R_{\rm ac}(1-1.5D)}r_L} \tag{11}$$

$$\text{AC gain}: \frac{V_m}{V_{\rm dc}} = \frac{m_a}{(1-1.5D)+\frac{m_a^2}{4R_{\rm ac}(1-1.5D)}r_L}. \tag{12}$$



(a) (b) (c)

Fig. 11. (a) Comparison of gain characteristics between CFSI ($r_L = 0.21\,\Omega$) and ICFSI (for $r_{L1} = r_{L2} = 0.21\,\Omega$.). Three-dimensional plot of ac gain with respect to D and m_a, for (b) CFSI and (c) ICFSI.

B. Comparison of Gain Characteristics of CFSI and ICFSI

DC gain $(V_C/V_{\rm dc})$ and ac gain $(V_m/V_{\rm dc})$ of both CFSI and ICFSI, using (11) and (12), are plotted for varying duty cycle (D) in Fig. 11(a). DC and AC gains are plotted for the boundary of (1), i.e, $m_a = 1 - D$. If DCR of the inductors is assumed to be zero, then the dc gain of ICFSI is $1/(1 - 1.5D)$ compared to $1/(1 - 2D)$ of CFSI [14]. Thus, the maximum gain is centered about duty cycle D of 0.66 in case of ICFSI, as it can be seen in Fig. 11(a).

Fig. 11(b) and (c) depict the three-dimensional curve, which show the relationship between ac gain with all possible combination of duty cycle (D) and the modulation index (m_a) of CFSI and ICFSI, respectively.

From Fig. 11(a), it is evident that ICFSI can be operated over a wider range of duty cycle. Theoretically, a maximum dc gain of 25 can be obtained in ICFSI. A significant increase in dc gain is observed, when compared to the maximum dc gain of 12 in CFSI. Similarly, 33% improvement in maximum ac gain can be achieved in ICFSI. As given in Fig. 11(c), a maximum ac gain of 8.2 can be obtained at the boundary $(m_a = 1 - D)$ whereas in CFSI the maximum achievable ac gain is 6.2 as shown in Fig. 11(b).

Fig. 11(a) is plotted for a r_L of 0.21 Ω. With the increase in r_L, the maximum gain reduces according to (11) and (12). Improved gain characteristic is obtained in case of ICFSI mainly due to the extended operating range of D. It is observed that operating range of D is widened by 32% in ICFSI, when compared to that of CFSI. The impact of nonideality on voltage conversion ratio considerably reduces by interleaving the inductors in ICFSI. Effective DCR of the interleaved inductors become half as compared to that of the single inductor in CFSI, when $D_1 = D_2 = D/2$.

IV. Small-Signal Analysis

A. Frequency Response of ICFSI

To obtain the small-signal model of ICFSI, the averaged equations given in (5)–(7) are perturbed around the dc operating point. $\hat{v}_{\rm dc}$, $\hat{v}_C$, $\hat{i}_{L_{m1}}$, $\hat{i}_{Lm_2}$, $\hat{i}_i$, $\hat{d}_1$, and $\hat{d}_2$ are the small perturbations near the dc operating bias points $V_{\rm dc}$, V_C, I_{Lm1}, I_{Lm2}, I_i, D_1, and D_2, respectively. After addition of small-signal perturbations in (5)–(7), the higher order terms are neglected. Equating the ac terms, (5)–(7) can be written as

$$L_1\frac{d\hat{i}_{Lm_1}}{dt} = \hat{v}_{\rm dc} - r_{L_1}\hat{i}_{L_{m1}} - \hat{v}_C\left(1 - 2D_1 - D_2\right) + V_C\left(2\hat{d}_1 + \hat{d}_2\right) \tag{13}$$

$$L_2\frac{d\hat{i}_{Lm_2}}{dt} = \hat{v}_{\rm dc} - r_{L_2}\,\hat{i}_{Lm_2} - \hat{v}_C\left(1 - 2D_2 - D_1\right) + V_C\left(\hat{d}_2 + 2\hat{d}_1\right) \tag{14}$$

$$C\frac{d\hat{v}_C}{dt} = \hat{i}_{L_{m1}}\left(1 - 2D_1 - D_2\right) - I_{Lm_1}\left(2\hat{d}_1 + \hat{d}_2\right) + \hat{i}_{Lm_2}\left(1 - 2D_2 - D_1\right) - I_{Lm_2}\left(\hat{d}_1 + 2\hat{d}_2\right) - \hat{i}_i\left(1 - D_1 - D_2\right) + I_i\left(\hat{d}_1 + \hat{d}_2\right). \tag{15}$$

Using (13)–(15), the small-signal model of ICFSI is drawn as shown in Fig. 12(a). Expressions for I_x, $V_{x_{m1}}$, $V_{x_{m2}}$ are given in the Appendix. There are two control variables ($\hat{d}_1$ and $\hat{d}_2$) in the system. Using Laplace transformations in (13)–(15), $\hat{v}_C(s)$, $\hat{i}_{Lm_1}(s)$, $\hat{i}_{Lm_2}(s)$ can be given as follows:

$$\begin{bmatrix} \hat{v}_C(s) \\ \hat{i}_{Lm_1}(s) \\ \hat{i}_{Lm_2}(s) \end{bmatrix} = \begin{bmatrix} G_{vd1}(s) & G_{vd2}(s) & G_i(s) & G_a(s) \\ G_{id11}(s) & G_{id12}(s) & G_{im1}(s) & G_{a1}(s) \\ G_{id12}(s) & G_{id22}(s) & G_{im2}(s) & G_{a2}(s) \end{bmatrix} \times \begin{bmatrix} \hat{d}_1(s) \\ \hat{d}_2(s) \\ \hat{i}_i(s) \\ \hat{v}_{dc}(s) \end{bmatrix}.$$

In Fig. 12(b), perturbations in $V_{\rm dc}$ ($\hat{v}_{\rm dc}$), and I_i ($\hat{i}_i$) are considered to be zero. The open-loop transfer functions of the system can be written as follows:

$$G_{vd1}(s) = \left.\frac{\hat{v}_C(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2=0} = G_{d1}\,\frac{\left(1 + a_1 s + a_2 s^2\right)}{\left(1 + b_1 s + b_2 s^2 + b_3 s^3\right)} \tag{16}$$

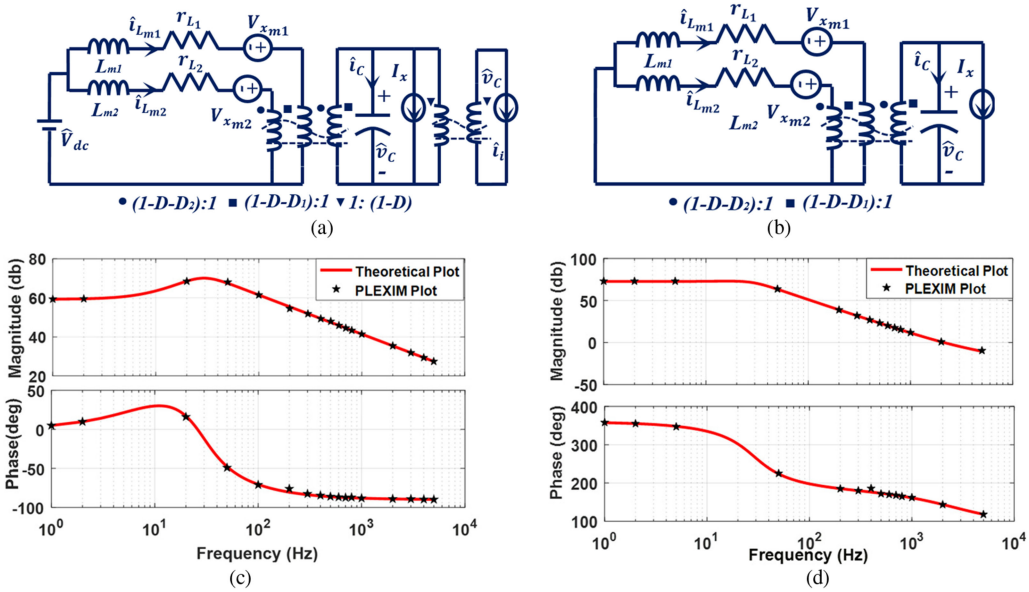


Fig. 12. (a) Complete small-signal model of ICFSI. (b) Small-signal model of ICFSI with $\hat{v}_{\rm dc} = 0$ and $\hat{i}_i = 0$. Verification of magnitude and phase plot of (c) $G_{id11}(s)$, and (d) $G_{vd1}(s)$ by PLEXIM simulation.

$$G_{vd2}(s) = \left.\frac{\hat{v}_C(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1=0} = G_{d2}\frac{\left(1+a_3s+a_4s^2\right)}{\left(1+b_1s+b_2s^2+b_3s^3\right)} \tag{17}$$

$$G_{id11}(s) = \left.\frac{\hat{i}_{Lm_1}(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2=0} = G_{i_1}\frac{\left(1+a_{x1}s+a_{x2}s^2\right)}{\left(1+b_1s+b_2s^2+b_3s^3\right)} \tag{18}$$

$$G_{id22}(s) = \left.\frac{\hat{i}_{Lm_2}(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1=0} = G_{i_2}\frac{\left(1+a_{y1}s+a_{y2}s^2\right)}{\left(1+b_1s+b_2s^2+b_3s^3\right)}. \tag{19}$$

The expressions of the coefficients and gains in (16)–(19) are given in the Appendix. The open-loop transfer functions in ICFSI are third-order transfer functions with right-half zeros, owing to the boost nature of the topology. From the small-signal analysis, it can be inferred that, by paralleling the interleaved modules, order of the system increases. A two-module interleaving results in a third-order system. The system has two zeros and three poles. Location of poles depend on the parameters of the converter such as L_{m1}, L_{m2}, and C. Location of zeros are decided by the dc operating points of the converter.

The small-signal model, as depicted in Fig. 12(b), is verified by PLEXIM simulation software. For $L_1 = L_2$, $D_1 = D_2$, and $r_{L1} = r_{L2}$, transfer functions G_{vd1}, G_{vd2} and G_{id11}, G_{id22} are equal. Thus, the transfer functions G_{id11} and G_{vd1} given in (16) and (18) are plotted in Fig. 12(c) and (d), respectively. Data points obtained from the simulation, with perturbations in duty cycles, are also plotted in the figures. The comparison between the two is done at the dc bias point of $D = 0.59$, $V_{\rm dc} = 48$ V, $V_{\rm out} = 110$ V, $R_{\rm ac} = 36\ \Omega$. It is observed that both the magnitude and phase plots are consistent.

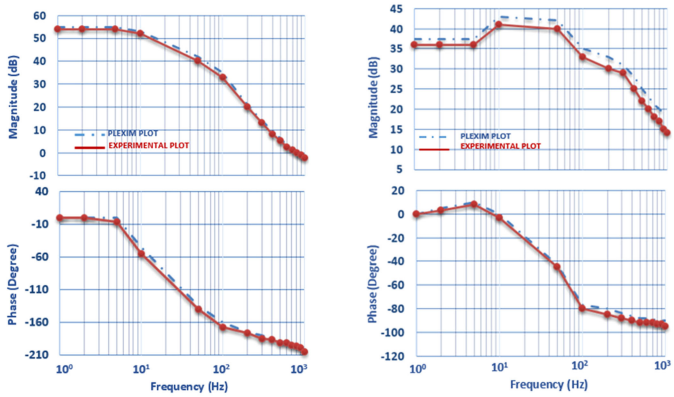


Fig. 13. Comparison of Bode plots of (a) $G_{vd1}(s)$, and (b) $G_{id11}(s)$ obtained experimentally and from PLEXIM simulation at dc bias point of $D = 0.59$, $V_{\rm dc} = 5$ V, $V_{\rm out} = 11$ V, $R_{\rm ac} = 36\ \Omega$.

The comparison of bode data of $G_{vd1}(s)$, and $G_{id11}(s)$ obtained experimentally using frequency response analyzer and the data obtained from PLEXIM simulation is given in Fig. 13(a) and (b), respectively. As given in Fig. 13, the experimental bode plot is consistent with the plot obtained from PLEXIM data. The experiment is conducted at relatively lower power rating and the comparison with the simulation data is carried out at the same power.

B. Voltage Mode Closed-Loop Control

The closed-loop voltage control in ICFSI is implemented in PLEXIM simulation software. Fig. 14(a) shows the control block diagram of ICFSI operating in stand-alone mode for solar roof top applications. In stand-alone mode, dc and ac voltages are controlled independently. DC-link voltage (V_C) is sensed and

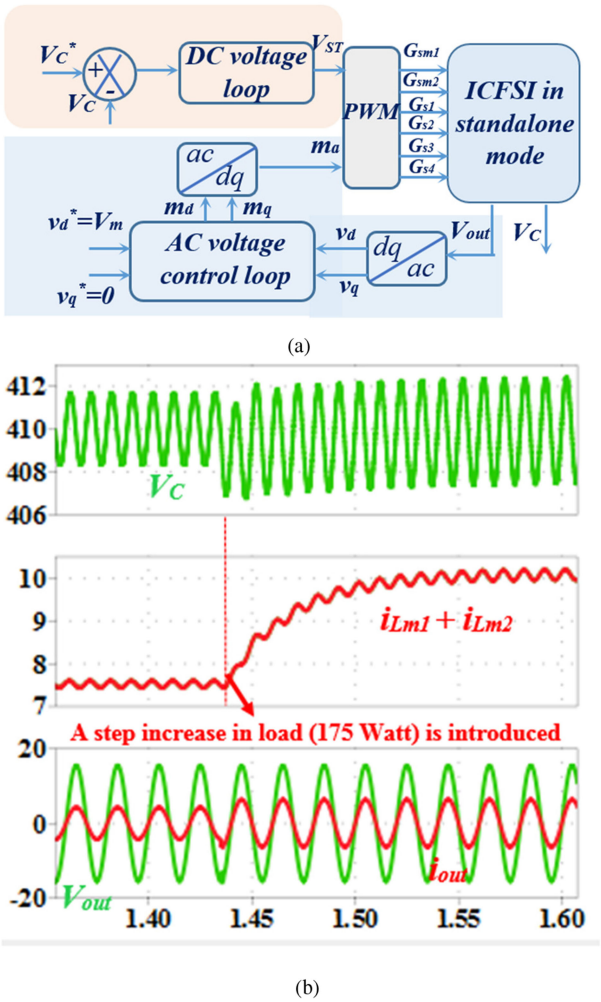


Fig. 14. (a) Control block diagram. (b) PLEXIM simulation results of dc-link voltage (V_C), inductor currents ($i_{Lm1} + i_{Lm2}$), ac output voltage (V_{out}), and load current (i_{out}).

compared to the reference value (V_C^*) and fed to the controller. The controller output (V_{ST}) is used in the PWM scheme, as given in Fig. 6(b), in order to decide the ST interval (D).

In ac-side control, modulation index (m_a) is used as the control variable to regulate the ac output voltage (V_{out}). V_{out} is sensed and transformed into *dq* domain to implement the controller. The controller output generates the corresponding modulation indices (m_d and m_q) in *dq* domain. The modulation index (m_a), obtained from inverse *dq* transformation, is used in the PWM scheme [see Fig. 6(b)], in order to decide the non-ST interval (power and zero interval).

Fig. 14(b) shows the PLEXIM simulation results for the voltage mode closed-loop control. At $t = 1.44$ s, a step increase in load of 175 W is introduced. As a consequence, the load current (i_{out}) increases from 1.46 to 3 A (rms value) leading to an increase in the inductor current ($i_{Lm1} + i_{Lm2}$) from 7.5 to 10 A. However, the dc voltage controller ensures the regulation of mean dc-link voltage (V_C) at the reference of 410 V (V_C^*). Increase in load current as well as inductor current leads to increase in second harmonic ripple in V_C. Similarly, the ac voltage controller regulates the peak value of ac output voltage (V_m) at the reference of 155 V (V_m^*). In Fig. 14(b), V_{out} is scaled by 0.1 in order to plot the voltage (V_{out}) and current (i_{out}) in the same axis. Parameters for implementing the control in simulation are given in Table IV.

TABLE IV
OPERATING CONDITIONS AND PARAMETERS IN PLEXIM SIMULATION

Operating Conditions		Parameters			
Input Voltage (V_{dc})	48 V	L_{m1}	1.49 mH	L_f	727 µH
				C_f	10 µF
Output Voltage (V_{out})	110 V, 50 Hz	L_{m2}	1.45 mH	*Step change in load (R_{ac})*	75 Ω to 36 Ω
DC link Voltage (V_C)	410 V	C	470 µF	*Step change in load (i_{out})*	1.46 A to 3 A

V. Loss Analysis

To establish a comparative analysis between ICFSI and CFSI, in terms of efficiency, categorization of various losses is carried out for different frequencies and duty cycles in Figs. 15 and 16. To compare the efficiency, CFSI and ICFSI are operated at the boundary of (1). Losses in the inverter stage are insignificant as compared to AFBS. Hence, inverter stage losses are not taken into account in this analysis.

Detailed loss analysis with the mathematical expressions is given in Table V. The comparative analysis between CFSI and ICFSI in terms of loss is carried out at a power rating of 500 W. The parameters for the comparison are listed in the table. Stepwise calculation of the steady-state parameters (D, V_C, I_L, I_{Lm1}, and I_{Lm2}) is presented in the table. Based on the calculation, various losses as categorized in Figs. 15 and 16 are calculated as per the mathematical expressions mentioned in the table.

Fig. 15(a) shows the distribution of losses in different components of ICFSI for a power output of 500 W at three operating duty cycles ($D = 2D_1 = 2D_2$). It is observed that the conduction loss in inductor DCR, for constant output power, is almost the same for all duty cycles. Since D_{m1}, D_{m2}, and D_a conduct for $(1 - D_1)T_s$, $(1 - D_2)T_s$, and $(1 - D)T_s$ durations, respectively, their losses increase as D decreases. However, the conduction loss in switches (S_{m1} and S_{m2}) decreases with the decrease in duty cycle owing to its proportionality to R_{dson} and D. Since the R_{dson} of the switches are very small, decrease in conduction loss in switches is insignificant as compared to other losses. Moreover, decreasing duty cycle reduces the dc-link voltage, thereby lowering the voltage stress across the switches. This reduces the switching loss. From Fig. 15(a), it is evident that the increase in conduction loss in D_a with the decrease in D is prevalent. Thus, better efficiencies are obtained at higher D for all power levels. The variation of efficiency with power output for different D is plotted in Fig. 16(a).

Fig. 15(b) shows an analysis comparing the losses in CFSI and ICFSI for a power output of 500 W. To achieve a fixed ac gain of 3.24, the analysis is carried out at different operating conditions in case of ICFSI ($D = 0.58$, $m_a = 0.418$) and CFSI

TABLE V
CALCULATION OF VARIOUS LOSSES IN CFSI AND ICFSI

Parameters of converters	***CFSI***	V_{dc}= 48 V, L=1 mH, C=1 μf, r_L=0.21 Ω, r_{dson}=65 mΩ, r_d=50 mΩ, V_f=1.8 V, t_{con}=11 ns, t_{coff}=9 ns
	ICFSI	V_{dc}= 48 V, L_1=1 mH, L_2=1 mH, C=1 μf, r_{L1}=r_{L2}=r_L= 0.21 Ω, r_{dson}=65 mΩ, r_d=50 mΩ, V_f=1.8 V, t_{con}=11 ns, t_{coff}=9 ns

Operating points with an AC gain of 3.24 (P=500 W, V_{dc}=48 V, V_{OUT}=110 V, V_m= 155.56 V, R_{ac}=V_m^2/2P)

CFSI	**Step-1** **Duty Cycle (D)**	$a = 4 + \frac{r_L}{2R_{ac}} - 2\,{}^{V_{dc}}/_{V_m}$ $b = -(4 + \frac{r_L}{R_{ac}} - 3\,{}^{V_{dc}}/_{V_m})$ $c = 1 + \frac{r_L}{2R_{ac}} - {}^{V_{dc}}/_{V_m}$ $D = \frac{(-b) - \sqrt{b^2 - 4*a*c}}{2(a)}$	**Step-2** **DC link voltage (V_C)**	$V_C = \frac{V_{dc}(1-2D)}{(1-2D)^2 + \frac{r_L}{2R_{ac}}(1-D)^2}$	**Step-3** **Inductor Current (I_L or I_{Lm1}, I_{Lm2})**	$I_L = \frac{(1-D)^2}{2 * R_{ac}(1-2D) * V_C}$
ICFSI		$a_1 = 2.25 + \frac{r_L}{4R_{ac}} - 1.5\,{}^{V_{dc}}/_{V_m}$ $b_1 = -(3 + \frac{r_L}{2R_{ac}} - 2.5\,{}^{V_{dc}}/_{V_m})$ $c_1 = 1 + \frac{r_L}{4R_{ac}} - {}^{V_{dc}}/_{V_m}$ $D = \frac{(-b_1) - \sqrt{{b_1}^2 - 4*a_1*c_1}}{2(a_1)}$ $D_1 = D_2 = {}^{D}/_{2}$		$x = {}^{0.5 * r_{L1} * r_{L2} * pf^2 * {m_a}^2}/_{R_{ac}}$ $V_C = \frac{V_{dc}[r_{L2}(1-D_1-D) + r_{L1}(1-D_2-D)]}{r_{L2}(1-D_1-D)^2 + r_{L1}(1-D_2-D)^2 + x}$ Where $m_a = 1-D$, $pf = 1$		$I_{Lm1} = {}^{V_{dc}[r_{L1}(D_1-D_2)(1-D-D_2)+(x)]}/_{r_{L1}} \Big/ {}^{r_{L2}(1-D_1-D)^2 + r_{L1}(1-D_2-D)^2 + x}$ $I_{Lm2} = {}^{V_{dc}[r_{L1}(D_1-D_2)(1-D-D_2)+(x)]}/_{r_{L2}} \Big/ {}^{r_{L2}(1-D_1-D)^2 + r_{L1}(1-D_2-D)^2 + x}$

Loss Calculation	CFSI	ICFSI
Conduction loss in switches	${I_L}^2 D r_{dson}$	$r_{dson}[({I_{Lm1}}^2 D_1) + ({I_{Lm2}}^2 D_2)]$
Switching loss in switches	$0.5 I_L * V_C * 2 f_s (t_{con} + t_{coff})$	$0.5 * 2 f_s (t_{con} + t_{coff})[I_{Lm1} + I_{Lm2}]$
Conduction loss in inductor	${I_L}^2 r_L$	$({I_{Lm1}}^2 r_{L1}) + ({I_{Lm2}}^2 r_{L2})$
Conduction loss in diode (D_a)	$[I_L(1-D)V_f] + [{I_L}^2(1-D)r_d]$	$[(I_{Lm1} + I_{Lm2})^2(1-D)r_d] + [(I_{Lm1} + I_{Lm2})(1-D)V_f]$
Conduction loss in diodes	$[I_L(1-D)V_f] + [{I_L}^2(1-D)r_d]$	$[\{{I_{Lm1}}^2(1-D+D_1)r_d\} + \{I_{Lm1}(1-D+D_1)V_f\}] + [\{{I_{Lm1}}^2(1-D+D_1)r_d\} + \{I_{Lm1}(1-D+D_1)V_f\}]$

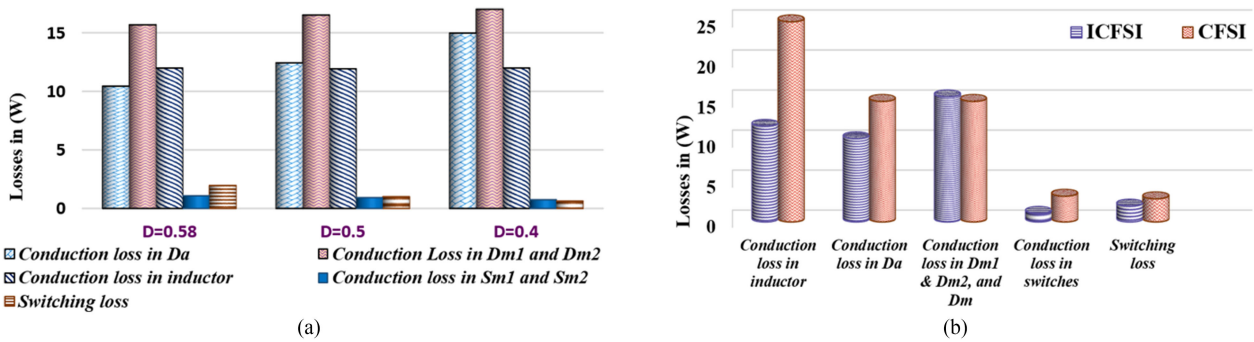


Fig. 15. (a) Distribution of losses in the boost stage of ICFSI. (b) Comparison of losses between ICFSI and CFSI at 500 W.

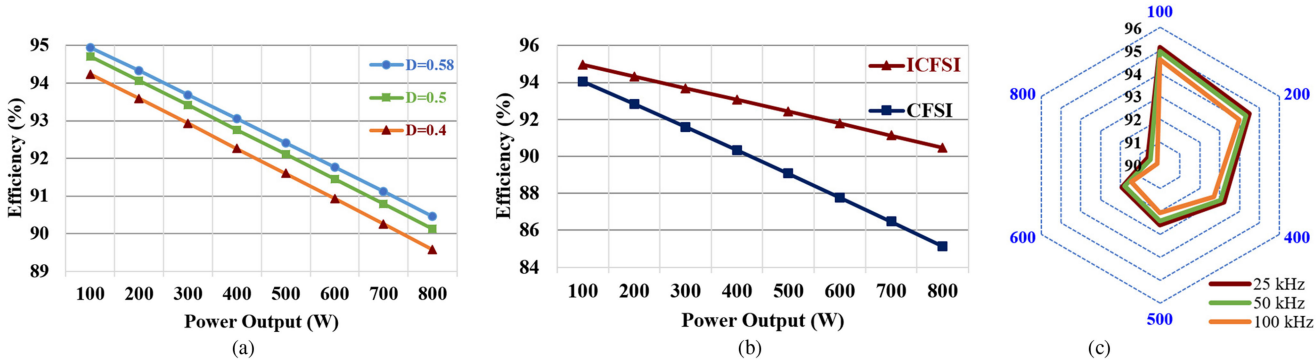


Fig. 16. (a) Efficiency curve of ICFSI at different values of D. (b) Efficiency versus power curve of CFSI and ICFSI. (c) Efficiencies for an ac gain of 3.24 at different power levels (100–800 W) at three different switching frequencies.

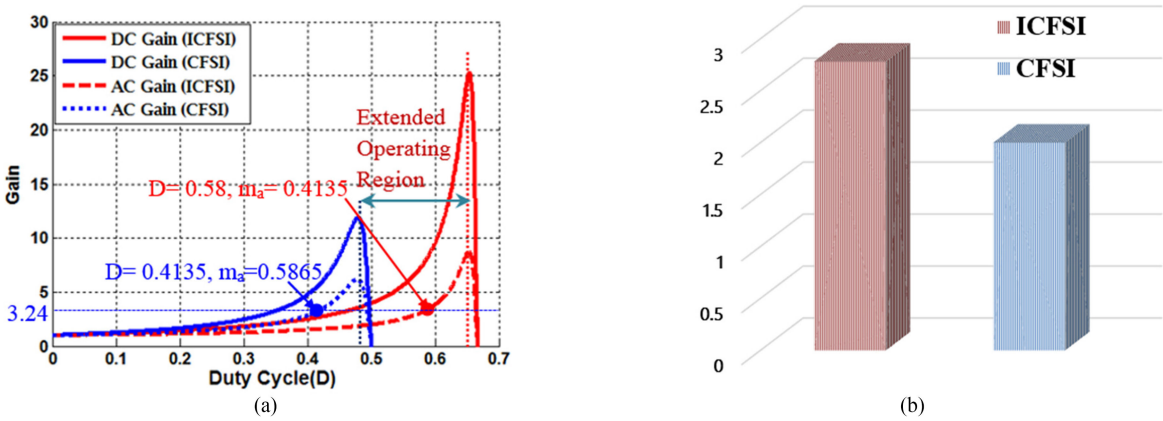


Fig. 17. (a) Operating points to achieve an ac gain of 3.24. (b) Comparison between CFSI and ICFSI in terms of THD.

($D = 0.4135$, $m_a = 0.586$). Interleaving facilitates sharing of input current by two inductors in ICFSI, whereas single inductor carries the entire current in CFSI. This reduces the conduction loss approximately by 50% in inductors of ICFSI. As a result of interleaving, the current flowing through the switches (S_{m1} and S_{m2}) is halved as compared to that of S_m. Along with the reduction in current, the conduction period of the switches is also lowered by 30% in ICFSI. Therefore, conduction loss in S_{m1} and S_{m2} also decreases. As discussed in Section III, switching frequency of boost stage switches in ICFSI reduces to half. However, the voltage stress across the switches increases slightly due to higher D in case of ICFSI. The dominance of reduction in both switching frequency and current, of S_{m1} and S_{m2}, over the rise in voltage stress reduces the combined switching loss.

It can also be inferred from Fig. 15(b) that the conduction loss in D_{m1} and D_{m2} of ICFSI is relatively higher as compared to conduction loss in D_m. This conduction loss depends on the current through the diode and its conduction period. In case of ICFSI, conduction periods of D_{m1} and D_{m2} are 21% higher and the current is half as compared to that of D_m in CFSI. The dominance of increase in conduction periods over the reduction in current justifies the increase in combined conduction loss of diodes D_{m1} and D_{m2}. However, D_a in both CFSI and ICFSI carry equal current for the same $(1 - D)T_s$ interval. The decrease in conduction loss in D_a of ICFSI, as given in Fig. 15(b), is attributed to the higher value of D for the fixed ac gain (3.24). Switching loss of diodes is not taken into account in the analysis due to negligible reverse recovery loss in SiC devices (C3D10065A).

Efficiencies of CFSI and ICFSI are compared in Fig. 16(b) for different power rating. It is observed that, as power rating goes up, ICFSI has a better performance in terms of efficiency. At 600 W, 4% improvement in efficiency is achieved as a result of interleaving. Variation of efficiency of ICFSI for different switching frequency and power levels is depicted in Fig. 16(c). It is observed that efficiency of ICFSI decreases slightly with increase in switching frequency due to increase in switching loss.

VI. Comparison With CFSI

A. Gain Ratio

The ac and dc gains of CFSI and ICFSI are compared in Fig. 17(a). It is evident from the figure that, at duty cycles lower than 0.5, CFSI has higher ac and dc gains. However, the operating region is limited up to $D = 0.5$ for CFSI. The maximum ac and dc gains that can be achieved are higher in ICFSI.

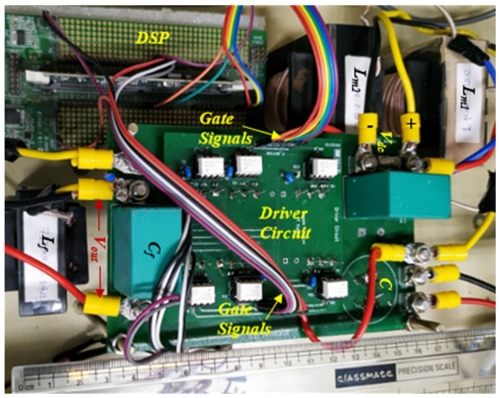


Fig. 18. Experimental prototype.

B. Voltage Stress

Voltage stress across the switches, diodes, and capacitor of the FBS in both CFSI and ICFSI depends on the dc gain of the converter. The switches and the diodes have to block the dc-link voltage (V_C), when they are turned OFF as discussed in Section III (modes of operation).The operating points to obtain an ac gain of 3.24 are identified in Fig. 17(a). To achieve the same ac output voltage (110 V), ICFSI requires a higher duty cycle, as evident from the figure. This leads to higher dc gain and consequently to higher voltage stress in ICFSI.

To achieve an ac gain of 3.24, voltage stress in ICFSI is 33% higher as compared to that of CFSI. However, the increase in voltage stress in ICFSI is compensated by decrease in switching frequency, while considering the contribution of voltage stress in switching loss.

C. THD

As shown in Fig. 17(b), THD in ICFSI is slightly higher as compared to that of CFSI. This can be attributed to the fact that to obtain same ac output voltage, modulation index (m_a) is less in ICFSI, as shown in Fig. 17(a). This leads to a slightly higher harmonic distortion in ICFSI.

VII. Experimental Results and Analysis

A prototype of 600 W, as shown in Fig. 18, has been developed to validate the proposed interleaved topology. Digital signal processor (*TMS320F28335*) is used to implement the proposed PWM scheme, introduced in Fig. 6(b). Wide band gap devices (SiC) have been used to operate the converter at higher switching frequency. Table VI lists the operating condition and components used in the experiments. 110-V ac output voltage is obtained from the dc input voltage of 48 V. The voltage levels and power rating of the converter are chosen so as to fit in stand-alone roof-top PV applications.

Proposed PWM scheme is implemented in the EPWM module of DSP to generate the gate pulses for the switches as shown in Fig. 19. It is observed that the gate pulse of the switches S_{m1} and S_{m2} is shifted by 180° as discussed in theory. It also shows that G_{sm1} and G_{sm2} are synchronized with gate pulse of

TABLE VI
Operating Conditions and Parameters in Experimental Prototype

Operating Conditions		Parameters			
Input Voltage (V_{dc})	48 V	L_{m1}	1.49 mH	L_f	727 µH
				C_f	10 µF
Output Voltage (V_{out})	110 V, 50 Hz	L_{m2}	1.45 mH	D_{m1}, D_{m2}, D_a	C3D10065A
Switching frequency	25-100 kHz	C	470 µF	S_{m1}, S_{m2}, S_1, S_2, S_3, S_4	C3M0065090

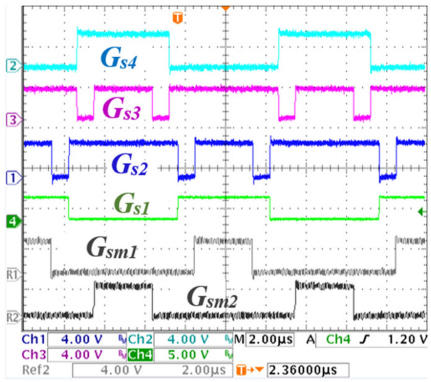


Fig. 19. PWM pulses for the gates of the switches.

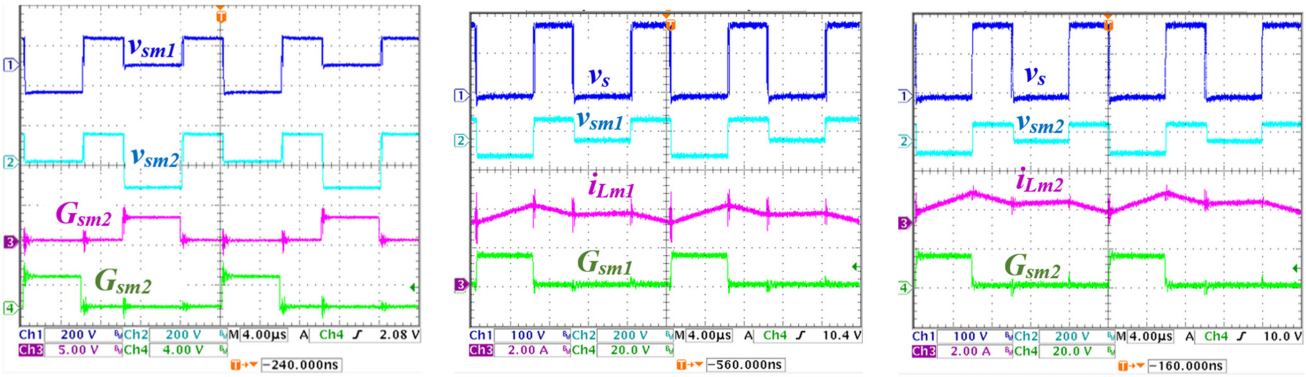
inverter switches, G_{s1}–G_{s4}. In Fig. 19, gate pulses are shown only for $m(t) > 0$, where the ST interval is added in G_{s2} and G_{s3}, alternately, similar to Fig. 6(b).

Fig. 20(a)–(c) depicts the steady-state waveforms of two interleaved modules. Gate voltages (G_{sm1} and G_{sm2}), switch node voltages (v_{sm1} and v_{sm2}), and the inductor currents (i_{Lm1} and i_{Lm2}) of both the modules of ICFSI are shown in the figure. Inductor current waveforms, as shown in Fig. 20(b) and (c), have three different slopes due to three operating modes. These experimental results are consistent with the theoretical analysis given in Figs. 7 and 8.

The prototype was also operated at three different switching frequencies to study the impact of increase in switching frequency. Fig. 21(a)–(c) gives the steady-state waveforms obtained at different switching frequencies, i.e., 25, 50, and 100 kHz. As shown in Fig. 21, with the increase in switching frequency, the switching frequency component in the inductor currents and capacitor voltage reduces.

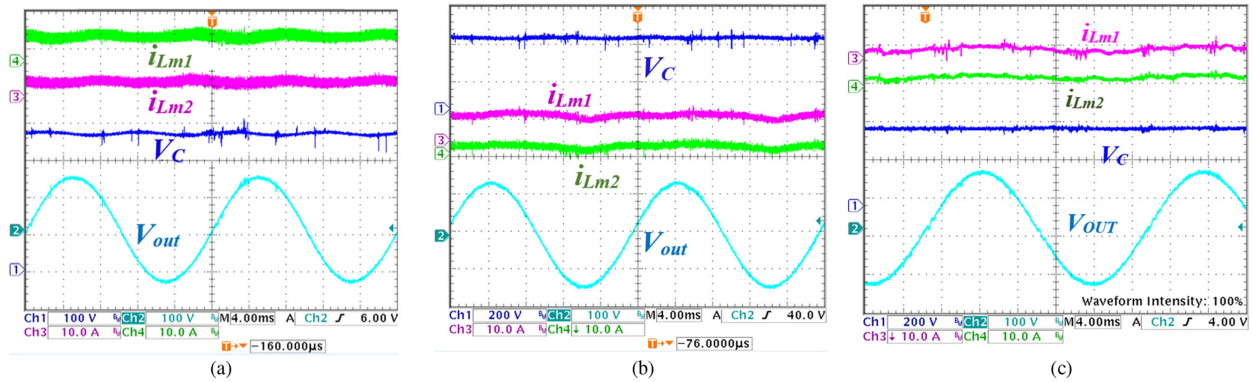
Currents in the interleaved inductors of input stage (i_{Lm1} and i_{Lm2}) contain both the second harmonic (100 Hz) and switching frequency component as evident from Fig. 21. Similarly, the second harmonic ripple is also noticeable in the capacitor voltage (V_C). This is due to the fact that the input inductors (L_{m1} and L_{m2}) and the capacitor (C) act as the low-frequency energy storage elements to cater to the mismatch between the instantaneous ac output power and the dc input power [33]. Moreover, increasing switching frequency does not affect this second harmonic component. Hence, inductors (L_{m1} and L_{m2}) with large values, as listed in Table VI, are designed to accommodate the second harmonic ripple.

The proposed topology is also validated by operating at different type of loads, as shown in Fig. 22. An ac gain of 3.24



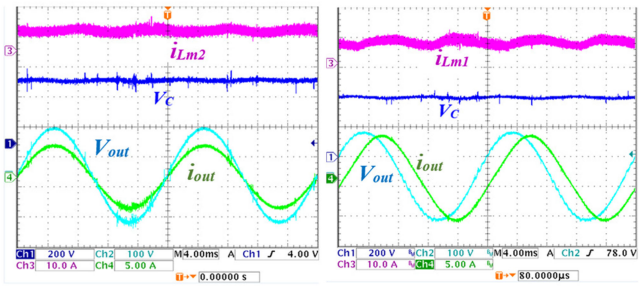
(a) (b) (c)

Fig. 20. (a) Switch node voltages (v_{sm1} and v_{sm2}) and PWM pulses for switches S_{m1} and S_{m2}. Steady-state waveforms in switching cycle of (b) Module 1 and (c) Module 2.



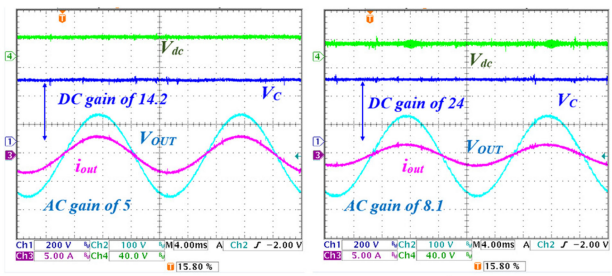
(a) (b) (c)

Fig. 21. Steady-state waveforms of both the inductor currents (i_{Lm1} and i_{Lm2}), capacitor voltage (V_C), and ac output voltage (V_{out}) at different switching frequencies: (a) 25, (b) 50, and (c) 100 kHz.



(a) (b)

Fig. 22. Operation of the converter at $f_s = 25$ kHz supplying (a) unity power factor load and (b) 0.866 lagging load.



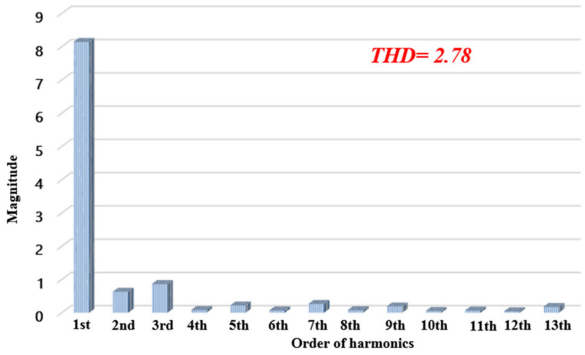
(a) (b)

Fig. 23. Verification of high gain at (a) duty cycle (D) 0.62 and modulation index (m_a) 0.36, and (b) duty cycle (D) 0.64 and modulation index (m_a) 0.34.

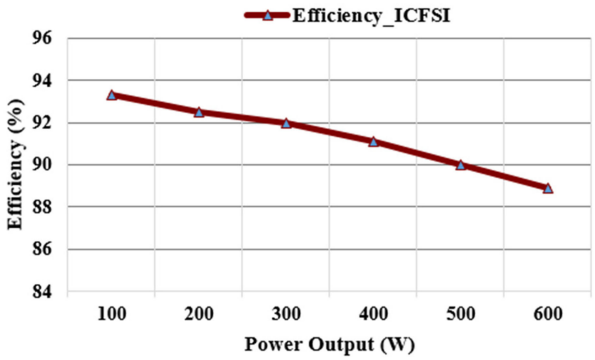
is achieved at a duty cycle (D) of 0.59 and a modulation index (m_a) of 0.4, which validates (12). Fig. 22(a) and (b) depicts the steady-state waveforms of the converter at a unity power load and a 0.866 lagging load, respectively.

To verify the gain ratio of ICFSI further, the converter is operated at the operating points ($D = 0.62$, $m_a = 0.36$ and $D = 0.64$, and $m_a = 0.34$). A dc gain of 14.2 and an ac gain of 5 is achieved at the operating point ($D = 0.62$, $m_a = 0.36$), as shown in Fig. 23(a). Fig. 23(b) shows that a dc gain of 24 and an ac gain of 8.1 are achieved at the operating point ($D = 0.62$, $m_a = 0.36$).

The experimental THD, at a power rating of 500 W, is given in Fig. 24(a). Experimental data up to 13th harmonics, obtained from a power analyzer (PA1000), are plotted in the figure. The THD in ICFSI is found to be 2.78. Measured efficiency of ICFSI up to 600 W is given in Fig. 24(b). The difference between the analytical efficiency and the measured efficiency can be attributed to the loss in the inverter stage (which is not considered in the analysis).



(a)



(b)

Fig. 24. (a) Experimental THD of ICFSI. (b) Measured efficiency versus power of ICFSI.

VIII. Conclusion

This article proposed an interleaved topology for CFSI. Performance analysis of the converter was done in the presented work. Steady-state behavior of the topology with the proposed PWM scheme and the gain characteristics was discussed. Small-signal analysis and the verification of the same were also carried out. Performance comparison of ICFSI and CFSI was done in terms of voltage conversion ratio and efficiency. It is concluded that, in ICFSI, 33% increment in the maximum ac gain and a 4% improvement in efficiency at 600 W are achieved.

Appendix

$$G_{d1} = \Psi_{m1}/\Delta, \quad G_{d2} = \Psi_{m2}/\Delta,$$

$$G_{i1} = \beta_{m1}/\Delta, \quad G_{i2} = \beta_{m2}/\Delta$$

$$\begin{aligned}\beta_{m1} = {} & (1-D-D_1)(2I_{L1}+I_{L2}-I_i)r_{L2} \\ & + (1-D-D_2)(1-3D_2)V_C\end{aligned}$$

$$\begin{aligned}\beta_{m2} = {} & (1-D-D_2)(2I_{L2}+I_{L1}-I_i)r_{L1} \\ & + (1-D-D_1)(1-3D_1)V_C\end{aligned}$$

$$\begin{aligned}\Psi_{m1} = {} & V_C r_{L1}(1-D-D_2) + 2V_C r_{L2}(1-D-D_1) \\ & - r_{L1}r_{L2}(I_{L2}+2I_{L1}-I_i)\end{aligned}$$

$$\begin{aligned}\Psi_{m2} = {} & V_C r_{L2}(1-D-D_1) + 2V_C r_{L1}(1-D-D_2) \\ & - r_{L1}r_{L2}(I_{L1}+2I_{L2}-I_i)\end{aligned}$$

$$\Delta = r_{L1}(1-D-D_2)^2 + r_{L2}(1-D-D_1)^2$$

$$\begin{aligned}a_1 = {} & [L_1V_C(1-D-D_2) + 2V_C L_2(1-D-D_1) \\ & - (L_1r_{L2}+L_2r_{L1})(2I_{L1}+I_{L2}-I_i)]/\Psi_{m1}\end{aligned}$$

$$\begin{aligned}a_3 = {} & [L_2V_C(1-D-D_1) + 2V_C L_1(1-D-D_2) \\ & - (L_2r_{L1}+L_1r_{L2})(2I_{L2}+I_{L1}-I_i)]/\Psi_{m2}\end{aligned}$$

$$a_2 = [L_1L_2(-2I_{L1}-I_{L2}+I_i)]/\Psi_{m1},$$

$$a_4 = [L_1L_2(-2I_{L2}-I_{L1}+I_i)]/\Psi_{m2}$$

$$\begin{aligned}a_{x1} = {} & [2V_C r_{L2}C + (1-D-D_1) \\ & \times (2I_{L1}+I_{L2}-I_i)L_2]/\beta_{m1}\end{aligned}$$

$$\begin{aligned}a_{y1} = {} & [2V_C r_{L1}C + (1-D-D_2) \\ & \times (2I_{L2}+I_{L1}-I_i)L_1]/\beta_{m2}\end{aligned}$$

$$a_{x2} = 2V_C L_2 C/\beta_{m1}, \quad a_{y2} = 2V_C L_1 C/\beta_{m2}$$

$$\begin{aligned}b_1 = {} & \Big[Cr_{L1}r_{L2} + L_1(1-D-D_2)^2 \\ & + L_2(1-D-D_1)^2\Big]\Big/\Delta\end{aligned}$$

$$b_2 = [C(L_1r_{L2}+L_2r_{L1})]/\Delta, \quad b_3 = L_1L_2C/\Delta$$

$$V_{x_{m1}} = V_C\left(2\hat{d}_1+\hat{d}_2\right), \quad V_{x_{m2}} = V_C\left(2\hat{d}_2+\hat{d}_1\right)$$

$$I_x = I_{L1}\left(2\hat{d}_1+\hat{d}_2\right) + I_{L2}\left(2\hat{d}_2+\hat{d}_1\right) + I_i\left(\hat{d}_1+\hat{d}_2\right).$$

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