Hybrid Buck–Boost Multioutput Quasi-Z-Source Converter With Dual DC and Single AC Outputs

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***Abstract*—This article presents two hybrid multioutput buck–boost quasi-Z-source converters (q-ZSCs) capable of giving two dc and one ac outputs simultaneously from a single dc input. One dc and the ac outputs of the proposed multioutput q-ZSCs have both buck and boost capabilities and the other dc output has the property of boosting the input voltage, thereby capable of giving a wide range of voltage gain both for dc and ac outputs. The rationale behind proposing two variants of the hybrid multioutput q-ZSCs is to have more flexibility on voltage gains as per the load requirements. The proposed converters are derived from the quasi-Z-source concept and hence inherit all the properties of q-ZSI, which realize buck/boost, single-stage inversion, and power conditioning with improved reliability along with inherent shoot-through protection capability. All the three outputs of the proposed converters can be independently controlled making them suitable for various applications. The proposed converters can be utilized for various modern multioutput dc–dc and dc–ac power conversion applications, such as renewables and the uninterrupted power supplies. Detailed steady-state operation, loss/efficiency analysis of the proposed converter, and discussion on the hybrid pulsewidth modulation are presented in this article. In order to bring out the advantages of the proposed multioutput converter, a detailed comparative analysis among the proposed and other closely related existing multioutput converters is carried out in this article. A 310-W prototype is developed to verify the performance of the proposed multioutput buck–boost q-ZSC.**

***Index Terms*—DC–DC converter, hybrid converter, impedance source, inverter.**

I. Introduction

NOWADAYS, single-output converters are not able to meet simultaneous requirements of different types and the voltage level of modern electrical applications, such as hybrid electric vehicles, hybrid microgrid, and standby power supplies [1]–[3]. On the other hand, multioutput converters are becoming popular because of their ability to supply simultaneous multioutputs, high power density, compact size, and lower cost. Owing to these benefits and the demand of multioutput converters, many research works are currently focusing on them [4]–[7].

Manuscript received July 6, 2019; revised October 25, 2019; accepted December 2, 2019. Date of publication December 14, 2019; date of current version March 13, 2020. This work was supported by the Department of Science and Technology, Government of India, under Grant DST/CERI/MI/SG/2017/086(IIT(BHU), Varanasi(G)). Recommended for publication by Associate Editor D. Vinnikov. *(Corresponding author: Kharan Shiluveru.)*

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Digital Object Identifier 10.1109/TPEL.2019.2960268

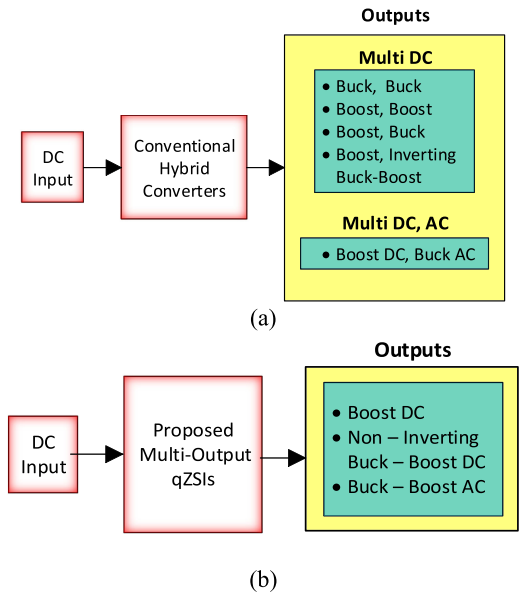

Fig. 1. (a) Representative system of conventional multioutput converters. (b) Representation of the proposed multioutput converter.

Lately, various multioutput converters are reported in the literature [8]–[18]. Multioutput converters discussed in [8]–[13] are predominantly dc–dc converters that only give multiple dc outputs and do not have ac at the output. Literature [14]–[18] give two simultaneous dc and ac outputs and do not have the provisions of multi dc and ac outputs. Moreover, the ac output obtained in the converters reported in the literature [14]–[18] is inherently step down. Split-source-based hybrid converter topology discussed in [19] gives one ac and one dc outputs. In this case also, the ac output is lower than the input voltage. Hybrid multioutput converter discussed in [20] gives *n*-ac and one dc outputs. The hybrid multioutput converter discussed in [20] gives one dc with boost capability and the ac outputs are lesser than the input voltage. A dual-input dual-output Z-source inverter is presented in [21]. In general, a representative system of the conventional multioutput converters can be shown, as given in Fig. 1(a). It may be observed from Fig. 1(a) that there are two categories of existing multioutput converters: 1) converters with multi dc outputs having buck and boost ability, and 2) multioutput converters giving dc and ac outputs simultaneously with boost dc and buck ac outputs. The conventional

multioutput converters giving ac as an output are derived from the voltage-source and current-source inverters. Hence, they are prone to electromagnetic interferences (EMI), which may result in shoot through or misgating. These problems need to be addressed strictly [22]–[24].

This article presents two quasi-Z-source-based hybrid buck–boost multioutput converters. The proposed multioutput qZSCs give three outputs:

1) boost dc;
2) buck–boost dc;
3) ac with buck and boost ability.

A representation of the proposed multioutput qZSCs is given in Fig. 1(b). It may be observed from Fig. 1(b) that the proposed multioutput converters give multi dc and ac outputs having buck and boost abilities for all the outputs. As the proposed multioutput converters are derived from the quasi-impedance network, they inherit all the properties of qZSI. Hence, the proposed converters are immune to the problems associated with EMI as they have the inherent shoot-through protection capability similar to the qZSIs [25], [26]. The presence of the quasi-Z-source network makes the converter capable of giving both boost and buck types of ac output. Furthermore, the proposed converters have single-stage inversion and power conditioning with improved reliability.

In order to achieve wider flexibility on the voltage gains (for all the three outputs), two variants of the proposed multi-output quasi-Z-source converter (q-ZSC) are presented in this article. The proposed converters are derived in such a way that all the outputs can be independently controllable, and hence regulated output voltages can be achieved. As all the outputs of the multi-output converters are independently controllable, the proposed q-ZSCs are suitable and adaptable for the industrial applications. Due to wide range of operation, high power density, and various advantages inherited from q-ZSI, the proposed multioutput q-ZSCs can be used in various applications, including the dc–dc and dc–ac power conversions in renewables, uninterrupted power supplies, etc. The detailed explanation of the suitability of the proposed converter is provided in Section VI-F.

This article is organized as follows. The proposed multioutput q-ZSC and its detailed operation are described in Section II. Pulsewidth modulation (PWM) technique to control the power flow of the proposed converters is discussed in Section III. The detailed power loss analysis is done in Section IV. Section V gives the comparative analysis among the proposed converters and other closely related existing topologies. Section VI presents the experimental verification of the proposed converter and applications. Finally, Section VII concludes this article.

II. Proposed Multioutput qZSCs

The circuit diagram of the proposed hybrid multioutput q-ZSC Type I and Type II is shown in Fig. 2(a) and (b), respectively. Both the converters have been derived from the quasi-impedance source network and have the property of giving one boost dc, one buck–boost dc, and one buck–boost ac outputs. It may be observed from Fig. 2(b) that the inverter bridge and the switch (S) positions are interchanged in Type II as compared with Type I. With this simple modification in the proposed Type I converter, the buck/boost range of the ac and dc outputs has increased. It is discussed in detail in the subsequent section after the steady-state analysis of the proposed Type I converter.

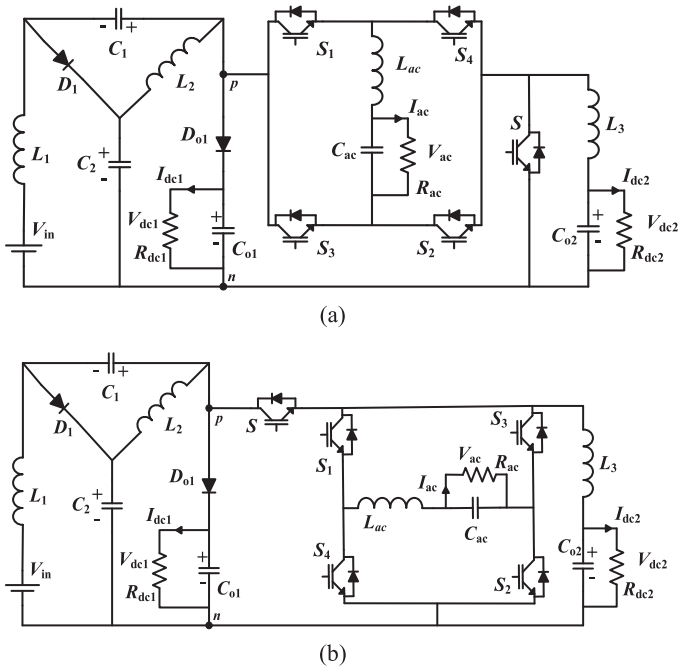

Fig. 2. (a) Type I of the proposed multioutput hybrid qZSC. (b) Type II of the proposed multioutput hybrid qZSC.

The operation of the proposed Type I and Type II converters is similar, and, therefore, a detailed analysis of Type I is discussed in the subsequent sections, and the gain factors of Type II converter is given after that.

A. Operation of the Proposed Multioutput qZSC

The proposed multioutput q-ZSC operates in three different intervals. The converter operation in the different intervals is as follows.

1) Complete Shoot-Through Operation (D_1T_s Operation—Interval I): The operation of the proposed converter in D_1T_s interval is shown in Fig. 3(a). In this interval, two switches of the inverter on the same leg and switch S are ON. In addition to this, another switch of the remaining leg is also switched ON so as to make the zero stage of the inverter. Diodes D_1, D_{o1} are OFF. Inductors L_1 and L_2 get charged and capacitors C_1, C_2, and C_{o1} and inductor L_3 discharge during this interval. Power flow in this interval is shown in Fig. 3(a). The governing equations during this interval are written as follows:

$$\left.\begin{aligned} v_{L1} = v_{IN} + v_{C1};\ v_{L2} = v_{C2};\ v_{L3} = -v_{\mathrm{dc2}} \\ i_{C1} = -i_{L1}\ ;\ i_{C2} = -i_{L2} \\ i_{CO1} = -i_{\mathrm{dc1}}\ ;\ i_{CO2} = i_{L3} - i_{\mathrm{dc2}} \end{aligned}\right\}. \quad (1)$$

2) Shoot-Through Operation of Inverter Leg (D_2T_s Operation—Interval II): The operation of the proposed converter in this interval is shown in Fig. 3(b). This interval is similar to the previous interval except that the switch S is switched OFF. Diodes D_1 and D_{o1} are ON in this interval. The power flow in the interval is shown in Fig. 3(b). Inductor L_1 and L_2 discharge, and L_3 and capacitor C_1 and C_2 charge in this interval. The equations

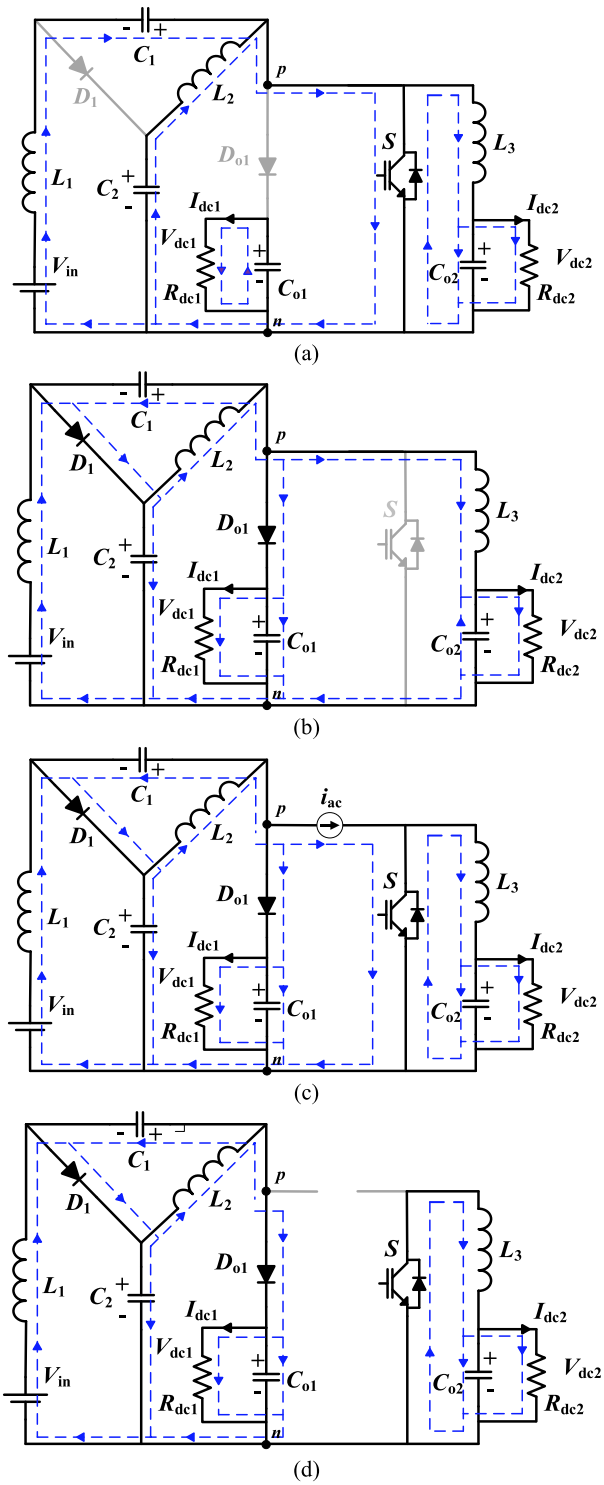

Fig. 3. Operation of the proposed multioutput converter. (a) During interval I. (b) During interval II. (c) Power stage during interval III. (d) Zero stage during interval III.

of the proposed converter during this interval are as follows:

$$\left.\begin{aligned} v_{L1} = v_{\text{IN}} - v_{C2};\ v_{L2} = -v_{C1} = v_{C2} - v_{\text{dc1}} \\ v_{L3} = v_{C1} + v_{C2} - v_{\text{dc2}} = v_{\text{dc1}} - v_{\text{dc2}} \\ i_{C1} + i_{CO1} = i_{L2} - i_{L3} - i_{\text{dc1}};\ i_{CO2} = i_{L3} - i_{\text{dc2}} \\ i_{C2} + i_{CO1} = i_{L1} - i_{L3} - i_{\text{dc1}} \end{aligned}\right\}. \tag{2}$$

3) Nonshoot-Through Operation (D_3T_s Operation—Interval III): This interval is a combination of the power stage and the zero stage of the inverter (ac output part). The length of these two stages depends on the modulation index M_a of the inverter (ac output part) and is not constant in every triangle wave. However, the total length of interval III is constant and is equal to D_3T_s. Fig. 3(c) shows inverter of the proposed q-ZSC being operated in the power stage, and Fig. 3(d) shows the zero-stage operation of the converter. In the power stage either set of switches S_1, S_2 or S_3, and S_4 are switched ON simultaneously. The inverter can be considered as a current device in this interval.

Only a few parts of the zero states of the sinusoidal PWM (SPWM) scheme are used for achieving the shoot-through, the remaining zero stages are observed in this interval. In the zero stage, either upper set of switches S_1, S_3 or lower set of switches S_2, S_4 of the inverter are switched ON simultaneously. The detailed explanation of the combination of these stages to form interval III is given in Section III-B. The equations during this interval are as follows:

$$\left.\begin{aligned} v_{L1} = v_{\text{IN}} - v_{C2};\ v_{pn} = v_{\text{dc1}} \\ v_{L2} = -v_{C1} = v_{C2} - v_{\text{dc1}};\ v_{L3} = -v_{\text{dc2}} \\ i_{C1} + i_{CO1} = i_{L2} - i_{\text{ac}} - i_{\text{dc1}}; \\ i_{C2} + i_{CO1} = i_{L1} - i_{\text{ac}} - i_{\text{dc1}};\ i_{CO2} = i_{L3} - i_{\text{dc2}} \end{aligned}\right\} \tag{3}$$

where i_{CO1} is the instantaneous current flowing through the capacitor C_{O1}.

It can be observed that in any interval, no two loads appear in series or the current of one load flows through the other load. The current flowing through a particular load does not affect the current flowing through the other loads. Hence, no special arrangement is required to balance the loads in the proposed converters.

The operational waveforms of the inductor currents and capacitors voltage is given in Fig. 4.

B. Steady-State Analysis of the Proposed Multioutput qZSC

It is important to mention that the following conditions need to be satisfied for the proposed multioutput q-ZSC:

$$\left.\begin{aligned} D_1 + D_2 + D_3 = 1 \\ M_a + D_1 + D_2 \le 1 \end{aligned}\right\} \tag{4}$$

where M_a is the modulation index, D_1 is complete shoot-through duty ratio, D_2 is the inverter leg shoot-through duty ratio, and D_3 is the nonshoot-through duty ratio.

By averaging (1)–(3), the following steady-state relations are obtained

$$V_{C2} = \frac{V_{\text{IN}} * (1 - D_1)}{1 - 2D_1}, \quad V_{C1} = \frac{V_{\text{IN}} * D_1}{1 - 2D_1} \tag{5}$$

$$I_{L1} = I_{L2} = I_L = \frac{I_{\text{dc1}} + I_{\text{dc2}} * D_2 + I_{\text{ac}} * (1 - D_1 - D_2)}{1 - 2D_1} \tag{6}$$

$$I_{L3} = I_{\text{dc2}} \tag{7}$$

$$V_{\text{dc1}} = \frac{V_{\text{IN}}}{1 - 2D_1} \tag{8}$$

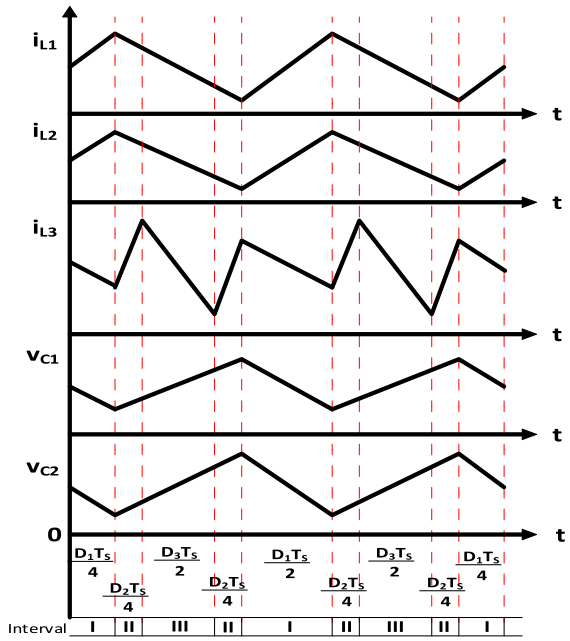

Fig. 4. Operational waveforms of the inductor currents and capacitor voltages.

$$V_{\mathrm{dc2}} = \frac{V_{\mathrm{IN}} * D_2}{1 - 2D_1} \tag{9}$$

$$\text{AC peak } V_{\mathrm{ac\_pk}} = \frac{V_{\mathrm{IN}} * M_a}{1 - 2D_1} \tag{10}$$

$$M_{a\_\max} = 1 - D_1 - D_2 \tag{11}$$

$$\text{Maximum ac peak gain} = \frac{1 - D_1 - D_2}{1 - 2D_1}. \tag{12}$$

The maximum value of D_2 is $1-D_1$. Hence, the maximum value of V_{dc2} at any operating point is equal to V_{dc1} at which the output ac voltage (V_{ac}) is equal to zero.

Fig. 5 represents the gain characteristics of the proposed converter. Fig. 5(a) shows the gain of dc voltage V_{dc2}. It is clear from Fig. 5(a) that the V_{dc2} has both buck and boost properties and it depends on the duty ratios D_1 and D_2. Fig. 5(b) shows the gain of dc voltage V_{dc1}. It may be observed from Fig. 5(b) that V_{dc1} depends on duty D_1 and gives boost output. Fig. 5(c) gives information about the ac gain, and it may be observed that the ac output voltage V_{ac} has both buck and boost properties. Relationship between ac and dc outputs is shown in Fig. 5(d). It may be observed from Fig. 5(d) that ac and dc gains are interdependent, and, thus, gain at one port is restricted by the gains of the other two ports. Furthermore, for an ideal case, the gain of V_{dc1} is 1–10, whereas that of V_{dc2} is 0–5.5 and that of $V_{\mathrm{ac\text{-}pk}}$ is 0–5.5 considering the maximum value of D_1 as 0.45.

The Type II converter is also operated in three intervals.

1) Complete shoot-through stage (Interval I D_1T_s).
2) Power operation of inverter leg (Interval II D_2T_s).
3) Inverter only shoot-through stage (Interval III D_3T_s).

The dc outputs have the same relation as in case of Type I. The ac peak of the ac output can be given by

$$\text{Maximum ac peak} = M_{a\_\max} * v_{pn} = \frac{V_{\mathrm{IN}} * D_2}{1 - 2D_1} \tag{13}$$

where

$$M_{a\_\max} = D_2 \tag{14}$$

$$\text{AC peak gain} = \frac{D_2}{1 - 2D_1}. \tag{15}$$

Fig. 5(e) shows the graph between D_1, D_2, and the ac peak gain of the proposed Type II converter. It can be observed that for certain values of D_1 and D_2, the ac peak gain is high when compared with Type I which can be observed from Fig. 5(c).

Fig. 5(f) shows the combined gain characteristics of Type I and Type II. The left side represents the gain characteristics of Type II, whereas the right side represents that of Type I. It can be clearly observed that just by interchanging switch and the inverter and thereby creating Type II, a wide range of operation is achieved. Hence, depending on the requirement, either of the converters can be chosen. From Fig. 5(f), it can be inferred that for operations where the V_{dc2} is desired to be of buck type, Type I converter may be used, and for those where it is desired to be of boost type, Type II converter may be used. This results in a wide range of operations of the proposed converters. The proposed converters are capable of boosting all dc and ac outputs simultaneously unlike the conventional multioutput inverters. This is one of the main distinctive properties of the proposed converters.

C. Sizing of the Components

To ensure the continuous conduction mode (CCM) operation of the circuit, desired ripple voltages in the capacitors, ripple currents in inductors, and design of passive components play a very important role. The following relations are helpful in finding the values of the passive components in the proposed converters:

$$L_y = \frac{V_{\mathrm{in}}\,(1 - D_1)\,D_1}{(1 - 2D_1) * \Delta i_{Ly}\% * I_L * 2f_{sw}} \quad y = 1, 2 \tag{16}$$

$$L_3 = \frac{V_{\mathrm{in}}\,(1 - D_2)\,D_2}{(1 - 2D_1) * \Delta i_{L3}\% * I_{L3} * 2f_{sw}} \tag{17}$$

$$C_y = \frac{I_L D_1}{\Delta v_{Cy}\% * V_{Cy} * 2f_{sw}} \quad y = 1, 2 \tag{18}$$

$$C_{O1} = \frac{I_{\mathrm{dc1}} D_1}{\Delta v_{\mathrm{dc1}}\% * V_{\mathrm{dc1}} * 2f_{sw}} \tag{19}$$

$$C_{O2} = \frac{V_{\mathrm{in}}\,(1 - D_2)\,D_2}{32\,(1 - 2D_1) * \Delta v_{\mathrm{dc2}}\% * V_{\mathrm{dc2}} * L_3 * f_{sw}^2} \tag{20}$$

where Δi_{Lx} is the percentage current ripple of the inductor L_x, and Δv_{Cx} is the percentage voltage ripple of the capacitor C_x.

The voltage and current stresses of the switches and diodes can be given as follows.

Maximum voltage stresses

$$\left.\begin{aligned} V_{D1} = V_{DO1} &= -(V_{C1} + V_{C2}) = \tfrac{-V_{\mathrm{IN}}}{1-2D_1} \\ V_S = V_{S1} = V_{S2} &= V_{S3} = V_{S4} = \tfrac{V_{\mathrm{IN}}}{1-2D_1} \end{aligned}\right\}. \tag{21}$$

Maximum current stresses

$$\left.\begin{aligned} I_S = I_{S1} = I_{S2} &= I_{S3} = I_{S4} = I_{L1} + I_{L2} = 2I_L \\ I_{DO1} &= \tfrac{I_{\mathrm{dc1}}}{1-D_1};\ I_{D1} = 2I_L - I_{\mathrm{dc1}}\tfrac{2-D_1}{1-D_1} \end{aligned}\right\}. \tag{22}$$

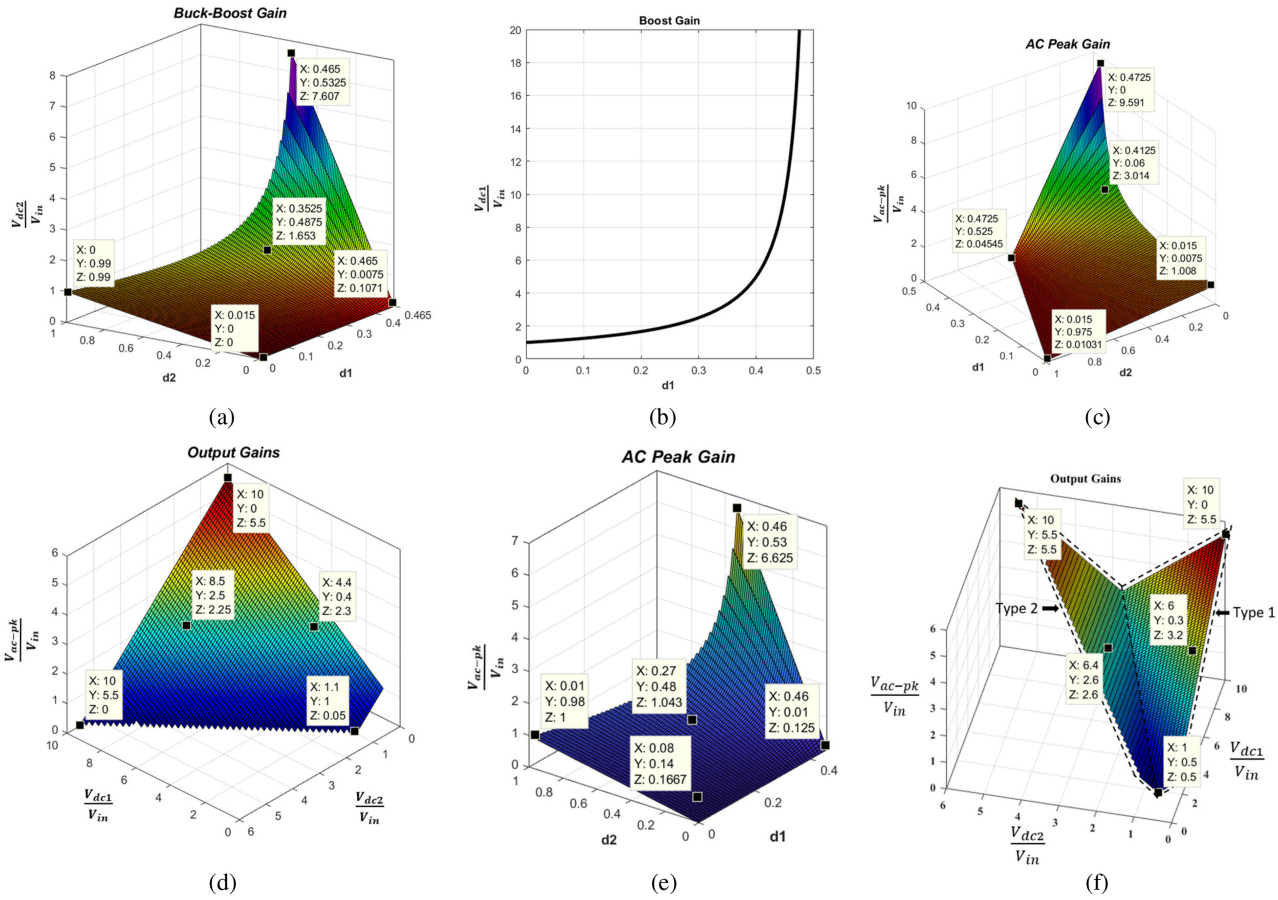

Fig. 5. Gain characteristics of the proposed multioutput q-ZSC. (a) $V_{\rm dc2}$ gain w.r.t. duty D_1 and D_2. (b) $V_{\rm dc1}$ gain w.r.t. D_1. (c) Type I AC gain with D_1 and D_2. (d) Type I gain between ac and dc outputs. (e) AC gain characteristics of the proposed Type II converter with D_1 and D_2. (f) AC and DC gain characteristics for the proposed Type I and Type II converters.

Depending on these voltage and current stress, the components can be chosen accordingly.

III. Control and PWM of the Proposed Converter

A. Closed-Loop Operation and the Proposed Control Scheme for the Proposed Converter

The closed-loop operation of the converter plays an important role in maintaining the output voltages of the proposed converter to their desired values. In the multioutput system, the main challenge is the independent control of every output voltage. The outputs of the proposed converter are governed by (8)–(10). Also, the duty ratios and modulation index D_1, D_2, and M_a are governed by (4). It can be observed that all the outputs are interdependent and hence cannot be decoupled completely. However, as long as (4) holds true, independent control operation of the outputs is achieved through the following process.

From voltage equations, it can be observed that $V_{\rm dc1}$ depends on D_1, $V_{\rm dc2}$ depends on D_1 and D_2, and $V_{\rm ac}$ depends on D_1 and M_a. $V_{\rm dc2}$ can be controlled either by D_1 or D_2 or both. If it is controlled by either D_1 or both D_1 and D_2, the controller tries to change the value of D_1 to regulate $V_{\rm dc2}$. $V_{\rm dc1}$, which is solely dependent on D_1, also changes, and the obtained value of voltage may not be equal to the desired value. Thus, D_1 is avoided for controlling $V_{\rm dc2}$ or $V_{\rm ac}$.

Since $V_{\rm dc1}$ is dependent on only D_1, it is used to control $V_{\rm dc1}$. $V_{\rm dc2}$ can be controlled only by changing the D_2 as D_1 cannot be disturbed to ensure constant $V_{\rm dc1}$. Similarly, $V_{\rm ac}$ can only be controlled by M_a. Thus, there are three independent variables for the control of the three output voltages as long as (4) holds true. The output voltages can be decoupled in such a way that $V_{\rm dc1}$, $V_{\rm dc2}$, and $V_{\rm ac}$ are controlled using D_1, D_2, and M_a, respectively. This would ensure that the change in one output does not affect the other outputs. However, it must be noted that there might be a small disturbance in all the outputs if the load on any of the output changes but the disturbance settles down in a small-time interval.

Fig. 6 shows the control scheme of the proposed converter. Here, $v^*_{\rm dc1}$ and $v^*_{\rm dc2}$ are the reference dc voltages, and v^*_d is the reference ac voltage in the *dq* domain. The ac voltage obtained is transformed from $\alpha\beta$ domain to *dq* domain in such a way that V_q is made equal to zero so that V_d becomes a constant value and easily controllable. The obtained output voltages are compared with the reference voltages, and the error is passed through the proportional–integral (PI) controllers. The output of the PI controllers is then passed through saturation block to ensure that the duty ratio remains within practical limits and the converter does not malfunction. In case of saturation of the ac controller, the maximum value of the saturation block is defined as $1-(D_1+D_2)$ to ensure (4) holds true.

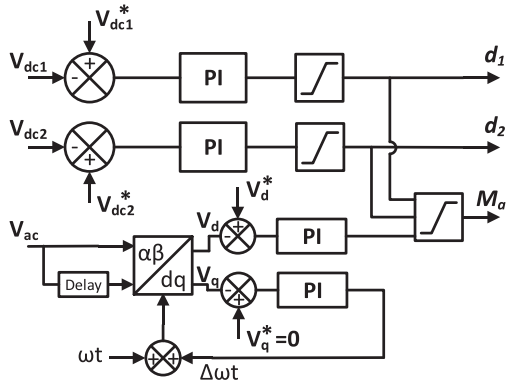

Fig. 6. Control Scheme of the proposed converter.

By changing the reference voltages, the output voltages can also be varied at any point of time in between the operations of the converter provided that the desired set of voltages fall in the operation limits of the converter.

B. Proposed PWM Technique

The PWM scheme of a converter is pivotal in obtaining the desired outputs. A novel PWM technique is proposed in this article, which is used to operate the proposed converter. The proposed PWM technique is derived from the standard SPWM scheme. The SPWM switching scheme essentially creates two stages of the inverter-power stage and zero stage. The power stages of SPWM are solely responsible for the power quality of the output ac. To ensure the power quality is not degraded, the power stages of the standard SPWM technique have not been disturbed. However, the zero stages may be used to achieve the shoot-through intervals. In the proposed converter, the inverter is in shoot-through stage in intervals I and II. In SPWM, for modulation index <1, every cycle of carrier triangle wave results in both the power stage and zero stage. However, the length of these stages is not constant in every triangle wave cycle as the reference sinusoidal wave continuously varies with higher time period than the carrier triangular wave. By limiting the value of modulation index (M_a), it can be ensured that a minimum length of zero stage $((D_1 + D_2)T_s)$ is present in every cycle of the triangle wave. This fixed length zero stage is used in achieving the total shoot-through and inverter only shoot-through intervals, i.e., intervals I and II by switching an extra switch in addition to the switches that are already switched ON. Thus, this fixed length zero stages form the intervals I and II. From the inverter point of view, shoot-through interval is same as the zero stage. After subtracting the fixed length zero stages from the continuously varying zero stages, the resultant is also continuously varying zero stages with less time than that of the original ones. These resultant continuously varying zero stages along with the continuously varying power stage combinedly form the interval III operation of the proposed converter. Due to the varying zero stage and power stage in each and every triangular wave, the pulses are periodical with the low frequency, i.e., 50 Hz rather than the triangular wave frequency. In the zero stage of the inverter, either the upper set of switches (S_1, S_4) or the lower set of switches (S_2, S_3) of the inverter are switched ON. To achieve the shoot through of the inverter in intervals I and II, one of the remaining two switches is forced is switched ON in addition to the abovementioned set of switches. This action of forced switching of the switches is done symmetrically to ensure that all the switches experience the same stress. When the reference sine wave is positive, S_3 is switched ON when the lower set of switches of the inverter are ON, and S_4 is forced switched ON when the upper set of switches of the inverter are ON. Similarly, when the reference sine wave is negative, either of the switches S_1 or S_2 is switched ON depending on PWM logic. Fig. 7(a) shows the switching pulses of the proposed PWM technique, and logic for generating the pulses is shown in Fig. 7(b).

For the total shoot-through interval (interval I) $V_{\rm qst}$ and $-V_{\rm qst}$ are compared with $V_{\rm tri}$. For the inverter only shoot-through stage, $V_{\rm ist}$ and $-V_{\rm ist}$ are compared with $V_{\rm tri}$. It can be clearly observed from Fig. 7(a) that interval I is followed and preceded by interval II, i.e., switches of the inverter are turned ON and OFF only in interval II, and they continue to conduct also in interval I. This type of PWM logic prevents turning ON or OFF the switches in the interval I, i.e., shoot-through interval thereby reducing the switching losses as the current flowing through the switches in interval I is higher when compared with the interval II. The lower switch (S) is ON during intervals I and III. If the triangle wave ($V_{\rm tri}$) for generating the gate pulses is defined from $-\widehat{V_{\rm tri}}$ to $\widehat{V_{\rm tri}}$, the values of the comparison signals can be defined as $V_{\rm qst} = \widehat{V_{\rm tri}}(1 - D_1)$, $V_{\rm ist} = \widehat{V_{\rm tri}}(1 - D_1 - D_2)$, and $V_{\rm sin} = \widehat{V_{\rm tri}} M_a \sin(\omega t)$. In case of Type II converter, the PWM technique used is similar except that the D_2T_s and D_3T_s intervals are interchanged.

It can be observed from Fig. 7(a) that in one complete cycle of the triangular wave, all the intervals appear twice with symmetry about the centre of the triangular wave. Thus, it can be said that the frequency of the intervals is twice that of the triangular wave frequency or the switching frequency. The time period of the intervals can be written as

$$T_s = \frac{1}{2f_{\rm tri}}$$

where $f_{\rm tri}$ is the triangular wave frequency.

IV. Power Loss Analysis

The power loss analysis of the circuit can be divided into following parts:

1) power loss analysis of H-bridge inverter switches;
2) power loss analysis of switch S;
3) power loss of diodes; and
4) ohmic losses.

The detailed discussion on losses of these parts is as follows.

A. Power Loss Analysis of H-Bridge Inverter Switches

1) Switching Losses: The switching losses have two components: 1) power stage switching loss, and 2) losses due to forced switching to attain the shoot-through stage of the proposed qZSC.

The switching process for the power stages of the inverter follows simple SPWM technique. Only the zero stages in the SPWM technique are used for the shoot-through stage of the

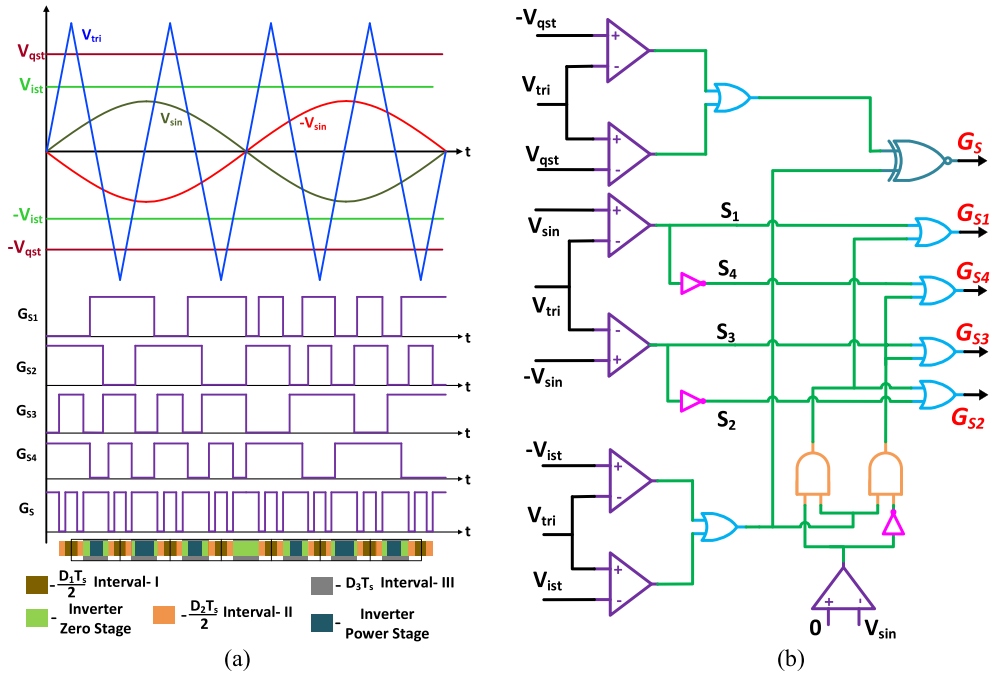

Fig. 7. (a) Switching signals of the proposed PWM technique. (b) Logic for pulse generation.

inverter. As a result, the regular power stages attained in the SPWM technique are not affected. The current flowing through the switches after they are ON is equal to $I_{\rm ac}$. Hence, the average switching loss in power stages is given by the following relation:

$$P_{SLP\_SH} = \frac{f_{si} * (E_{\rm on} + E_{\rm off}) * V_{pn} * I_{\rm ac}}{V_{\rm ref} * I_{\rm ref}} \tag{23}$$

where $E_{\rm on}$ and $E_{\rm off}$ are, respectively, the switching ON and OFF energies of the switches at the reference voltage $V_{\rm ref}$ and current $I_{\rm ref}$. $f_{\rm tri}$ is the frequency of the carrier triangle wave, and $f_{\rm ac}$ and $T_{\rm ac}$ are the frequency and time period of the reference wave, respectively. The switching frequency of the inverter bridge switches can be defined as $f_{\rm si} = \frac{f_{\rm tri}}{f_{\rm ac}}$.

It is important to mention that a part of the zero stages in the SPWM behave as the shoot-through stage of the inverter. In this process, each switch of the H-bridge inverter is forced to switch ON either in the positive half or the negative half of the reference wave. Hence, the switching frequency of forcing the switches is half of the switching frequency of the inverter. Also, each switch in turned ON in the shoot-through stage only for $(D_1 + D_2)/2$ effectively. The current flowing through the switch after it is switched ON in zero state is equal to the shoot-through current, i.e., I_{L3}. The average switching loss of the switches in the inverter only shoot-through stage is given by the following relation:

$$P_{SLS\_SH} = \frac{f_{si} * (E_{\rm on} + E_{\rm off}) * V_{pn} * I_{L3}}{2 * V_{\rm ref} * I_{\rm ref}}. \tag{24}$$

It should be noted that no switch is being switched ON or OFF during shoot-through stage (D_1T_s interval). The switches continue to be in the same stage as they were in the D_2T_s interval, and hence no switching losses occur during that interval.

2) Conduction Losses: The conduction losses are also divided into conduction losses during the shoot-through stage of the proposed qZSC (D_1T_s interval), conduction losses during the inverter only shoot-through stage(D_2T_s interval), and conduction losses during the power stage.

a) Conduction losses during the shoot-through stage (D_1T_s interval): In this stage, the current flowing through the switch is $I_{L1} + I_{L2}$. Hence, the average and rms currents flowing through the switches are

$$\left.\begin{aligned} I_{qST_{\rm avg}SH} &= \tfrac{1}{T_{\rm ac}} \int_0^{T_{\rm ac}} (I_{L1}+I_{L2})\, \tfrac{D_1}{2}\, dt = (I_{L1}+I_{L2})\, \tfrac{D_1}{2} \\ I_{qST\_{\rm rms}\_SH} &= \left(\tfrac{1}{T_{\rm ac}} \int_0^{T_{\rm ac}} (I_{L1}+I_{L2})^2 * \tfrac{D_2}{2} dt\right)^{\frac{1}{2}} \end{aligned}\right\}. \tag{25}$$

b) Conduction losses during the inverter only shoot-through stage (D_2T_s interval): The current flowing through the switches in this stage is I_{L3}. Hence, the average and rms currents flowing through the switches of the proposed q-ZSC are

$$I_{iST\_{\rm avg}\_SH} = \frac{1}{T_{\rm ac}} \int_0^{T_{\rm ac}} I_{L3} * \frac{D_2}{2}\, dt = I_{L3} * \frac{D_2}{2} \tag{26}$$

$$I_{iST\_{\rm rms}\_SH} = \left(\frac{1}{T_{\rm ac}} \int_0^{T_{\rm ac}} I_{L3}^2 * \frac{D_1}{2}\, dt\right)^{\frac{1}{2}}. \tag{27}$$

c) Conduction losses during the nonshoot-through operation (D_3T_s interval): The active stages are similar to the phase shift-PWM discussed in [27]. The average and rms currents flowing are given by

$$I_{P\_{\rm avg}\_SH} = \frac{1}{2\pi} \int_0^{2\pi} I_{\rm ac} d\,(t)\; d\,(\omega t) \tag{28}$$

$$I_{P\_{\rm rms}\_SH} = \left(\frac{1}{2\pi} \int_0^{2\pi} I_{\rm ac}^2 d\,(t)\; d\,(\omega t)\right)^{\frac{1}{2}} \tag{29}$$

where

$$d(t) = \frac{1 + M_a \sin(\omega t)}{2} - \frac{D_1 + D_2}{2}. \quad (30)$$

B. Power Loss Analysis of Switch S

The switch S is ON during the shoot-through stage and the nonshoot-through operation of the inverter.

1) Switching Losses: Switching losses of switch S has two components: 1) switching losses during the shoot-through stage and 2) switching losses during the power stage.

a) Switching losses during the inverter only shoot-through stage (D_2T_s interval): The switching frequency of S is twice that of the inverter switching frequency. The current flowing through switch S after it is ON is equal to $I_{L1} + I_{L2} - \mathrm{I}_{L3}$ as the inductor L_3 current tries to discharge along this path. Hence, the switching loss is given by

$$P_{SLS\_S} = \frac{2 * f_{si} * (E_{\text{on}} + E_{\text{off}}) * V_{pn} * (I_{L1} + I_{L2} - I_{L3})}{V_{\text{ref}} * I_{\text{ref}}}. \quad (31)$$

b) Switching losses during the nonshoot-through operation (D_3T_s interval): The losses in this stage depend on the value of I_{ac} and I_{L3}. If $I_{\text{ac}} > I_{L3}$, then the current flows through the switch and loss can be given by

$$P_{SLP\_S} = \frac{2 * f_{si} * (E_{\text{on}} + E_{\text{off}}) * V_{pn} * (I_{\text{ac}} - I_{L3})}{V_{\text{ref}} * I_{\text{ref}}}. \quad (32)$$

However, if the value of $I_{\text{ac}} < I_{L3}$, then the current flows through the antiparallel diode. The turn-ON losses are very minute and neglected. The turn-OFF loss is given by

$$P_{SLP\_S} = \frac{2 * f_{si} * Q_{\text{rr}} * V_{pn}}{2} \quad (33)$$

where Q_{rr} is the reverse recovery charge of the diode.

2) Conduction Losses: Switch S conduct during complete shoot-through operation and nonshoot-through operation. The conduction losses during these states are as follows.

The conduction loss of switch can be calculated by the formula

$$P_{con} = I_{\text{rms}}^2 R_{\text{ON}} + I_{\text{avg}} V_{\text{ON}}. \quad (34)$$

a) Conduction losses during the shoot-through stage (D_1T_s interval): The average and rms current can be given by

$$I_{qST\_\text{avg}\_S} = \frac{1}{T_{\text{ac}}} \int_0^{T_{\text{ac}}} 2 * (I_{L1} + I_{L2}) * D_1 \, dt \quad (35)$$

$$I_{qST\_\text{rms}\_S} = \left(\frac{1}{T_{\text{ac}}} \int_0^{T_{\text{ac}}} 2 * (I_{L1} + I_{L2})^2 * D_1 dt \right)^{\frac{1}{2}}. \quad (36)$$

b) Conduction losses during the nonshoot-through operation (D_3T_s interval): The average rms current can be given by

$$I_{P\_\text{avg}\_S} = \frac{1}{T_{\text{ac}}} \int_0^{T_{\text{ac}}} 2 * |I_{\text{ac}} - I_{L3}| * d(t) \; dt \quad (37)$$

$$I_{P\_\text{rms}\_S} = \left(\frac{1}{T_{\text{ac}}} \int_0^{T_{\text{ac}}} 2 * (I_{\text{ac}} - I_{L3})^2 d(t) \; dt \right)^{\frac{1}{2}}. \quad (38)$$

The conduction losses can be calculated from (29).

C. Diode Losses

The diode D1 is switched ON and OFF only in D_2T_s interval. The switching losses of both the diodes can be given by

$$P_{SL\_D1} = 2 * f_{si} * Q_{\text{rr}} * V_{D1} \quad (39)$$

$$P_{SL\_Do} = 2 * f_{si} * Q_{\text{rr}} * V_{\text{dc1}}. \quad (40)$$

The average diode conduction losses can be given by $P = V_F * I_{\text{avg}}$. The average currents flowing through the diodes can be given by

$$\left. \begin{aligned} I_{\text{avg}\_D1} &= (I_{L1} + I_{L2} - I_{\text{dc1}})(1 - D_1) - I_{L3} D_2 - I_{\text{ac}} D_3 \\ I_{\text{avg}\_Do} &= I_{\text{dc1}} (1 - D_1) \end{aligned} \right\}. \quad (41)$$

D. Ohmic Losses

The ohmic losses of capacitors and inductors are given by $P = I_{\text{rms}}^2 r_x$, where I_{rms} is the rms current flowing through the passive element, and r_x is equivalent series resistance of capacitor/dc resistance of inductor.

V. Comparative Analysis Among the Conventional Multioutput and the Proposed Converter

The proposed qZSC is compared with conventional multioutput converters. Table I gives the details of the comparison among the proposed and the conventional multioutput converters. It may be observed from Table I that multioutput converters discussed in [3], [8], and [12] give two dc outputs with boost capability. The authors of [11], [13], and [16] present multioutput converters with one boost and a buck dc output. Multioutput converters discussed in [15] and [18] give simultaneous dc and ac outputs with boost dc and buck ac. Multioutput converter discussed in [20] gives *n* number of stepped down ac outputs and with one boost dc. In general, it may be observed that the conventional multioutput converters have three categories:

1) converters with dc outputs with boosting capability;
2) converters with two dc outputs having one boost dc and one buck dc;
3) converters with simultaneous ac and dc outputs with buck ac and boost dc.

Moreover, all these converters are derived from the voltage-source inverters (VSIs) and, therefore, possess the challenges associated with it. The multiutput q-ZSC proposed in this article gives the following three outputs:

1) boost dc;
2) buck–boost dc;
3) buck–boost ac.

In this way, the proposed converter has the property of giving dc and ac outputs with both buck and boost capabilities in one single converter, unlike the conventional multioutput converters. In addition, the proposed multioutput converter is derived from the q-ZSI and, therefore, has inherent shoot-through protection and improved reliability unlike the conventional VSI-derived multioutput converters.

TABLE I
COMPARISON AMONG CONVENTIONAL MULTIOUTPUT CONVERTERS AND THE PROPOSED CONVERTER

Reference	No. of Outputs	Type of Outputs	Nature of Outputs	Equations
[3]	2	DC, DC	Boost, Boost	$\frac{V_{O1}}{V_{in}}=\frac{1}{1-D}$; $\frac{V_{O2}}{V_{in}}=\frac{2}{1-D}$
[8]	2(Extendable)	DC, DC	Boost, Boost	$\frac{V_{o1}}{V_{in}}=\frac{nD_0^{'}}{n\left(D_0^{'}\right)^2+(D_0+D_1)^{'2}}$; $\frac{V_{o2}}{V_{in}}=\frac{(D_0+D_1)^{'}}{n\left(D_0^{'}\right)^2+(D_0+D_1)^{'2}}$ $n=\frac{R_{L1}}{R_{L2}}$
[12]	2	DC, DC	Boost, Boost	$\frac{V_{O1}}{V_{in}}=\frac{1}{1-D_1+D_x}$; $\frac{V_{O2}}{V_{in}}=\frac{N+1}{1-D_1}$; $N=\frac{N_2}{N_1}$
[13]	2	DC, DC	Boost, Buck	$\frac{V_O}{V_{in}}=1+\frac{(1-n)RD_2}{(2nL_{lkg}f_s-RD_2)(1-D_2)}$; $\frac{V_{O1}}{V_{in}}=\frac{D_1-D_2}{1-D_2}$
[11]	2	DC, DC	Boost, Buck	$\frac{V_{O1}}{V_{in}}=\frac{1}{2-D_1-D_2}$; $\frac{V_{O2}}{V_{in}}=\frac{1-D_2}{2-D_1-D_2}$
[16]	2	DC, DC	Boost, Buck	$\frac{V_{O1}}{V_{in}}=\frac{1}{1-D_1}$; $\frac{V_{O2}}{V_{in}}=\frac{D_2}{1-D_1}$; $D_1+D_2\leq 1$
[15]	2	DC, AC	Boost DC, Buck AC	$\frac{V_{dc}}{V_{in}}=\frac{1}{1-D}$; $V_{ac-pk}=\frac{MV_{in}}{1-D}$; $D+M\leq 1$
[18]	2	DC, AC	Boost DC, Buck AC	$\frac{V_{dc}}{V_{in}}=\frac{(2-D-D_{st})}{(1-D)(1-D_{st})}$; $V_{ac-pk}=\frac{MV_{in}}{1-D}$
[20]	2(Extendable)	DC, AC	Boost DC, Buck-Boost AC	$\frac{V_{dc}}{V_{in}}=\frac{1}{(1-D_{st})^2}$; $\frac{V_{O2}}{V_{in}}=\frac{M_a}{(1-D_{st})^2}$; $D_{st}+M_a\leq 1$
Proposed q-ZSCs (Type I and Type II)	3	DC, DC, AC	Boost DC, Buck-Boost DC, Buck-Boost AC	$V_{dc1}=\frac{V_{IN}}{1-2D_1}$; $V_{dc2}=\frac{V_{IN}*D_2}{1-2D_1}$; $V_{ac-pk}=\frac{MV_{in}}{1-2D_1}$ M+D_1+D_2≤1(for Type I); M+D_1+D_3≤1(for Type II)

TABLE II
TABLE OF COMPONENTS AND THEIR PARAMETERS

Component	Part No/Value
IGBT	IKW30N65ES5
Diode	40EPF06
L_1, L_2	PCV-2-564-08L, 560 µH, 0.09 Ω
L_3	2.25 m, 0.08 Ω
C_1	150 µF, 0.04 Ω
C_2	100 µF, 0.05 Ω
C_{O1}	13.6 µF, 0.05 Ω
C_{O2}	13.6 µF, 0.02 Ω
V_{in}	48 V
D_1	0.3
D_2	0.2
M_a	0.432

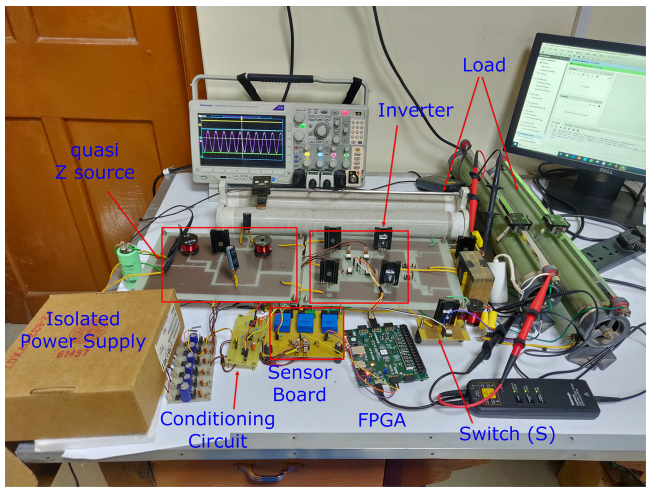

Fig. 8. Photograph of experimental setup.

VI. EXPERIMENTAL VERIFICATION

The proposed multioutput q-ZSC is validated on a 310-W scaled-down prototype. Table II lists the parameters along with their attributes. Photograph of the experimental setup is shown in Fig. 8. Detailed steady-state experimental results of the proposed multioutput q-ZSC are discussed in subsequent sections.

The below presented results are of Type I converter with one boost dc, one buck dc, and buck ac outputs. The values of the load resistances R_{dc1}, R_{dc2}, and R_{ac} are taken as 90, 5.76, and 26.52Ω, respectively, for the validation of steady-state analysis.

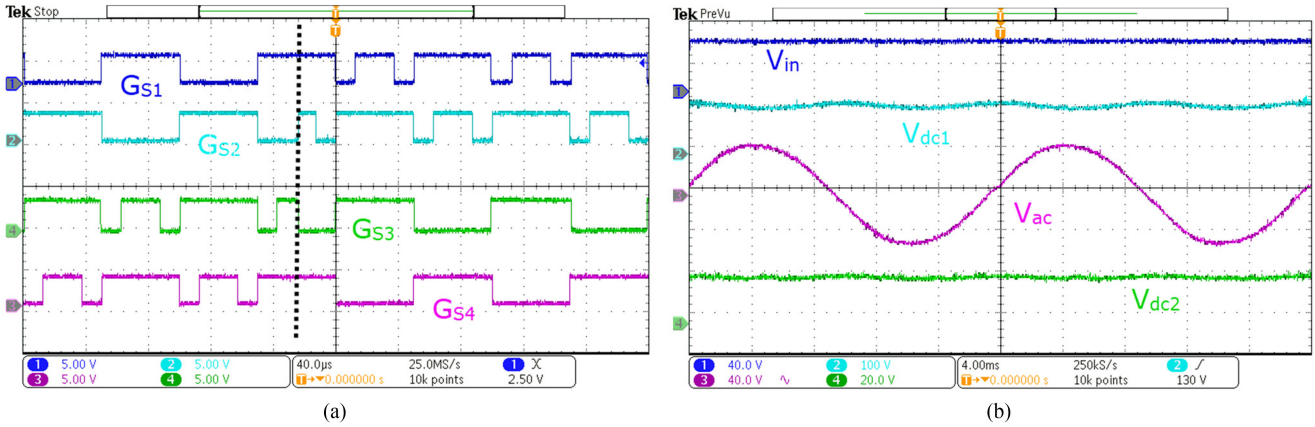

Fig. 9. (a) Gating pulse of the switches of the converter. (b) Steady-state output waveforms along with the input voltage.

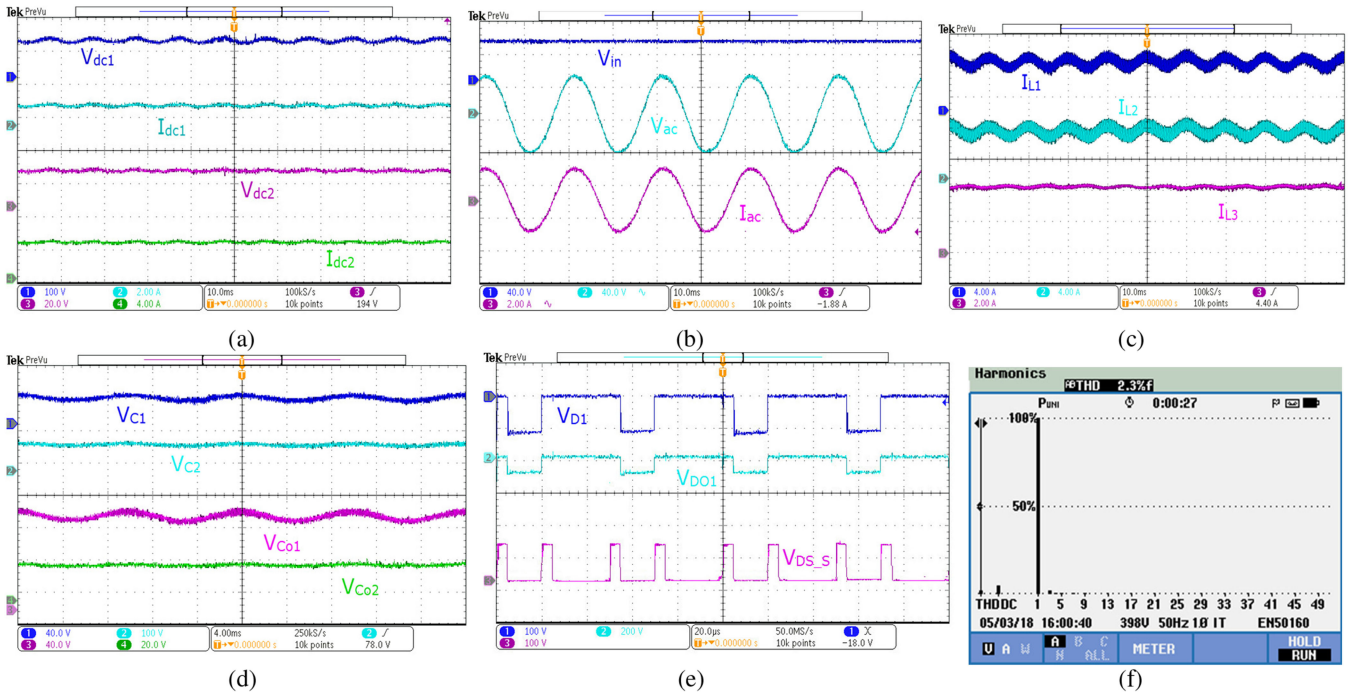

Fig. 10. (a) Output dc voltages and currents. (b) Output ac voltage and current along with input voltage. (c) Inductor currents. (d) Capacitor voltages. (e) Diodes and switch S voltage stress. (f) THD of the output ac voltage.

A. Steady-State Performance of the Proposed Multioutput qZSC

Fig. 9(a) shows the gating pulses of the proposed converter switches S_1, S_2, S_3, and S_4 respectively. The gating pulses on the left side of the dotted black line indicates the PWM when the reference signal $V_{\sin} > 0$, where the switches S_3 and S_4 are switched ON during the zero states to get the shoot-through stage. The gating pulses on the right side of the black line indicate the PWM when the reference signal $V_{\sin} < 0$, where the switches S_1 and S_2 are switched ON during the dead states to get the shoot-through stage.

Fig. 9(b) shows the performance of the proposed converter for one boost dc, one buck dc, and buck ac output simultaneously. In this case, the converter is operated at $D_1 = 0.3$, $D_2 = 0.2$, and $M_a = 0.432$. It may be observed that for $V_{\text{in}} = 48$ V, the proposed converter gives $V_{\text{dc1}} = 114$ V, $V_{\text{dc2}} = 21.5$ V, and $V_{\text{ac-pk}} = 46$ V. The results confirm that the proposed converter gives one boost, one buck, and one buck ac output simultaneously. Fig. 10(a) shows the output dc voltages and respective currents. It may be noticed from Fig. 10(a) that $V_{\text{dc1}} = 114$ V, $V_{\text{dc2}} = 21.5$ V, $I_{\text{dc1}} = 1.267$ A, and $I_{\text{dc2}} = 4.2$ A. Fig. 10(b) shows the output ac voltage and current along with the input voltage. It is observed that the peak value of ac voltage is 46 V and that of current is 1.9 A. The rms values of voltage and current are 32.526 V and 1.343 A, respectively. Fig. 10(c) shows the steady-state currents flowing through the inductors. For the prototype mentioned above, the inductor currents of L_1 and L_2 are found to be equal and is equal to 6.5 A, and the current flowing through inductor L_3 is $I_{L3} = 4.2$ A. Fig. 10(d) gives the steady-state capacitor voltage of the proposed converter.

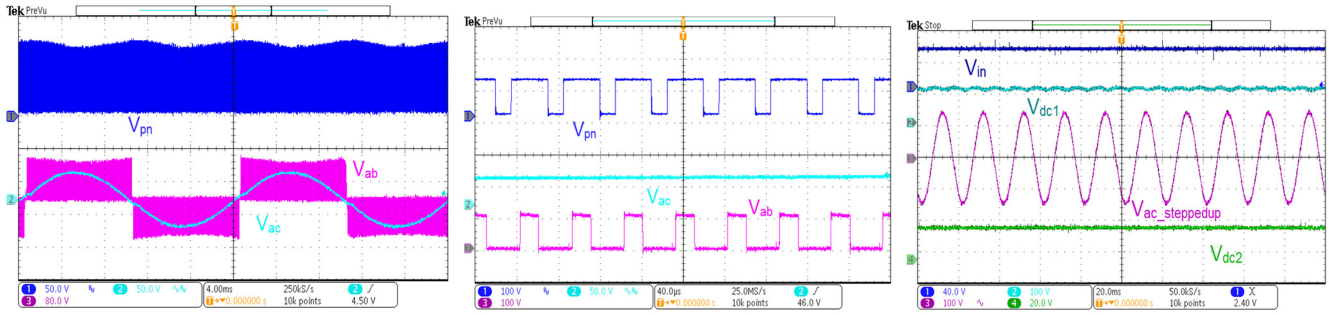

Fig. 11. (a) DC-link voltage, unfiltered and filtered ac output voltages at fundamental frequency. (b) DC-link voltage, unfiltered and filtered ac output voltages for four switching periods. (c) Input and output voltages when $V_{\rm ac}$ is stepped up using a low-frequency transformer.

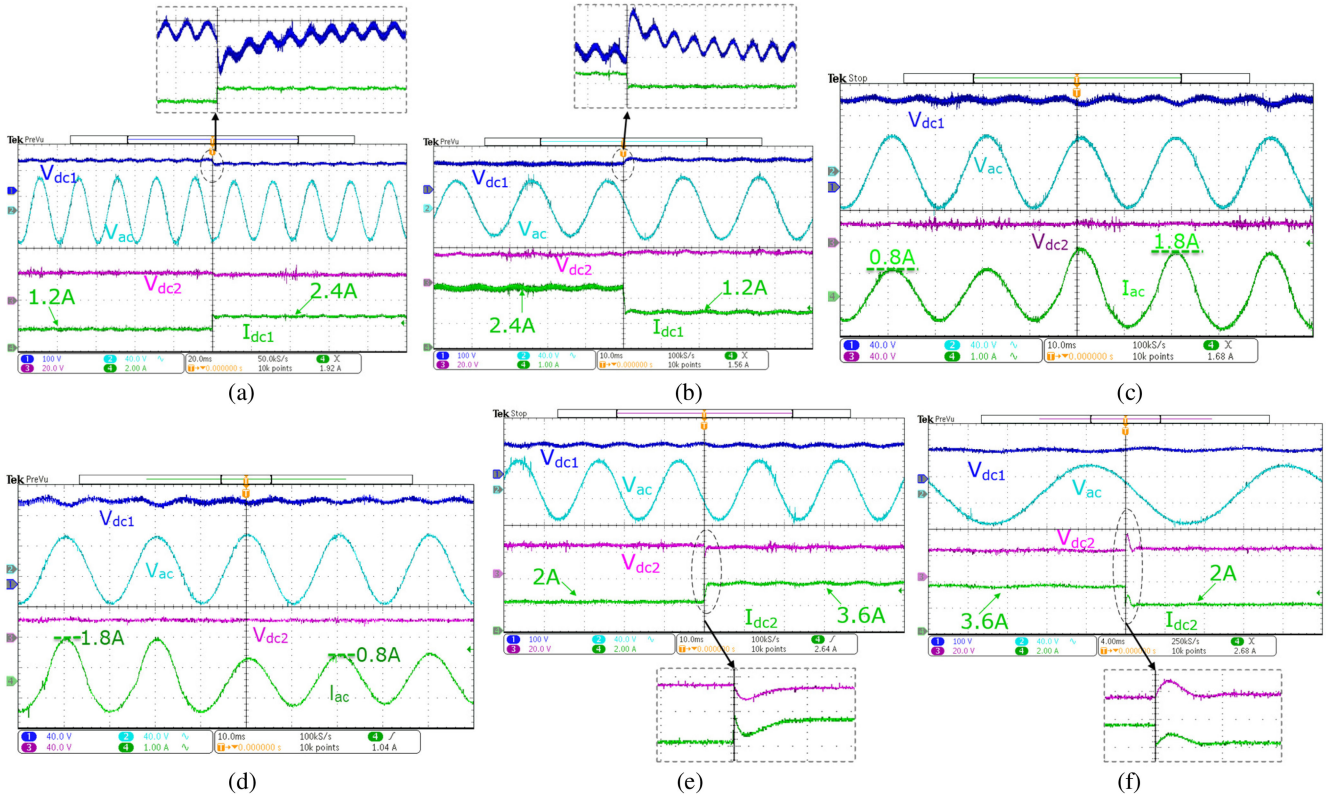

Fig. 12. Experimental results showing the open-loop load dynamics during (a) step-up $I_{\rm dc1}$ load change, (b) step-down $I_{\rm dc1}$ load change, (c) step-up $I_{\rm ac}$ load change, (d) step-down $I_{\rm ac}$ load change, (e) step-up $I_{\rm dc2}$ load change, and (f) step-down $I_{\rm dc2}$ load change.

For an input voltage of $V_{\rm in} = 48$ V, the capacitor voltages are found to be $V_{C1} = 32$ V, $V_{C2} = 81$ V, $V_{CO1} = 114$ V, and $V_{CO2} = 21.5$ V. Fig. 10(e) shows the voltage stress across the diodes D_1 and D_{O1} and the drain to source voltage of switch S. Fig. 10(f) shows the harmonic spectrum of the proposed converter for voltage. It can be observed that the total harmonic distortion (THD) for output ac voltage $V_{\rm AC}$ is 2.31%.

Fig. 11(a) shows the waveforms of the dc-link voltage (V_{pn}), unfiltered ac output voltage $(V_{\rm ab})$, and the filtered ac voltage $(V_{\rm ac})$ at the fundamental frequency, and Fig. 11(b) shows the waveforms of the dc-link voltage (V_{pn}), unfiltered ac output voltage $(V_{\rm ab})$, and the filtered ac voltage $(V_{\rm ac})$ during four switching periods. Fig. 11(c) shows the input and output voltages when the obtained output ac voltage $V_{\rm ac}$ is stepped up using a low-frequency transformer. It can be observed that the peak of the obtained ac voltage is 150 V, i.e., the rms voltage is 106.53 V.

B. Open-Loop Dynamics

This section shows the experimental results of the open-loop load dynamics of the proposed converter. Fig. 12(a) and (b) shows the load dynamics of the $V_{\rm dc1}$ load. The value of $R_{\rm dc1}$ is stepped down making the current to increase from 1.2 to 2.4 A, as shown in Fig. 12(a). As soon as the load is stepped up, a dip in the output voltage $V_{\rm dc1}$ can be observed. The zoomed version of the result taken in ac mode shows the voltage dip clearly. Similarly, Fig. 12(b) shows the output voltages when the load

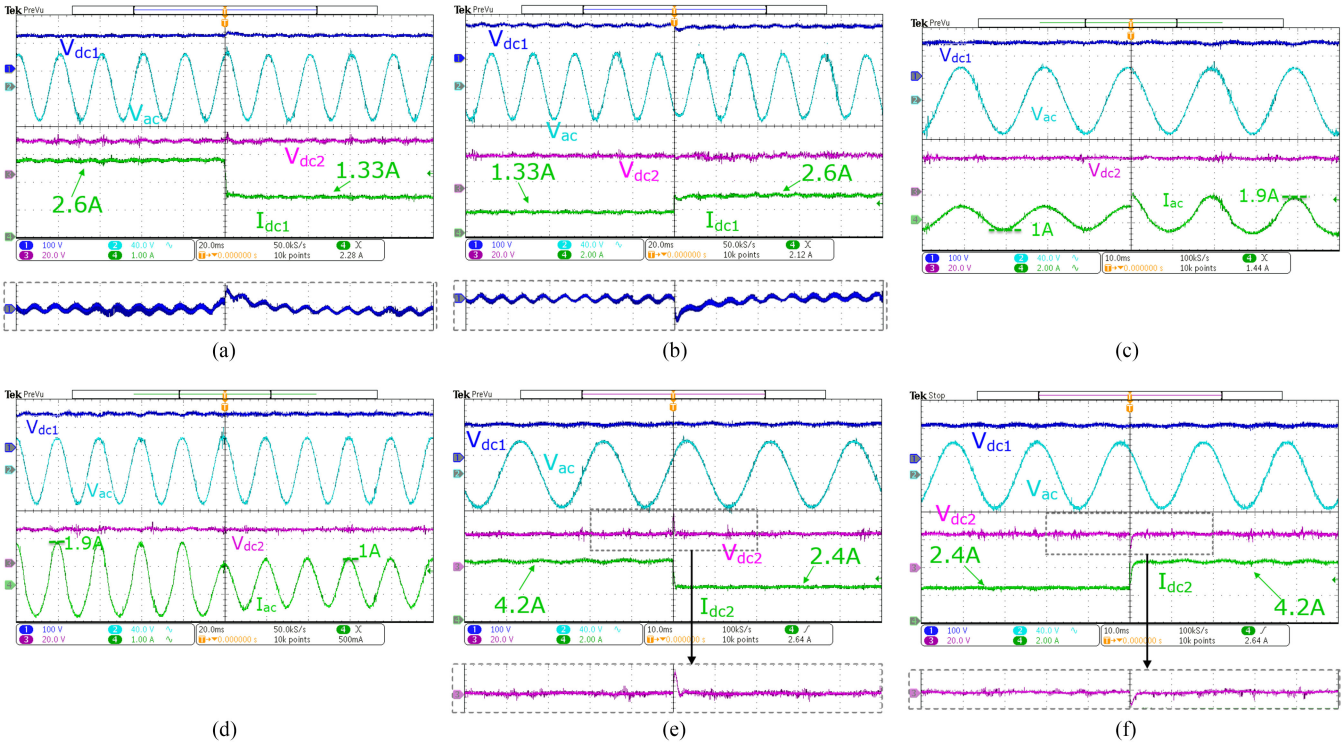

Fig. 13. Experimental results showing the closed-loop load dynamics during (a) step-down I_{dc1} load change, (b) step-up I_{dc1} load change, (c) step-up I_{ac} load change, (d) step-down I_{ac} load change, (e) step-down I_{dc2} load change, and (f) step-up I_{dc2} load change.

is stepped down making the current to decrease to 1.2 from 2.4 A. Similarly, the dynamics caused due to change in V_{ac} and V_{dc2} loads are shown in Fig. 12(c)–(f), respectively. From all the results presented, a dip or rise can be clearly observed in the output voltages immediately after the load change which later settles to some value, which is slightly different from the voltage values before the load change. It is because of the change in the voltage drops across the different components due to the change in the current flowing through them. It can be observed that there are no unstable oscillations taking place due to load change indicating that the output voltages are stable. Thus, it can be concluded that as long as the converter is operating in CCM, the proposed converter does not experience the cross-regulation problem.

C. Closed-Loop Dynamics

This section presents the results of the closed-loop operation of the proposed converter. The control strategy discussed in Section III-A has been used for this operation. The Nexys 4 DDR Artix 7 kit is used for implementing the digital controller.

Fig. 13(a) and (b) shows the closed-loop dynamics of the proposed converter due to the step-change in the I_{dc1}. The dotted part indicates the V_{dc1} waveform taken in the ac coupling mode to observe the error. Fig. 13(a) shows the dynamics when the load is stepped down from 2.6 to 1.3 A. From the ac coupling result, it can be observed that there is a rise in the voltage immediately after the load change. However, the voltage settles back and follows the reference value within three ac cycles. Also, a small change can be observed in all the output voltages; however, due to controller action, all the output voltage settles back to the reference voltage levels. Fig. 13(b) represents the dynamics caused due to stepping up the load current I_{dc1} from 1.33 to 2.6 A. A voltage dip can be observed, which is compensated by the controller thereby making the voltage to follow the reference voltage.

Similarly, from Fig. 13(c)–(f), the dynamics due to the step changes in I_{ac} and I_{dc2} can be observed, respectively. The current values before and after the load changes can also be observed from the respective figures.

As explained earlier, a small change in the output voltages can be seen immediately after the load changes. However, due to the control action of the proposed controller, all the voltage levels settle back to the reference value within a span of two to four ac cycles, i.e., 40–80 ms. From all the abovementioned results, the partially decoupled output voltages control strategy of the proposed converter has been verified.

D. Loss and Efficiency Analysis

As per Table II, insulated gate bipolar transistor (IGBT) IKW30N65ES5 is used for developing the prototype. The electrical parameters of the IKW30N65ES5 are $E_{\mathrm{on}} = 0.26$ mJ, $E_{\mathrm{off}} = 0.17$ mJ at $V_{\mathrm{ref}} = 400$ V and $I_{\mathrm{ref}} = 15$ A and forward voltage drop $V_F = 0.6$ V. The diode 40EPF06 has a forward voltage drop of 0.6 V when the current flowing is 1 A and 0.8 V when the current flowing is 6.5 A. From the steady-state performance results, the output power can be calculated as $114 * 1.267 + 21.5 * 4.2 + 32.526 * 1.343 = 279$ W. The input power to the converter is $48 * I_L = 48 * 6.5 = 312$ W. The IGBT losses were found to be 17 W, diode losses 7 W, capacitor effective series resistance (ESR) losses 4.39 W, and the inductor ESR losses 3.95 W. Loss

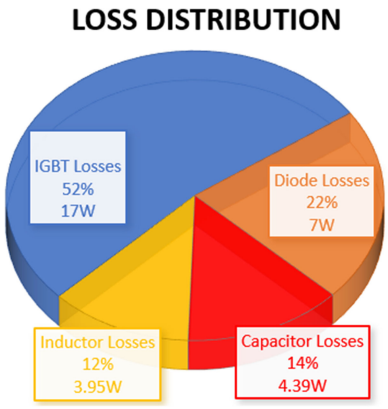

Fig. 14. Power loss distribution in the proposed converter for a 310-W prototype.

distribution of the proposed converter is shown in Fig. 14. The efficiency was found to be 89.2%.

Power loss distribution with respect to the load variation is shown in Fig. 15(a)–(c). Two of the output loads have been kept constant and one load is changed. Fig. 15(a) shows loss distribution for $I_{\rm dc1}$ load variation with the other two remaining constant. Similarly, Fig. 15(b) and (c) shows the loss distribution for the $I_{\rm dc2}$ and $I_{\rm ac}$ load variations, respectively. Fig. 16 shows the experimental efficiency of the proposed converter at different gains of a particular output while the gains of the other two outputs are kept constant. Fig. 16(a) shows the efficiency of the proposed converter at different gains of $V_{\rm dc1}$ while the gains of $V_{\rm dc2}$ and $V_{\rm ac}$ are kept unchanged at prototype power rating of 310 W. Similarly, Fig. 16(b) and (c) shows the efficiency at different gains of $V_{\rm dc2}$ and $V_{\rm ac}$, respectively.

It can be observed from the abovementioned experimental results presented in Figs. 15 and 16 that the proposed converter is capable of working efficiently at different gains and loading conditions. The efficiency is observed to be of the range 88%–90% in the abovementioned cases. The conventional multi output converters that give both dc outputs have a typical efficiency of around 92%–95%, whereas that of those which give an ac outputs is around 86%–92%. The proposed converter also gives an ac output and the efficiency is at par with the conventional multioutput converters involving ac output. The usage of optimized devices and components for the proposed converter would increase the efficiency by 1%–3%. From this it can be inferred that the proposed converter is efficient for a wide range of voltage gains and loading conditions, enabling a wide operation range of the converter and making it suitable for many applications.

E. Different Operating Modes

The proposed q-ZSC is capable of giving one boost dc output, one buck–boost dc output, and one buck–boost ac output, i.e., four different modes of operation are possible of which one mode is explained above. The abovepresented results are for one boost dc, one buck dc, and ac outputs. This section presents the steady-state results of the proposed q-ZSC in different modes of operation.

Fig. 17(a) shows the steady-state results for the converter being operated at $D_1 = 0.34$, $D_2 = 0.4$, and $M_a = 0.25$ for the input voltage $V_{\rm in} = 48$ V giving the output voltages $V_{\rm dc1} = 142$ V, $V_{\rm dc2} = 56$ V, and $V_{\rm ac\text{-}pk} = 36$V. The result confirms that the proposed converter gives two boost dc outputs and one buck ac output.

Fig. 17(b) shows the steady-state results for the converter being operated at $D_1 = 0.38$, $D_2 = 0.265$, $M_a = 0.34$ for the input voltage $V_{\rm in} = 48$ V giving the output voltages $V_{\rm dc1} = 190$ V, $V_{\rm dc2} = 50$ V, and $V_{\rm ac\text{-}pk} = 56$ V. The result confirms that the proposed converter is capable of giving all boost type outputs.

Fig. 17(c) shows the steady-state results for the converter being operated at $D_1 = 0.3$, $D_2 = 0.1$, and $M_s = 0.56$ for the input voltage $V_{\rm in} = 48$ V giving the output voltages $V_{\rm dc1} = 112$ V, $V_{\rm dc2} = 10.5$ V, and $V_{\rm ac\text{-}pk} = 62$ V. The result confirms that the proposed converter gives one boost dc, one buck dc and boost ac output voltages.

It is important to note that if the two dc outputs are of boost type, the maximum permissible value of modulation index M_a becomes very small as D_1 and D_2 constitute the major part of (4). Due to the lower value of M_a, the power quality of the output ac voltage might get affected. For such requirements, Type II converter is used where the maximum value of M_a is equal to D_2. Since D_2 has already a big value, the inverter can be operated at a higher M_a to ensure the proper power quality. Thus, depending on the load requirement one among the proposed q-ZSCs can be used.

F. Applications of the Proposed Converter

The proposed buck–boost multioutput q-ZSC is able to give two dc outputs with boost and buck–boost capabilities and one ac output with buck–boost capability. It possesses high power density and can be applied to modern electrical applications, such as renewables and uninterruptible power supplies (UPS) for households. The details of the proposed q-ZSC for renewables and UPS applications along with the specification justification are given as follows.

1) Renewables: For the input voltage range of (>72 dc) generated from the renewable sources, the proposed multioutput q-ZSC gives $V_{\rm dc1} = 380$ V and $V_{\rm dc2} = 48$ V (two dc outputs) and $V_{\rm ac} = 110$ V (rms). For an input voltage of 84 V, the abovementioned voltages are generated for $D_1 = 0.39$, $D_2 = 0.133$, and $M_a = 0.43$. It may be noticed that 110 V(rms) ac is a standard ac voltage used for commercial and households, 380 V dc can be used as standard dc bus voltage, and 48 V dc is a standard dc voltage used for many custom dc appliances. In this way, the proposed q-ZSC can be practically applied in renewable energy applications, such as hybrid microgrids.

2) Uninterruptible Power Supplies: The proposed q-ZSC can also be applied for UPS for households. One practical scenario is that if the proposed q-ZSC is operated with 24 V input voltage, for $D_1 = 0.25$, $D_2 = 0.104$, and $M_a = 0.646$, the output voltages would be $V_{\rm dc1} = 48$ V, $V_{\rm dc2} = 5$ V, and $V_{\rm ac} = 22$ V ac. 48 V and 5 V dc can be used directly for custom appliances, and with the help of small line frequency transformer, 22 V(rms) ac can be upgraded to 110 V (rms) ac for its practical uses.

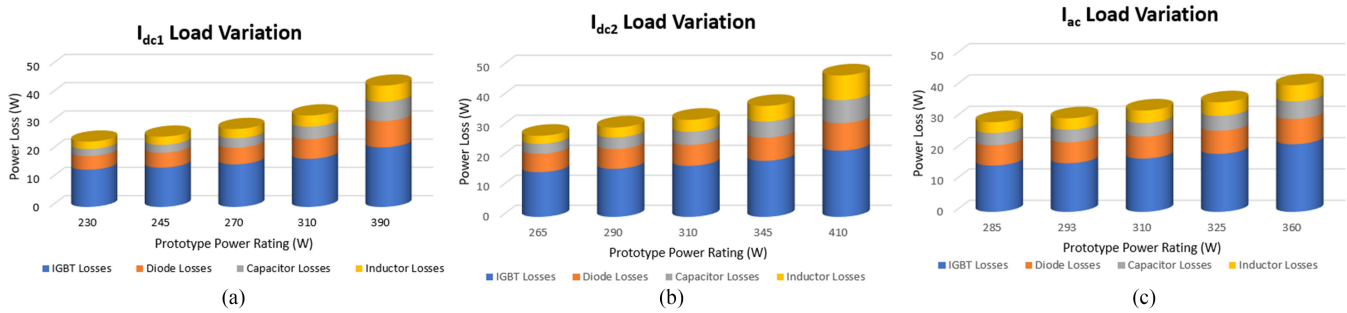

Fig. 15. (a) Loss distribution with change in I_{dc1} and keeping other two loads constant. (b) Loss distribution with change in I_{dc2} and keeping other two loads constant. (c) Loss distribution with change in I_{ac} and keeping other two loads constant.

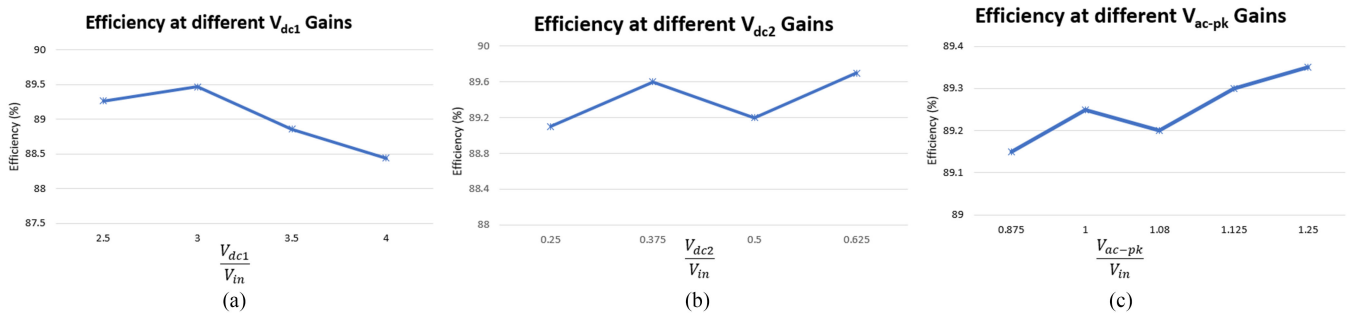

Fig. 16. Efficiency versus (a) V_{dc1} gain when other output gains are constant, (b) V_{dc2} gain when other output gains are constant, and (c) V_{ac} gain when other output gains are constant and the total prototype rating is maintained constant.

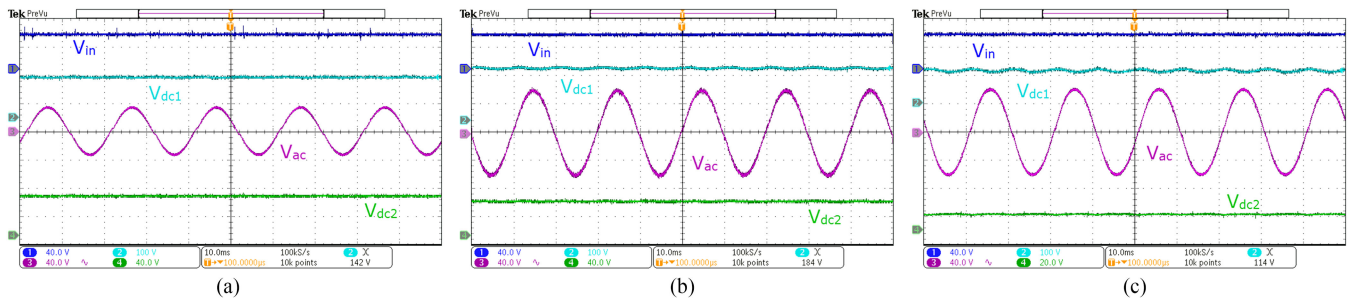

Fig. 17. Steady-state operation of the proposed multioutput q-ZSC, (a) with two boost dc and buck ac outputs, (b) with two boost dc and ac outputs, and (c) with one boost dc, one buck dc, and boost ac outputs.

It is important to note that the proposed converter can operate for a range of input dc voltage levels for the abovementioned applications. As per the constraints on the duty ratio discussed in (4), (8), (9), and (10) and the nonidealities of components, the input voltage can be decided as per the requirement of the application.

VII. Conclusion

In this article, two hybrid multioutput buck–boost q-ZSCs capable of giving two dc and one ac outputs simultaneously have been presented. The proposed q-ZSCs have the capability to give both buck and boost ac outputs, as well as buck and boost dc outputs, unlike the conventional multioutput converters. Owing to the buck–boost capability of the outputs, the proposed q-ZSCs give a wide range of voltage gain for both ac and dc outputs. The outputs of the proposed q-ZSC can be independently regulated making it suitable for various multioutput dc–dc and dc–ac power conversions for modern applications, such as renewables and UPS. It is important to mention that the rationale behind proposing two variants of the proposed concept is to give extra flexibility in voltage gain as per the load requirement. Moreover, as the proposed q-ZSCs have been derived from quasi-Z-source concept, they inherit all the characteristics of the qZSIs, such as inherent shoot-through protection and improved reliability in contrast to the VSI-derived conventional multioutput topologies. Detailed steady-state operation, loss analysis, and discussion on the novel PWM technique of the proposed q-ZSC have been presented in this article. In order to bring out the distinctive property of the proposed q-ZSC, a comparative analysis among the proposed and other closely related conventional multioutput topologies has also been carried out. The proposed hybrid multioutput q-ZSC has been validated experimentally on a 310-W prototype for open-loop operation as well as closed-loop operation.

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