Effect of Asymmetric Layout and Unequal Junction Temperature on Current Sharing of Paralleled SiC MOSFETs With Kelvin-Source Connection

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***Abstract*—Parallel connection of silicon carbide (SiC) MOSFETs is a popular solution for high-capacity applications. In order to improve the switching speed of paralleled SiC MOSFETs, Kelvin-source connection is widely employed. However, the influences of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with Kelvin-source connection are not clear. This article addresses the issue for the first time by theoretical analysis and experimental verifications. The mechanism of current imbalance resulting from asymmetric layout and unequal junction temperature in the case with Kelvin-source connection is comprehensively investigated. Then, some significant discoveries are obtained. The static current sharing performance can be affected by drain and power source parasitic inductance, which is seldom mentioned before. Besides, this article first points out that the effect of power source parasitic inductance on dynamic current sharing is dominant compared with other parasitic inductance. What is more, the thermal–electric analyzing results suggest that there is a risk of thermal runaway for paralleled SiC MOSFETs with Kelvin-source connection at high switching frequency due to positively temperature-dependent dynamic current and switching losses. Based on the discoveries, some guidelines are provided for layout design and application of paralleled SiC MOSFETs with Kelvin-source connection.**

***Index Terms*—Asymmetric layout, current sharing, Kelvin-source connection, paralleled silicon carbide (SiC) MOSFETs, unequal junction temperature.**

I. Introduction

SILICON carbide (SiC) MOSFETs are promising in fields such as electric vehicle (EV) chargers, EV main inverters, and photovoltaic inverters due to their high efficiency, fast switching speed, and excellent thermal performance [1], [2]. However, the maximum current rating of commercial chips is generally limited by 100 A for SiC MOSFETs [3]. Therefore, parallel operation of SiC MOSFETs is a popular method to improve current capacity. However, inconsistent device parameters, asymmetric layout, and unequal junction temperature can lead to unbalanced current among paralleled SiC MOSFETs [4]. The unbalanced current can further result in unequal conduction and switching losses [5]. It also challenges the stability and security of paralleled chips even the whole system. Therefore, paralleled SiC MOSFETs tend to be derated in operation [6]. In order to fully utilize the capacity of each SiC MOSFET chip and improve the general reliability, it is necessary to take measures to mitigate the unbalanced current among paralleled SiC MOSFETs. The methods to suppress current imbalance can be divided into two categories: active methods and passive methods. First, there are some active methods for current balancing. Some active gate drivers and current sensors can form a closed loop to suppress current imbalance [6]–[9]. However, current sensors are too bulky to be integrated into multichip power modules and the active drivers are generally complicated and expensive. Second, there are some passive methods. In [10]–[13], some magnetic components are inserted into paralleled branches to enhance current sharing performance. Several methods to achieve symmetric layout are proposed to promote current sharing in [14]–[17]. Besides, the length of bonding wires is adjusted to balance parasitic inductance for better current sharing performance in [18]. However, it is difficult to achieve absolutely symmetric layout and interconnections in practice. Thus, the mechanism of current imbalance should be analyzed to figure out the main factors affecting current sharing. Then, the unbalanced current can be effectively suppressed by mitigating the mismatches of major affecting factors.

Some research works have been done to investigate the effect of various mismatches on current sharing. In [19] and [20], the impact of mismatched device parameters on current sharing is discussed. The results show that the ON-state resistance (R_{ds}) and threshold voltage (V_{th}) can affect static and dynamic current sharing, respectively. In [21], the influence of asymmetric layout on current sharing of paralleled SiC MOSFETs is analyzed for the first time. It reveals that the common source parasitic inductance mismatches can cause dynamic current imbalance but have little effect on static current sharing. It also suggests that the mismatched drain parasitic inductance can result in unbalanced static current. However, all the discussions above are based on the case without Kelvin-source connection.

Kelvin-source connection has been widely applied in paralleled SiC MOSFETs to improve switching speed and reduce switching losses [22]–[24]. The parasitic circuit models of a double pulse tester for two paralleled SiC MOSFETs with and without Kelvin-source connection are shown in Fig. 1. The parameters

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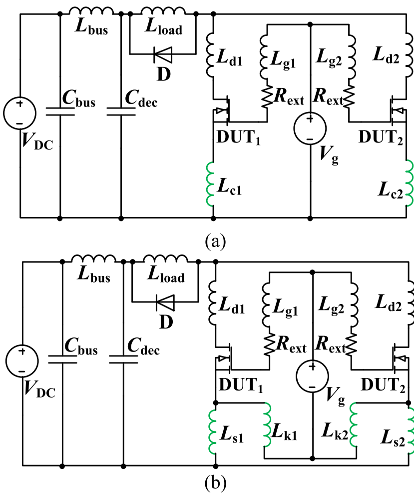

Fig. 1. Parasitic circuit models (a) without and (b) with Kelvin-source connection.

TABLE I
PARAMETERS IN PARASITIC CIRCUIT MODELS

Symbols	Parameters
V_{DC}	DC bus voltage
V_g	Drive voltage
R_{ext}	Drive resistance
C_{bus}	Bus capacitance
C_{dec}	Decoupling capacitance
L_{bus}	Parasitic inductance on DC bus
L_{load}	Load inductance
L_{d1}, L_{d2}	Drain parasitic inductance
L_{s1}, L_{s2}	Power source parasitic inductance
L_{g1}, L_{g2}	Gate parasitic inductance
L_{k1}, L_{k2}	Drive source parasitic inductance
L_{c1}, L_{c2}	Common source parasitic inductance

in the models are listed in Table I. It can be seen that the common source parasitic inductance disappear, whereas power source and drive source parasitic inductance appear when Kelvin-source connection is introduced. The Kelvin-source connection can greatly change the parasitic circuit models of paralleled SiC MOSFETs. Thus, it is necessary to reconsider the effect of various mismatches, such as inconsistent device parameters, asymmetric layout, and unequal junction temperature, on current sharing performance of paralleled SiC MOSFETs with Kelvin-source connection.

The influence of inconsistent device parameters on current sharing in the case with Kelvin-source connection has been basically discussed in [10]. And this article focuses on the influences of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with Kelvin-source connection. The case with two paralleled SiC MOSFETs is discussed for clear illustration. And the parasitic circuit model is shown in Fig. 1(b). Besides, there are some definitions in (1), which can be applied to all variables mentioned in following sections

$$\begin{cases} \Delta x = x_1 - x_2 \\ x = x_1 + x_2. \end{cases} \tag{1}$$

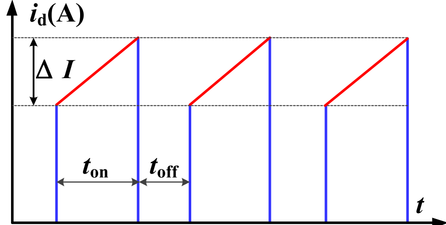

Fig. 2. Qualitative current waveforms of SiC MOSFETs in most applications with inductive load.

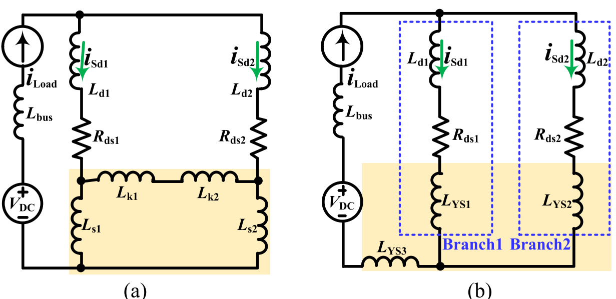

Fig. 3. Static circuit models. (a) Initial and (b) simplified static circuit models.

The rest of this article is organized as follows. Section II discusses about static current sharing. The static circuit model is built up according to the operation region of SiC MOSFETs. Based on the model, the mechanism of static current imbalance is analyzed by mathematical methods. Then, the effect of asymmetric layout and unequal junction temperature on static current sharing is separately discussed. In Section III, dynamic current sharing performance is investigated by a similar method. Then, some experimental results are presented in Section IV to verify the analysis in Sections II and III. Finally, the conclusion and design guidelines are summarized in Section V.

II. STATIC CURRENT SHARING

There are few research works about static current sharing of paralleled SiC MOSFETs on account of its self-balanced capability resulting from positively temperature-dependent ON-state resistances [25], [26]. However, the ON-state resistances of SiC MOSFETs are less sensitive to junction temperature compared to Si MOSFETs [12]. Thus, the self-balanced capability of static current for paralleled SiC MOSFETs is limited. Besides, the mismatched parasitic inductance can also lead to static current imbalance because the ON-state current is not constant during conduction periods, as shown in Fig. 2. Thus, the static current sharing of paralleled SiC MOSFETs should be investigated in detail.

A. Static Circuit Model

The devices under test (DUTs) can be replaced by their ON-state resistances (R_{ds1} and R_{ds2}) during conduction periods, and the freewheeling diode is reversely blocked. Besides, the load inductor can be modeled as a current source. Thus, the initial static circuit model is shown in Fig. 3(a). It can be further transformed into Fig. 3(b) based on Δ-*Y* transformation, where

L_{YS1}, L_{YS2}, and L_{YS3} are

$$\begin{cases} L_{YS1} = \dfrac{L_{s1}\left(L_{k1}+L_{k2}\right)}{L_{s1}+L_{s2}+L_{k1}+L_{k2}} = \dfrac{\left(L_s+\Delta L_s\right)L_k}{2\left(L_s+L_k\right)} \\ L_{YS2} = \dfrac{L_{s2}\left(L_{k1}+L_{k2}\right)}{L_{s1}+L_{s2}+L_{k1}+L_{k2}} = \dfrac{\left(L_s-\Delta L_s\right)L_k}{2\left(L_s+L_k\right)} \\ L_{YS3} = \dfrac{L_{s1}L_{s2}}{L_{s1}+L_{s2}+L_{k1}+L_{k2}} = \dfrac{L_s^2-\Delta L_s^2}{4\left(L_s+L_k\right)}. \end{cases} \quad (2)$$

The simplified circuit model in Fig. 3(b) suggests that the unbalanced static current depends on the difference between branches 1 and 2.

B. Mathematical Analysis of Static Current Imbalance

Branches 1 and 2 in Fig. 3(b) satisfy Kirchhoff's voltage law (KVL), which can be expressed as

$$a_1\frac{di_{Sd1}}{dt} + b_1\frac{di_{Sd2}}{dt} + a_2 i_{Sd1} + b_2 i_{Sd2} = 0 \quad (3)$$

where a_1, b_1, a_2, and b_2 are

$$\begin{cases} a_1 = L_{d1} + L_{YS1} \\ b_1 = -L_{d2} - L_{YS2} \\ a_2 = R_{ds1} \\ b_2 = -R_{ds2}. \end{cases} \quad (4)$$

According to (1), (3) can be rewritten as

$$k_1\frac{di_{Sd}}{dt} + k_2\frac{d\Delta i_{Sd}}{dt} + \Delta R_{ds} i_{Sd} + R_{ds}\Delta i_{Sd} = 0 \quad (5)$$

where k_1 and k_2 are

$$\begin{cases} k_1 = \Delta L_d + \dfrac{\Delta L_s L_k}{L_s + L_k} \\ k_2 = L_d + \dfrac{L_s L_k}{L_s + L_k}. \end{cases} \quad (6)$$

Based on (5) and (6), the unbalanced static current can be derived as

$$\Delta i_{Sd} = G_{Ss}\Delta L_s + G_{Sd}\Delta L_d + G_{SR}\Delta R_{ds} \quad (7)$$

where G_{Ss}, G_{Sd}, and G_{SR} are

$$\begin{cases} G_{Ss} = -\dfrac{sL_k i_{Sd}}{\left(sk_2+R_{ds}\right)\left(L_s+L_k\right)} \\ G_{Sd} = -\dfrac{si_{Sd}}{\left(sk_2+R_{ds}\right)} \\ G_{SR} = -\dfrac{i_{Sd}}{\left(sk_2+R_{ds}\right)} \end{cases} \quad (8)$$

where s is the Laplace operator.

The coefficients G_{Ss}, G_{Sd}, and G_{SR} can reflect the effect of ΔL_s, ΔL_d, and ΔR_{ds} on static current sharing, respectively.

C. Effect of Asymmetric Layout on Static Current Sharing

The asymmetric layout can lead to mismatched power source and drain parasitic inductance. This can further result in unbalanced static current according to (7). Assuming that there is no junction temperature difference and device parameter mismatches for paralleled SiC MOSFETs, and based on (7) and (8), Δi_{Sd} with maximum amplitude can be expressed as

$$\Delta i_{Sd(\text{max_amp})} = -\frac{L_k}{R_{ds}\left(L_s+L_k\right)}\frac{di_{Sd}}{dt}\Delta L_s - \frac{1}{R_{ds}}\frac{di_{Sd}}{dt}\Delta L_d. \quad (9)$$

Considering that di_{Sd}/dt is positive in most applications with inductive load (see Fig. 2), it can be deduced that

$$\begin{cases} \dfrac{\partial \Delta i_{Sd(\text{max_amp})}}{\partial \Delta L_s} = -\dfrac{L_k}{R_{ds}\left(L_s+L_k\right)}\frac{di_{Sd}}{dt} < 0 \\ \dfrac{\partial \Delta i_{Sd(\text{max_amp})}}{\partial \Delta L_d} = -\dfrac{1}{R_{ds}}\frac{di_{Sd}}{dt} < 0. \end{cases} \quad (10)$$

Equation (10) indicates that the device with larger power source and drain parasitic inductance will carry less static current. In addition, there is

$$\frac{|G_{Sd}|}{|G_{Ss}|} = \frac{L_s + L_k}{L_k} > 1 \quad (11)$$

which suggests that the unbalanced static current caused by ΔL_d is larger than that by equal ΔL_s.

In general, the mismatched power source and drain parasitic inductance can lead to static current imbalance. The static current tend to go through the device with less power source and drain parasitic inductance. And the unbalanced static current is more sensitive to the mismatched drain parasitic inductance than the mismatched power source parasitic inductance.

D. Effect of Unequal Junction Temperature on Static Current Sharing

By (7), it is clear that the unbalanced static current can be caused by ΔR_{ds}, and according to [27], the ON-state resistances of SiC MOSFETs are affected by junction temperature. Hence, the junction temperature difference (ΔT_j) can lead to mismatches of ON-state resistances, which further affect the static current sharing performance. Then, the influences of ΔT_j on static current sharing are investigated from the thermal–electric coupling perspective.

The curve of ON-state resistance versus junction temperature is generally provided by manufacturers in the datasheet. Some discrete data can be extracted from the curve. Then, the mathematical relationship between ON-state resistance and junction temperature can be obtained by curve fitting. Take the SiC MOSFET C3M0120100K as an example. The extracted data and fitting curve are shown in Fig. 4.

The mathematical relationship between ON-state resistance and junction temperature for DUT_i ($i = 1$ or 2) can be expressed as

$$R_{dsi} = 115 + 0.06398T_{ji} + 0.00191T_{ji}^2. \quad (12)$$

According to (1) and (12), there are

$$\begin{cases} \Delta R_{ds} = \left(0.06398 + 0.00191T_j\right)\Delta T_j \\ R_{ds} = 330 + 0.06398T_j + 0.00096T_j^2 + 0.00096\Delta T_j^2. \end{cases} \quad (13)$$

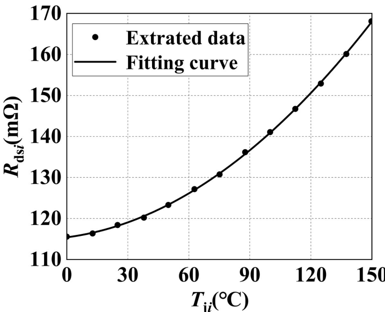

Fig. 4. ON-state resistance versus junction temperature for C3M0120100K with drive voltage of 18 V.

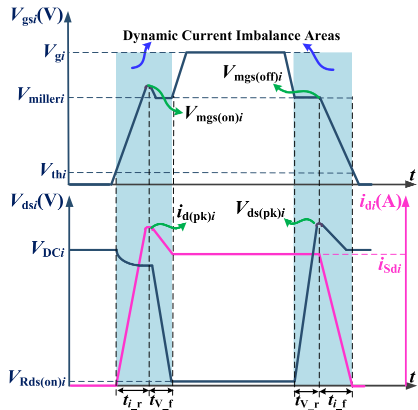

Fig. 5. Qualitative switching waveforms of SiC MOSFETs.

Assuming the layout is symmetric and according to (7), (8), and (13), the unbalanced static current caused by unequal junction temperature can be written as (14) shown at bottom of the page.

Based on (14), Δi_{Sd} with maximum amplitude is

$$\Delta i_{Sd(\text{max_amp})} = -\frac{(0.06398 + 0.00191T_j)\, i_{Sd}}{330 + 0.06398T_j + 0.00096T_j^2 + 0.00096\Delta T_j^2}\Delta T_j. \quad (15)$$

Assuming $T_j > 0$ and $\Delta T_j > 0$ and according to (15), there is

$$\frac{\partial \Delta i_{Sd(\text{max_amp})}}{\partial \Delta T_j} < 0. \quad (16)$$

Equation (16) reveals that the unbalanced static current of paralleled SiC MOSFETs with Kelvin-source connection is negatively related to ΔT_j. And the device with higher junction temperature will carry less static current than the one with lower junction temperature.

The unbalanced conduction losses due to unequal junction temperature are also discussed. Assuming that the total conduction current of two paralleled devices is constant at I and the layout is symmetric, the ON-state loss power can be expressed as

$$\begin{cases} P_{S1} = R_{ds1}\left(\dfrac{IR_{ds2}}{R_{ds1}+R_{ds2}}\right)^2 \\ P_{S2} = R_{ds2}\left(\dfrac{IR_{ds1}}{R_{ds1}+R_{ds2}}\right)^2. \end{cases} \quad (17)$$

According to (1) and (17), the mismatched ON-state loss power can be derived as

$$\Delta P_S = P_{S1} - P_{S2} = \frac{I^2\left(\Delta R_{ds}^3 - R_{ds}^2 \Delta R_{ds}\right)}{4R_{ds}^2}. \quad (18)$$

By (18), there is

$$\frac{\partial \Delta P_S}{\partial \Delta T_j} = \frac{I^2\left(3\Delta R_{ds}^2 - R_{ds}^2\right)}{4R_{ds}^2}\frac{\partial \Delta R_{ds}}{\partial \Delta T_j} - \frac{I^2 \Delta R_{ds}^3}{2R_{ds}^3}\frac{\partial R_{ds}}{\partial \Delta T_j}. \quad (19)$$

In most applications, the junction temperature is limited by the allowed maximum junction temperature in datasheets. Thus, the junction temperature of DUTs in this case should be lower than 150 °C. Based on (13), it can be deduced that

$$3\Delta R_{ds}^2 - R_{ds}^2 < 0. \quad (20)$$

Besides, when $T_j > 0$ and $\Delta T_j > 0$, there are

$$\begin{cases} \dfrac{\partial \Delta R_{ds}}{\partial \Delta T_j} > 0 \\ \dfrac{\partial R_{ds}}{\partial \Delta T_j} > 0. \end{cases} \quad (21)$$

By (19)–(21), it can be deduced that

$$\frac{\partial \Delta P_S}{\partial \Delta T_j} < 0. \quad (22)$$

Equation (22) indicates that the mismatched ON-state losses of paralleled SiC MOSFETs are negatively related to ΔT_j.

In general, unbalanced static current and mismatched ON-state losses of paralleled SiC MOSFETs with Kelvin-source connection are negatively related to ΔT_j, which is beneficial to current sharing and junction temperature balancing.

III. Dynamic Current Sharing

A. Dynamic Circuit Model

The qualitative switching waveforms of DUT$_i$ ($i = 1$ or 2) are shown in Fig. 5 [28]. The dynamic current imbalance mainly occurs in the areas marked by shadow. During these periods, SiC MOSFETs operate in saturation regions. Thus, they can be modeled as current sources controlled by gate–source voltage

$$\Delta i_{Sd} = -\frac{(0.06398 + 0.00191T_j) \times 10^{-3} i_{Sd}}{sk_2 + \left(330 + 0.06398T_j + 0.00096T_j^2 + 0.00096\Delta T_j^2\right) \times 10^{-3}}\Delta T_j \quad (14)$$

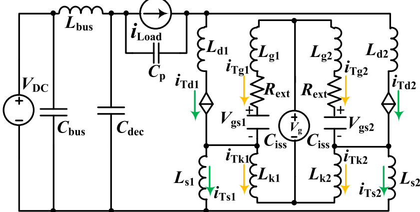

Fig. 6. Initial dynamic circuit model.

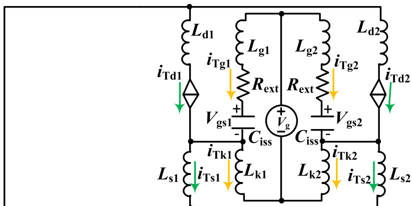

Fig. 7. Differential part of the dynamic circuit model.

(V_{gs}). The load inductor clamped by freewheeling diodes can be modeled as a current source paralleled with the parasitic capacitance (C_p). The drain–source parasitic capacitance (C_{ds}) of SiC MOSFETs can be neglected according to [23], and the gate–source parasitic capacitance (C_{gs}) and gate–drain parasitic capacitance (C_{gd}) behave dynamically as they are in parallel [29]. Based on the above-mentioned analysis, the initial dynamic circuit model is built up, as shown in Fig. 6, where the capacitance C_{iss} is given by

$$C_{iss} = C_{gs} + C_{gd}. \tag{23}$$

Considering that the unbalanced dynamic current is mainly related to the differential part of paralleled branches, the initial dynamic circuit model can be simplified as Fig. 7. Then, it can be seen that the drain parasitic inductances (L_{d1} and L_{d2}) are in series with current sources. Thus, L_{d1} and L_{d2} can be neglected because of the infinite impedance of current sources. Then, the circuit in Fig. 7 can be further simplified as Fig. 8(a). According to the saturation model of SiC MOSFETs, the current through the two current sources can be expressed as

$$\begin{cases} i_{Td1} = g(V_{gs1} - V_{\text{th1}})^2 & V_{gs1} > V_{\text{th1}} \\ i_{Td2} = g(V_{gs2} - V_{\text{th2}})^2 & V_{gs2} > V_{\text{th2}}. \end{cases} \tag{24}$$

By Thevenin's theorem, Fig. 8(a) can be transformed into Fig. 8(b) and the voltage across the voltage source is given by

$$V = s\left(i_{Td1}L_{s1} - i_{Td2}L_{s2}\right). \tag{25}$$

Further, the dynamic circuit model in Fig. 8(b) is equivalent to Fig. 8(c) based on Norton's theorem, where the current through the current source can be written as

$$i = \frac{V}{s\left(L_{s1} + L_{s2}\right)} = \frac{i_{Td1}L_{s1} - i_{Td2}L_{s2}}{L_{s1} + L_{s2}} = \frac{1}{2}\left(\frac{\Delta L_s}{L_s} i_{Td} + \Delta i_{Td}\right). \tag{26}$$

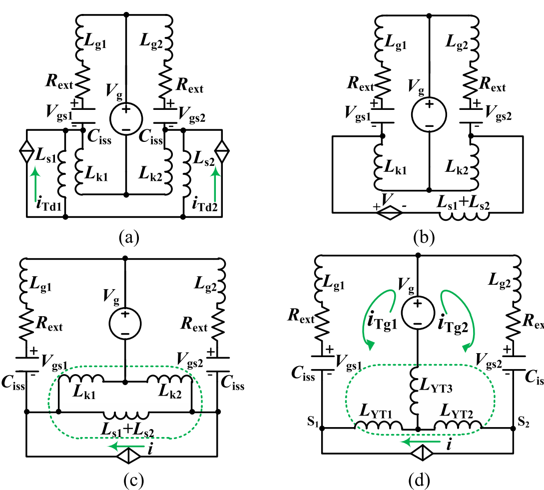

Fig. 8. Transformation of the differential part of the dynamic circuit model.

Applying Δ-*Y* transformation to the network circled by dash line in Fig. 8(c), the circuit can be modified as Fig. 8(d), where L_{YT1}, L_{YT2}, and L_{YT3} are

$$\begin{cases} L_{YT1} = \dfrac{L_{k1}\left(L_{s1} + L_{s2}\right)}{L_{s1} + L_{s2} + L_{k1} + L_{k2}} = \dfrac{\left(L_k + \Delta L_k\right) L_s}{2\left(L_s + L_k\right)} \\ L_{YT2} = \dfrac{L_{k2}\left(L_{s1} + L_{s2}\right)}{L_{s1} + L_{s2} + L_{k1} + L_{k2}} = \dfrac{\left(L_k - \Delta L_k\right) L_s}{2\left(L_s + L_k\right)} \\ L_{YT3} = \dfrac{L_{k1}L_{k2}}{L_{s1} + L_{s2} + L_{k1} + L_{k2}} = \dfrac{L_k^2 - \Delta L_k^2}{4\left(L_s + L_k\right)}. \end{cases} \tag{27}$$

B. Mathematical Analysis of Unbalanced Dynamic Current

The circuit model in Fig. 8(d) satisfies KVL, which can be expressed as

$$L_{g1}\frac{di_{Tg1}}{dt} + R_{\text{ext}}i_{Tg1} + V_{gs1} + L_{YT1}\frac{d(i_{Tg1} + i)}{dt} + L_{YT3}\frac{d(i_{Tg1} + i_{Tg2})}{dt} = V_g \tag{28}$$

$$L_{g2}\frac{di_{Tg2}}{dt} + R_{\text{ext}}i_{Tg2} + V_{gs2} + L_{YT2}\frac{d(i_{Tg2} - i)}{dt} + L_{YT3}\frac{d(i_{Tg1} + i_{Tg2})}{dt} = V_g. \tag{29}$$

When (29) is subtracted by (28), we obtain

$$s\left(\left(\Delta L_g + \frac{\Delta L_k L_s}{L_s + L_k}\right) i_{Tg} + \left(L_g + \frac{L_k L_s}{L_s + L_k}\right) \Delta i_{Tg} + \frac{2L_k L_s}{L_s + L_k} i\right) + 2R_{\text{ext}}\Delta i_{Tg} + 2\Delta V_{gs} = 0. \tag{30}$$

By (1) and (24), the unbalanced drain current can be expressed as

$$\Delta i_{Td} = i_{Td1} - i_{Td2} = g\left(V_{gs} - V_{\text{th}}\right)\left(\Delta V_{gs} - \Delta V_{\text{th}}\right). \tag{31}$$

According to (31), the unbalanced gate–source voltage can be written as

$$\Delta V_{gs} = \frac{\Delta i_{Td}}{g\left(V_{gs} - V_{\text{th}}\right)} + \Delta V_{\text{th}}. \tag{32}$$

Based on the characteristic of capacitance, the unbalanced gate current is

$$\Delta i_{Tg} = sC_{iss}\Delta V_{gs}. \tag{33}$$

Take (32) into (33), then the unbalanced gate current can be rewritten as

$$\Delta i_{Tg} = \frac{sC_{iss}\Delta i_{Td}}{g\left(V_{gs} - V_{\text{th}}\right)} + sC_{iss}\Delta V_{\text{th}}. \tag{34}$$

Take (26), (32), and (34) into (30), the unbalanced drain current can be derived as

$$\Delta i_{Td} = G_{Tg}\Delta L_g + G_{Tk}\Delta L_k + G_{Ts}\Delta L_s + G_{TV}\Delta V_{\text{th}} \tag{35}$$

where G_{Tg}, G_{Tk}, G_{Ts}, and G_{TV} are

$$\begin{cases} G_{Tg} = -\dfrac{s}{\alpha} i_{Tg} \\ G_{Tk} = -\dfrac{sL_s}{\alpha\left(L_s + L_k\right)} i_{Tg} \\ G_{Ts} = -\dfrac{sL_k}{\alpha\left(L_s + L_k\right)} i_{Td} \\ G_{TV} = -\dfrac{\beta}{\alpha} \end{cases} \tag{36}$$

where α and β are given by

$$\begin{cases} \alpha = \dfrac{s^2 C_{iss}}{g\left(V_{gs} - V_{\text{th}}\right)}\left(L_g + \frac{L_k L_s}{L_s + L_k}\right) \\ \quad + s\left(\dfrac{2C_{iss}R_{\text{ext}}}{g\left(V_{gs} - V_{\text{th}}\right)} + \dfrac{L_k L_s}{L_s + L_k}\right) + \dfrac{2}{g\left(V_{gs} - V_{\text{th}}\right)} \\ \beta = s^2 C_{iss}\left(L_g + \dfrac{L_k L_s}{L_s + L_k}\right) + 2sC_{iss}R_{\text{ext}} + 2. \end{cases} \tag{37}$$

The coefficients G_{Tg}, G_{Tk}, G_{Ts}, and G_{TV} can reflect the effect of ΔL_g, ΔL_k, ΔL_s, and ΔV_{th} on dynamic current sharing of paralleled SiC MOSFETs with Kelvin-source connection, respectively.

C. Effect of Asymmetric Layout on Dynamic Current Sharing

By (35), it can be seen that ΔL_g, ΔL_k, and ΔL_s can lead to dynamic current imbalance. In practice, the current in the power loop is much larger than that in the drive loop, which suggests that

$$i_{Td} \gg i_{Tg}. \tag{38}$$

Then based on (36), there are

$$\begin{cases} |G_{Ts}| \gg |G_{Tg}| \\ |G_{Ts}| \gg |G_{Tk}|. \end{cases} \tag{39}$$

Equation (39) suggests that the effect of ΔL_g and ΔL_k on dynamic current sharing is negligible compared with ΔL_s. Then, the effect of ΔL_s on dynamic current sharing is further investigated in time domain. Δi_{Td} with maximum amplitude is extracted to evaluate the dynamic current sharing performance. When $|\Delta i_{Td}|$ reaches its maximum value, we obtain

$$\frac{d\Delta i_{Td}}{dt} = 0. \tag{40}$$

Assuming that all the parameters are matched for paralleled SiC MOSFETs except power source parasitic inductance and according to (35)–(37) and (40), Δi_{Td} with maximum amplitude can be approximately expressed as

$$\Delta i_{Td(\text{max_amp})} \approx -\frac{g\left(V_{gs} - V_{\text{th}}\right)L_k}{2\left(L_k + L_s\right)}\frac{di_{Td}}{dt}\Delta L_s. \tag{41}$$

The value of di_{Td}/dt at turn-ON and turn-OFF transients can be separately approximated as

$$\begin{cases} S_{\text{on}} = \dfrac{di_{Td}}{dt} \approx \dfrac{i_{\text{Load}}}{t_{i_r}} \\ S_{\text{off}} = \dfrac{di_{Td}}{dt} \approx -\dfrac{i_{\text{Load}}}{t_{i_f}} \end{cases} \tag{42}$$

where i_{Load} is the total current of two DUTs. By (41) and (42), $\Delta i_{Td(\text{max_amp})}$ at turn-ON and turn-OFF transients can be separately expressed as

$$\begin{cases} \Delta i_{Td(\text{max_amp})_\text{on}} \approx -\dfrac{g\left(V_{gs} - V_{\text{th}}\right)L_k i_{\text{Load}}}{2\left(L_k + L_s\right)t_{i_r}}\Delta L_s \\ \Delta i_{Td(\text{max_amp})_\text{off}} \approx \dfrac{g\left(V_{gs} - V_{\text{th}}\right)L_k i_{\text{Load}}}{2\left(L_k + L_s\right)t_{i_f}}\Delta L_s. \end{cases} \tag{43}$$

Then, there are

$$\begin{cases} \dfrac{\partial\Delta i_{Td(\text{max_amp})_\text{on}}}{\partial\Delta L_s} \approx -\dfrac{g\left(V_{gs} - V_{\text{th}}\right)L_k i_{\text{Load}}}{2\left(L_k + L_s\right)t_{i_r}} < 0 \\ \dfrac{\partial\Delta i_{Td(\text{max_amp})_\text{off}}}{\partial\Delta L_s} \approx \dfrac{g\left(V_{gs} - V_{\text{th}}\right)L_k i_{\text{Load}}}{2\left(L_k + L_s\right)t_{i_f}} > 0. \end{cases} \tag{44}$$

Equation (44) indicates that the turn-ON and turn-OFF unbalanced currents caused by the mismatched power source parasitic inductance are opposite in polarity. Specifically, the SiC MOSFET with larger power source parasitic inductance will carry less turn-ON current but more turn-OFF current than the one with smaller power source parasitic inductance.

D. Effect of Unequal Junction Temperature on Dynamic Current Sharing

According to (35), ΔV_{th} can affect the dynamic current sharing performance, and the threshold voltage of SiC MOSFETs is negatively temperature dependent [27]. Thus, the unequal junction temperature can lead to threshold voltage mismatches, which can further result in dynamic current imbalance.

Take the SiC MOSFET C3M0120100K as a case. Some discrete data can be extracted from the curve of threshold voltage versus junction temperature in the datasheet. Then, the mathematical relationship between the threshold voltage and junction temperature is obtained by curve fitting. The discrete date and fitting curve are presented in Fig. 9.

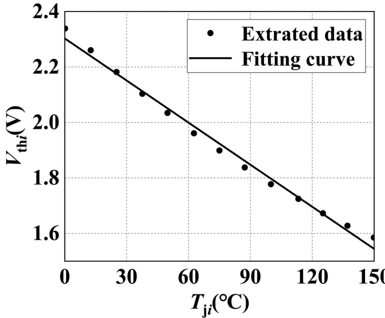

Fig. 9. Threshold voltage versus junction temperature for C3M0120100K.

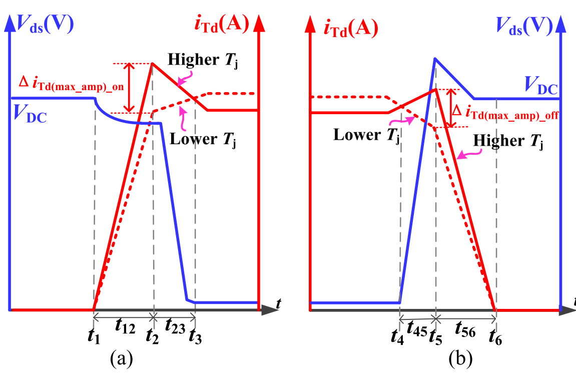

Fig. 10. Qualitative switching waveforms of paralleled SiC MOSFETs with unequal junction temperature at (a) turn-ON and (b) turn-OFF transients.

The mathematical relationship between the threshold voltage and junction temperature for DUT$_i$ ($i = 1$ or 2) can be expressed as

$$V_{\mathrm{th}i} = 2.3029 - 0.00506 T_{ji}. \tag{45}$$

By (45), the mismatched threshold voltage can be derived as

$$\Delta V_{\mathrm{th}} = V_{\mathrm{th1}} - V_{\mathrm{th2}} = -0.00506 \Delta T_j. \tag{46}$$

Assuming that the layout is symmetric and according to (35) and (46), the unbalanced dynamic current resulting from the unequal junction temperature can be written as

$$\Delta i_{Td} = -0.00506 G_{TV} \Delta T_j. \tag{47}$$

According to (36), (37), and (47), Δi_{Td} with maximum amplitude resulting from the unequal junction temperature can be expressed as

$$\Delta i_{Td(\mathrm{max_amp})} = 0.00506 g \left(V_{gs} - V_{\mathrm{th}}\right) \Delta T_j. \tag{48}$$

Based on (48), it can be deduced that

$$\frac{\partial \Delta i_{Td(\mathrm{max_amp})}}{\partial \Delta T_j} = 0.00506 g \left(V_{gs} - V_{\mathrm{th}}\right) > 0. \tag{49}$$

Equation (49) reveals that the unbalanced dynamic current of paralleled SiC MOSFETs with Kelvin-source connection is positively related to ΔT_j. Both turn-ON and turn-OFF currents for the device with higher T_j are larger than that for the device with lower T_j, which is a little different from the case with the mismatched power source parasitic inductance.

Based on the above-mentioned analysis, the switching waveforms of paralleled SiC MOSFETs with different junction temperature are qualitatively depicted in Fig. 10. Based on the waveforms, the unbalanced switching losses can be further discussed.

According to (48) and Fig. 5, Δi_{Td} with maximum amplitude caused by ΔT_j at turn-ON and turn-OFF transients can be further written as

$$\begin{cases} \Delta i_{Td(\mathrm{max_amp})_\mathrm{on}} \approx 0.00506 g (V_{mgs(\mathrm{on})} - V_{\mathrm{th}}) \Delta T_j \\ \Delta i_{Td(\mathrm{max_amp})_\mathrm{off}} \approx 0.00506 g (V_{mgs(\mathrm{off})} - V_{\mathrm{th}}) \Delta T_j. \end{cases} \tag{50}$$

Based on Fig. 10, the unbalanced dynamic current on different stages can be approximately expressed as

$$\begin{cases} \Delta i_{Td}(t) \approx \dfrac{\Delta i_{Td(\mathrm{max_amp})_\mathrm{on}}}{t_{12}} (t - t_1)\,(t_1 < t < t_2) \\ \Delta i_{Td}(t) \approx \dfrac{\Delta i_{Td(\mathrm{max_amp})_\mathrm{on}}}{t_{23}} (t_3 - t)\,(t_2 < t < t_3) \\ \Delta i_{Td}(t) \approx \dfrac{\Delta i_{Td(\mathrm{max_amp})_\mathrm{off}}}{t_{45}} (t - t_4)\,(t_4 < t < t_5) \\ \Delta i_{Td}(t) \approx \dfrac{\Delta i_{Td(\mathrm{max_amp})_\mathrm{off}}}{t_{56}} (t_6 - t)\,(t_5 < t < t_6). \end{cases} \tag{51}$$

According to [30], the mismatched drain–source voltage of paralleled SiC MOSFETs due to unequal junction temperature can be neglected. Then based on (1), we obtain

$$v_{ds1} \approx v_{ds2} \approx \frac{v_{ds}}{2}. \tag{52}$$

Then, the switching losses of paralleled SiC MOSFETs are

$$\begin{cases} E_{\mathrm{on1}} = \int_{t_1}^{t_2} \dfrac{v_{ds} i_{Td1}}{2} dt + \int_{t_2}^{t_3} \dfrac{v_{ds} i_{Td1}}{2} dt \\ E_{\mathrm{on2}} = \int_{t_1}^{t_2} \dfrac{v_{ds} i_{Td2}}{2} dt + \int_{t_2}^{t_3} \dfrac{v_{ds} i_{Td2}}{2} dt \\ E_{\mathrm{off1}} = \int_{t_4}^{t_5} \dfrac{v_{ds} i_{Td1}}{2} dt + \int_{t_5}^{t_6} \dfrac{v_{ds} i_{Td1}}{2} dt \\ E_{\mathrm{off2}} = \int_{t_4}^{t_5} \dfrac{v_{ds} i_{Td2}}{2} dt + \int_{t_5}^{t_6} \dfrac{v_{ds} i_{Td2}}{2} dt. \end{cases} \tag{53}$$

By (50)–(53), the unbalanced switching losses can be derived as

$$\Delta E_T = (E_{\mathrm{on1}} + E_{\mathrm{off1}}) - (E_{\mathrm{on2}} + E_{\mathrm{off2}}) \approx (k_{\mathrm{on}} + k_{\mathrm{off}}) \Delta T_j \tag{54}$$

where k_{on} and k_{off} are

$$\begin{cases} k_{\mathrm{on}} = 0.00506 g (V_{gs(\mathrm{max_on})} - V_{\mathrm{th}}) \\ \qquad \times \left(\int_{t_1}^{t_2} \frac{v_{ds}(t - t_1)}{2t_{12}} dt + \int_{t_2}^{t_3} \frac{v_{ds}(t_3 - t)}{2t_{23}} dt \right) \\ k_{\mathrm{off}} = 0.00506 g (V_{gs(\mathrm{max_off})} - V_{\mathrm{th}}) \\ \qquad \times \left(\int_{t_4}^{t_5} \frac{v_{ds}(t - t_4)}{2t_{45}} dt + \int_{t_5}^{t_6} \frac{v_{ds}(t_6 - t)}{2t_{56}} dt \right). \end{cases} \tag{55}$$

Based on (54) and (55), it can be deduced that

$$\frac{\partial \Delta E_T}{\partial \Delta T_j} \approx k_{\mathrm{on}} + k_{\mathrm{off}} > 0. \tag{56}$$

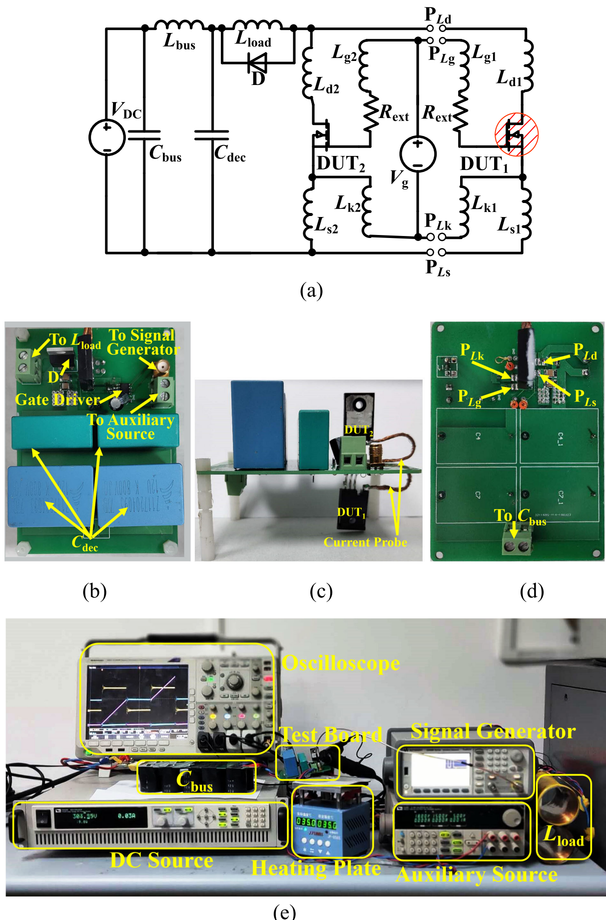

Fig. 11. Experimental test rig. (a) Schematic diagram. (b) Top view of the test board. (c) Side view of the test board. (d) Bottom view of the test board. (e) Test facilities.

Equation (56) indicates that the mismatched switching losses are positively related to ΔT_j, which could lead to thermal runaway for paralleled SiC MOSFETs. To avoid the risk, the mismatches of total loss power (ΔP_{total}) should be negatively related to ΔT_j, which can be expressed as

$$\frac{\partial \Delta P_{\text{total}}}{\partial \Delta T_j} = \frac{\partial \left(D\Delta P_S + f\Delta E_T\right)}{\partial \Delta T_j} < 0 \tag{57}$$

where D and f are duty ratio and switching frequency, respectively.

By (57), the switching frequency of paralleled SiC MOSFETs is limited by

$$f_{(\max)} = -D\frac{\partial \Delta P_S}{\partial \Delta T_j} \bigg/ \frac{\partial \Delta E_T}{\partial \Delta T_j}\ . \tag{58}$$

When the practical switching frequency is larger than $f_{(\max)}$, the mismatched total loss power could be positively related to junction temperature difference. Then, there is a risk of thermal runaway. Thus, it is better to limit the switching frequency within $f_{(\max)}$ for paralleled SiC MOSFETs.

TABLE II
INITIAL PARASITIC INDUCTANCE

Parts	Initial Value
L_{d1}, L_{d2}	20nH
L_{s1}, L_{s2}	20.61nH
L_{g1}, L_{g2}	20.78nH
L_{k1}, L_{k2}	19.95nH

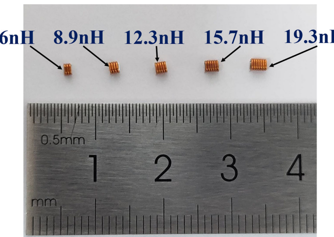

Fig. 12. Ultramini square inductors from Coilcraft.

TABLE III
TEST CONDITIONS

Parameters	Value
V_{DC}	400V
V_g	18V
C_{bus}	470μF (500V Electrolytic capacitors)
L_{load}	120uH (Air-core inductor)
C_{dec}	12μF (800V Film capacitors)
R_{ext}	30Ω

IV. Experimental Verifications

A. Experimental Setup

The double pulse test workbench is established as is shown in Fig. 11. The SiC MOSFETs, C3M0120100K, and SiC diodes, C4D08120A, are employed as DUTs and freewheeling diodes, respectively. The current probe TCP0020 (20 A/50 MHz) is employed to detect the drain current of paralleled SiC MOSFETs. The ports P_{Ld}, P_{Ls}, P_{Lg}, and P_{Lk} are left for inserting external inductors, as shown in Fig. 11(a) and (d). The layout is symmetrically designed and the initial parasitic inductance due to the layout and device package is extracted as is shown in Table II. Then, some ultramini square inductors from Coilcraft are employed as inserted inductors, as seen in Fig. 12. The inductance of inserted inductors varies from 6 to 19.3 nH, which is reasonable in practice. The DUTs are preselected by Agilent 1505 to avoid mismatches of device parameters. In this way, the effect of asymmetric layout on current sharing performance can be investigated. In order to investigate the influence of unequal junction temperature on current sharing performance, the DUT$_1$ is heated up by a heating plate to make the junction temperature of paralleled DUTs different.

The specific test conditions are summarized in Table III. Both static and dynamic currents of initial circuit are balanced, as shown in Fig. 13.

B. Effect of Asymmetric Layout on Static Current Sharing

When the external inductor of 19.3 nH is successively inserted in P_{Ld}, P_{Ls}, P_{Lg}, and P_{Lk}, the overall current waveforms are

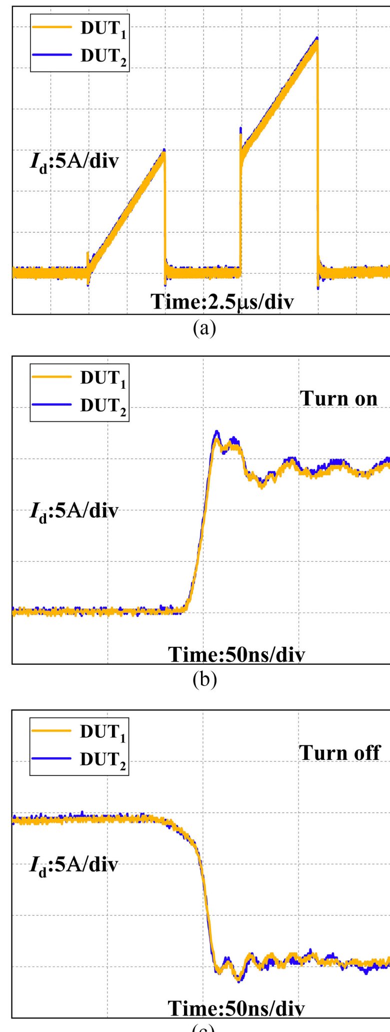

Fig. 13. Initial current waveforms of paralleled DUTs. (a) Overall, (b) turn-ON, and (c) turn-OFF current waveforms.

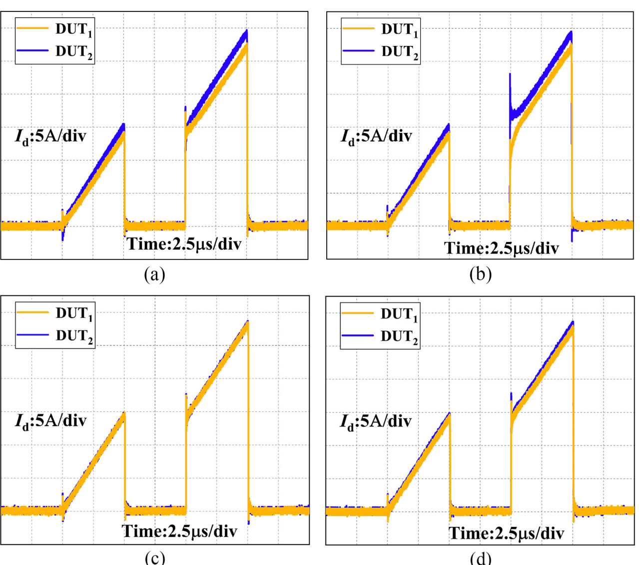

Fig. 14. Overall current waveforms when the inductor of 19.3 nH is inserted in (a) P_{Ld}, (b) P_{Ls}, (c) P_{Lg}, and (d) P_{Lk}.

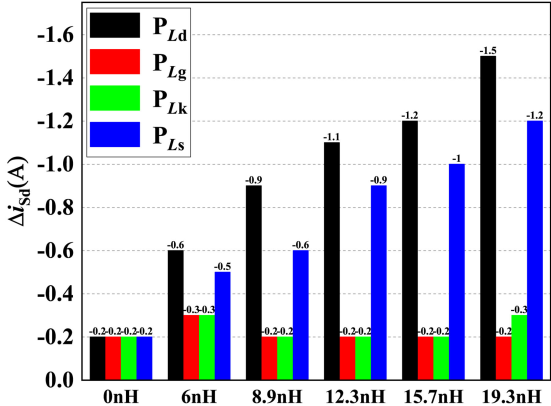

Fig. 15. Unbalanced static current caused by inserted inductors of various inductance values in different ports when load current is 30 A.

shown in Fig. 14. It can be seen that the static current is unbalanced when the inductor is inserted in P_{Ld} and P_{Ls}, whereas the static current is still balanced when the inductor is inserted in P_{Lg} and P_{Lk}. The results qualitatively indicate that ΔL_d and ΔL_s can severely affect static current sharing, whereas ΔL_g and ΔL_k have little effect on static current sharing performance.

Then, the effect of asymmetric layout is further investigated by adjusting the inserted inductance. The static current sharing performance is evaluated by the unbalanced static current when the total load current is 30 A. The results are presented in Fig. 15. The amplitude of unbalanced static current dramatically increases with the inductance inserted in P_{Ld} or P_{Ls}. However, the unbalanced static current is just around its initial value when the inductors with different inductance value are inserted in P_{Lg} or P_{Lk}. The results further verify that ΔL_d and ΔL_s can result in static current imbalance, whereas ΔL_g and ΔL_k can hardly affect static current sharing. And the negative value of Δi_{Sd} means that the static current of DUT_1 is smaller than that of DUT_2, which verifies that the device with larger drain and power source parasitic inductance will carry less static current. Besides, the unbalanced static current caused by external inductors in P_{Ld} is larger than that by inductors of equal value in P_{Ls}, which verifies that the unbalanced static current is more sensitive to ΔL_d than ΔL_s. All the above-mentioned results are consistent with the analysis in Section II.

C. Effect of Asymmetric Layout on Dynamic Current Sharing

The dynamic current waveforms at turn-ON and turn-OFF transients are shown in Fig. 16 when the external inductor of 19.3 nH is successively inserted in P_{Ld}, P_{Ls}, P_{Lg}, and P_{Lk}. The results show that the dynamic current is greatly unbalanced when the external inductor is inserted in P_{Ls}, and the dynamic current sharing performance is hardly affected when the inductors are inserted in P_{Ld}, P_{Lg}, or P_{Lk}. The results qualitatively suggest that ΔL_s can severely affect the dynamic current sharing performance, whereas ΔL_d, ΔL_g, and ΔL_k have little effect on dynamic current sharing. Besides, Fig. 16(b) shows that the turn-OFF current of DUT_1 is larger than that of DUT_2, whereas the turn-ON current of DUT_1 is smaller than that of DUT_2.

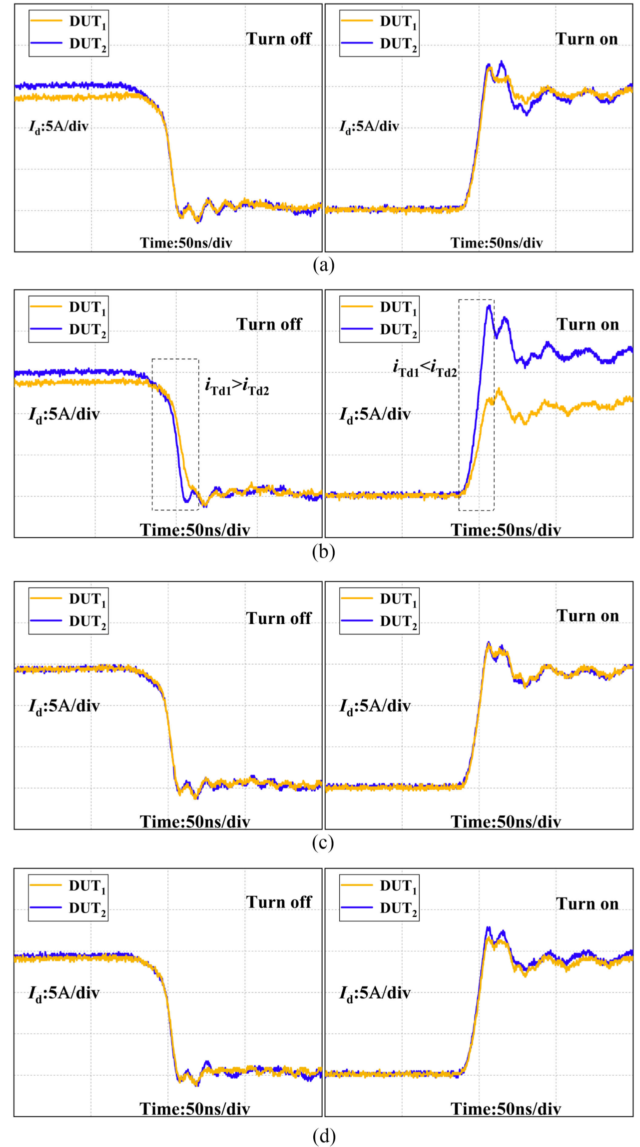

Fig. 16. Turn-OFF and turn-ON current waveforms when the inductor of 19.3 nH is inserted in (a) P_{Ld}, (b) P_{Ls}, (c) P_{Lg}, and (d) P_{Lk}.

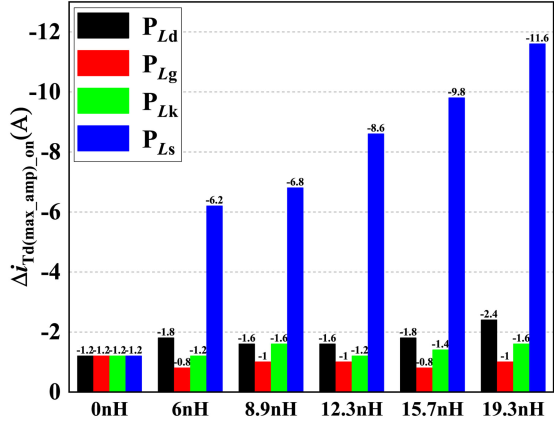

Fig. 17. Unbalanced turn-ON current with maximum amplitude caused by inserted inductors of various inductance values in different ports when load current is 30 A.

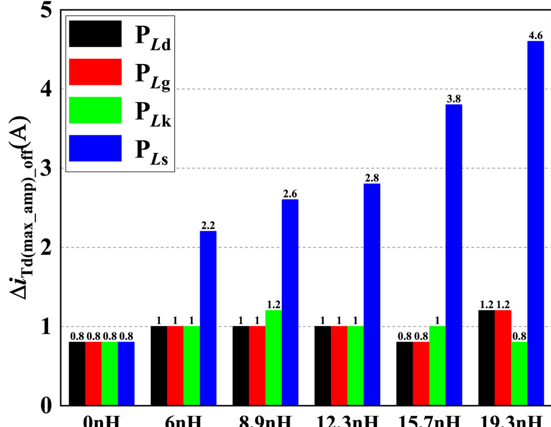

Fig. 18. Unbalanced turn-OFF current with maximum amplitude caused by inserted inductors of various inductance values in different ports when load current is 30 A.

It suggests that the device with larger power source parasitic inductance will carry more turn-OFF current but less turn-ON current.

The turn-ON and turn-OFF imbalanced currents are further investigated by adjusting the inserted inductance. The unbalanced turn-ON and turn-OFF currents with maximum amplitude, $\Delta i_{Td(\max_amp)_on}$and $\Delta i_{Td(\max_amp)_off}$, are separately extracted to evaluate the dynamic current sharing performance. The results are described in Figs. 17 and 18. It can be seen that the amplitudes of $\Delta i_{Td(\max_amp)_on}$ and $\Delta i_{Td(\max_amp)_off}$ dramatically increase with the inductance inserted into P_{Ls}. However, when various inductors are inserted into P_{Ld}, P_{Lk}, or P_{Lg}, the amplitudes of $\Delta i_{Td(\max_amp)_on}$ and $\Delta i_{Td(\max_amp)_off}$ are almost equal to the initial value. The results suggest that ΔL_s can dominate unbalanced dynamic current and the effect of ΔL_d, ΔL_k, and ΔL_g on dynamic current sharing can be neglected to some degree. Besides, the opposite polarities of $\Delta i_{Td(\max_amp)_on}$ and $\Delta i_{Td(\max_amp)_off}$ indicate that the larger power source parasitic inductance can result in smaller turn-ON current but larger turn-OFF current for paralleled SiC MOSFETs with Kelvin-source connection. All the above-mentioned results accord with the analysis in Section III.

D. Effect of Unequal Junction Temperature on Static and Dynamic Current Sharing

Considering that it is difficult to directly detect the junction temperature, the case temperature is measured to approximately reflect the junction temperature. All the external inductors are removed to guarantee that the layout is symmetric. Then, the DUT_1 is heated up by a heating plate to increase its case temperature, whereas the case temperature of DUT_2 keeps constant at ambient temperature. Then, the current waveforms with case temperature difference (ΔT_c) of 75 °C are shown in Fig. 19. The results show that both static and dynamic currents are unbalanced for paralleled chips with unequal junction temperature. The DUT_1 carries smaller static current than DUT_2. But both turn-ON and turn-OFF currents of DUT_1 are larger than that of DUT_2. It suggests that the unbalanced turn-ON and turn-OFF

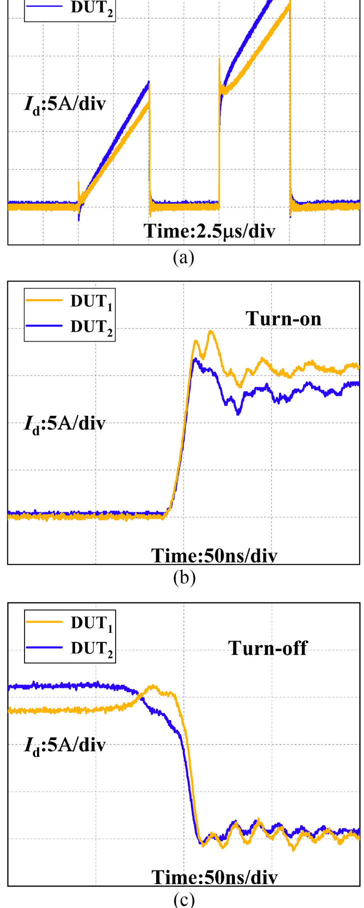

Fig. 19. Current waveforms with case temperature difference of 75 °C. (a) Overall, (b) turn-ON, and (c) turn-OFF current waveforms.

currents caused by junction temperature difference are of the same polarity. Specifically, both turn-ON and turn-OFF currents are larger for the device with higher junction temperature.

Then, the unbalanced static and dynamic currents resulting from unequal junction temperature are further investigated when ΔT_c varies from 15°C to 75°C.

The unbalanced static current at different ΔT_c with load current of 30 A is extracted in Fig. 20. The negative slope of fitting curve indicates that the unbalanced static current is negatively related to ΔT_c. Then, the unbalanced ON-state loss power (ΔP_s) for paralleled DUTs is evaluated as well. The results are presented in Fig. 21. It suggests that the mismatched ON-state loss power is also negatively related to ΔT_c, which is beneficial for current sharing and junction temperature balancing.

In Fig. 22, the unbalanced dynamic current with maximum amplitude at various ΔT_c is extracted when the load current is 30 A. The results indicate that the mismatched turn-ON and turn-OFF currents are positively related to ΔT_c.

The unbalanced switching losses at different ΔT_c with load current of 30 A are also evaluated. The results are shown in Fig. 23. It can be seen that the unbalanced turn-ON and turn-OFF

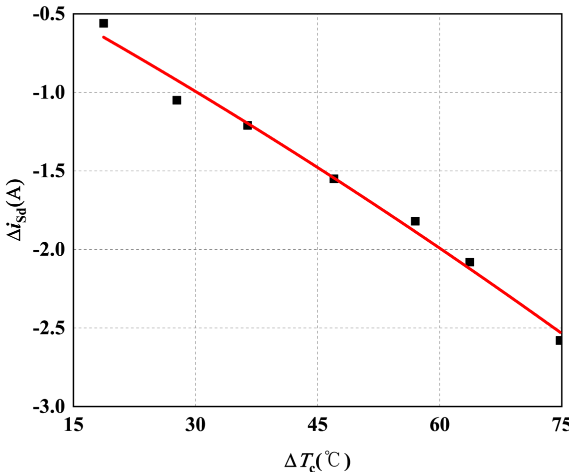

Fig. 20. Unbalanced static current for paralleled DUTs at various ΔT_c with load current of 30 A.

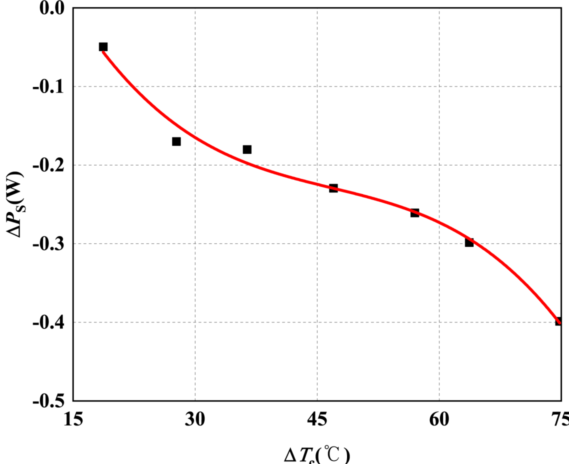

Fig. 21. Unbalanced ON-state loss power for paralleled DUTs at various ΔT_c with load current of 30 A.

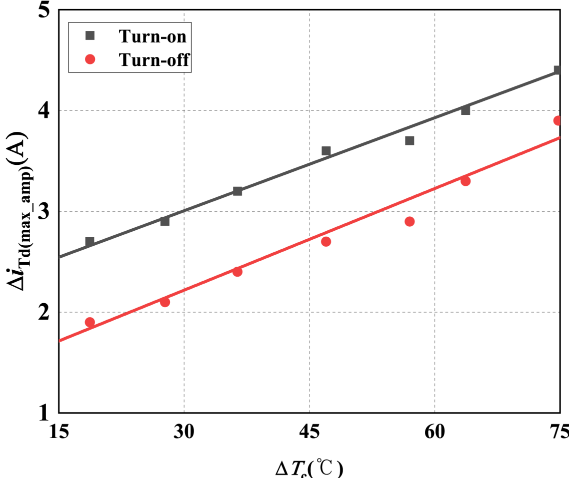

Fig. 22. Unbalanced dynamic current with maximum amplitude at various ΔT_c with load current of 30 A.

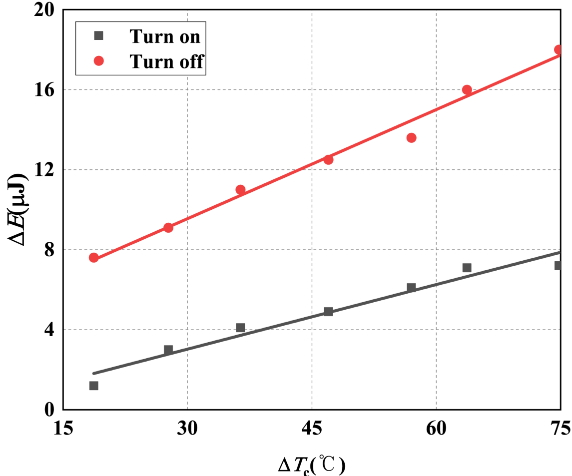

Fig. 23. Unbalanced switching losses at various ΔT_c with load current of 30 A.

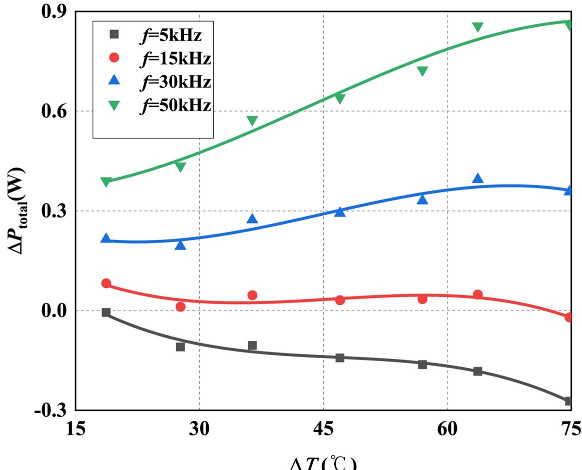

Fig. 24. Total unbalanced loss power versus ΔT_c at various switching frequencies.

losses are positively related to ΔT_c, which is bad for current sharing and junction temperature balancing.

Based on Figs. 21 and 23, the curves of total unbalanced loss power ΔP_{total} versus ΔT_c at various switching frequencies are depicted in Fig. 24 when the duty ration is approximately equal to 1. The results show that the mismatched total loss power is negatively related to ΔT_c when the switching frequnecy is 5 or 15 kHz. However, the unbalanced total loss power turns to be positively related to ΔT_c when the switching frequency increases to 30 or 50 kHz. It suggests that there is a risk of thermal runaway for paralleled SiC MOSFETs at high switching frequency. All the above-mentioned results agree with the analysis in Section III.

V. Conclusion

This article comprehensively investigates the effect of asymmetric layout and unequal junction temperature on static and dynamic currents sharing performance of paralleled SiC MOSFETs with Kelvin-source connection by methods of theoretical analysis and experimental verifications. And the results are summarized as follows.

Both power source and drain parasitic inductance mismatches can cause static current imbalance. The device with larger drain and power source parasitic inductance always carries less static current. And ΔL_d can result in larger unbalanced static current than equal ΔL_s. Dynamic current imbalance mainly results from the mismatches of power source parasitic inductance, whereas the mismatches of other parasitic inductance have little effect on dynamic current sharing. The device with larger power source parasitic inductance always carries less turn-ON but more turn-OFF current than the one with smaller power source parasitic inductance.

Unequal junction temperature can lead to unbalanced static and dynamic current. The unbalanced static current and mismatched conduction losses are negatively related to ΔT_j, whereas the unbalanced dynamic current and mismatched switching losses are positively related to ΔT_j for paralleled SiC MOSFETs. And the positive relationship between ΔT_j and mismatched switching losses could lead to thermal runaway for paralleled SiC MOSFETs at high switching frequency.

Based on the above-mentioned results, there are some guidelines for layout design and application of paralleled SiC MOSFETs with Kelvin-source connection.

To mitigate static and dynamic unbalanced currents resulting from asymmetric layout, it is necessary to suppress both drain and power source parasitic inductance mismatches. In multichip power modules, the power source parasitic inductance mainly results from bonding wires. Thus, it is a good way to mitigate ΔL_s by adjusting bonding wires. The copper traces on direct bonding copper (DBC) substrates are the main causes of drain parasitic inductance. Therefore, the copper traces on DBC should be carefully designed to mitigate the mismatches of drain parasitic inductance.

To avoid the risk of thermal runaway for paralleled SiC MOSFETs at high switching frequency, there are two potential methods. First, the switching losses can be further reduced to make the unbalanced total losses negatively related to ΔT_j at high switching frequency. This can be achieved by employing lower drive resistances or active drive schemes. Second, the thermal coupling among paralleled SiC MOSFET chips can be strengthened to reduce the junction temperature difference. The thermal coupling among dies in multichip power modules is generally stronger than that among paralleled discrete chips. Thus, the switching frequency of multichip power modules can be higher than that of paralleled discrete devices.

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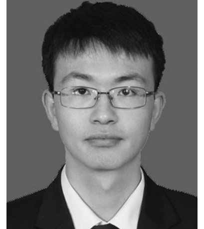

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