Letters

Dynamic Model of the DC Fault Clearing Process of a Hybrid Modular Multilevel Converter Considering Commutations of the Fault Current

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***Abstract*—Hybrid modular multilevel converter that consists of a combination of half-bridge submodules and full-bridge submodules (FBSMs) can block dc fault current. However, in the case of distant bulk power transmission, the large excess energy that stored in the long-distance line will greatly affect the fault clearing time and FBSM capacitor overvoltage. During the fault clearing process, several commutations of the fault current from one arm to another may occur during the fault clearing process. A dynamic model, in which the commutations of the fault current are considered, is proposed to describe the fault clearing process after converter blocking in precise detail. The fault clearing time and FBSM overvoltage can be exactly estimated. The analytical analysis model is verified by the simulation and experimental results.**

***Index Terms*—DC fault clearing, dc short-circuit fault, hybrid modular multilevel converter (MMC), voltage-sourced converter-based high-voltage dc (VSC-HVdc).**

I. Introduction

THE voltage-sourced converter-based high-voltage direct current (HVdc) transmission system has been increasingly applied in recent years [1]–[3]. Modular multilevel converters (MMCs) have become an attractive solution to receiving-end converters in long-distance bulk-power HVdc transmission systems because MMCs are not at risk for commutation failures. For example, an ±800 kV HVdc project in China is set to be commissioned in 2020 to transmit bulk power from the Wudongde Hydropower Station to the Pearl River Delta region through 1500 km overhead lines. As a solution to instability problems in the receiving-end grid resulting from commutation failures, ±800 kV/5000 MW and ±800 kV/3000 MW MMCs are employed in the two receiving-ends.

The half-bridge submodules (HBSMs) based MMC cannot clear the dc fault by itself. Various new submodule (SM) topologies based on clamp circuits, such as clamp-double SMs [4], cross-connected SMs [5], [6], diode clamp SMs [7], and unipolar-voltage full-bridge SMs [8] have been proposed. Full-bridge SM (FBSM) based MMCs not only have an inherent dc fault blocking capability, but also have the unique advantage of utilizing the negative voltage states of FBSMs to extend the ac-side output voltage range and obtain an adjustable dc-link voltage [9]–[11]. A hybrid MMC that consists of a combination of FBSMs and HBSMs uses fewer semiconductor devices and entails a lower power loss [12], [13]. In the Wudongde ±800 kV HVdc project, hybrid MMCs have been chosen as the receiving-end converters to ensure the dc fault clearing capability.

The dc fault handling of hybrid MMCs is usually implemented by the converter blocking approach [12], [13]. However, the impacts of long-distance lines on the dc fault clearing process are still not well explored. The FBSM capacitor overvoltage caused by the large excess energy that stored in the long-distance line is revealed and estimated in [14], where the worst-case FBSM overvoltage is estimated by assuming that the energy needs to be absorbed by two arms. However, because the large line inductance results in a long fault-clearing time, several commutations of the fault current from one arm to another may occur during the fault clearing process. This greatly complicates the dynamics of the fault current clearing process. In order to guide the design of the converter parameters and fault-clearing strategy, a more exact dynamic model of the fault-clearing process is needed.

In this letter, a dynamic model of the fault-clearing process after converter blocking is proposed. In the proposed model, the commutations of the fault current are considered to describe the fault-clearing process in detail. The impacts of line distance and the number of FBSMs in each arm on the fault-clearing time and the FBSM overvoltage are comprehensively analyzed and can be exactly estimated.

II. Dynamic Model of the DC Fault Clearing Process Through Converter Blocking

The total number of SMs in each arm is N. Each arm comprises N_{fb} FBSMs, and the other SMs are HBSMs to provide a dc

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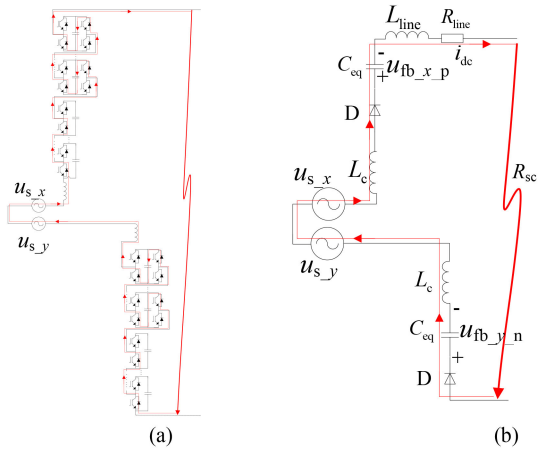

Fig. 1. Fault current loop during dc fault clearance. (a) Fault current loop. (b) Equivalent circuit.

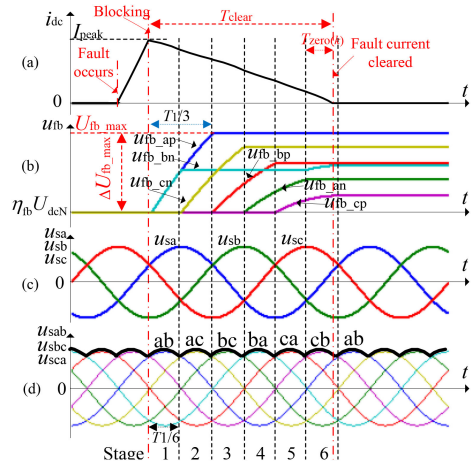

Fig. 2. Diagram of the fault clearing process.

fault blocking capability. The proportion of FBSMs in an arm is defined as follows:

$$\eta_{\rm fb} = \frac{N_{\rm fb}}{N}. \tag{1}$$

Fig. 1(a) shows an example of the fault current loop after converter blocking. The capacitor voltages of the FBSMs generate reverse voltages to block the fault current. In Fig. 1, x and y are used to denote the phase legs of the upper and lower arms in the fault current loop, respectively, where $x = $ a, b, c, $y = $ a, b, c, and $x \neq y$; and $u_{{\rm fb}\_x\_{\rm p}}$ and $u_{{\rm fb}\_y\_{\rm p}}$ denote the sum of all the FBSM capacitor voltages in the upper and lower arms, respectively. The equivalent inductance in this circuit can be expressed as follows:

$$L_{\rm eq} = 2L_c + L_{\rm line} \tag{2}$$

where L_c is the arm inductance and $L_{\rm line}$ is the equivalent lumped inductance of the dc line from the MMC to the short-circuit point. The equivalent resistance can be expressed as follows:

$$R_{\rm eq} = R_{\rm sc} + R_{\rm line} \tag{3}$$

where $R_{\rm sc}$ is the short-circuit resistance and $R_{\rm line}$ is the equivalent lumped resistance of the dc line.

As illustrated in Fig. 1(b), before the current decreases to zero, the equivalent circuit is a second-order resistor–inductor–capacitor (RLC) circuit. The dynamics of this circuit is described as follows:

$$\begin{cases} L_{\rm eq}\frac{di_{\rm dc}(t)}{dt} + R_{\rm eq}i_{\rm dc}(t) \\ \quad = -(u_{{\rm fb}\_x\_{\rm p}}(t) + u_{{\rm fb}\_y\_{\rm n}}(t) - (u_{{\rm s}\_x} - u_{{\rm s}\_y})) \\ C_{\rm eq}\frac{du_{{\rm fb}\_x\_{\rm p}}(t)}{dt} = C_{\rm eq}\frac{du_{{\rm fb}\_y\_{\rm n}}(t)}{dt} = i_{\rm dc}(t) \end{cases} \tag{4}$$

where

$$C_{\rm eq} = \frac{C_{\rm sm}}{N_{\rm fb}} \tag{5}$$

where $C_{\rm sm}$ is the SM capacitance. The diodes in the fault current loop prevent the current flow in the reverse direction. Thus, the dc fault current is cleared as soon as the fault current decreases to zero.

The three-phase ac voltages play a dominant role in determining which arms will be inserted in the fault current loop. A practical way is to assume that the fault current will flow through the upper arm in the phase leg with the highest instantaneous ac voltage and through the lower arm in the phase leg with the lowest instantaneous ac voltage. As illustrated in Fig. 2, at each cross-point of the instantaneous three-phase ac voltages, the fault current commutates from one arm to another. It should be noted that the commutation cannot be completed instantaneously in the real system because of the arm inductance. The commutation overlap angle is determined by the arm inductance, the fault current and the capacitor voltages. However, owing to the complexity of the exact modeling of the commutation overlap effects, the commutation overlap is not considered in Fig. 2. Comparison with simulation results will show that it is still accurate enough to estimate the fault clearing time and the worst-case capacitor overvoltage in engineering practice.

The state variables $u_{{\rm fb}\_x\_{\rm p}}$ and $u_{{\rm fb}\_y\_{\rm n}}$ in (4), which denote the total FBSM capacitor voltages of the inserted arms, are discontinuous when commutation occurs and a new arm is inserted. To solve the discontinuity problem, this article proposes a dynamic model by dividing the dynamic process into several stages according to the cross-points of the three-phase ac voltages. At the beginning of each stage, one of the two arms in the fault current loop is replaced by a newly inserted arm. The summed FBSM capacitor voltage of the newly inserted arm in each stage is denoted by $u_{{\rm fb}(k)}(t)$, where k denotes the stage number. The summed FBSM capacitor voltage of the already inserted arm is $\Delta U_{(k)}$ higher than that of the newly inserted arm because it has been charged by the fault current in the previous stage. In each stage, the voltage increase speeds of the two inserted arms are identical. Therefore, using $u_{{\rm fb}(k)}(t)$ and $i_{{\rm dc}(k)}(t)$ as the state variables, the dynamics in the k-th stage can be expressed as follows:

$$\begin{cases} L_{\rm eq}\frac{di_{{\rm dc}(k)}(t)}{dt} + R_{\rm eq}i_{{\rm dc}(k)}(t) \\ \quad = -\left(2u_{{\rm fb}(k)}(t) + \Delta U_{(k)} - 1.35U_{\rm s}\right) \\ C_{\rm eq}\frac{du_{{\rm fb}(k)}(t)}{dt} = i_{{\rm dc}(k)}(t) \end{cases} \tag{6}$$

where $0 \le t < T_1/6$ and T_1 is the line frequency period. $u_{s\_x} - u_{s\_y}$ in (4) is the three-phase uncontrolled rectifier voltage, as indicated in Fig. 2. It is approximated using the ideal no-load dc voltage of the six-pulse rectifier as expressed as follows:

$$u_{s\_x} - u_{s\_y} \approx \frac{3\sqrt{2}}{\pi} U_s \approx 1.35 U_s \tag{7}$$

where U_s is the root mean square value of the line—line grid voltages.

Equation (6) is the differential equation of a typical second-order RLC circuit. The attenuation coefficient and the attenuated oscillation angular frequency can be calculated as

$$\delta = \frac{R_{eq}/2}{2(L_{eq}/2)} = \frac{R_{eq}}{2L_{eq}} \tag{8}$$

$$\omega_d = \sqrt{\frac{1}{\frac{1}{2}L_{eq}C_{eq}} - \delta^2}. \tag{9}$$

The solution of (6) in the *k*th stage can be expressed as

$$\begin{cases} u_{fb(k)}(t) = Ae^{-\delta t}\sin(\omega_d t + \beta) + \frac{1.35U_s - \Delta U_{(k)}}{2} \\ i_{dc(k)}(t) = -C_{eq}A\delta e^{-\delta t}\sin(\omega_d t + \beta) \\ \qquad\qquad + C_{eq}\omega_d A e^{-\delta t}\cos(\omega_d t + \beta). \end{cases} \tag{10}$$

The coefficients in (10) can be calculated as follows:

$$A = \sqrt{\begin{array}{l}\left(U_{0(k)}(0) - \frac{1.35U_s - \Delta U_{(k)}}{2}\right)^2 \\ + \left(I_{0(k)} + \frac{RC}{2L}\left(U_{0(k)}(0) - \frac{1.35U_s - \Delta U_{(k)}}{2}\right)\right)^2 \frac{L}{2C}\end{array}} \tag{11}$$

$$\beta = \arcsin\left(\frac{U_{0(k)}(0) - \frac{1.35U_s - \Delta U_{(k)}}{2}}{A}\right). \tag{12}$$

The fault current is continuous, and its initial value in each stage is the end value of the previous stage

$$\begin{cases} I_{0(1)}(0) = I_{peak} \\ I_{0(k)}(0) = i_{dc(k-1)}(T_1/6), \text{ when } k > 1. \end{cases} \tag{13}$$

If an arm is inserted into the fault current loop for the first time, the initial value of the summed FBSM capacitor voltage of this arm is its rated value, which is expressed as follows:

$$U_{0(k)}(0) = N_{fb}U_c = \eta_{fb}U_{dcN} \tag{14}$$

where U_c is the rated SM capacitor voltage. The voltage difference, $\Delta U_{(k)}$, in the *k*th stage is the voltage rise of the already inserted arm in the previous stage and can be calculated as follows:

$$\begin{cases} \Delta U_{(1)} = 0 \\ \Delta U_{(k)} = u_{fb(k-1)}\left(\frac{T_1}{6}\right) - N_{fb}U_c, \quad \text{when } 1 < k \le 6. \end{cases} \tag{15}$$

Equations (10)–(15) provide practical time domain solutions for each stage of the fault clearing process. The dc fault current and the FBSM voltage can be solved stage by stage using these equations, and then the fault-clearing time and the FBSM overvoltage can also be estimated.

According to (10), if the next commutation is ignored, the time that the current decreases to zero relative to the beginning of each stage can be calculated as follows:

$$T_{zero(k)} = \frac{\arctan(\omega_d/\delta) - \beta}{\omega_d}. \tag{16}$$

If $T_{zero(k)}$ is less than $T_1/6$ for a certain stage, then the dynamic process can be finished in this stage, and the fault current clearing time can be estimated as follows:

$$T_{clear} = (k-1)\frac{T_1}{6} + \frac{\arctan(\omega_d/\delta) - \beta}{\omega_d}. \tag{17}$$

During the fault current clearing process, the six arms are inserted into the fault current loop alternately with the variations of the three-phase ac voltages, and the FBSM capacitors in the inserted arms are charged alternately, as illustrated in Fig. 2. The duration that each arm can be inserted into the fault current loop is up to two stages, and the fault current decreases stage by stage. Fig. 2 shows an example of the worst scenario of FBSM overvoltage. In this scenario, converter blocking occurs at a cross-point of the three-phase ac voltage. Consequently, one of the arms is charged during the entire first two stages, and the FBSM overvoltage of this arm is the highest. Therefore, if the fault clearing time is less than T_1, the maximum FBSM voltage can be estimated as follows:

$$U_{fb\_max} = \begin{cases} u_{fb(1)}(T_{clear}), & \text{when } T_{clear} \le T_1/6 \\ \Delta U_{(2)} + u_{fb(2)}(T_{clear}), & \text{when } T_1/6 \le T_{clear} < T_1/3 \\ \Delta U_{(2)} + u_{fb(2)}(T_1/6) & \text{when } T_1/3 \le T_{clear} < T_1. \end{cases} \tag{18}$$

If the fault clearing time is greater than T_1, the FBSM capacitor in each arm is charged again when $t > T_1$. In this case, the overvoltage should be accumulated.

III. Simulation

The current ±800 kV MMC-HVdc project in China is used as the case study. Two 400 kV/1250 MW hybrid MMCs are series connected to form an 800 kV/2500 MW MMC, which is used as the pole of a receiving-end converter. For simplicity, the two series-connected 400 kV/1250 MW converters are considered one 800 kV/2500 MW converter in this case study, and the main parameters are given in Table I. The simulation model of the 800 kV/2500 MW hybrid MMC was built and simulated using PSCAD/EMTDC The hybrid MMC was operated in the constant dc link voltage control mode before the fault occurred and was transmitting an active power of 800 MW.

Fig. 3 illustrates the simulated waveforms of the fault clearing process of the blocking approach when the FBSM proportion was $\eta_{fb} = 0.5$. A dc fault occurred at t_0, and the fault location was 1500 km away from the MMC. Then, the fault current increased, and the overcurrent protection was triggered to block the converter when the dc current exceeded the threshold (i.e., 4 kA) at time t_1, as depicted in Fig. 3(a). In accordance with the analysis in Section II-A, the fault current commutated from one arm to another at each cross-point of the instantaneous three-phase ac

TABLE I
KEY PARAMETERS OF THE 800 kV/2500 MW HYBRID MMC

Parameters	Value
Rated capacity (P_N)	2500 MW
Rated DC link voltage (U_{dcN})	800 kV
Rated DC link current (I_{dcN})	3125 A
Rated AC side voltage (U_{acN})	488 kV
Arm inductance (L_c)	80 mH
Number of SMs in one arm (N)	400
Rated DC voltage of SM (U_c)	2000 V
SM capacitance (C_{sm})	18 mF
Distance of the overhead linesc (D)	1500 km
Line inductance	1 mH/ km
Line Resistance	0.004 Ω/ km
Short-circuit Resistance (R_{sc})	0 Ω

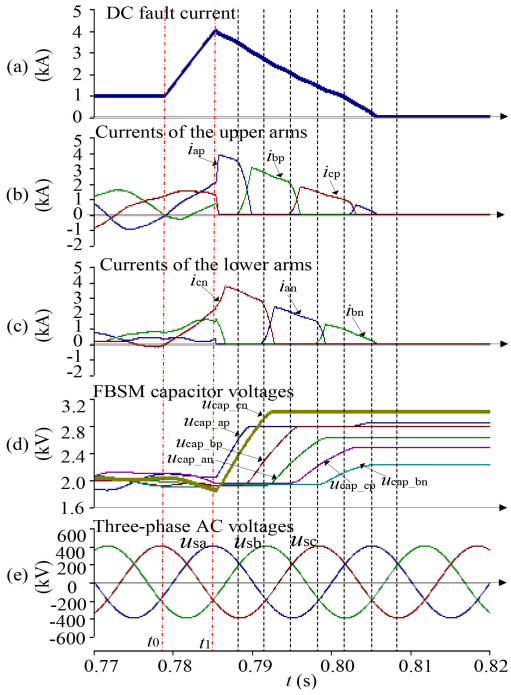

Fig. 3. Simulated waveforms of the fault clearing process when $\eta_{fb} = 0.5$ and $D = 1500$ km.

voltages, as illustrated in Fig. 3(b) and (c). The commutation overlap, which is not considered in the analytical model, can be observed in Fig. 3(b) and (c). As depicted in Fig. 3(d), the FBSM capacitors in the six arms were charged alternately with the commutation from one arm to another. As illustrated in Fig. 3, converter blocking occurred at the cross-point instant of u_{sc} and u_{sb}. Therefore, the FBSM capacitors in the lower arm of phase C were charged during the entire first two stages. Consequently, the FBSMs in this arm had the largest overvoltages during the fault clearing process. The simulated result of the fault clearing process illustrated in Fig. 3 is consistent with the dynamic model presented in Section II.

To verify the proposed model for estimating the fault clearing time and FBSM overvoltages, numerous simulations on various cases of FBSM proportion and fault distance were conducted. The simulated fault clearing times for various FBSM proportions under the fault distance of 1500 km are illustrated in Fig. 4(a). The obtained FBSM overvoltages are illustrated in Fig. 4(b).

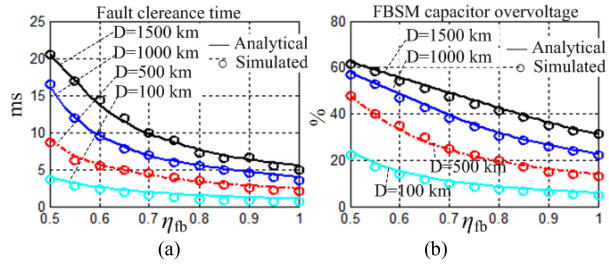

Fig. 4. Curves of fault clearing time and the FBSM capacitor overvoltage of the converter blocking approach.

TABLE II
KEY PARAMETERS OF THE EXPERIMENTAL SYSTEM

Parameters	Value
Rated dc link voltage (U_{dcN})	200 V
Rated dc link current (I_{dcN})	6.7 A
Rated ac side voltage (U_{acN})	100 V
Arm inductance (L_c)	5 mH
Number of SMs in one arm (N)	4
Rated dc voltage of SM (U_c)	50 V
SM capacitance (C_{sm})	1.0 mF
Line inductance	315 mH
Line Resistance	1.2 Ω
Short-circuit Resistance (R_{sc})	0 Ω

The simulation results are consistent with the analytically calculated values using the proposed models. Although the commutation overlap effects are not included in the analytical model, the comparison between the analytically calculated and simulated results shows that the accuracy is acceptable to understand the fault current clearing process and estimate the fault clearing time and the worst-case FBSM capacitor voltages in engineering practice.

IV. EXPERIMENTAL RESULTS

Experiments were performed on an MMC prototype to verify the proposed dynamic model. The main parameters of the experimental system are given in Table II. All the SMs in the experimental prototype are FBSMs. Prior to the occurrence of the dc fault, the MMC prototype operated as a rectifier and the dc output voltage was 180 V. A 30 Ω resistor was connected to the dc-side of the MMC to simulate the normal dc load. Then, the dc lines were short-circuited and the dc inductance between the MMC and the short-circuit point was 315 mH. The overcurrent protection was triggered to block the converter when the dc current exceeded 13.3 A. Because of the limitation of the number of channels of the scope, four FBSM voltages in different arms and the dc fault current were selected to be recorded. As illustrated in Fig. 5, after converter blocking, the dc fault current decreased and the FBSM capacitors in the six arms were charged alternately with the fault current commutated from one arm to another. This phenomenon is fairly correspondent with the theoretical analysis and simulation results. As depicted in Fig. 5, the fault clearing time and FBSM overvoltages are 9.27 ms and 70%, respectively, which are all correspondent with the theoretically calculated results.

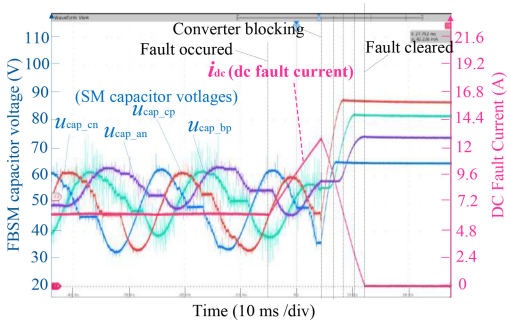

Fig. 5. Experimental waveforms of the fault clearing process.

V. Conclusion

In long-distance overhead line applications, the impact of line inductance on fault clearing time and FBSM overvoltage must be considered. In this letter, a detailed dynamic model of the dc fault current clearing process of hybrid MMCs after converter blocking is proposed. The fault clearing process can be described in detail, and the fault clearing time and the FBSM overvoltage can be estimated accurately because the commutations of the fault current are considered in the proposed model. The proposed dynamic model for the fault clearing process is verified by the simulation and experimental results. The impacts of line distance and number of FBSMs on fault clearing time and FBSM capacitor overvoltage are also comprehensively analyzed. The proposed dynamic model can be used to guide the design of the converter parameters and fault clearing strategy for minimizing the fault clearing time and capacitor overvoltages.

In order to provide a simple and practical way, the commutation overlap effects are not included in the presented model. Although the dynamic model is accurate enough to estimate the fault clearing time and the FBSM capacitor voltage in engineering practice, the accuracy can be further improved by exactly modeling the commutation overlap effects in future research.

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