Common Mode Noise Reduction of Three-Level Active Neutral Point Clamped Inverters With Uncertain Parasitic Capacitance of Photovoltaic Panels

Jianing Wang, *Member, IEEE*, Xiaohui Liu, *Student Member, IEEE*, Yuanwu Xun, *Student Member, IEEE*, and Shaolin Yu, *Student Member, IEEE*

***Abstract*—SiC devices can upgrade the inverter performance to a new level by its potentially more than ten times higher switching speed compared to its Si counterpart. However, the high switching frequency and dv/dt, di/dt worsen the electromagnetic interference. Reduction of the common mode (CM) noise of the non-isolated photovoltaic (PV) inverters is addressed by many researchers through adding filters or balancing the circuit. However, most methods rely on the certainty of the parasitics in the system in advance. It is usually not practical for a PV inverter because the parasitic capacitance of PV panels that are to be installed in plants varies from case to case and further can be seriously affected by the damp environment. This article proposes a practical way to reduce the CM noise of the three-level active neutral point clamped (ANPC) inverters with uncertain parasitic capacitance of PV panels. First, the CM model of ANPC inverters with all parasitic capacitances is established. Next, most existing hardware-based reduction methods of the CM noise are summarized based on a unified mathematical model and further compared with each other. After the comparison, a practical method is proposed to reduce the CM noise of the ANPC inverter with uncertain parasitic capacitances, which just adds little volume and cost to the whole system. Finally, the simulation and experiments are conducted to validate the proposed method.**

***Index Terms*—Active neutral point clamped (ANPC) topology, common mode (CM), electromagnetic interference (EMI), EMI elimination, uncertain parasitic capacitance.**

I. Introduction

SIC devices can upgrade the performance of medium and large power inverters to a new level by its potentially more than ten times higher switching speed compared to its Si counterpart [1], [2]. The three-level (3L) active neutral point clamped (ANPC) inverters with composition of Si and SiC devices are becoming popular for transformerless photovoltaic (PV) inverters around hundreds kW for better efficiency and comparatively low system cost [3]–[7]. Fig. 1 shows the system topology, where many PV panels are connected to the dc side, and the ac side is tied to the grid. Due to parasitic capacitances in the system, there is common mode (CM) noise current flowing in the system. The SiC-based inverters are intended to have much higher switching frequency than traditional 10–20 kHz in medium power applications. The increased switching frequency as well as dv/dt, di/dt of SiC devices can greatly increase the magnitude of the CM current in the interested 150 kHz–30 MHz range, especially when the switching frequency increases beyond 150 kHz [8]–[10]. The high frequency and speed of the SiC device increases the possibility to break the equipment electromagnetic interference (EMI) emission limit specified in standard, such as Chinese government standards NB/T 32004-2018, and requires better filtering techniques.

To evaluate the CM noise of the 3L-ANPC inverter with parasitic capacitances, the CM model of the system should be first built. Usually, the approaches can be divided into two types, which are time-domain method and frequency-domain method [11].

For the time-domain method, the researchers conduct behavioral calculation of the switching transient in simulation software such as Saber and Pspice and obtain the time-domain signals and further the noise spectrum through Fourier transformation in the simulation [12]–[14]. This method is usually time consuming and cannot clearly address the dependence of the CM noise current on the circuit element [15].

The frequency-domain method uses voltage or current sources replacing switching devices according to the substitution theorem to convert the non-linear power electronic circuit into a linear one [16]. If the accurate CM noise current needs to be calculated based on the model, the accurate source should be obtained, which can be simply triangular waveforms, trapezoidal waveforms, or more accurate waveforms by double Fourier analysis [15]–[18]. However, in many cases, the goal of building the model is for the reduction of CM noise current rather than the accurate value. Thus, the waveforms of the sources are not

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The authors are with the College of Electrical Engineering and Automation, Hefei University of Technology, Hefei 230009, China (e-mail: jianingwang@hfut.edu.cn; 497676042@qq.com; 1402900164@qq.com; hajcysl@163.com).

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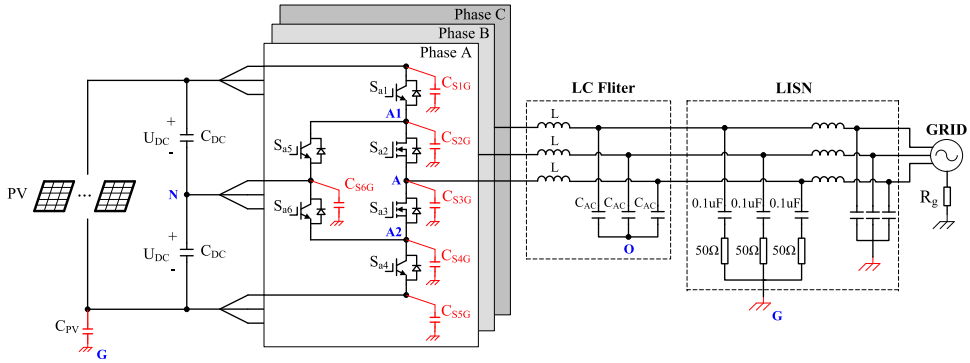


Fig. 1. Three-phase (3P) 3L-ANPC PV inverter with line impedance stabilization network (LISN).

that important. The authors in [19]–[22] study the CM model of single-phase two-level (2L) inverters and the corresponding modulation strategies to reduce the CM noise. The authors in [23] and [24] extend the modeling to three-phase (3P) 2L inverters. The modeling of 3L inverter becomes more difficult because there are three voltage-varying nodes, while 2L inverter only has one. How to combine multiple noise sources in each phase into one is a problem to be solved when the phase relation of these sources is uncertain. Zhang *et al*. [25] exhibit a comprehensive analysis and modeling for CM noise for three-level neutral point clamped inverters, which contains three high frequency noise sources. The simplification of the models cannot be directly used for 3L-ANPC topology that contains both high-frequency and low-frequency noises as well as different modulation methods. Thus, it is necessary and meaningful to develop a comprehensive and accurate model for 3L-ANPC topology.

After the modeling, the reduction of the CM noise is a matter of concern. The approaches can be grouped into two types, which are based on modification of software that usually includes improvement of modulation and control methods and modification of hardware that usually refers to improvement of topologies and adding EMI filters. The authors in [26]–[32] propose a method to restrain CM voltage by choosing appropriate modulation vectors, but it needs to achieve this goal by sacrificing the total harmonic distortion and other performance of inverters. The authors in [33] and [34] present an elimination method by controlling modulation signals based on the measurement and feedback of the CM current, but extra sensors are added. Some researchers reduce the leakage current and CM noise by adding additional bridge arms to offset the CM voltage [35], [36] or using soft-switching method [37] to reduce the dv/dt, but this method is seldom used in industry due to the extra addition of many components. The authors in [28], [38], and [39] parallel two inverters and make their CM voltage opposite by appropriate modulation strategy so that the value remains unchanged. But this method is not suitable for the case of only one inverter. The CM current can also be reduced by an integrated busbar filter [40], [41], but the reduction effect is limited due to the difficulty of realizing a large inductance with appropriate power. Chen *et al*. [42] propose a low-pass filter at the output side and connect the filter back to the neutral point of the dc side to reduce the CM current. But this method can only reduce the leakage current at low frequency but has limited effect on reducing CM noise at high frequency. Based on this topology, an inductor is further added on the feedback loop to realize an impedance balance for better reduction of CM noise [25], [43]. This is an excellent technical method without adding much volume and cost to the system but not that practical in the real industry environment because it strongly depends on the foreseeing of all the parasitics in the circuit. However, due to uncertainty of the PV plant as well as the climate, the parasitic capacitance can vary in a large range due to the number of the panels or the damp environment [44], [45]. Thus, the designed balance can be broken in reality, which leads to failure of the elimination of the CM current.

To overcome limits of the existing approaches, this article first presents the modeling of the 3P-3L-ANPC inverters for the CM current by the frequency-domain method. Then, most existing hardware-based reduction methods are summarized based on a unified mathematical way and further compared with each other. After the comparison, a practical method is further proposed to reduce the CM noise of the ANPC inverter with uncertain parasitic capacitances, which just adds little volume and cost to the whole system. Finally, the simulation and experiments are conducted to validate the proposed method.

II. Modeling of the 3P-3L-ANPC Inverters for the CM Current

First, the single-phase EMI model of 3P-3L-ANPC inverter will be established. As shown in Fig. 2(a), $S_{a2}-S_{a3}$ are SiC switches for high-frequency operation and the others are Si switches for low-frequency operation. The parasitic capacitances between the switches and the ground or heat sink that are usually grounded are shown in the figure, noted as C_{S1G}–C_{S6G}. The capacitance C_{dc} represents dc capacitors with capacitance usually more than 1 mF. The parasitic inductance of the capacitor C_{dc} can be very low by paralleling many thin film capacitors with low ESL in practical design, so it can be ignored. Besides, the parasitic inductance of connections between the dc capacitor and the switches can also be very low by using laminated busbar.

Second, the voltage sources are used to replace the non-linear switches according to the substitution theorem. The C_{dc} can be regarded as shorted in high-frequency analysis, as shown in Fig. 2(b). The voltage sources S_{a1} and S_{a5} can be simplified as

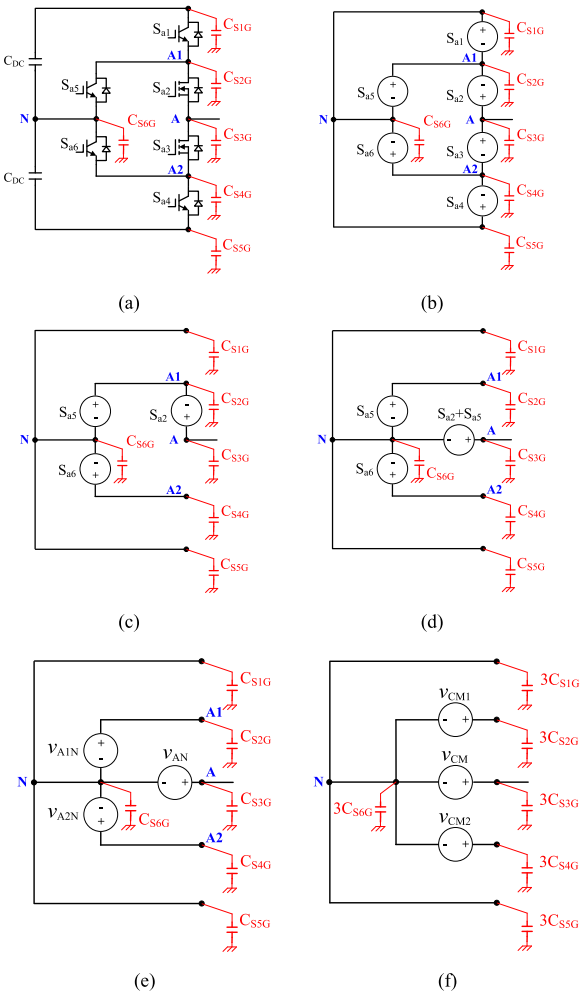


Fig. 2. 3L-ANPC modeling for CM noise. (a) Topology of phase A. (b) Replace the switches with voltage sources. (c) DC capacitors are regarded as short circuit at high frequency and parallel voltage source are merged. (d) Equivalent transformation by keeping the voltage of the nodes A, A1, and N unchanged. (e) Use v_{AN}, v_{A1N}, and v_{A2N} instead of $\mathrm{S_{a2}}+\mathrm{S_{a5}}$, $\mathrm{S_{a5}}$, and $\mathrm{S_{a6}}$. (f) Three-phase CM noise model.

one because of their parallel connections. And the same can be done for $\mathrm{S_{a4}}$ and $\mathrm{S_{a6}}$.

By eliminating $\mathrm{S_{a1}}$ and $\mathrm{S_{a4}}$, the remaining sources, $\mathrm{S_{a2}}$, $\mathrm{S_{a3}}$, $\mathrm{Sa_5}$, and $\mathrm{Sa_6}$, form a close loop, in which any of the sources can be regarded as parallel to the rest of the circuit. Thus, it can be further simplified as shown in Fig. 2(c). It can be further changed equivalent to Fig. 2(d) and (e), by keeping the voltage of the nodes A, A1, and N unchanged. Finally, the model of single phase in Fig. 2(e) can be extended to Fig. 2(f), where

$$v_{\mathrm{CM}} = \frac{v_{AN} + v_{BN} + v_{CN}}{3} \tag{1}$$

$$v_{\mathrm{CM1}} = \frac{v_{A1N} + v_{B1N} + v_{C1N}}{3} \tag{2}$$

$$v_{\mathrm{CM2}} = \frac{v_{A2N} + v_{B2N} + v_{C2N}}{3} \tag{3}$$

After modeling the switches, the impedance network at both dc and ac sides shown in Fig. 1 needs to be modeled. The dc

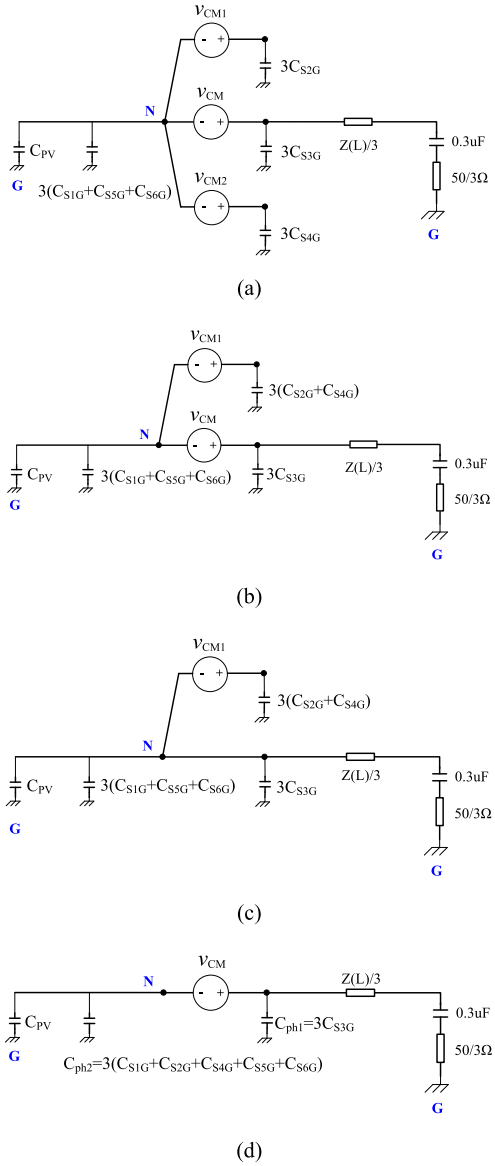


Fig. 3. Simplification of the 3P-3L-ANPC model for CM noise. (a) Three-phase CM noise model. (b) Combine V_{CM1} and V_{CM2}. (c) Separate response analysis of V_{CM1}. (d) The final CM noise model.

side only contains the parasitic capacitance of PV panels that can be simply added to the node N, as shown in Fig. 3(a). For the ac side, the impedance of the inductor in the line impedance stabilization network (LISN) is large enough at high frequency to effectively block the CM noise passing to the grid. Thus, only the branch of 0.1 uF capacitor and 50 Ω resistor needs to be considered in modeling. For the three phases at the ac side, the branches are in parallel mode in the CM noise model, which is also the same for the inductor L. There is no CM current flowing through the capacitors C_{ac}, so they can be ignored. The 3P CM noise model is subsequently shown in Fig. 3(a).

There are three sources in Fig. 3(a) based on the specific modulation strategy of ANPC topology. Table I shows the relationship between the switching sequences of phase A and

TABLE I
RELATION BETWEEN PHASE A SWITCHING SEQUENCE AND NOISE SOURCES

		S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	v_{A1N}	v_{A2N}	v_{AN}
Positive	P	ON	ON	OFF	OFF	OFF	ON	$U_{\rm dc}$	0	$U_{\rm dc}$
	O	ON	OFF	ON	OFF	OFF	ON	$U_{\rm dc}$	0	0
Negative	O	OFF	ON	OFF	ON	ON	OFF	0	$-U_{\rm dc}$	0
	N	OFF	OFF	ON	ON	ON	OFF	0	$-U_{\rm dc}$	$-U_{\rm dc}$

the voltage of the three noise sources. It can be found that the variations of $v_{\rm A1N}$ and $v_{\rm A2N}$ are the same with a dc bias in between, which can be expressed as follows:

$$v_{A1N} - v_{A2N} = U_{\rm dc} \tag{4}$$

According to the symmetry of three phases, it can be obtained

$$v_{B1N} - v_{B2N} = U_{\rm dc} \tag{5}$$

$$v_{C1N} - v_{C2N} = U_{\rm dc} \tag{6}$$

By substituting (4)–(6) in (2) and (3), it is found as

$$v_{CM1} - v_{CM2} = U_{\rm dc} \tag{7}$$

The dc component does not contribute to the CM current, so $v_{\rm CM1}$ can be regarded as the same as $v_{\rm CM2}$ in the CM model, and they can be merged into one as shown in Fig. 3(b). The current response in the linear circuit in Fig. 3(b) can be analyzed as the two noise sources separately excite on the circuit. Thus, Fig. 3(c) first shows the circuit for the noise analysis excited only by the noise source $v_{\rm CM1}$, of which the expression is shown in (2). A common modulation strategy of ANPC circuit is to operate the switches S_{a2} and S_{a3} at high frequency to utilize the high speed advantage of SiC MOSFET and switch the Si insulated gate bipolar transistor (IGBT) at 50 Hz to lower the switching losses. Thus, $V_{\rm A1N}$ is a square wave with a frequency of 50 Hz, and amplitudes of $U_{\rm dc}$, $V_{\rm B1N}$, and $V_{\rm C1N}$ have the same amplitude as $V_{\rm A1N}$ with 120° phase shift between each other. Consequently, the $v_{\rm CM1}$ for three phases is a waveform with an amplitude of $U_{\rm dc}/3$ and a frequency of 150 Hz. Similarly, the amplitude of $v_{\rm CM}$ is $U_{\rm dc}/3$, but its frequency is three times the switching frequency of S_{a2} and S_{a3}, which is 40 kHz in our design. Therefore, in the interested frequency range for CM noise, which is from 150 kHz to 30 MHz, the amplitudes of $v_{\rm CM1}$ are much smaller than that of $v_{\rm CM}$ after Fourier transform. In addition, the response circuit of $v_{\rm CM1}$ shown in Fig. 3(c) includes parasitic capacitance $3(C_{\rm S2G} + C_{\rm S4G})$ of pF level and is in series with the rest of the network. Thus, the total impedance of $v_{\rm CM1}$ response circuit is much larger than that of $v_{\rm CM}$ as shown in Fig. 3(d). Considering the above two points, the response of $v_{\rm CM1}$ in the circuit is much smaller than that of $v_{\rm CM}$. Thus, the source $v_{\rm CM1}$ can be ignored in the model, and the final CM model is obtained as shown in Fig. 3(d). For the convenience of the following expressions, $C_{\rm ph1}$ is used to represent $3C_{\rm S3G}$, and $C_{\rm ph2}$ is used to replace the result of $3(C_{\rm S1G} + C_{\rm S2G} + C_{\rm S4G} + C_{\rm S5G} + C_{\rm S6G})$.

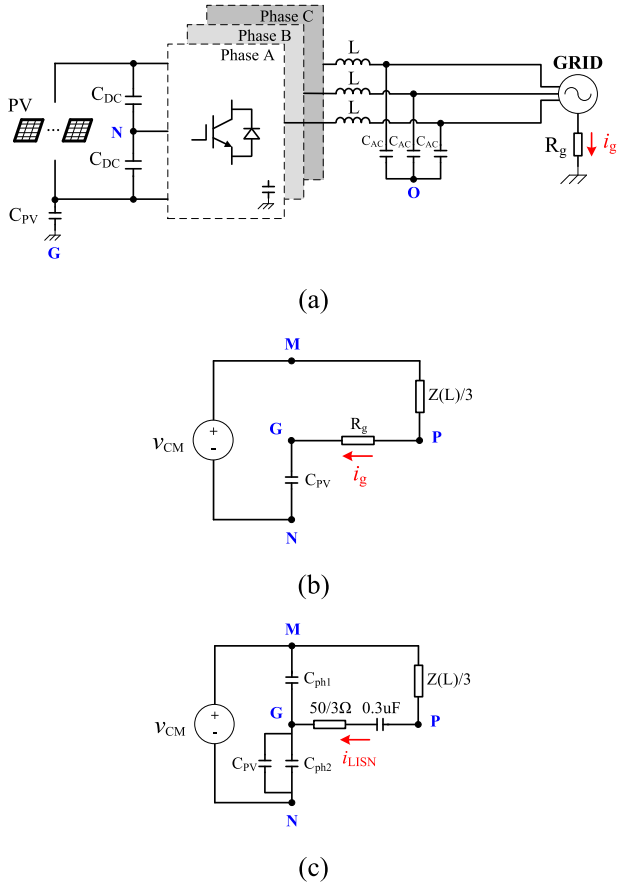


Fig. 4. Comparison between leakage current and CM EMI noise. (a) Schematic for analysis of leakage current. (b) The leakage current model. (c) The CM noise model.

III. REVIEW AND COMPARISON OF HARDWARE-BASED REDUCTION METHODS FOR CM NOISE

In this section, a comprehensive review of the major CM noise reduction methods based on modification of hardware is explored. And then, these methods are compared from five aspects: CM noise reduction performance, leakage current level, cost, volume, and sensitivity to $C_{\rm PV}$.

Before the review, the difference between CM EMI noise and leakage current needs to be clarified, which sometimes are confused in papers.

The leakage current usually concerns the current flowing through the ground, of which the interested harmonic frequency is below 300 kHz [42]. When leakage current is of interest, the LISN is usually not added in the system, as shown in Fig. 4(a), where $R_{\rm g}$ signifies the ground connection resistor. The corresponding leakage current model contains the relative large parasitic capacitance $C_{\rm pv}$, and the small structural parasitics can be ignored due to their large impedance below 300 kHz to simplify the analysis, as shown in Fig. 4(b). However, the CM EMI noise is clearly defined as the current flowing through the LISN and the tested spectrum of that is from 150 kHz to 30 MHz. The load and the $R_{\rm g}$ are disconnected for the high-frequency noise; thus, they are not included in the model shown in Fig. 4(c). Besides, the small parasitics play a role in the noise at this

TABLE II
THE PARASITIC CAPACITANCE OF THE MODULE VINCOTECH ANPC-SPILT-1500V-SG-01T FOR SINGLE PHASE

Symbol	Value
Cs_{1G}	625.66 pF
C_{S2G}	766.8 pF
C_{S3G}	763.29 pF
C_{S4G}	763.85 pF
C_{S5G}	658.94 pF
C_{S6G}	756.25 pF

TABLE III
KEY PARAMETERS OF THE 3P-3L-ANPC INVERTER

$2U_{dc}$	1500 V	L	330 uH
f	40 kHz	C_{AC}	10 uF
R_g	2 Ω	C_{PV}	140 nF/20 uF

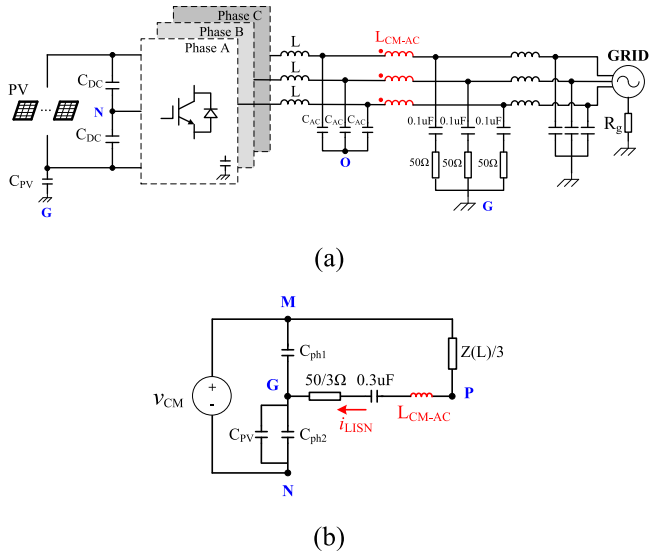


Fig. 5. $L_{\text{CM-ac}}$ is added at the ac side to reduce the CM current. (a) The schematic. (b) The CM noise model.

frequency range. Fig. 4(c) shows the model that differs from Fig. 4(b) on the structural parasitic capacitance C_{ph1} and C_{ph2} and the targeted current i_{LISN}. The point P in the figure is where LISN is connected to ac side and M is the equivalent point of 3P outputs.

In the following, four types of existing hardware-based reduction methods of CM noise are compared based on a unified mathematical model. To quantitatively clarify their pros and cons, a case study is conducted, which is the real setup of 3P-ANPC inverter with 1500 V dc input and 140 kW output power. The hybrid Si and SiC modules ANPC-SPLIT-1500V-SG-01T used are customized from Vincotech whose capacitances between switch and ground/heat sink are measured by an impedance analyzer Wayne Kerr 6500B and shown in Table II. Based on these measurements, C_{ph1} and C_{ph2} are calculated as 2289.9 and 10 714.5 pF, respectively.

The L and C_{ac} of the LC filter in the setup are designed as 330 uH and 10 uF, respectively, to effectively reduce the differential mode noise. According to [44], the parasitic capacitance of PV panels varies from 1 to 90 nF/kW in normal environment and can reach 138 nF/kW in damp environment, so two typical points are chosen for the C_{PV} for the dry and damp environment as 140 nF and 20 uF in the case of 140-kW PV panels. The minimum value of R_{g} recommended by the IEEE standards is 2 Ω [42]. The switching frequency of the inverter is set to 40 kHz. The key parameters of the 3P-3L-ANPC inverter are given in Table III.

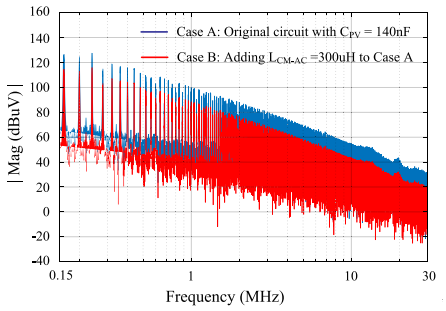
A. Adding $L_{\text{CM-ac}}$ to AC Side

To reduce the CM current, the most common way is to add a CM inductor at the ac side. The schematic and corresponding CM model are shown in Fig. 5. The circuit of one bridge in Fig. 1 is simplified as a switch symbol here. It can be clearly seen from Fig. 5(b) that the CM inductor $L_{\text{CM-ac}}$ significantly increases the impedance of PG branch which leads to an effective reduction of CM current. In order to further increase noise attenuation, Y capacitors can be added to form an LC filter.

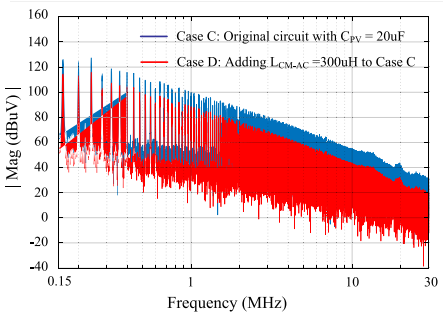
To verify this method, a 300-uH CM inductor that is similar to the DM inductor, which is commonly seen in real product, is added to the ac side in the case study. The simulation results are shown in Fig. 6. It can be seen from Fig. 6(a) and (b) that the different C_{PV} has little effect on the reduction effect of this method. The reason is that the impedance of the branch PN is dominated by C_{PV} due to its ten times larger capacitance of C_{ph2}, and it becomes quite small compared to that of other branches in the frequency range 150 kHz–30 MHz, with little influence on the LISN current.

Due to the large impedance of C_{ph1}, the branch MG can be regarded as open. Thus, the model is left with the branch MPG connected in series with the branch GN. By simple calculation, the resonant frequency is much smaller than 150 kHz. Thus, for the 150 kHz–30 MHz range, the inductance $L_{\text{CM-ac}}$ and L dominate the CM current. Thus, to sufficiently reduce the CM noise, large inductance needs to be added, which is usually at mH level. As shown in Fig. 6, 300 uH is not good enough to reduce the CM noise at a low frequency range and a much larger CM inductor should be added. For example, if the magnitude of the current noise needs to be decreased to 80 dBuV at 150 kHz, the current needs to be decreased for another 35 dBuV which means the $L_{\text{CM-ac}}$ needs increase at least more than 56 times larger. By adding large CM inductor at the ac side, the root mean square (RMS) value of leakage current can also be effectively reduced for the two cases by the similar principle, which is shown in Fig. 6(c).

This method is easy to implement and the effect of noise reduction is obvious. The change of C_{PV} has little effect on it. But its drawbacks are obvious as well. First, in order to achieve a good reduction effect in the low-frequency band, the value of $L_{\text{CM-ac}}$ can be very large such as tens or hundreds of mH level. Second, $L_{\text{CM-ac}}$ is connected in series in the main circuit,



(a)



(b)

	Case A	Case B	Case C	Case D
i_g (RMS)	44.56A	41.3mA	4.53A	240.2mA

(c)

Fig. 6. Spectra of CM noise and RMS value of leakage current. (a) The spectra of Case A: Original circuit with $C_{PV} = 140$ nF and Case B: Adding $L_{CM\text{-}ac} = 300$ uH to Case A. (b) The spectra of Case C: Original circuit with $C_{PV} = 20$ uF and Case D: adding $L_{CM\text{-}ac} = 300$ uH to Case C. (c) The RMS value of leakage current of Case A, Case B, Case C, and Case D.

and the wire of the inductor has to handle the rated current of the main power. In addition, the 3P CM inductor needs three thick windings, which takes a relatively large window area of the inductor. For example, considering commonly used ring magnetic cores, 300 uH with 120-A inductor $L_{CM\text{-}ac}$ needs a core with 85-mm outer diameter and 50-mm thickness. The core of a 16.8-mH inductor can be estimated by 56 previous cores in parallel. And six strands of copper wires with 2-mm diameter each needs to be paralleled and three turns are required for the three phases. In total, the volume of the inductor can be calculated as 16 419 cm^3 and the cost is Chinese Yuan (CNY) 10 000. The volume and cost are too large for a 140-kW inverter; thus, in reality, this large CM inductor is seldom used.

B. Connecting the Middle Point of the DM Capacitor O Back to the Neutral Point N

In order to overcome the above drawbacks, Chen *et al.* [42] propose to connect the middle point of the DM capacitance O back to the middle point of the dc side N, as shown in Fig. 7(a). By doing so, the previous CM noise model can evolve to a bridge with an added branch between P and N, as shown in Fig. 7(b). In this model, the new added capacitance is $3C_{ac}$ because the three capacitances are in parallel. Based on this

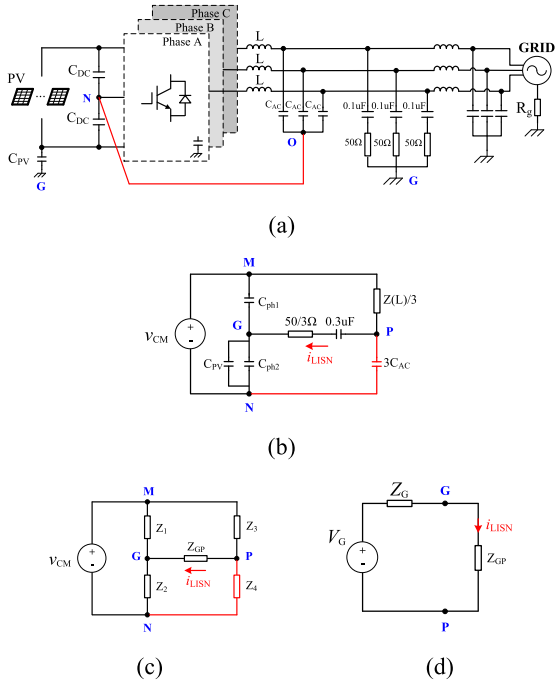


Fig. 7. Connect the middle point of the DM capacitor O back to the neutral point N. (a) The schematic. (b) The CM noise model. (c) The unified model. (d) The Thevenin circuit of Fig. 7(c).

idea, different reduction methods can be proposed [25], [43], which can be summarized as making change of each branch impedance to finally balance the circuit to equal the voltage of node G to node P. Thus, a unified model can be derived as shown in Fig. 7(c), in which the branch is represented just by an impedance. Based on this model, a unified mathematic way can be derived to explain most different existing reduction ways. The current i_{LISN} can be derived based on the further simplified Thevenin circuit of Fig. 7(d). The model shown in Fig. 7(c) and (d) can also be used for the calculation of leakage current when Z_{GP} signifies R_g.

In the simplified Thevenin circuit, the expression of V_G is

$$V_G = (k_1 - k_2) \times v_{CM} \tag{8}$$

where the k_1 and k_2 are expressed as follows:

$$k_1 = \frac{Z_2}{Z_1 + Z_2} \tag{9}$$

$$k_2 = \frac{Z_4}{Z_3 + Z_4} \tag{10}$$

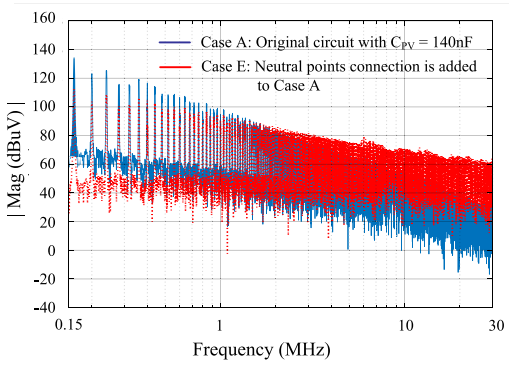
The expression of Z_G is

$$Z_G = \frac{Z_1 Z_2}{Z_1 + Z_2} + \frac{Z_3 Z_4}{Z_3 + Z_4} \tag{11}$$

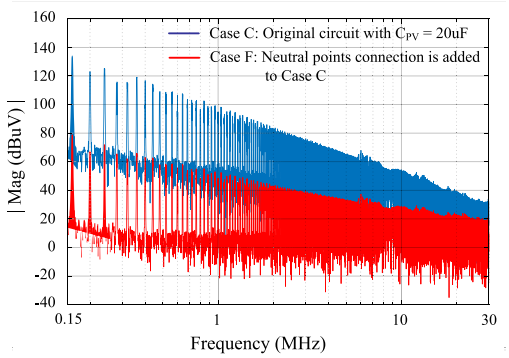
According to (8) and (11), it is easy to get the expression of i_{LISN} in Fig. 7(d):

$$i_{LISN} = \frac{k_1 - k_2}{Z_G + Z_{GP}} \times v_{CM} \tag{12}$$

From (12), it is obvious that if k_1 is equal to k_2, the equivalent source V_G is 0 and the corresponding current i_{LISN} will be 0,



(a)



(b)

	Case E	Case F
i_g (RMS)	356.4mA	702.2mA

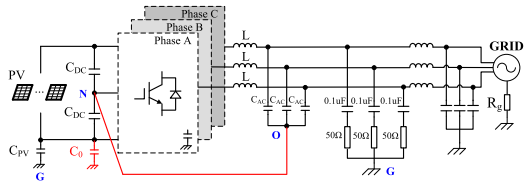
(c)

Fig. 8. Spectra of CM noise and RMS value of leakage current. (a) The spectra of Case A and Case E: Neutral points are connected to Case A. (b) The spectra of Case C and Case F: Neutral points are connected to Case C. (c) The RMS value of leakage current of Case E and Case F.

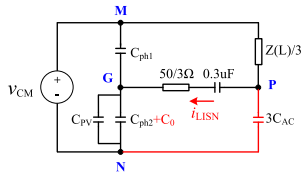
which means the bridge circuit is balanced and the CM noise can be effectively reduced. Different bridge balance methods are all based on this principle.

In the case of neutral connection, C_{PV} is usually much larger than C_{ph1} and C_{ph2}, so the value of k_1 is very small. It changes from 0.0152 to 0.000114 when C_{PV} changes from 140 nF to 20 uF. By connecting the point O to N as shown in Fig. 7(b), Z_4 represents the impedance of $3C_{\mathrm{ac}}$ that is usually above 10 uF in practice. At 150 kHz, the impedance of $3C_{\mathrm{ac}}$ is 0.036 Ω and that of $L/3$ is 103.6 Ω. Consequently, k_2 is 3.5×10^{-4} that can be simply regarded as 0. Thus, the difference of k_1 and k_2 by connecting the neutral points are much smaller than that in the original case shown in Fig. 4(c), where $k_1 - k_2$ is close to -1. Resultantly, the equivalent noise source V_{G} is much decreased leading to a good reduction of the current i_{LISN}.

However, on the other hand, the branch PN reduces the impedance of Z_{G} according to (11). Therefore, in order to obtain a good reduction effect, $C_{\mathrm{PV}} + C_{\mathrm{ph2}}$ must be much larger than C_{ph1} to make k_1 as close to zero as possible to offset the negative effect of impedance reduction caused by PN branch. Fig. 8(a) and (b) proves the analysis well. The k_1 in the case with C_{pv} of



(a)



(b)

Fig. 9. Add the C_0 to dc bus. (a) The schematic. (b) The CM noise model.

140 nF is larger than that with C_{pv} of 20 uF; thus, the latter case has better reduction effect than the former. It can be seen that the CM noise reduction of neutral connection is not good if C_{pv} is small and greatly affected by the change of C_{PV}; so this method needs further improvement to apply to the practical application.

The RMS value of leakage current is shown in Fig. 8(c), which is much smaller than the original Cases A and C. By ignoring the parasitic capacitance in the analysis of leakage current, the $3C_{\mathrm{ac}}$ can be seen as providing a very low impedance in parallel with the R_{g}, which significantly reduces the leakage current. Moreover, this method does not increase any volume and cost to the system.

C. *Adding C_0 to DC Bus to Reduce k_1*

Based on the above analysis, decrease of the impedance Z_2 leads to better reduction effect of CM noise in the topology shown in method B. A commonly used way in the industry is to simply add capacitance C_0 to the dc bus shown in Fig. 9(a). By simply modeling, the capacitance is in parallel with C_{pv}, as shown in the Fig. 9(b).

Because the impedance Z_2 is much smaller than Z_1, thus, k_1 as shown in (9) is approximately equal to $C_{\mathrm{ph1}}/(C_{\mathrm{ph2}} + C_{\mathrm{PV}} + C_0)$. Thus, as C_0 becomes larger, k_1 becomes smaller and closer to k_2 that is almost 0, as analyzed before. Correspondingly, the reduction effect becomes better. Based on Fig. 8, it can be seen that when the total capacitance increases to 20 uF, the current noise can be reduced to 80 dBuV at 150 kHz. Thus, in real design, the dc bus capacitance C_0 should be designed as around 20 uF for dry environment when C_{pv} is only 140 nF. In the damp environment when C_{pv} increases to 20 uF, the total capacitance of branch GN increases to 40 uF, and the system can have even better reduction effect. The RMS value of the leakage current is around 702.2 mA when C_0 is 20 uF and C_{pv} is 140 nF. The Z_{G} in (11) is very small in this case when comparing to Z_{GP} that signifies R_{g}. Thus, further increase of the total capacitance of the branch GN has little influence on the leakage current.

However, in real industry design, the capacitance C_0 cannot be too large. It will cause low-frequency grounding current through

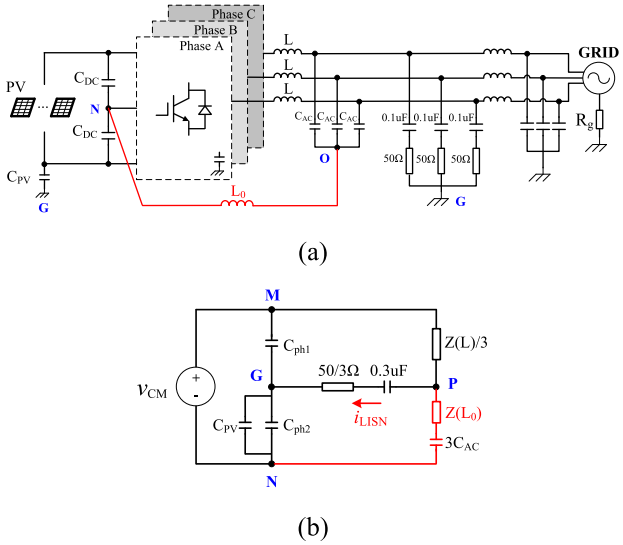


Fig. 10. Add the L_0 between O and N. (a) The schematic. (b) The CM noise model.

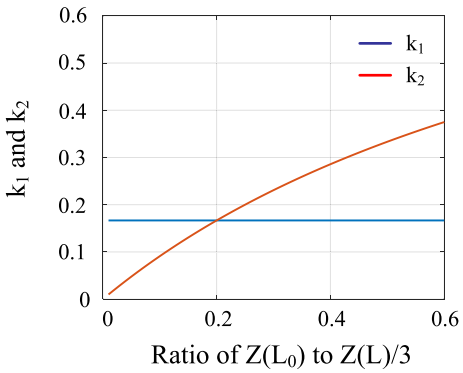
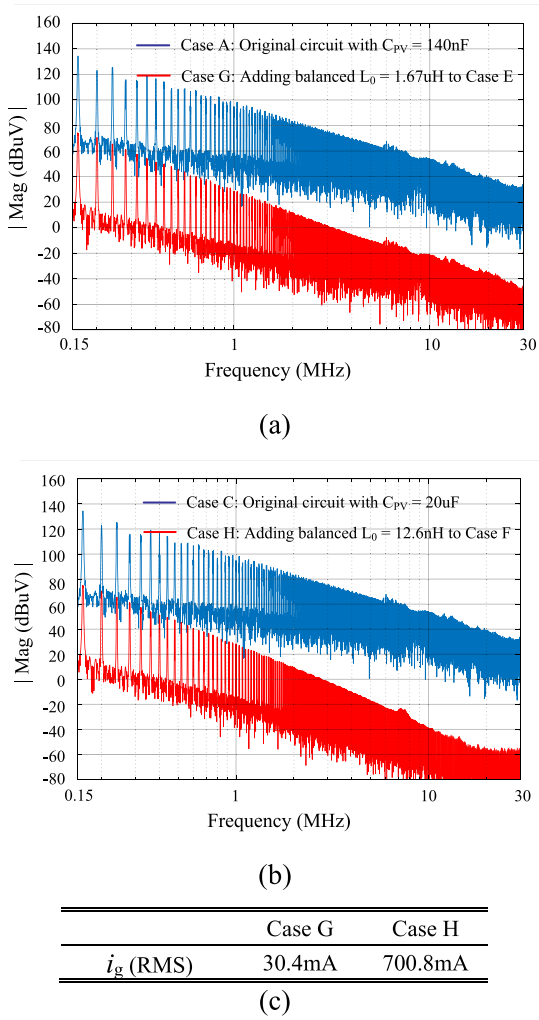


Fig. 11. k_1 and k_2 with ratio of $Z(L_0)$ to $Z(L)/3$.



	Case G	Case H
i_g (RMS)	30.4mA	700.8mA

(c)

Fig. 12. Spectra of CM noise and RMS value of leakage current. (a) The spectra of Case A and Case G: Adding $L_0 = 1.67$ uF to Case E. (b) The spectra of Case C and Case H: Adding $L_0 = 12.6$ nH to Case F. (c) The RMS value of leakage current of Case G and Case H.

the grounding wire to the inverter shell that is defined in standards for user safety, which is around tens of mA. The structural capacitance $C_{\rm ph1}$ is usually larger in large power inverters due to bigger physical size compared to the inverters with small power. Thus, the C_0 is intended to be larger and is more risky to break the standards for large power inverters. Usually, Y capacitors should be chosen for the added bus capacitor due to safety standard and many Y capacitors are connected in parallel to reduce the parasitic inductance. Thus, here 20 1-uF Y capacitors C43Q1105KBS from FARATRONIC [46] are chosen for the 20 uF C_0. The total volume and cost are 520.3 cm^2 and CNY 24.

D. Adding L_0 Between O and N to Increase k_2

Another way to balance the bridge is to increase k_2 by adding L_0 between the middle point of the DM capacitance O and the neutral point of the dc side N as shown in Fig. 10 [25], [43]. The total impedance of the branch PN is dominated by the inductor L_0 in the 150 kHz–30 MHz by a proper design to make the resonant frequency of L_0 and $3C_{\rm ac}$ much lower than 150 kHz. The Z_3 and Z_4 in the unified model are $Z(L)/3$ and $Z(L_0)$, respectively. Then k_2 can be expressed as follows according to (10):

$$k_2 = \frac{Z(L_0)}{Z(L)/3 + Z(L_0)} = \frac{1}{\frac{Z(L)/3}{Z(L_0)} + 1} \tag{13}$$

With a fixed $C_{\rm PV}$, k_1 is a constant value, as shown in Fig. 11. When (14) is satisfied, k_2 equals k_1, the bridge circuit is balanced, and the $i_{\rm LISN}$ is almost 0 according to (12).

$$Z(L_0) = \frac{C_{\rm ph1}}{C_{\rm PV} + C_{\rm ph2}} \times \frac{Z(L)}{3} \tag{14}$$

According to (14), when $C_{\rm PV}$ is 140 nF, L_0 equals 1.67 uH, and when $C_{\rm PV}$ is 20 uF, L_0 equals 12.6 nH. The simulation results are shown in Fig. 12. It can be seen that this balance method has a significant reduction of CM noise, which the spectra are reduced by more than 40 dBuV in the frequency range of 150 kHz–30 MHz. The leakage current RMS value reduction in Case G is

TABLE IV
REDUCTION PERFORMANCE COMPARISON OF ABOVE REDUCTION METHODS

	Reduction performance
Adding L_{CM-AC}	The L_{CM-AC} need to be quite large to well reduce CM noise
Neutral pointes connections	Reduction effect is good only when C_{PV} is large
Adding C_0	Reduction effect is limited due to the limitation of the DC bus capacitance C_0
Adding L_0	Reduction effect is good in the whole frequency range of 150 kHz−30 MHz

TABLE V
OTHER PERFORMANCE COMPARISON OF ABOVE REDUCTION METHODS

		Adding L_{CM-AC}	Neutral points connecti ons	Adding C_0	Addin g L_0
Leakage Current / mA	C_{PV} = 140 nF	41.3	356.4	702.2	30.4
	C_{PV} = 20 uF	240.2	702.2	827.9	700.8
Cost / CNY		10000	0	24	5
Volume / cm^3		16419	0	520.3	7.7
Sensitivity to C_{PV}		Little	Strong	General	Strong

more than Case H because the impedance Z_G in (11) increases a lot due to the increased L_0 and decreased C_{PV}.

Theoretically, compared with the previous method by adding dc bus capacitance, the method has a better reduction effect on CM noise because k_1 and k_2 can be almost exactly matched. And it will not lead to increase of low-frequency grounding current. Moreover, the L_0 will not increase the system's much extra volume and cost because its value and current stress are both relatively small. Regarding the ring magnetic core, a 1.67-uH L_0 with 20-A current capacity needs a core with 26-mm outer diameter and 13-mm thickness and two strands of copper wires with 1.4-mm diameter in parallel. The volume and cost are 7.7 cm^3 and CNY 5, respectively.

However, the drawback of this method is that the determination of L_0 depends greatly on the advance prediction of parasitic parameters. The C_{PV} is closely related to installation conditions, ambient temperature, and humidity, so it varies in a wide range that leads to large variation of k_1. It will break the designed balance and worsen the CM current. Another point is that when C_{PV} becomes quite large in damp environment, the value of L_0 is very small, which makes it very sensitive to the parasitic inductance. Therefore, this problem needs to be further analyzed and solved.

In the end, the performance comparison of the above reduction methods are shown in Tables IV and V. The method by adding L_0 among the above methods has a good reduction effect of CM noise with little additional cost, volume, and leakage current. However, the strong sensitivity to C_{PV} makes it hard to be implemented in industrial applications. In the following, an improved way is proposed to reduce the CM EMI noise by considering uncertain C_{PV}.

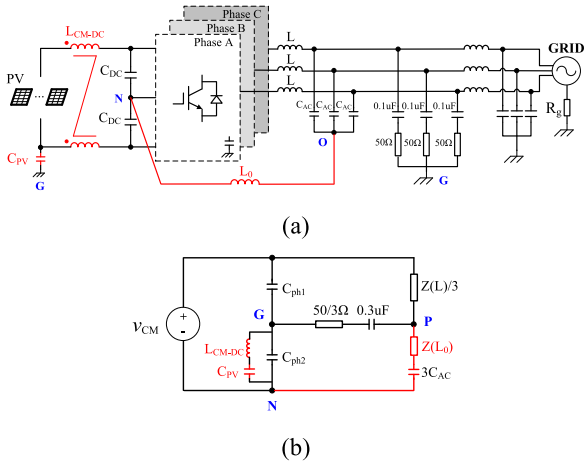


Fig. 13. Proposed CM EMI reduction method. (a) The schematic. (b) The CM noise model.

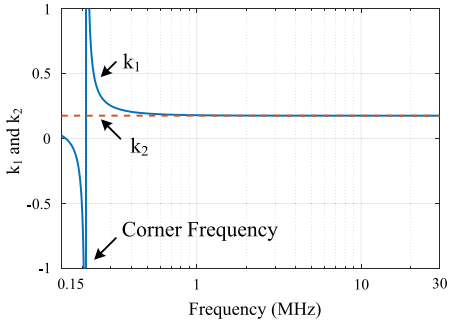


Fig. 14. The relationship between k_1, k_2 curves and frequency.

IV. PROPOSED CM NOISE REDUCTION METHOD CONSIDERING UNCERTAIN C_{PV}

Fig. 13 shows the proposed method to overcome the variation of the capacitance C_{PV}. First, an inductor L_0 is still added between the middle point of the DM capacitance O and the neutral point of the dc side N to achieve impedance balance without considering C_{PV}. Second, a CM inductance $L_{CM\text{-}dc}$ is added between the PV panels and the dc capacitors to weaken the effect of the variation of C_{PV} on the balance. Its schematic and CM noise model are shown in Fig. 13. For the CM noise model in Fig. 13(b), the expression of k_1 is

$$k_1 = \frac{[Z(L_{CM\text{-}dc}) + Z(C_{PV})]//Z(C_{ph2})}{Z(C_{ph1}) + [Z(L_{CM\text{-}dc}) + Z(C_{PV})]//Z(C_{ph2})} = \frac{s^2 L_{CM\text{-}dc} C_{PV} C_{ph1} + C_{ph1}}{s^2 L_{CM\text{-}dc} C_{PV}(C_{ph1} + C_{ph2}) + (C_{PV} + C_{ph1} + C_{ph2})} \quad (15)$$

Fig. 14 shows the relationship of k_1, k_2 with the frequency. The factor k_2 is defined in (13) and constant in the 150 kHz–30 MHz range. The other factor k_1 is more complex. The curve is obtained

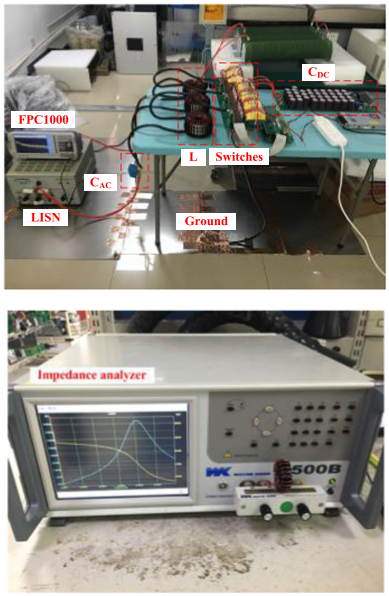


Fig. 15. The experiment setup.

with given inductance and capacitance, but the curve shape keeps the same for different parameters as long as the inductance $L_{\text{CM-dc}}$ meets certain requirements, which are explained as follows.

When the frequency is low enough, the impedance of $L_{\text{CM-dc}}$ is very small compared to that of C_{PV}. Thus, the impedance of their series connection is dominated by the capacitance C_{PV}, and the factor k_1 is equal to $C_{\text{ph1}}/(C_{\text{PV}} + C_{\text{ph1}} + \text{C}_{\text{ph2}})$ which is relatively small. When the frequency is high enough, the impedance of $L_{\text{CM-dc}}$ becomes large enough compared to the impedance of C_{PV}. Thus, the variation of C_{PV} has little influence on the total impedance of their series connection. Moreover, the impedance of $L_{\text{CM-dc}}$ is also much larger than that of C_{ph2}; thus, the total impedance of the branch GN is almost dominated by C_{ph2}. Correspondingly, the factor k_1 is equal to $C_{\text{ph1}}/(C_{\text{ph1}} + C_{\text{ph2}})$ in the high frequency range, which is only determined by the fixed structural capacitance of the equipment. In the medium range of the frequency, the factor k_1 decreases from $C_{\text{ph1}}/(C_{\text{PV}} + C_{\text{ph1}} + C_{\text{ph2}})$ to the negative infinite at the corner frequency that is determined by the resonant point of the denominator of (15) and then jumps to the positive infinite and further decreases to $C_{\text{ph1}}/(C_{\text{ph1}} + C_{\text{ph2}})$.

Equation (15) can be rewritten as follows:

$$k_1 = \frac{C_{\text{PV}}C_{\text{ph1}} - C_{\text{ph1}}/\omega^2 L_{\text{CM-dc}}}{C_{\text{PV}}(C_{\text{ph1}}+C_{\text{ph2}}) - (C_{\text{PV}}+C_{\text{ph1}}+C_{\text{ph2}})/\omega^2 L_{\text{CM-dc}}} \tag{16}$$

It can be easily found that when the inductance $L_{\text{CM-dc}}$ meets the requirements stated in the following equations:

$$\omega^2 L_{\text{CM-dc}} \gg \frac{1}{C_{\text{PV}}} \tag{17}$$

$$\omega^2 L_{\text{CM-dc}} \gg \frac{1}{C_{\text{ph1}} + C_{\text{ph2}}} + \frac{1}{C_{\text{PV}}} \tag{18}$$

the factor k_1 is almost equal to $C_{\text{ph1}}/(C_{\text{ph1}} + \text{C}_{\text{ph2}})$. Here, C_{PV} is usually much larger than $C_{\text{ph1}} + C_{\text{ph2}}$. Thus, as long as $L_{\text{CM-dc}} >> 1/\omega^2(C_{\text{ph1}} + C_{\text{ph2}})$, the inductance can both satisfy (17) and (18). This means that as long as the impedance of $L_{\text{CM-dc}}$ is much larger than that of the capacitance $(C_{\text{ph1}} + C_{\text{ph2}})$, the variation of C_{PV} has little influence on the k_1 and will not worsen the reduction effect with balance. Moreover, the inductor $L_{\text{CM-dc}}$ itself also has little influence on the balance. In the design, the impedance of $L_{\text{CM-dc}}$ set as five times larger than that of $(C_{\text{ph1}} + C_{\text{ph2}})$ at 150 kHz is good enough. This guideline is listed as follows:

$$L_{\text{CM-dc}} = \frac{5}{(2\pi \times 150 \times 10^3)^2} \times \frac{1}{C_{\text{ph1}} + C_{\text{ph2}}}. \tag{19}$$

According to the parameters in Tables II and III, the $L_{\text{CM-dc}}$ is calculated as around 0.4 mH. The CM current in this inductor is quite low; thus, small core can be used with two turns of windings capable for DM current. Regarding ring magnetic core, a core with 55-mm outer diameter and 42-mm thickness is required. Besides, five strands of copper wires with 2-mm diameter each that can handle 100-A input DM current needs to be paralleled and two turns are required. The cost is around CNY 100 for retail. The volume and cost for the inductor adds relatively small burden to the 140-kW inverter. After adding a simple CM inductor, the CM noise can be well reduced by matching the parameter $C_{\text{ph1}}/C_{\text{ph2}}$ and $3L_0/L$.

Obviously, on one hand, by using an inductor of 0.4 mH, the capacitance C_{PV} does not play a role in the factor k_1, and as a result, its variation due to the practical conditions can be well eliminated. On the other hand, the inductor L_0 for the balance will not decrease to nH level, which can happen due to the large C_{PV} and always keeps at tens of uH level, which is because of the relatively large ratio of $C_{\text{ph1}}/C_{\text{ph2}}$ and DM inductance of the system. Thus, its sensitivity to the circuit parasitic inductance decreases. Moreover, the large inductance of L_0 helps limiting the RMS value of the leakage current. As shown in Table IV, the leakage current is 30.4 mA in the method D with 140 nF C_{PV} without the proposed $L_{\text{CM-dc}}$. By adding the inductor $L_{\text{CM-dc}}$, the influence of the C_{PV} on the balance is eliminated, resulting in a larger L_0 of 23.6 uH. Thus, the leakage current will further decrease to around 3 mA.

In reality, the CM inductor always has a parasitic capacitance. However, usually the turns number of CM inductor is low due to the high permeability of the magnetic core used; thus, the parasitic capacitance is quite low and much smaller than C_{PV}. Thus, it has little influence on the effect of $L_{\text{CM-dc}}$. In practice, the wire connecting the PV panels and the inverter has a certain inductance. For example, the self-inductance of a round wire is 197 uH with the length of 100 m and the cross-sectional area 16 mm^2 that is suitable for 120-A current [47], [48]. On one hand, the CM inductance of the wire is not large enough for our case with this long distance. On the other hand, the wire differs from case to case; thus, the inductance of the wire cannot be taken into consideration of designing the inductor $L_{\text{CM-dc}}$ without the knowledge of the real conditions. This inductance can be utilized as part of the inductor $L_{\text{CM-dc}}$. It always enhances

the effect of eliminating the variation of the C_{PV} by increasing the value of $L_{\mathrm{CM\text{-}dc}}$.

In the end, the design procedure of the proposed method can be concluded as follows:

1) the parasitic capacitance between the switches and the ground $C_{\mathrm{S1G}} - C_{\mathrm{S6G}}$ should be obtain to determine C_{ph1} and C_{ph2} based on the equipment;
2) the inductor L_0 in the neutral connections can be quickly calculated as follows. Due to the parasitics, the impedance of the DM inductor Z(L) in 150 kHz–30 MHz should be measured and the L_0 should also be designed to match it.

$$Z(L_0) = \frac{C_{\mathrm{ph1}}}{C_{\mathrm{ph2}}} \times \frac{Z(L)}{3} \tag{20}$$

3) $L_{\mathrm{CM\text{-}dc}}$ is calculated based on (19) and added into the system as shown in Fig. 13(a).

V. Simulation and Experiment

A 140-kW 3P-ANPC inverter is made to validate the above analysis. Due to the power limit in the laboratory, the input voltage is set at 300 V for the experiment. The other parameters are the same as listed in Tables II and III. The change of the input voltage only changes the spectrum of the noise source v_{CM} in the model, as shown in Fig. 3(d), but has little influence on the dependence of the i_{LISN} on the network. Thus, the low voltage experiment can also validate the above theory.

The LISN used in this article is ZN3770B that is V-type 50 Ω/50 uH circuit defined in Chinese government standards GB/T 6113.102-2018. Three 2-uF capacitors with low parasitic inductance are connected in parallel between the three inputs of LISN in order to filter the differential mode current. The CM spectrum is picked up by spectrum analyzer Rohde & Schwarz FPC1000. The experiment setup is shown in Fig. 15.

By the proposed suppression method, the components that affect the balance are C_{ph1}, C_{ph2}, $Z(L)/3$, and $Z(L_0)$, if the $L_{\mathrm{CM\text{-}dc}}$ is well designed. The structural capacitances C_{ph1} and C_{ph2} have ideal impedance of capacitance in the interested frequency range. However, the DM inductor L can have non-ideal spectrum due to its parasitics. The impedance of the inductor L is measured by 6500B, which is shown in Fig. 16(a). There is a resonant point near 1.6 MHz and another near 20 MHz. A high-order model is made which well fits the measurement, as shown in Fig. 16(b).

In order to achieve impedance balance, the impedance of L_0 should satisfy (20). It is not practical to order an inductor from suppliers based on impedance curve. However, this can be easily made by the inverter manufacturer. First, an inductor is made based on the claimed inductance of DM inductor and the balance requirement. In the experiment, a 23.5-uH inductor is made. Fig. 17(a) shows its impedance curve and (c) shows the fitted model. Obviously, the impedance cannot match that of the DM inductor. In real setup, there is a 1.1-uH parasitic inductance for the neutrals connection and the contact. Considering this, then, a 382-pF capacitor and a 4.7-kΩ resistor are connected in parallel to L_0 to change the resonant frequency and the resonant impedance of the combination based on the real impedance of L and (20). Fig. 17(c) shows the measured impedance curve for the final model that is shown in (d). It can be seen that the curve can match that of DM inductor well except for the high frequency range above 10 MHz.

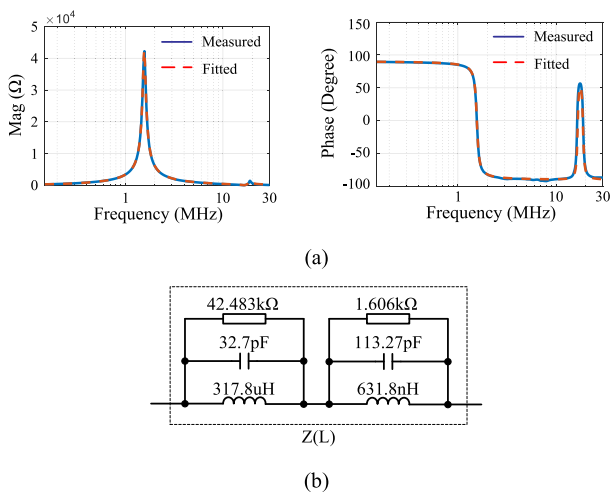


Fig. 16. The DM inductor L considering parasitics. (a) Measured and fitted impedance. (b) Fitted high-order model of L.

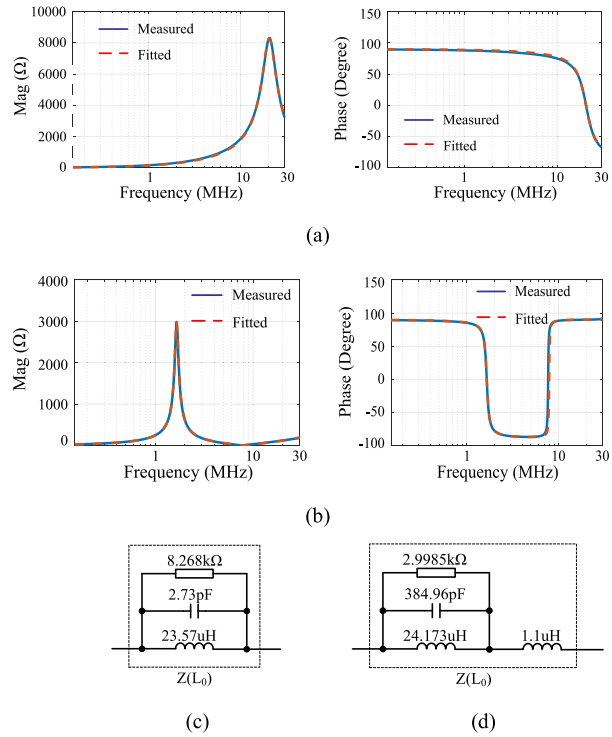


Fig. 17. Modeling of the inductor L_0. (a) Measured and fitted impedance before matching. (b) Measured and fitted impedance after matching. (c) Fitted model before matching. (d) Fitted model after matching.

First, the reduction effect of CM noise by adding matched L_0 is validated in simulation and experiment, and the results are shown in Fig. 18 and Fig. 19 respectively. The simulation is done in MATLAB Simulink for the circuit operating in time domain. By adding a matched inductor L_0, the CM noise can be well reduced, which is shown in both simulation and the experiment.

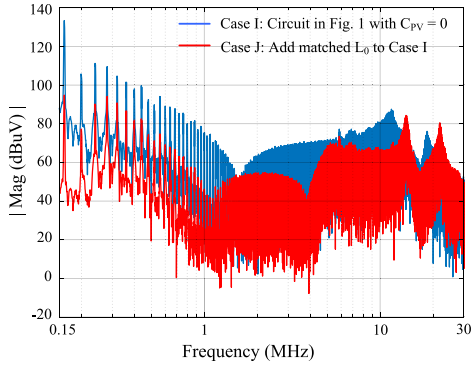


Fig. 18. Simulated spectra of different cases. (1) Case I: Circuit in Fig. 1 with $C_{\mathrm{PV}} = 0$. (2) Case J: Add matched L_0 to Case I.

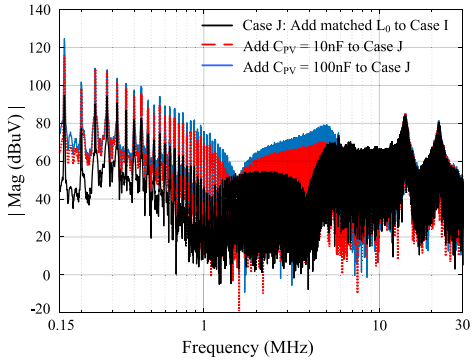


Fig. 20. Simulated spectra of the cases by adding C_{PV} of 10 and 100 nF to Case J.

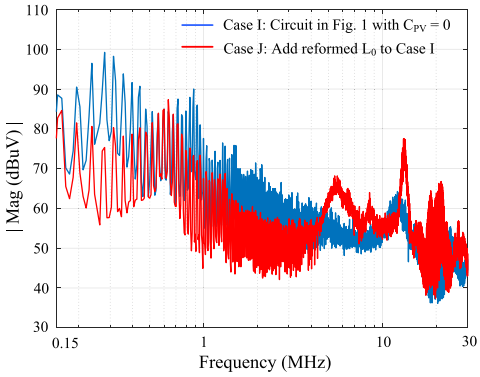


Fig. 19. Measured spectra of different cases. (1) Case I: Circuit in Fig. 1 with $C_{\mathrm{PV}} = 0$. (2) Case J: Add matched L_0 to Case I.

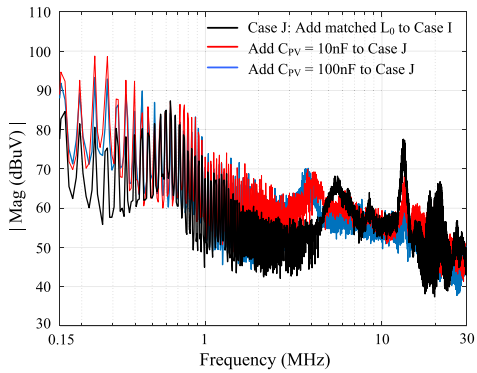


Fig. 21. Measured spectra of the cases by adding C_{PV} of 10 and 100 nF to Case J.

However, even for the Case I without matched L_0, there are two major differences between the simulation and the experiment results.

1) There is an unexpected peak at around 900 kHz in the experiment. This peak is due to the noise from the driver. The i_{LISN} has been tested in the condition that the driver circuit normally operates and the main power is not given. It can be found that there is a peak at around 900 kHz. The 40-kHz gate voltage works as another noise source that coupled into the CM noise model of the main circuit through the capacitance between gate and the ground as well as the Miller capacitance. The driver behavior is not easy to implement in the simulation conducted in MATLAB Simulink.
2) The valley at 1.6 MHz in the simulation is not obvious in the experiment. In the simulation, the v_{AN}, v_{BN}, and v_{CN} are ideal square waves, so the v_{CM} is also an ideal square wave and its high frequency component is very rich. Based on [37], the amplitude of an ideal square wave decreases at 20 dB/dec after the corner frequency, which is lower than 150 kHz in our case. However, the real switching wave is more like an S-shape wave that decreases at 40 dB/dec and further 60 dB/dec after around 400 kHz in our case. Thus, compared with the simulated result, the magnitude of the tested source can be much lower at a high frequency range. And this lower source compensates the peak of the impedance L, resulting in disappearing of the valley.

These two differences exist for the other results shown in this part as well. However, it has little influence on the validation of the theory and the effect of the proposed reduction method because they can be considered as background noises on the CM current.

In the above two figures, there are some other peaks. A peak at 5.5 MHz is caused by the 1.1-uH parasitic inductance for the neutral connections. The peaks at 11 and 19 MHz are caused by the parasitic inductance of the ground loop, and they will move to higher frequency if this parasitic inductance can be reduced. These peaks are shown both in the simulation and experiment results.

In order to show the effect of C_{PV} on the balance in the absent of $L_{\mathrm{CM\text{-}dc}}$, a series of simulations and experiments have been carried out. Fig. 20 shows the results of simulation when C_{PV} of 10 and 100 nF are added to Case J. It can be seen that with the change of C_{PV}, the CM noise increases a lot due to the break of the balance. According to (9), k_1 is an inversely proportional function of C_{PV}. Thus, the initial small increase of C_{PV} by 10 nF from the balance point leads to a rapid decrease of k_1, resulting in a rapid increase of CM noise as shown in the figure. Further increase from 10 to 100 nF leads to relatively small increase of the CM noise. The experiment results in Fig. 21 also shows that

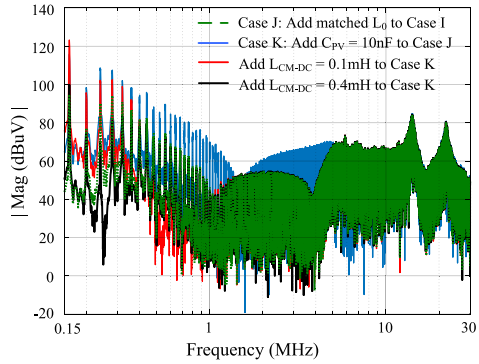


Fig. 22. Simulated spectra of different cases. (1) Case J: Add matched L_0 to Case I. (2) Case K: Add $C_{\mathrm{PV}} = 10$ nF to Case J. (3) Add $L_{\mathrm{CM\text{-}dc}} = 0.1$ mH to Case K. (4) Add $L_{\mathrm{CM\text{-}dc}} = 0.4$ mH to Case K.

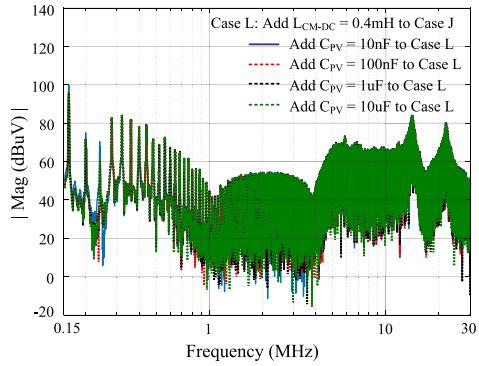


Fig. 24. Simulate spectra of different cases. (1) Add $C_{\mathrm{PV}} = 10$ nF to Case L. (2) Add $C_{\mathrm{PV}} = 100$ nF to Case L. (3) Add $C_{\mathrm{PV}} = 1$ uF to Case L. (4) Add $C_{\mathrm{PV}} = 10$ uF to Case L.

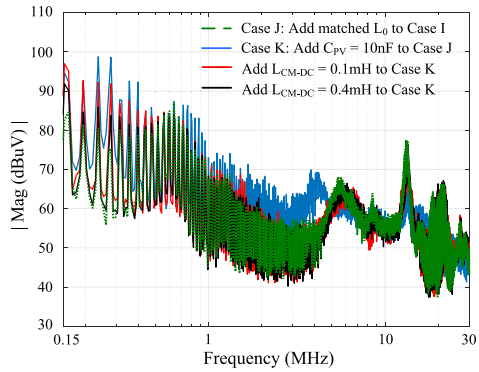


Fig. 23. Measure spectra of different cases. (1) Case J: Add matched L_0 to Case I. (2) Case K: Add $C_{\mathrm{PV}} = 10$ nF to Case J. (3) Add $L_{\mathrm{CM\text{-}dc}} = 0.1$ mH to Case K. (4) Add $L_{\mathrm{CM\text{-}dc}} = 0.4$ mH to Case K.

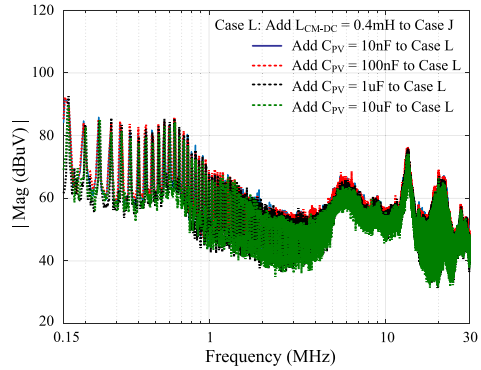


Fig. 25. Measure spectra of different cases. (1) Add $C_{\mathrm{PV}} = 10$ nF to Case L. (2) Add $C_{\mathrm{PV}} = 100$ nF to Case L. (3) Add $C_{\mathrm{PV}} = 1$ uF to Case L. (4) Add $C_{\mathrm{PV}} = 10$ uF to Case L.

the variation of C_{PV} has a strong increase of CM noise that has originally been reduced by the balance technique.

To eliminate the influence by the variation of C_{PV} on the suppression effect of CM noise, a CM inductor at the dc side can be added at the dc side based on the proposed method. Here, the CM inductors of 0.1 and 0.4 mH are, respectively, added to the dc side in Case K to show the elimination effect, and the simulated and experimental results are shown in Fig. 22 and Fig. 23 respectively. Based on (19), a 0.4-mH inductor can well eliminate the effect of C_{PV} on the reduction of CM noise. In the previous deduction, the C_{PV} is regarded much larger than the structural capacitances of the switches. Here in the experiment, a more severe case of 10-nH C_{PV} is conducted, which in theory requires larger dc CM inductor. The experiment results show that even with 0.4 mH, the increase of CM noise by the variation of C_{PV} can be almost totally eliminated, as shown in black curve. Even with a 0.1-mH inductor, the envelope of the CM noise shown as the red curve can move back to that in Case J when the circuit is well balanced, with only some differences of spikes.

Finally, with a CM inductor $L_{\mathrm{CM\text{-}dc}}$ of 0.4 mH, different capacitances C_{PV} are added to the system to show that the uncertainty of C_{PV} has little influence on the CM noise. Figs. 24 and 25 exhibit the results. In the simulation and experiment, the C_{PV} changes from 10 nF to 10 uF. It can be seen that the CM current is almost independent on the variation of C_{PV}, which well validates the proposed method.

VI. Conclusion

As SiC devices push the switching frequency of converters to a higher magnitude, the EMI should be carefully designed. For ANPC topology that is now often used in PV inverters, the CM current needs more attention and to be dedicatedly reduced for the SiC-based converters. This article proposes a simple way to reduce the CM current for ANPC inverters with uncertain parasitic capacitance C_{PV} of the PV panel, which is the practical situation. This technique is just to add a CM inductor at the dc side compared to some existing methods. The principle to derive the inductance is addressed. This technique increases a relatively small volume and cost of the equipment and is robust to the component parasitics. Although there are already some existing methods, they are not that practical for the real industry applications. Apart from the new reduction technique, the article also derives the CM current frequency-domain model for the ANPC topology and summarizes and compares most existing hardware-based reduction techniques with a unified model.

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Jianing Wang (S'08–M'11) was born in Anhui, China. He received the M.S. degree in power electronics from the Power Electronics and Renewable Energy Center in Xi'an Jiaotong University, Xi'an, China, in 2010, and received the Ph.D. degree from the Electrical Power Processing Group (EPP), Faculty of Electrical Engineering, Delft University of Technology, Delft, The Netherlands, in 2014.

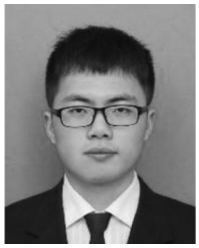
At the end of 2014, he became an Associate Professor with Hefei University of Technology, Hefei, China. He was the Deputy Secretary with ECCE ASIA 2016, Hefei, and became a Member of China Power Supply Society (CPSS) since then. Since 2016, he has been the Associate Editor for the *Chinese Journal of Electrical Engineering*. His current research interests include the integration of power electronics converters, the application of wide bandgap power devices, and the analysis of parasitics in converters and PV modules.

Xiaohui Liu was born in Anhui, China, in 1990. He received the B.S. degree in electrical engineering and automation from Hefei University of Technology, Hefei, China, in 2011. He is currently working toward the M.S. degree at the Department of Electrical Engineering and Automation, Hefei University of Technology.

His current research interests include common current elimination and the parasitic parameters of the wide bandgap devices.

Yuanwu Xun was born in Anhui, China. He received the B.S. degree in electrical engineering from Anhui Agricultural University, Hefei, China, in 2017. He is currently working toward the M.S. degree in electric engineering and automation at Hefei University of Technology, Hefei, China.

His current research interests include the parasitics of the photovoltaic modules, the application of wide bandgap power devices, and soft-switching application in inverters.



Shaolin Yu received the B.S. degree in electrical engineering from the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, in 2015, and the M.S. degree in control engineering from the School of Electrical Engineering and Automation, Hefei University of Technology in 2018, where he is currently working toward the Ph.D. degree at the Department of Electrical Engineering and Automation.

His current research interests include modeling of parasitic parameter in converters and power electronics applications for wide bandgap devices.