Common-Mode EMI Noise Analysis and Reduction for AC–DC–AC Systems With Paralleled Power Modules

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***Abstract*—In this article, the common-mode (CM) noise model is developed for an ac–dc–ac system with paralleled power modules. The CM noise contributions from both rectifiers and motor drives are analyzed. The interaction between the ac/dc rectifiers and dc/ac motor drives is explored. The CM noise reduction techniques which include a decoupling inductor technique and a CM noise balance technique are proposed to reduce the CM noise on the ac input side. Experiments and simulations were conducted to validate the developed CM noise model, rectifier and inverter interaction theory and CM noise reduction techniques.**

***Index Terms*—AC–DC–AC system, common mode (CM) noise, decoupling inductor, electromagnetic interference (EMI), motor drive inverter, paralleled power modules, wheatstone balance technique.**

I. Introduction

PARALLELED converters are usually employed to reduce input current ripple, increase system's reliability and scale up power [1] in ac–dc–ac systems. Electromagnetic interference (EMI) noise, especially common mode (CM) noise generated by the ac/dc converters and the dc/ac motor drive inverters could degrade the performance and reliability of the system [2]. EMI standards such as IEC-61800 [3] regulate the EMI emission in these variable frequency drive systems. In order to understand and reduce CM EMI noise, the CM noise model for the ac–dc–ac systems with paralleled power modules should be developed. Based on the developed model, CM EMI can be analyzed, and EMI reduction techniques can be developed.

The EMI model for a single cell ac-dc-ac converter system is discussed in [4]. However, the model lacks CM parasitic capacitance between inverter's voltage pulsating nodes and the ground, so the equivalent model is inaccurate. In [5], a three-cell back-to-back converter system is analyzed. However, the parasitic components are not quantified. In [6], a CM noise cancellation technique is proposed by synchronizing switching commutations for a back-to-back converter system. However, ignoring the parasitic parameters between the dc bus and the ground leads to inaccurate models.

Conventionally, passive EMI filters are used in ac–dc–ac converter systems to reduce EMI noise [7], [8]. However, these filters are usually bulky. Optimized modulations [9], [10] are used to reduce CM noise, however, these techniques are limited to certain topologies or certain control algorithms. Also, these optimized modulation techniques hardly have capability of reducing EMI above several MHz. Balance technique [2], [11], [12], [16] has been adopted in CM noise reduction in recent years. Compared with passive filters, the balance technique can achieve a large noise attenuation with smaller inductance or capacitance. The balance technique has been developed in [12] for single power factor correction (PFC) boost converters and was extended to other topologies such as neutral point clamped inverters [11], and interleaved PFC converters [16]. It is, therefore, necessary to investigate balance technique for ac–dc–ac systems with paralleled power modules.

In this article, a CM noise model will be developed for an ac–dc–ac system with paralleled power modules in Section II. The CM noise contributions from rectifiers and inverters are analyzed. The CM noise interaction between the rectifier and inverter subsystems is discussed in Section III. Based on the analysis, a decoupling inductor technique is applied to inverter and motor's grounding path and a Wheatstone bridge balance technique is implemented to parallel rectifiers in Section IV to reduce CM noise. The parameter design for the developed technique is also discussed. In Section V, experiments are conducted to verify the proposed technique.

II. Common-Mode EMI Noise Modeling for AC–DC–AC System With Paralleled Power Modules

A. AC-DC-AC Converter Systems With CM Parasitic Capacitance

Fig. 1 shows an ac–dc–ac system under investigation with two paralleled full bridge boost ac/dc rectifiers and one three-phase dc/ac motor drive inverter. The parallel ac/dc rectifiers are usually used to reduce input current ripple, EMI filter size, improve system reliability and improve power capability of the system. Both ac/dc rectifiers and the dc/ac motor drive inverter

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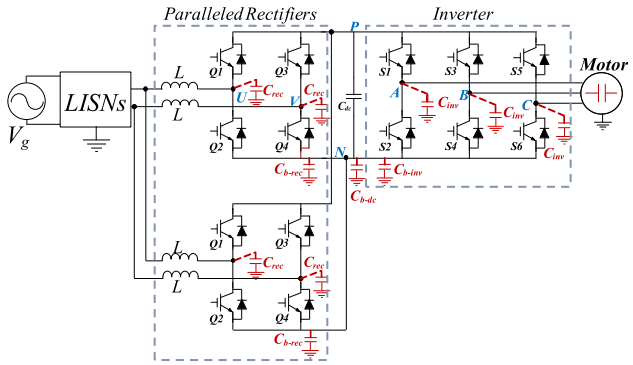


Fig. 1. AC–DC–AC system with paralleled power modules.

operate at four quadrants. The ac input voltage can be from 120 to 277 V. The dc-bus voltage can be from 300–400 V. The EMI of the whole system will be tested when the motor is working from 1 to 4 kVA.

The dc bus has a 2000 μF bulk capacitor $C_{\rm dc}$ which has a small impedance at high frequencies so it can be considered as short-circuit in the CM noise analysis. Each rectifier uses a single-phase H-bridge isolated-gate bipolar transistor (IGBT) module MITSUBISHI PM75B5L1C060 and the motor drives uses a three-phase IGBT module FUJI 2MBI1400VXB-120P-54. The top and cross-sectional views of one rectifier IGBT module are shown in Fig. 2(a) and (b). The views of inverter IGBT module are not shown here due to limited space.

In Fig. 1 and Fig. 2(a) and (b), the critical CM parasitic capacitance includes: the parasitic capacitance $C_{\rm rec}s$ between the collectors of the lower IGBTs of the rectifier bridges and the ground via the IGBT module's grounded metal base plate, heatsinks and rectifier metal box; $C_{\rm inv}s$ between the collectors of the lower IGBTs of the motor drive bridge and the ground via the IGBT module's grounded metal base plate, heatsinks and inverter metal box; $C_{b-{\rm dc}}$ between the dc-bus bulk capacitor and the ground; $C_{b-{\rm rec}}s$ (it includes $C_{P-{\rm rec}}s$, rectifier's positive dc bus to ground capacitance paralleled with $C_{N-{\rm rec}}s$, rectifier's negative dc bus to ground capacitance via the grounded rectifier metal box); and $C_{b-{\rm inv}}$ (it includes $C_{P-{\rm inv}}$, inverter's positive dc bus to ground capacitance via the grounded inverter metal box paralleled with $C_{N-{\rm inv}}$, inverter's negative dc bus to ground capacitance via the grounded inverter metal box) between the dc bus and the ground. The chassis of the motor is grounded, so there is also CM parasitic capacitance between the stator winding of the motor and the ground. For the layout in the IGBT modules under investigation, the following condition is approximately hold: all $C_{\rm rec}s$ are equal; two $C_{b-{\rm rec}}s$ are equal and all $C_{\rm inv}s$ are equal.

In order to extract individual parasitic capacitance of $C_{\rm rec}s$ and $C_{\rm inv}s$, the wire-bonds between the emitters of the upper switches and the ac port, between the emitters of the lower switches and the negative dc bus plate were removed. $C_{P-{\rm rec}}s$ and $C_{P-{\rm inv}}$ are equivalently in parallel with $C_{N-{\rm rec}}s$ and $C_{N-{\rm inv}}$ due to the small impedance of $C_{\rm dc}$, so $C_{P\_{\rm rec}} + C_{N\_{\rm rec}}$ is defined as $C_{b-{\rm rec}}$ and $C_{P-{\rm inv}} + C_{N-{\rm inv}}$ is defined as $C_{b-{\rm inv}}$.

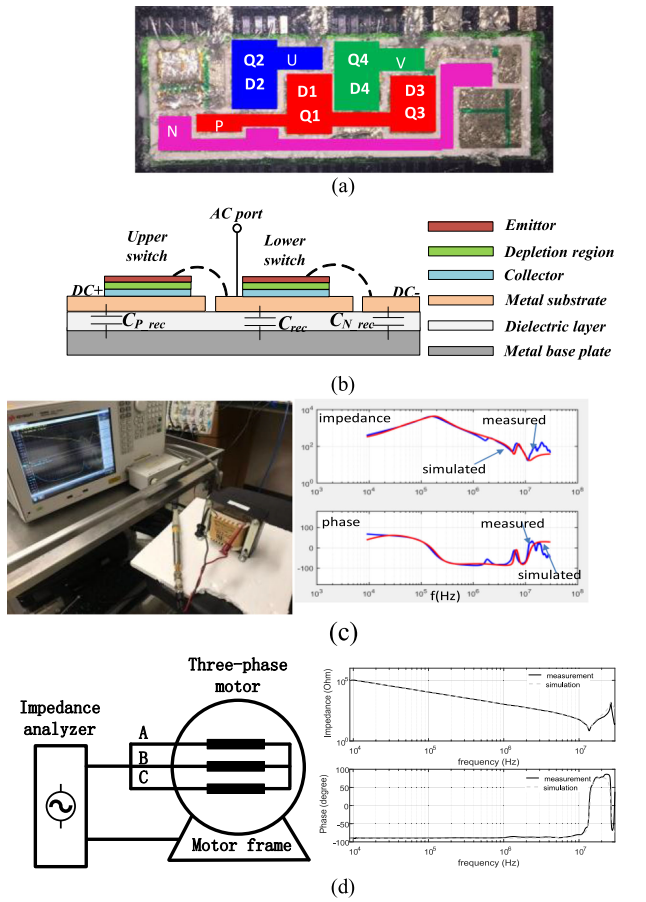


Fig. 2. (a) Top and (b) cross-sectional views of one H-bridge IGBT module, (c) inductor impedance measurement setup and results, and (d) ac motor CM impedance measurement setup and results.

TABLE I
EXTRACTED PARAMETERS VIA MEASUREMENTS

Symbol	Descriptions	Value
$C_{\rm rec}$	Rectifier lower IGBT collector to heatsink capacitance	32 pF
C_{inv}	Inverter lower IGBT collector to heatsink capacitance	1.7 nF
$C_{b\text{-}rec}$	Rectifier DC bus to heatsink capacitance	0.13 nF
$C_{b\text{-}dc}$	DC bus bulk capacitor to ground capacitance	0.43 nF
$C_{b\text{-}inv}$	Inverter DC bus to heatsink capacitance	5.62 nF
L	Line inductor inductance	10 mH
C_L	Winding capacitance of the line inductor L	0.2 nF
$C_{\rm DC}$	DC bus capacitor	2000 µF

The parameters are extracted in Table I via impedance measurements [13]. C_L and $Z_{\rm L}$ are the winding capacitance and impedance of the line inductor L. The impedance of the system is measured with an impedance analyzer Keysight E4990A which can accurately measure impedances from 20 Hz to 120 MHz. The calibrations (open-circuit and short-circuit calibrations) should be performed before the measurements. Line inductor L and ac motor's CM impedance are directly measured using the impedance probe of the impedance analyzer, as shown in Fig. 2(c) and (d). The impedance fitting technique for the simulations is discussed in [13] and [21].

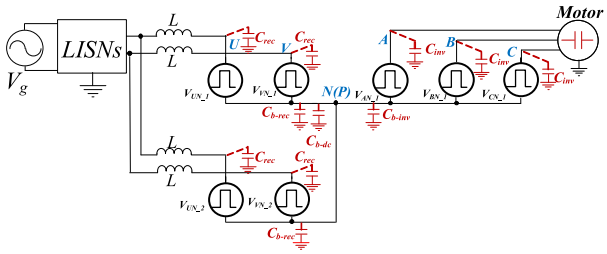


Fig. 3. Equivalent EMI model of the whole system.

$Z_{\rm rec}$, $Z_{\rm inv}$, $Z_{b-{\rm rec}}$, $Z_{b-{\rm dc}}$, and $Z_{b-{\rm inv}}$ are the impedances of $C_{\rm rec}$, $C_{\rm inv}$, $C_{b-{\rm rec}}$, $C_{b-{\rm dc}}$, and $C_{b-{\rm inv}}$ branches. At low frequencies, they are dominated by capacitances. $Z_{\rm MT}$ is the CM impedance of a 1.5 m cable and the induction motor. Because of the bulky size of dc bus capacitor, $C_{b-{\rm dc}}$ is not small.

B. CM Noise Model

Based on the substitution theorem, all the lower switches can be replaced with equivalent voltage sources V_{UN_1}, $V_{\rm VN\ 1}$, V_{UN_2}, V_{VN_2}, $V_{\rm AN}$, $V_{\rm BN}$, and $V_{\rm CN}$, which have the same voltage waveforms as the drain to source voltages of the switches to be replaced, and all upper switches can be replaced with equivalent current sources which have the same current waveforms as the drain to source currents of the switches to be replaced [12], [13], [18]. It should be pointed out that because the voltage sources and current sources have exactly the same voltage and current waveforms as those of the switching devices replaced, the voltage and current sources have all the information of the modulation schemes of the rectifiers and the inverter. Based on superposition theory, all the current sources are shorted by voltage sources, so they do not contribute to CM noise at ac input. As a result, the EMI equivalent model is reduced in Fig. 3.

In Fig. 3, it is assumed that the circuit parameters of all paralleled modules are identical. The two voltage sources of each rectifier module can be decomposed to a differential mode (DM) and a CM voltage sources. The CM voltage source generates CM noise. The DM voltage source does not generate CM noise, so it will not be analyzed here. Similarly, the three voltage sources of the inverter can be decomposed to a CM voltage source (zero sequence) and two DM voltage sources (positive and negative sequences) [20]. Only CM voltage source will be analyzed as the DM voltage sources do not generate CM noise unless the system parameters are asymmetric. The CM noise model is thus reduced to Fig. 4(a). The comparison of the simulated CM noise and the measured CM noise is shown in Fig. 4(b). The simulation matches the measurement very well before 10 MHz. The impedance fitting techniques and the CM EMI for an ac–dc–ac system have been discussed in [13] and [21], respectively. The influence of the spectrum analyzer to EMI measurement and the mechanisms of the inaccuracy of simulations at high frequencies are discussed in [22]. It should be noted that the measurement in Fig. 4(b) was conducted with a Tektronix RSA306 spectrum analyzer with 10 Hz resolution bandwidth (RBW) and Kaiser IF filter.

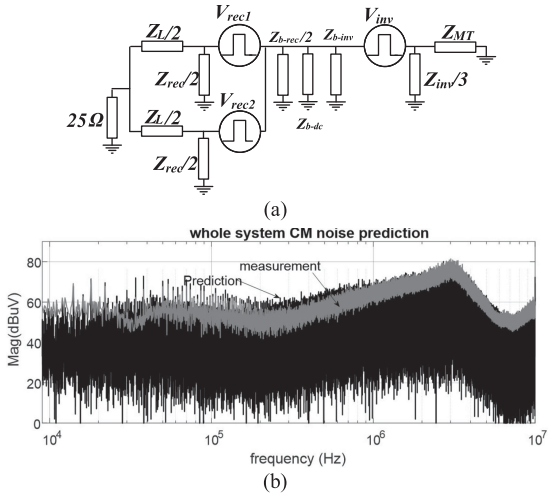


Fig. 4. (a) Reduced equivalent CM circuit of the whole system. (b) Simulation and experiment comparison for 1 kW system.

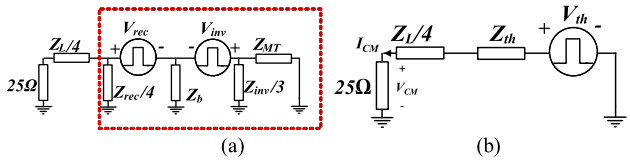


Fig. 5. Further reduced CM circuit.

In Fig. 4, $V_{\rm rec1}$, $V_{\rm rec2,}$ and $V_{\rm inv}$ represent the equivalent CM voltage sources, which are given by (1) and (2), of the *i*th rectifier (i = 1,2) and the inverter

$$V_{{\rm rec}\_i} = \frac{1}{2}\left(V_{{\rm UN}\_i} + V_{{\rm VN}\_i}\right) \tag{1}$$

$$V_{\rm inv} = \frac{1}{3}\left(V_{\rm AN} + V_{\rm BN} + V_{\rm CN}\right). \tag{2}$$

In Fig. 4, depending on the phase difference of paralleled rectifiers, there is CM current flowing through linear impedance stabilization networks (LISNs) or circulating current within rectifiers. Because circulating current does not contribute to CM noise at ac input, the CM equivalent circuit can be further reduced to Fig. 5(a) by averaging the CM voltage sources of two rectifiers. In Fig. 5(a), $Z_b = (Z_{b-{\rm rec}}/2)//Z_{b-{\rm dc}}//Z_{b-{\rm inv}}$. $V_{\rm rec}$ is the average of $V_{\rm rec1}$ and $V_{\rm rec2}$. By applying the Thevenin's theorem to the circuit in the dash line box, the model can be further reduced to Fig. 5(b) with equivalent source impedance $Z_{\rm th}$ and equivalent CM voltage source $V_{\rm th}$ defined as

$$Z_{\rm th} = \frac{Z_{\rm rec}}{4}//Z_b//\frac{Z_{\rm inv}}{3}//Z_{\rm MT} \tag{3}$$

$$V_{\rm th} = k_{\rm rec}V_{\rm rec} - k_{\rm inv}V_{\rm inv} \tag{4}$$

$$k_{\rm rec} = \frac{\frac{Z_{\rm rec}}{4}}{\frac{Z_{\rm rec}}{4} + Z_b//\frac{Z_{\rm inv}}{3}//Z_{\rm MT}} \tag{5}$$

$$k_{\rm inv} = \frac{\frac{Z_{\rm rec}}{4}//Z_b}{\frac{Z_{\rm rec}}{4}//Z_b + \frac{Z_{\rm inv}}{3}//Z_{\rm MT}}. \tag{6}$$

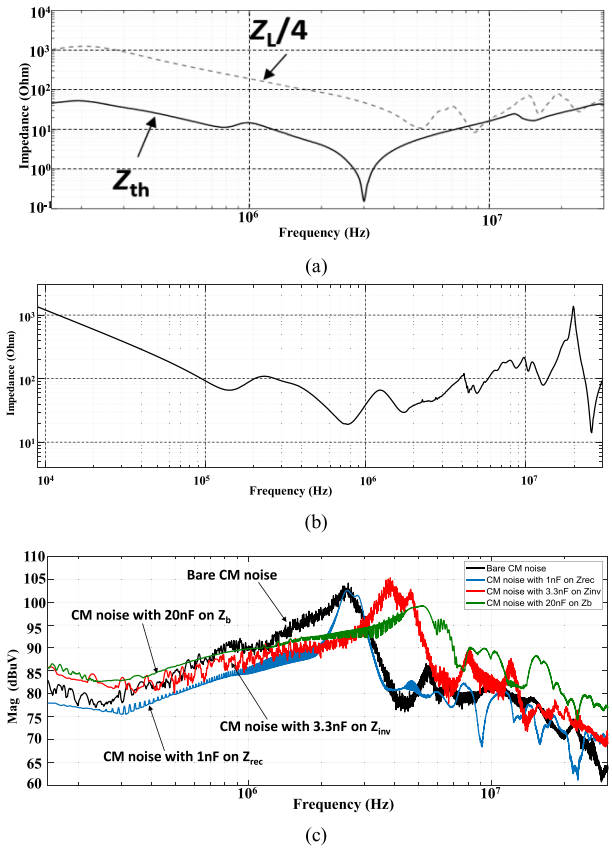


Fig. 6. (a) $Z_L/4$ vs $Z_{\rm th}$, (b) $Z_{\rm MT}$, and (c) effects of impedances on CM noise.

As shown in (4), $V_{\rm th}$ is the difference between the open-circuit CM voltages due to the rectifiers and the inverter. However, this doesn't necessarily lead to CM voltage cancellation because their switching frequencies, modulation index, initial phase etc., can be different. The full cancellation only happens when the two terms on the right of (4) have the same switching frequency, phase and magnitude. Videt *et al.* [6] proposed a CM noise source cancellation technique by synchronizing the switching commutations of the rectifiers and inverters. This method is valid only if $k_{\rm rec} = k_{\rm inv}$ when Z_b can be ignored. However, Z_b represents the capacitance between dc bus and the ground so it could be large as given in Table I. Z_b should therefore not be ignored.

In Fig. 5(b), CM noise $I_{\rm CM}$ is given by (7). The measured impedances of Z_L and $Z_{\rm th}$ are shown in Fig. 6(a) for the system under investigation. In the frequency ranges (150 kHz, 8 MHz) and (10 MHz, 22 MHz), Z_L is much larger than $Z_{\rm th}$. This indicates that Z_L dominates the loop impedance in Fig. 5(b) at most of frequencies

$$I_{\rm CM} = \frac{V_{\rm th}}{Z_{\rm th} + Z_L/4 + 25}. \tag{7}$$

Fig. 6(b) shows the measured $Z_{\rm MT}$. At the low frequencies from 150 kHz to 15 MHz, it is much smaller than any impedances of the rectifiers.

TABLE II
INFLUENCE OF THE PARASITIC PARAMETERS TO CM NOISE

	$\|k_{rec}\|$	$\|k_{inv}\|$	$\|I_{CM}\|$
$\|Z_{rec}\|$ ↓	↓	↓	↓
$\|Z_{b\text{-}rec}\|$ ↓	↑	↓	*Uncertain*
$\|Z_{b\text{-}dc}\|$ ↓	↑	↓	*Uncertain*
$\|Z_{b\text{-}inv}\|$ ↓	↑	↓	*Uncertain*
$\|Z_{inv}\|$ ↓	↑	↑	↑
$\|Z_{MT}\|$ ↓	↑	↑	↑

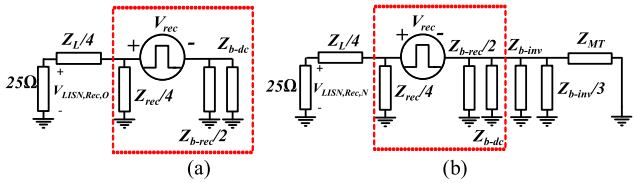


Fig. 7. Inverter's influence to the CM noise of the rectifiers. (a) Model for CM noise generated by the rectifiers. (b) Model for CM noise under the influence of inverter and motor's CM impedances.

Based on Fig. 6(a) and (b); and (3)–(7), the influence of parasitic parameters to the CM noise $I_{\rm CM}$ can be derived in Table II. In general, decreasing $Z_{\rm rec}$ (increasing $C_{\rm rec}s$) decreases the CM noise since $Z_{\rm rec}$ bypasses the CM noise flowing to LISNs. A decrease of $Z_{b-{\rm rec}}$, $Z_{b-{\rm dc}}$ or $Z_{b-{\rm inv}}$ (increasing the capacitance between the dc bus and the ground) helps to reduce the CM noise generated from the inverters, however, it increases the CM noise generated from the rectifiers so the influence is uncertain. Decreasing $Z_{\rm inv}$ (increasing $C_{\rm inv}$s) or decreasing $Z_{\rm MT}$ increases the CM noise generated from both rectifiers and inverters. Because of the high order parasitic effects and possible resonances of these impedances at high frequencies, Table II is more applicable and easier to use in LF range than in high frequency (HF) range. The measured CM noise in Fig. 6(c) verified the analysis. After a 1 nF capacitor is paralleled with $Z_{\rm rec}$, CM noise is reduced. After paralleling a 3.3 nF capacitor with $Z_{\rm inv}$, the CM noise is increased in whole frequency range except from 320 kHz to 3 MHz. The CM noise decreasing from 320 kHz to 3 MHz is possibly due to the movement of resonant frequency in the CM equivalent circuit as the noise spike frequency changes in the figure. Reducing $Z_{b-{\rm dc}}$ by adding a 20 nF capacitor between the dc bus and the ground has an uncertain effect on CM noise.

III. Interaction of the Rectifiers and the Inverter and Their Effect on the CM Noise on LISNs

Since the rectifier and inverter subsystems are connected and coupled together, it is critical to study the interaction between the rectifier and inverter subsystems.

A. Inverter's Influence to the CM Noise of Recitifers

Fig. 7 shows inverter's influence to the CM noise on the input of rectifies. In Fig. 7(a), when the inverter is disconnected, the rectifiers generate CM voltage $V_{\rm LISN,Rec,O}$, which is given by

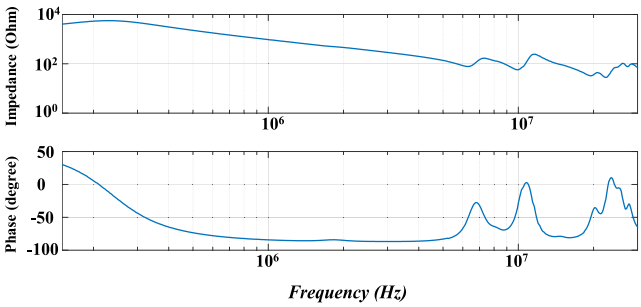


Fig. 8. Impedance and phase of the line inductor *L*.

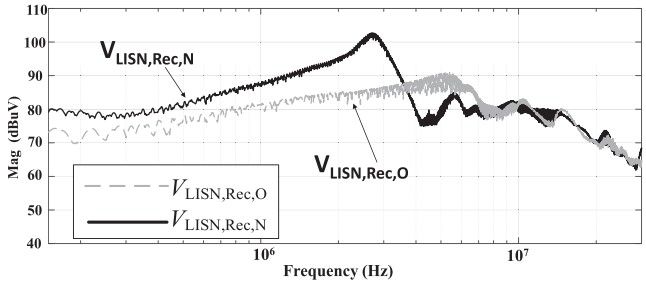


Fig. 9. CM noise before and after connecting the inverter to the rectifiers.

(8), on LISNs

$$V_{\mathrm{LISN,Rec},O} = \frac{\frac{25\frac{Z_{\mathrm{rec}}}{4}}{\frac{Z_{\mathrm{rec}}}{4}+\frac{Z_{b-\mathrm{rec}}}{2}//Z_{b-\mathrm{dc}}}V_{\mathrm{rec}}}{\frac{Z_L}{4}+\frac{Z_{\mathrm{rec}}}{4}//\frac{Z_{b-\mathrm{rec}}}{2}//Z_{b-\mathrm{dc}}+25}. \quad (8)$$

The CM impedance between the dc bus and the ground is $(Z_{b-\mathrm{rec}}/2)//Z_{b-\mathrm{dc}}$. When the inverter is connected to dc bus as in Fig. 5(a), based on superposition theory, the CM noise generated from the rectifiers can be analyzed by shorting V_{inv} in Fig. 5(a). The impedance of the inverter and motor are therefore in parallel with $(Z_{b-\mathrm{rec}}/2)//Z_{b-\mathrm{dc}}$, as in Fig. 7(b). Because the CM impedance between the dc bus and the ground is changed, a new CM noise voltage $V_{\mathrm{LISN,Rec},N}$ is generated on LISNs as given by

$$V_{\mathrm{LISN,Rec},N} = \frac{25k_{\mathrm{rec}}V_{\mathrm{rec}}}{\frac{Z_L}{4}+Z_{\mathrm{th}}+25}. \quad (9)$$

The change of the noise on LISNs due to inverter's impedances is characterized by insertion gain $IG_1 = V_{\mathrm{LISN,Rec},N}/V_{\mathrm{LISN,Rec},O}$. In the system under investigation, the line inductor *L* is made of silicon steel and Z_L from 150 kHz to 30 MHz is shown in Fig. 8. It is mostly capacitive in most of the frequency range due to its parasitic capacitance. As shown in Table I and Fig. 6, for the system under investigation, the inverter, motor and LISN's CM impedances are mostly smaller than the impedances of the rectifiers, so IG_1 can be approximated by

$$\mathrm{IG}_1 = \frac{V_{\mathrm{LISN,Rec},N}}{V_{\mathrm{LISN,Rec},O}} \approx 1+4\left(\frac{1}{Z_{\mathrm{rec}}}+\frac{1}{Z_L}\right) \times\left(\frac{Z_{b-\mathrm{rec}}}{2}//Z_{b-\mathrm{dc}}\right). \quad (10)$$

In (10), in low frequency (LF) range, $Z_{b-\mathrm{rec}}$, $Z_{b-\mathrm{dc}}$, Z_{rec} and Z_L are mostly capacitive, so the magnitude of IG_1 is larger than 1. This indicates the inverter increases the CM noise generated from the rectifiers at low frequencies. Plugging the values of Table I in (10), $\mathrm{IG}_1 \approx 5.2$ dB.

The measured CM noise before and after connecting the inverter to the rectifiers is shown in Fig. 9. At low frequencies, the CM noise is increased by 6 dB as predicted.

At high frequencies, the impedances, and therefore, the CM noise, were dominated by HF parasitic effects.

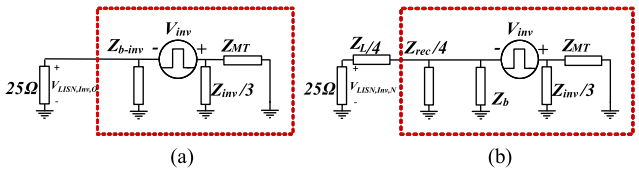


Fig. 10. Rectifier's influence to the CM noise of the inverter. (a) CM noise generated by the inverter. (b) CM noise under the influence of rectifier's CM impedances.

B. Rectifier's Influence to the CM Noise of Inverters

The inverter also generates CM current flowing through LISNs. The CM noise voltage drop $V_{\mathrm{LISN,Inv},O}$ on LISNs without the rectifiers can be calculated from Fig. 10(a) in (11). Based on superposition theory, the CM noise voltage drop $V_{\mathrm{LISN,Inv},N}$ on LISNs with the rectifiers can be calculated from Fig. 10(b) in (12)

$$V_{\mathrm{LISN,Inv},O} = \frac{-Z_{b-\mathrm{inv}}//25}{Z_{MT}//\frac{Z_{\mathrm{inv}}}{3}+Z_{b-\mathrm{inv}}//25}V_{\mathrm{inv}} \quad (11)$$

$$V_{\mathrm{LISN,Inv},N} = \frac{-25k_{\mathrm{inv}}V_{\mathrm{inv}}}{\frac{Z_L}{4}+Z_{\mathrm{th}}+25}. \quad (12)$$

The change of the CM noise on LISNs due to rectifier's impedances is characterized by $IG_2 = V_{\mathrm{LISN,Inv},N}/V_{\mathrm{LISN,Inv},O}$.

Because the inverter, motor and LISN's CM impedances are much smaller than the impedances of the rectifiers at low frequencies, as shown in Table I and Fig. 6, IG_2 can be approximated by (13)

$$\mathrm{IG}_2 = \frac{V_{\mathrm{LISN,Inv},N}}{V_{\mathrm{LISN,Inv},O}} \approx \frac{1}{1+\frac{Z_L/4}{25+Z_{\mathrm{th}}}}. \quad (13)$$

As shown in (13), impedance of the rectifiers reduces the CM noise generated from the inverter. The calculated IG_2 at low frequencies is -30.6 dB based on Table I. The measured CM noise in Fig. 11 shows the rectifiers reduce the CM noise generated from the inverter by around 30 dB at low frequencies as expected.

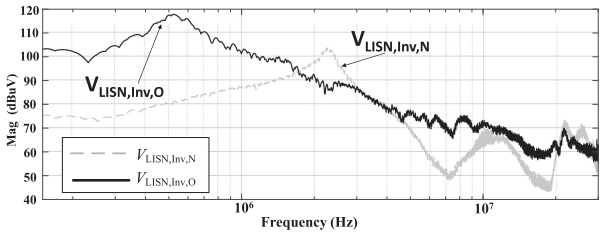


Fig. 11. CM noise before and after connecting the rectifiers to the inverter.

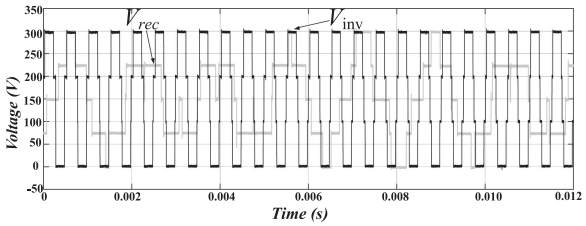


Fig. 12. Time domain of $V_{\rm rec}$ and $V_{\rm inv}$.

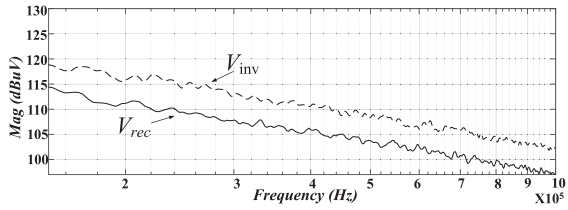


Fig. 13. Frequency domain of $V_{\rm rec}$ and $V_{\rm inv}$.

C. Rectifier and Inverter's Contributions to the Input CM Noise

Based on (9) and (12), the ratio of the CM voltages on LISNs due to rectifiers to that due to the inverter is given by

$$\left|\frac{V_{\rm LISN,Rec,}N}{V_{\rm LISN,Inv,}N}\right| = \left|\frac{k_{\rm rec}}{k_{\rm inv}}\frac{V_{\rm rec}}{V_{\rm Inv}}\right|. \tag{14}$$

Equation (14) identifies the major CM noise source in frequency domain. At a frequency, if the ratio is larger than 1, the CM noise is mostly contributed from the rectifiers; otherwise it is mostly from the inverter. For the system under investigation, the rectifiers have a switching frequency of 600 Hz and the inverter has a switching frequency of 2 kHz. The measured CM voltages $V_{\rm rec}$ and $V_{\rm inv}$ in time and frequency domains are shown in Figs. 12 and 13, respectively. Since the inverter has a higher modulation frequency than the rectifiers below 150 kHz and the magnitude of $V_{\rm inv}$ is higher than that of $V_{\rm rec}$ in time domain, $V_{\rm inv}$ has a bigger magnitude than $V_{\rm rec}$ in the LF range in Fig. 13. At high frequencies, other factors, such as rising and falling time, HF ringings, etc., determine HF CM EMI, but it is not the focus of this article. Plugging the values of Table I in (14), the ratio is around -2.8 dB. In Fig. 14, the measured $V_{\rm LISN,Rec,}N$ generated from the rectifiers is very close to the measured $V_{\rm LISN,Inv,}N$ generated from the inverter at low frequencies, which approximately meets (14). It is shown that above 3 MHz, the rectifiers dominate the CM noise.

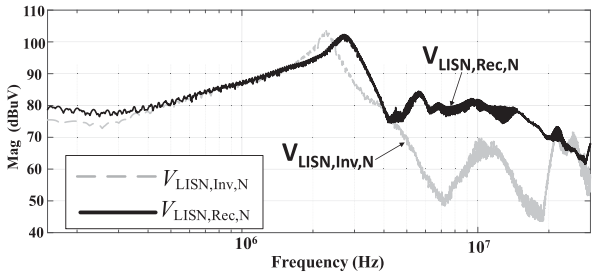


Fig. 14. Contributions of the rectifiers and inverter to CM noise.

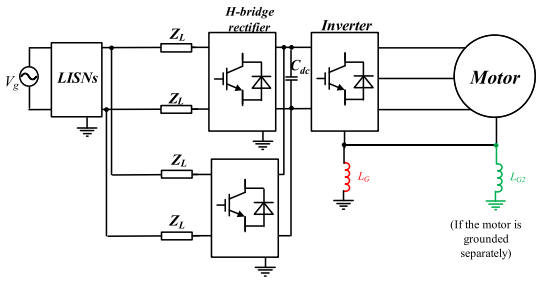


Fig. 15. Decoupling inductors L_G and L_{G2} reduce the CM noise due to the inverter.

IV. CM Noise Reduction With Decoupling Inductors and Balance Technique

A. Decoupling Inductors to Reduce Inverter's CM Noise

Based on Section III, the inverter can either directly generate CM noise or increase the CM noise generated from the rectifiers on ac input side. Its CM noise contribution may be as significant as the rectifiers, as shown in Fig. 14. From Figs. 5(a), 7(b), and 10(b), if the CM impedances of the inverter and motor can be greatly increased, the CM noise due to the inverter can be greatly reduced. Decoupling inductors on the grounding path are introduced here to reduce the CM noise generated from the inverter. The grounding of the power inverter's heatsink, inverter's metal case and motor's metal frame is required based on the safety requirement in case of short-circuit fault.

The principle is increasing $Z_{\rm inv}/3$ and $Z_{\rm MT}$. If the motor shares the inverter's grounding path, which is the case of the system under investigation, one decoupling inductor L_G can be added between the metal box of inverters and the ground, as in Fig. 15.

If the motor is grounded separately, the decoupling inductors L_G and L_{G2} can be added between the metal box of inverters and the ground as well as between the metal frame of the motor and the ground, as in Fig. 15. Fig. 16 shows the CM noise model for the system under investigation with the decoupling inductor L_G added. To reduce the influence of inverter to rectifiers' CM noise, the impedances $Z_{\rm LG}$ of the decoupling inductor should be much larger than $(Z_{b-\rm rec}/2)//Z_{b-\rm dc}$. To reduce the CM noise generated from the inverter, $Z_{\rm LG}$ should be much larger than $(25 + Z_L/4)//(Z_{\rm rec}/4)//(Z_{b-\rm rec}/2)//Z_{b-\rm dc}$ and $Z_{b-\rm inv}//(Z_{\rm inv}/3)//Z_{\rm MT}$.

In Fig. 16, although the parasitic winding capacitance of the inductor L_G and the parasitic capacitance between the metal

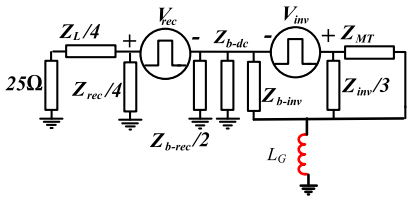
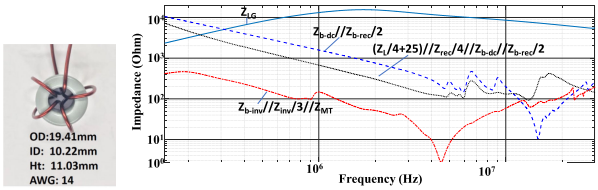


Fig. 16. CM equivalent circuit with the decoupling inductor L_G.



(a) (b)

Fig. 17. (a) Decoupling inductor L_G. (b) Impedance meets condition (15).

box of the inverter and the ground, between the motor's metal frame and the ground may bypass CM noise to the ground at high frequencies, as long as the impedances of these parasitic capacitances are much bigger than $(Z_{\rm inv}/3)//Z_{b-\rm inv}//Z_{\rm MT}$, $(25+Z_L/4)//(Z_{\rm rec}/4)//(Z_{b-\rm rec}/2)//Z_{b-\rm dc}$ and $(Z_{b-\rm rec}/2)//Z_{b-\rm dc}$, the CM noise can still be greatly reduced.

The magnetic core of L_G should have high permeability and high core loss. Lossy ferrite magnetics ZW41809TC is used here. Also, the grounding impedance at 60 Hz should be less than 0.1–5 Ω [15], [19] depending on the safety standards. It is equivalent to a 265 μH-13 mH inductance. Because of this, L_G, should be smaller than 265 μH-13 mH for safety considerations. The design of L_G should therefore meet (15). Since this inductor is connected between inverter's metal frame and the ground, only small CM noise current flows through this inductor. The core can hardly be saturated, so the core size can be small. In the design, the decoupling inductance is first designed based on the impedance requirement defined in (15) and Fig. 17. Second, the winding copper wire gauge is selected based on the maximum allowable short-circuit current (AWG14 in our case) because it should handle the current during short-circuit fault for safety protection. Third, magnetic cores are selected based on core's A_L to meet the impedance condition in (15). Fourth, the window size of the core is checked to make sure the winding can fit to the core window without issues. Finally, a single layer winding is preferred because the equivalent parallel capacitance of the inductor can be reduced. It should be noted that magnetic core with HF power loss is recommended, because it can keep inductor's HF impedance large and resistive

$$\max\left(\left|\frac{Z_{b-\rm rec}}{2}//Z_{b-\rm dc}\right|,\left|Z_{b-\rm inv}//\frac{Z_{\rm inv}}{3}//Z_{\rm MT}\right|,\left|\left(25+\frac{Z_L}{4}\right)//\frac{Z_{\rm rec}}{4}//\frac{Z_{b-\rm rec}}{2}//Z_{b-\rm dc}\right|\right)<|Z_{\rm LG}|<(0.1\Omega,5\Omega). \quad (15)$$

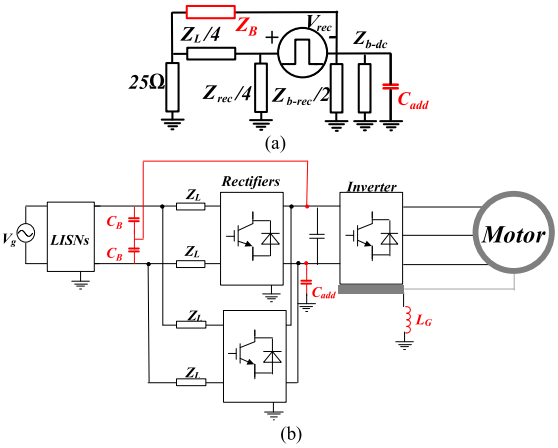


Fig. 18. (a) Balance bridge to reduce CM noise. (b) Circuit realization.

In the experiment, a four-turn 240 μH small inductor in Fig. 17(a) is designed as the decoupling inductor. Fig. 17(b) shows the measured $Z_{\rm LG}$ and other impedances. Although $Z_{\rm LG}$ does not meet (15) below 300 kHz, a 4.7 nF $C_{\rm add}$ will be added between dc bus and ground in Section IV B for balance technique. This makes $Z_{\rm LG}$ to meet (15).

It should be pointed out if the inverter or motor is directly grounded so L_G cannot be added between the ground and the inverter metal box or motor's metal frame, to decouple the inverter and motor, a CM inductor should be added on the dc bus or between the cable and the inverter, and a big $C_{\rm add}$ is also needed. However, due to the high load currents, the CM inductor size will be much bigger than L_G.

B. Balance Technique to Reduce Rectifier's CM Noise

A decoupling inductor has been implemented to greatly reduce the influence of the inverter to the rectifiers' CM noise and to reduce the CM noise generated from the inverter previously. A capacitor $C_{\rm add}$ will be added between the dc bus and the ground to further decouple the inverter from the rectifiers. Because of this, the inverter will not be shown in the figures in this section for convenience. The CM noise generated from the rectifiers can be reduced using the Wheatstone bridge balance technique as in Fig. 18(a). In Fig. 18(a), a balance impedance Z_B is connected between the dc bus and the ac input. However, different from [11] and [12], from Table I and Fig. 6(a), Z_L is dominated by winding capacitance C_L up to 5 MHz. So, Z_B should be capacitive. Based on the investigation in [11] and [12], a large impedance ratio helps to overcome the unbalance and achieve good CM noise reduction. A 4.7 nF $C_{\rm add}$ is, therefore, selected to increase the impedance ratio from 5.4 to 42 in the LF range. This also helps to meet (15). The CM noise can be greatly reduced if Z_B meets

$$\frac{Z_B}{Z_L}=\frac{\frac{Z_{b-\rm rec}}{2}//Z_{b-\rm dc}//Z_{C\rm add}}{Z_{\rm rec}}. \quad (16)$$

In (16), $Z_{C\rm add}$ is the impedance of $C_{\rm add}$. Based on the capacitance of $Z_{\rm rec}$ and $Z_{b-\rm rec}$ in Table I, Z_B should be a 33.7 nF capacitor. The circuit realization is in Fig. 18(b).

In Fig. 18(b), because Z_B is realized using two identical CM capacitors C_B, each desired C_B would be 16.8 nF for LF CM noise balance. The C_B will be adjusted in final experiments based on EMI measurements. At high frequencies, because of the parasitic inductances on impedance branches, the condition (16) is no longer met, so the balance performance will be degraded.

Since Z_L is no longer a good capacitance above 5 MHz, it is expected that the balance will not be as efficient as below 5 MHz. Above 5 MHz, other techniques, such as HF magnetic inductors, are needed on ac lines to further reduce HF CM noise if the EMI is above the EMI standards. So, the proposed technique is effective in low and mid-frequency ranges and it can largely reduce the size of LF EMI filters.

It should be pointed out that developed methodology here is independent from the system layout, casing and grounding etc. because the developed model is a generalized model which includes all conductive EMI parasitic impedances of the systems with the same topology. Different layouts only change the parasitic impedance and the final EMI spectrum. It does not invalidate the developed methodology.

V. Experiments and Analysis

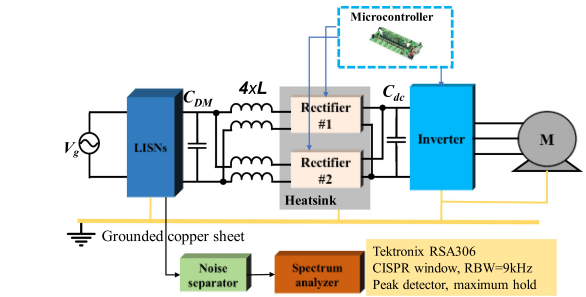
In this section, both the decoupling inductor and balance techniques will be verified in experiments. The prototype to verify the proposed technique has an ac-side inductance of 0.4 p.u. and a switching frequency of 600 Hz. The proposed technique can be extended to general paralleled power modules systems. The experiment setup is in Fig. 19. The circuit parameters are given in Table III. As stated in Section II, the system's power was scaled down from a high-power system for EMI research purpose based on the limited capability of lab facility. The motor shares the same grounding path as the inverter. A 1 μF DM capacitor $C_{\rm DM}$ is added between LISNs and *Ls* so DM noise can meet EMI standard in Fig. 19(e). The four-quadrant rectifier system employs a voltage close loop control as shown in Fig. 19(c). Fig. 19(d) shows the phasor diagram. The reference dc-bus voltage is at 300 V with 120 Vac input or 400 V with 277Vac input. Equations (17) and (18) show the deviation of power incremental $\Delta P_{\rm in}$ and the phasor for the new H-bridge voltage $V_{\rm HB}$ of the rectifier. It should be noted that the H-bridges are four-quadrant converters, so the power factor between the grid voltage and current ranges from -1 to 1 (not limited to unit power factor) based on different operation conditions. Fig. 19(b) shows the phasor diagram when the system works at PF = 1

$$\Delta P_{\rm in}(t) = \frac{{V_{\rm dc}}^{*2} - V_{\rm dc}(t)^2}{R_{\rm load}}. \tag{17}$$

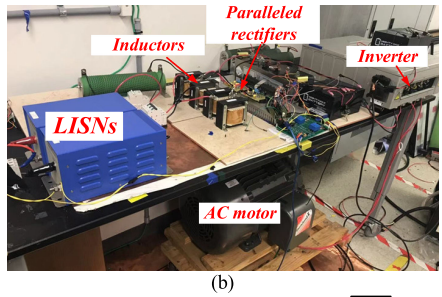
The new H-bridge phasor can be calculated based on

$$V'_{\rm HB} = {V_{\rm HB}}^* - j\omega L\Delta I_g = {V_{\rm HB}}^* - j\omega L\frac{\Delta P_{\rm in}(t)}{V_g}$$

$$= {V_{\rm HB}}^* - j\omega L\frac{{V_{\rm dc}}^{*2} - V_{\rm dc}(t)^2}{V_g R_{\rm load}}. \tag{18}$$



(a)



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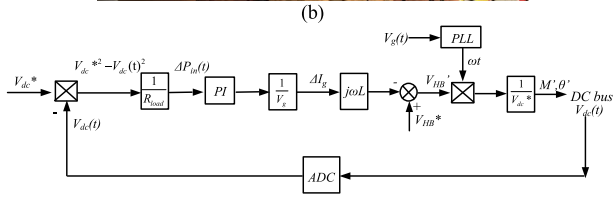
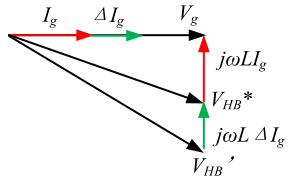


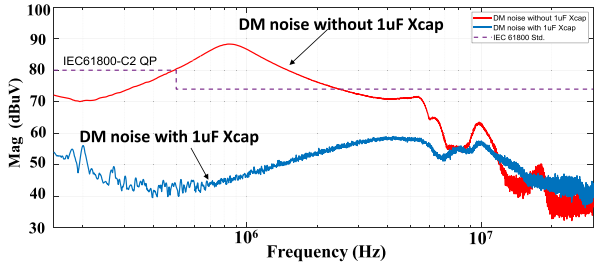
V_{dc}*: preset DC bus voltage
V_{dc}(t): instantaneous DC bus voltage
ΔP_{in}(t): power increments/decrements
V_g: Grid voltage
I_g: grid current
ΔI_g: grid current increments/decrements
V_{HB}*: original V_{HB} phasor

R_{load}: load resistance
PLL: phase lock loop (to get grid voltage's 0° position)
V_{HB}': new V_{HB} phasor
M': new modulation index
θ': new initial phase
L: line inductance

(c)



(d)



(e)

Fig. 19. (a) Experimental setup. (b) Experiment setup photo. (c) Control scheme. (e) Phasor diagram. (e) DM EMI meets the limit with $C_{\rm DM}$.

In Fig. 19(c), the new modulation index *M'* and initial phase θ' can be derived based on the phase lock loop of the grid voltage and dc-bus voltage.

The inverter and the motor are from the CRRC Company and the Baldor motor, respectively. The induction motor is M4103T-9. The inverter uses three phase FUJI 2MBI1400VXB-120P-54 module. The IGBT driver is Concept 2-SD-315-AI.

TABLE III
CIRCUIT PARAMETERS

Parameters	Symbol	Value
AC grid voltage	V_g	120 V/277 V
DC bus voltage	V_{DC}	300 V/400 V
Total power	S_{total}	1 kVA/4 kVA
Rectifier switching frequency	$f_{s\text{-}rec}$	600 Hz
Inverter switching frequency	$f_{s\text{-}inv}$	2 kHz

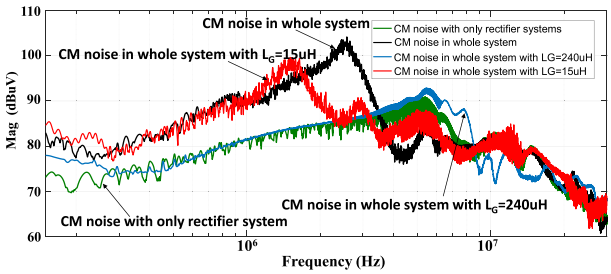


Fig. 20. CM noise comparison to validate the decoupling inductor technique.

The motor is controlled by an open-loop with variable voltage variable frequency modulation [23] for EMI research purpose. The fundamental component of three phase sine pulse width modulation (SPWM) waveform is generated based on the preset phase voltages and frequencies.

A. Verification of the Decoupling Inductor Technique

Four experiments were conducted in Fig. 20 at 120 Vac input and 300 Vdc bus. In the first experiment, the CM EMI of the whole original system was measured as the black curve. In the second experiment, the CM EMI with only the rectifiers under the same load condition was measured as the green curve. It is lower than the CM noise of the whole original system because the inverter contributes to CM noise. In the third and fourth experiments, a 15 and 240 μH decoupling inductor $L_{\rm G}$s were added to the whole original system, respectively, as shown in Figs. 15 and 16. The red and blue curves are the measured CM noise for 15 and 240 µH $L_{\rm G}$, respectively. As discussed earlier, based on Fig. 17, a 240 μH $L_{\rm G}$ can meet (15) above 300 kHz, but a 15 μH L_G cannot. As a result, 15 μH $L_{\rm G}$ does not reduce the CM noise well, but 240 μH $L_{\rm G}$ can reduce CM noise to the same level as the CM noise with rectifiers only above 300 kHz because the CM noise from the inverter was decoupled from the ac input of the rectifiers.

B. Verification of the Balance Technique

To validate the proposed balance technique in the last section, four experiments will be conducted for the whole system including both rectifiers and the inverter at 120 Vac input and 300 Vdc bus. In the first experiment, 240 μH $L_{\rm G}$ and 4.7 nF $C_{\rm add}$ will be implemented. C_Bs will be adjusted for bridge balance based on the calculated 16.8 nF and the measured EMI to achieve the lowest CM noise. In the second experiment, based on the first experiment, a small CM inductor $L_{\rm CM}$ will be further used on ac line to suppress HF CM EMI to meet the EMI standard. In the third experiment, the decoupling inductor will be implemented but C_{Bs} will not be employed. The same C_Bs and the small CM

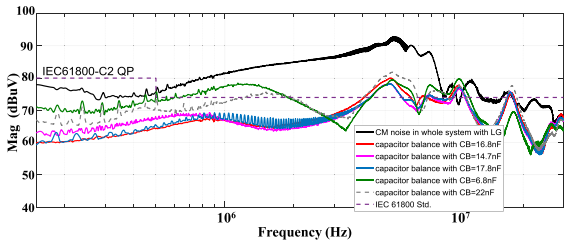


Fig. 21. CM EMI reduction with different balance capacitors.

inductor as in the second experiment will be used as CM filter capacitors and inductor to suppress CM noise. The objective is to fairly demonstrate that balance capacitors can reduce CM noise more than the CM filter which uses the same capacitance and inductance. In the last experiment, a conventional CM EMI filter will be designed to suppress CM EMI and meet the EMI standard without C_Bs, L_G, $C_{\rm add}$ and $L_{\rm CM}$ employed. The CM EMI filter size will be compared with the size of C_Bs, L_G, $C_{\rm add}$, and $L_{\rm CM}$. The EMI measurement will be conducted using a Tektronix RSA306 spectrum analyzer with 9 kHz RBW, as specified in the EMI standard IEC61800-C2. The peak EMI will be measured with maximum hold and compared with quasi-peak EMI standard from 150 kHz to 30 MHz. Because quasi-peak EMI is not higher than peak EMI, as long as peak EMI meets the quasi-peak EMI standard, quasi-peak EMI will meet the standard.

In the first experiment, different C_Bs from 6.8 to 22 nF are used as balance capacitors. The measured CM EMI is shown in Fig. 21. As shown in the figure, without the balance, the CM EMI is over the EMI standard from 500 kHz to 20 MHz. With the balance, as expected from the calculation, it is shown that in the range from 14.7 to 17.8 nF, which includes the calculated 16.8 nF, the CM noise reduction is the best. Within this range, the CM noise due to $V_{\rm rec}$ is greatly reduced, the CM noise due to other factors such as unbalanced parameters, voltage ripples on dc bus or the inverter noise will be dominant and they cannot be reduced with the balance. So, CM noise reduction is not very sensitive to C_B in this range. If the balance capacitance is bigger or smaller than this range, CM noise reduction will be smaller as the bridge is more unbalanced. In the experiment, C_B is achieved by using a 10 nF capacitor paralleled with a 6.8 nF capacitor. It is shown in Fig. 21 that, the CM noise is greatly reduced by up to 20 dB, a factor 10, within the whole frequency range except around 10 and 18 MHz. CM EMI is still several dB above the EMI standard around 5.2, 11 and 18 MHz.

In the second experiment, a small, lossy, one-turn 4.8 μH CM inductor $L_{\rm CM}$ is used on the AC input side to reduce HF CM noise as shown in Fig. 22. The inductor is made of VITROPERM 500F material and the core model is T60004-L2016-W373. The measured impedance of this inductor is shown in Fig. 23. It is shown that the impedance of $L_{\rm CM}$ is 40, 60 and 90 Ω at 5.2, 11, and 18 MHz. $L_{\rm CM}$ and the LISNs are a voltage divider. Because LISN's CM impedance is 25 Ω, the $L_{\rm CM}$ can reduce CM noise voltage on LISNs. The measured CM EMI with $L_{\rm CM}$ can meet the EMI standard in Fig. 24.

In the third experiment, two C_Bs in Fig. 22 are not connected to dc bus as balance capacitors but grounded as CM capacitors.

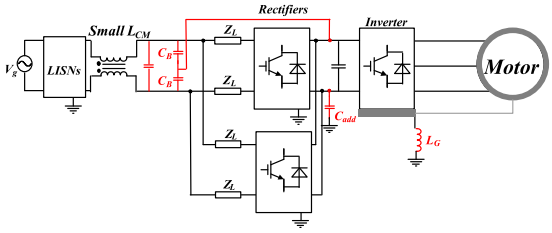


Fig. 22. Adding a small L_{CM} to reduce HF CM noise.

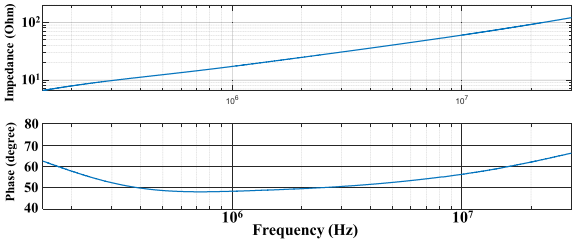


Fig. 23. Impedance of L_{CM}.

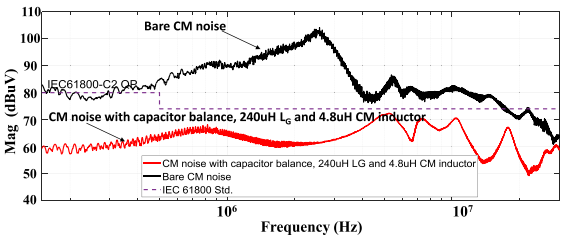


Fig. 24. CM EMI with $C_B = 16.8$ nF, $L_G = 240$ μH and $L_{\mathrm{CM}} = 4.8$ μH.

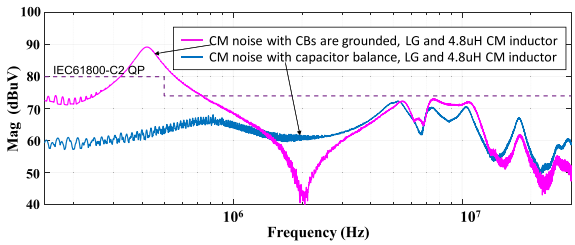


Fig. 25. CM EMI when C_Bs are used as CM capacitors.

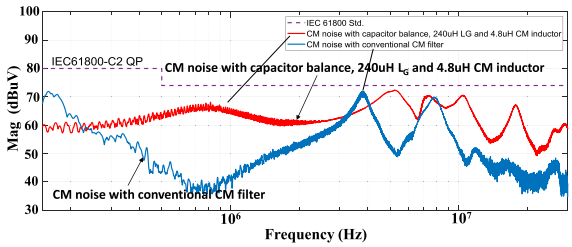


Fig. 26. Conventional CM EMI filter to meet the EMI standard.

TABLE IV
COMPONENT SIZE COMPARISON

Balance Technique			Conventional CM filter		
Components	Part No.	Volume	Components	Part No.	Volume
L_{G}	ZW4180 9TC	2833 mm^3	L_{cm1}	B64290L 0618X83 0	5151 mm^3
Small L_{cm}	T60004-L2016-W373	1148 mm^3	L_{cm2}	ESD-R-25SD	5887 mm^3
C_{B}s	2X(10 nF+ 6.8 nF)	2654 mm^3	C_{Y}s	2X(10 nF+ 6.8 nF+2.2 nF)	3422 mm^3
C_{add}	4.7 nF	614 mm^3			
Total		7249 mm^3	Total		14460 mm^3

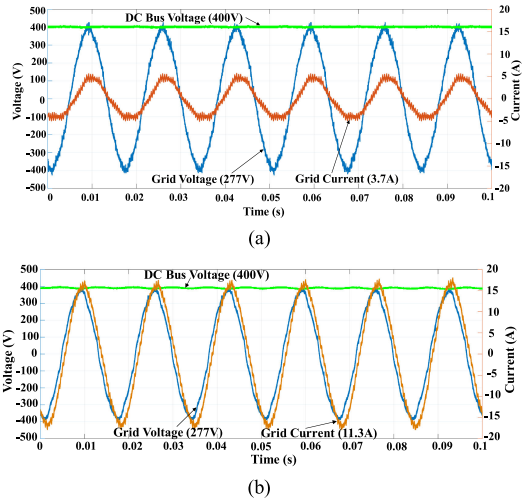


Fig. 27. Grid voltage, grid current and dc-bus voltage at load of (a) 963 W+ 350 var and (b) 3.03 kW+818 var.

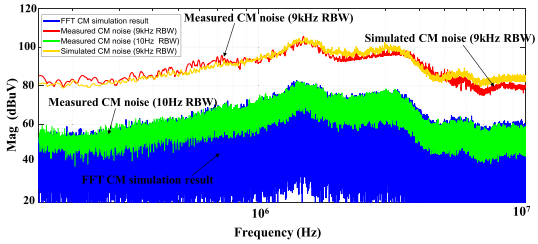
The measured CM EMI is shown in Fig. 25. EMI cannot meet the standard. The balance technique is therefore more efficient than CM filters.

In the fourth experiment, a conventional $L_{cm1} - 2C_y - L_{cm2}$ T-type CM EMI filter is designed to reduce CM noise and meet the EMI standard in Fig. 26 without proposed techniques applied. Table IV shows the component size comparison between the proposed techniques and the conventional CM EMI filter. 50% volume reduction is achieved.

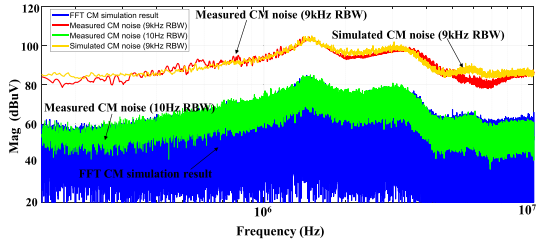
In order to verify the proposed technique in the ac–dc–dc system with paralleled power modules operated at different power conditions, the CM noise at load of 963 W+350 var in Fig. 27(a) and the CM noise at load of 3.03 kW+818 var in Fig. 27(b) are compared in Fig. 29. The input voltage is 277 Vac and the dc-bus voltage is 400 Vdc.

The comparisons of the predicted and measured results at two different power levels are shown in Fig. 28. The EMI modeling technique has been discussed in Section II-A and Section II-B. The EMI simulation technique including the effects of RBW of the spectrum analyzer was developed in [22]. The predicted results match the measured results very well in both 10 Hz and 9 kHz RBW settings.

It is shown that the bare CM noise is almost the same at different power levels with the same system setup as the parameters in the developed CM noise model are unchanged although the power change. By applying the proposed EMI reduction technique in Fig. 22, both CM noise were greatly reduced before 5 MHz. This further proved that the developed EMI reduction technique is independent from power level and modulation schemes.



(a)



(b)

Fig. 28. Comparison of the predicted and measured EMI at two power levels. (a) 963 W+350 var. (b) 3.03 kW+818 var.

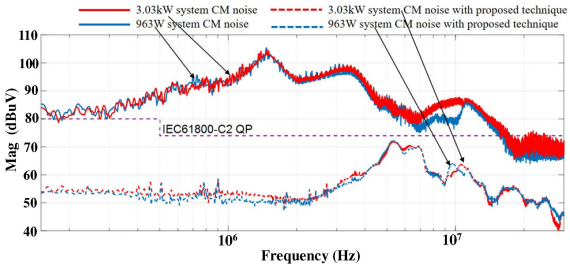


Fig. 29. CM noise reduction at different power conditions.

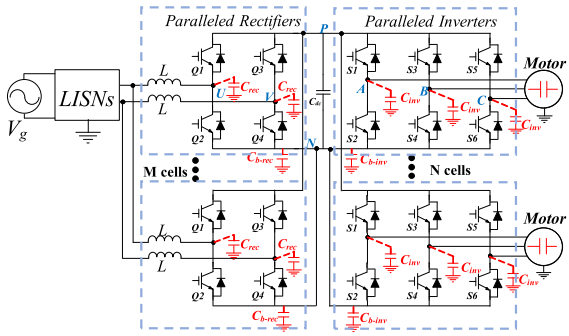


Fig. 30. Generalized system with *M* rectifiers and *N* inverters.

C. Extend the Techniques to General Cases

If the system has *M* paralleled rectifiers and *N* paralleled inverters in Fig. 30. The proposed techniques still apply. The CM noise model can be derived similarly in Fig. 31. The reduced CM noise model and Thevenin equivalent model are shown in Fig. 32. In Fig. 32, $V_{\text{rec\_}i}$ and $V_{\text{inv\_}j}$ represent the equivalent CM voltage sources, which were given by (19) and (20), of the *i*th rectifier and the *j*th inverter

$$V_{\text{rec\_}i} = \frac{1}{2}(V_{\text{UN\_}i} + V_{\text{VN\_}i}) \tag{19}$$

$$V_{\text{inv\_}j} = \frac{1}{3}(V_{\text{AN\_}j} + V_{\text{BN\_}j} + V_{\text{CN\_}j}). \tag{20}$$

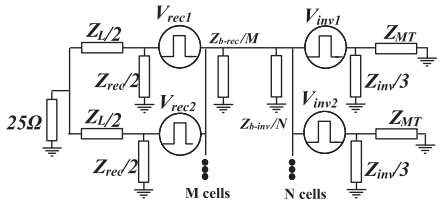
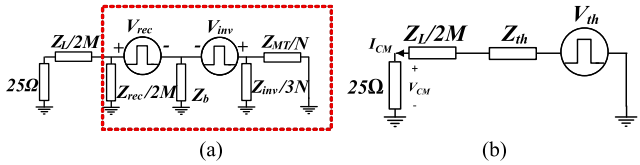


Fig. 31. Equivalent CM circuit of a generalized ac–dc–ac system with paralleled power modules.



(a) (b)

Fig. 32. (a) Reduced CM equivalent circuit. (b) Thevenin equivalent circuit.

In Fig. 32(a), $Z_b = (Z_{b-\text{rec}}/M)//Z_{b-\text{dc}}//(Z_{b-\text{inv}}/N)$. V_{rec} is the average of $V_{\text{rec}}s$ and V_{inv} is the average of all $V_{\text{inv}}s$. The equivalent source impedance Z_{th} and equivalent CM voltage source V_{th} are derived from (21) to (24). The CM current I_{CM} on LISNs is given by (25). The interactions between rectifiers and inverters, and the influence of rectifiers and inverters to input CM noise can be analyzed similarly. The CM voltage $V_{\text{LISN,Rec},N}$ on LISNs due to rectifiers with inverters connected and the CM noise voltage $V_{\text{LISN,Inv},N}$ on LISNs due to inverters with the rectifiers connected are given by (26) and (27). The contributions of rectifiers and inverters to CM noise can still be characterized by (14). The decoupling inductor and balance techniques can still apply

$$Z_{\text{th}} = \frac{Z_{\text{rec}}}{2M}//Z_b//\frac{Z_{\text{inv}}}{3N}//\frac{Z_{MT}}{N} \tag{21}$$

$$V_{\text{th}} = k_{\text{rec}}V_{\text{rec}} - k_{\text{inv}}V_{\text{inv}} \tag{22}$$

$$k_{\text{rec}} = \frac{\frac{Z_{\text{rec}}}{2M}}{\frac{Z_{\text{rec}}}{2M} + (Z_b//\frac{Z_{\text{inv}}}{3N}//\frac{Z_{\text{MT}}}{N})} \tag{23}$$

$$k_{\text{inv}} = \frac{\frac{Z_{\text{rec}}}{2M}//Z_b}{(\frac{Z_{\text{rec}}}{2M}//Z_b) + (\frac{Z_{\text{inv}}}{3N}//\frac{Z_{\text{MT}}}{N})} \tag{24}$$

$$I_{\text{CM}} = \frac{V_{\text{th}}}{Z_{\text{th}} + Z_L/(2M) + 25} \tag{25}$$

$$V_{\text{LISN,Rec},N} = \frac{25k_{\text{rec}}V_{\text{rec}}}{\frac{Z_L}{2M} + Z_{\text{th}} + 25} \tag{26}$$

$$V_{\text{LISN,Inv},N} = \frac{-25k_{\text{inv}}V_{\text{inv}}}{\frac{Z_L}{2M} + Z_{\text{th}} + 25}. \tag{27}$$

As discussed previously, the methodology developed in this paper for the ac–dc–ac systems with parallel power modules can be applied to the systems with similar topologies at different power levels. Different switching schemes will only change the waveforms of V_{rec} and V_{inv}, they do not change the developed model and EMI reduction technique. Different system layout, casing, shielding and grounding conditions only change the values of the parasitic impedances in the model, so the developed

EMI modeling, analysis and reduction techniques still hold. When $M = N = 1$, the technique developed in this paper applies to the single rectifier and inverter systems.

VI. Conclusion

In this article, the CM noise model of an ac–dc–ac system with paralleled power modules is developed. Based on the developed noise model, the influence of CM impedances on input CM noise is analyzed. The interactions between inverters and rectifiers are investigated. The contributions of rectifiers and inverters to input CM noise are analyzed. The decoupling inductor and Wheatstone bridge balance techniques were explored and the CM noise can be largely attenuated. Experimental results verified the proposed techniques.

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