Analysis and Improvement of Capacitance Effects in 360–800 Hz Variable On-Time Controlled CRM Boost PFC Converters

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***Abstract*—In critical conduction mode (CRM) boost power factor correction (PFC) converters, the input filter capacitor (IFC) is used to limit the propagation of switching noise into the ac line and the inherently existing parasitic capacitance of power semiconductor devices resonates with the boost inductor to achieve soft switching, which is voltage dependent and nonlinear. However, IFC leads to the crossover distortion of the rectified input voltage and thus the zero-crossing distortion of input current, which is ignored at the utility line frequency (50–60 Hz) since the effect of IFC is relatively small in this case. However, for wide variable frequency (360–800 Hz) power system, the effect of IFC becomes severe and unnegligible, which causes the deterioration of input current total harmonics distortion (THD). Besides, the nonlinearity of the parasitic capacitance is ignored and an equivalent constant linear capacitance is used in existing variable on-time (VOT) controls, which will cause the inaccuracy of VOT control, and thus, exacerbates the input current distortion. In order to improve the input current THD at high line frequency, this article proposes the IFC compensation method to minimize the effect of IFC and a variable parameter control is also achieved to suppress the effect of nonlinear parasitic capacitance. The experimental results of an 115-Vac-input 160-W/270-Vdc-output CRM boost PFC prototype are presented to verify the effectiveness and advantages of the proposed VOT methods. With the proposed methods, the input current THD is only 2.04% at 360 Hz input with full load and 3.14% at 800 Hz input with full load.**

***Index Terms*—Critical conduction mode (CRM) boost power factor corrector (PFC) converter, input filter capacitor (IFC) current compensation, total harmonics distortion (THD), variable on-time (VOT), variable parameter control.**

I. Introduction

DUE to the characteristics of zero-voltage switching (ZVS) or valley switching for the power switch and zero-current switching for the diode, critical conduction mode (CRM) boost power factor corrector (PFC) converter is prevalent in low-to-medium power condition [1]–[7], as shown in Fig. 1. In the CRM boost PFC converter, the input filter capacitor (IFC), $C_{\rm in}$ is required to limit the propagation of the switching noise into the ac line, which locates between the rectifier and the boost converter [8]–[11]. Besides, the parasitic capacitance ($C_{\rm oss}$ or $C_{\rm dp}$) is inherently existent in the power semiconductor device and is usually nonlinear and voltage dependent, which resonates with the boost inductor to achieve soft switching in CRM boost PFC converters [12]–[21]. However, the existence of these two capacitances leads to the distortion of input current, especially at high line frequency and light load.

The current flowing through the IFC, i_C, leads to the crossover distortion of the rectified input voltage and thus the zero-crossing distortion of input current due to the unidirectional conductivity of the diodes in the rectifier [8]–[11], as shown in Fig. 2(a). Moreover, at the utility line frequency (50–60 Hz), the IFC current is relatively small and will not cause obvious distortion, in which case, the effect of IFC is usually ignored. However, as line frequency increases and output power decreases, the effect

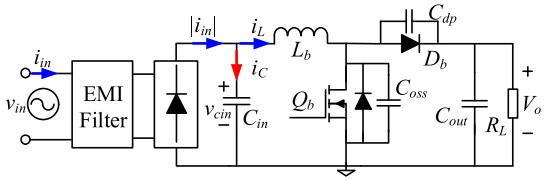

Fig. 1. Circuit diagram of the boost PFC converter.

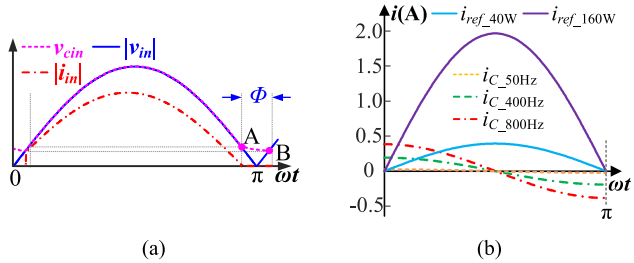

Fig. 2. Effect of IFC. (a) Crossover distortion of rectified input voltage $v_{\rm cin}$ and input current $i_{\rm in}$. (b) Waveforms of IFC current i_C at different line frequency.

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of IFC results in severer input current distortion and thus the deterioration of input current power factor (PF) and total harmonics distortion (THD) [8], which is shown in Fig. 2(b). Therefore, for wide variable frequency (360–800 Hz) single-phase ac system, such as in-seat power supply [7], whose output power ranges from tens of watts to several hundred watts, the effect of IFC is pronounced and unnegligible, especially at light load, and thus, efforts should be made to alleviate the effect of IFC.

On the other hand, in existing variable on-time (VOT) controls, which are implemented to improve the input current distortion caused by the soft-switching process, the nonlinearity of parasitic capacitance of power switches is ignored and an equivalent constant capacitance is used [12]–[21]. Since VOT is the function of parasitic capacitance, ignoring the nonlinearity of parasitic capacitance results in the inaccuracy of VOT and thus the deterioration of input current THD, which may further dissatisfy the high requirements of power quality in the high line frequency power system.

In this article, the effect of nonlinear parasitic capacitance and the IFC on the rectified input voltage and input current distortion is discussed in detail. In order to improve the input current THD at high line frequency, the compensation method for IFC current is proposed and variable parameter control is also achieved to reduce the effect of nonlinear parasitic capacitance. The effectiveness and advantages of the proposed methods are verified by an 115-Vac-input 160-W/270-Vdc-output CRM boost PFC prototype.

II. Capacitance Effects on Input Current Distortion With VOT Control

First, some definitions are made as follows: in Fig. 1, L_b and $C_{\rm in}$ are, respectively, boost inductor and IFC. Q_b is the power switch and $C_{\rm oss}$ is the output junction capacitance of Q_b. D_b is the diode and $C_{\rm dp}$ is the parasitic capacitance of D_b. $C_{\rm out}$ and R_L are, respectively, output capacitor and load. $v_{\rm in}$ and $i_{\rm in}$ are input voltage and input current. $v_{\rm cin}$ and V_o are the rectified input voltage and output voltage. i_L and i_C are inductor current and the current through $C_{\rm in}$ (IFC current).

In order to suppress the effect of resonant processes of L_b, $C_{\rm oss}$ and $C_{\rm dp}$ and obtain sinusoidal average inductor current, the generalized explicit VOT expression is established in [8], as follows:

$$T_{\rm on}(t)=\frac{2\sqrt{L_bC_{\rm eq}}V_o}{v_{\rm in}(t)}+\frac{2L_bP_o}{U_{\rm rms}^2}-2.2\sqrt{L_bC_{\rm eq}} \quad (1)$$

where $U_{\rm rms}$ and P_o are the rms value of input voltage and the output power, respectively, and $C_{\rm eq}=C_{\rm oss}+C_{\rm dp}$.

A. Average Inductor Current Distortion Caused by Nonlinear C_{eq}

The parasitic capacitances of power switches Q_b and D_b ($C_{\rm oss}$ and $C_{\rm dp}$) are nonlinear and dependent on the operation voltage, which can be obtained from the datasheets of the power switches, as shown in Fig. 3. (Detailed explanation is given in Appendix A.) Nonlinear $C_{\rm eq}$ shows a steep variance when the voltage between drain and source $v_{\rm ds}$ varies from several hundred volts to zero, especially when $v_{\rm ds}<V_T$ (V_T represents the operation voltage where parasitic capacitance varies steeply). In previous analysis [12]–[21], an equivalent constant $C_{\rm eq}$ is used and the nonlinearity of $C_{\rm eq}$ is ignored, which results in the inaccuracy of $T_{\rm on}$ and the distortion of $i_{\rm Lavg}$, and, therefore, the distortion of $i_{\rm in}$.

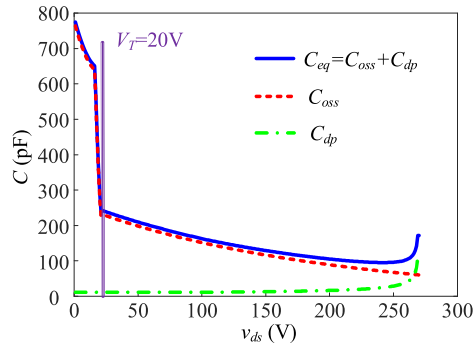

Fig. 3. Capacitance–$v_{\rm ds}$ curves.

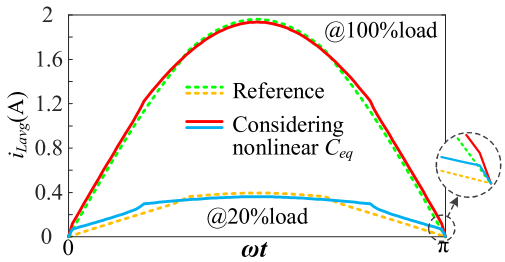

Fig. 4. Waveforms of $i_{\rm Lavg}$ during half-line cycle at 20% or 100% load with nonlinear $C_{\rm eq}$.

Fig. 4 shows the waveforms of $i_{\rm Lavg}$ during half-line cycle at 20% or 100% load with nonlinear $C_{\rm eq}$ in Fig. 3 (calculating circuit parameters: $L_b=100\,\mu$H, $U_{\rm rms}=115$ V, $P_{o\max}=160$ W, and $V_o=270$ Vdc). In Fig. 4, solid line represents $i_{\rm Lavg}$ when considering nonlinear $C_{\rm eq}$ while dash line represents reference of sinusoidal $i_{\rm Lavg}$. It is noted that $i_{\rm Lavg}$ is calculated by operation analysis [21] with $T_{\rm on}$ in (1). From Fig. 4, when the nonlinearity of $C_{\rm eq}$ is considered, $i_{\rm Lavg}$ shows a severe distortion, especially at light load. $i_{\rm Lavg}$ is larger at ZVS mode, which means that $i_{\rm Lavg}$ is overcompensated with conventional $T_{\rm on}$ in (1).

In order to further explain the effect of nonlinear $C_{\rm eq}$, Fig. 5 calculates $T_{\rm on}$ by the iterative algorithm in [21], which is desired to achieve sinusoidal input current, whether considering nonlinear $C_{\rm eq}$ or not in the analysis at 20% or 100% load. In Fig. 5, dash line represents desired $T_{\rm on2}$ when considering nonlinear $C_{\rm eq}$ while solid line represents $T_{\rm on1}$ when ignoring nonlinear $C_{\rm eq}$ and dot-dashed line represents the difference $\Delta T_{\rm on}$ between $T_{\rm on1}$ and $T_{\rm on2}$ which denotes the degree of overcompensation. From Fig. 5, $T_{\rm on2}$ is smaller than $T_{\rm on1}$, which means that $i_{\rm Lavg}$ is actually overcompensated with conventional $T_{\rm on1}$; therefore, the distortion of $i_{\rm Lavg}$ occurs. It is obvious that $T_{\rm on1}$ introduces a severe overcompensation around the zero crossing of input voltage, while approximately equals to $T_{\rm on2}$ near the peak input

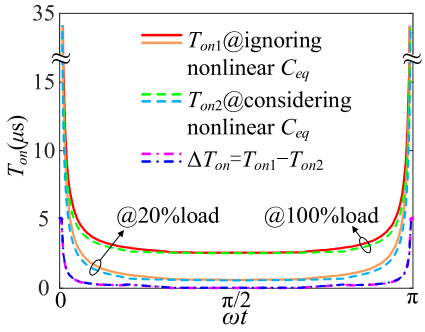

Fig. 5. Desired on-time $T_{\rm on}$ when considering or ignoring nonlinear $C_{\rm eq}$ at 20% or 100% load.

voltage. Besides, under different load conditions, $\Delta T_{\rm on}$ is almost the same since nonlinear $C_{\rm eq}$ mainly influences two resonant processes, especially the reverse resonant process, which is irrelevant to the load condition.

B. Crossover Distortion Caused by IFC

As shown in Fig. 2, due to the effect of IFC current, $v_{\rm cin}$ deviates from $|v_{\rm in}|$ at Point A and converges with $|v_{\rm in}|$ at Point B (the diode forward voltage of the rectifier is ignored). Define the dead angle between A and B as Φ. During Φ, the rectifier blocks since $v_{\rm cin} > |v_{\rm in}|$ and $|i_{\rm in}| = 0$; otherwise, the rectifier conducts and $v_{\rm cin} = |v_{\rm in}|$.

Considering the effect of IFC current, the total input current $|i_{\rm in}|$ is the sum of $i_{\rm Lavg}$ and i_C

$$|i_{\rm in}(t)| = i_{\rm Lavg}(t) + i_C(t). \tag{2}$$

If $v_{\rm in}(t) = \sqrt{2}U_{\rm rms}\sin(\omega t)$, i_C can be expressed as follows:

$$i_C(t) = C_{\rm in}\frac{dv_{\rm cin}}{dt} = \begin{cases} \sqrt{2}\omega U_{\rm rms}C_{\rm in}\cos(\omega t), & v_{\rm cin}(t) = |v_{\rm in}(t)| \\ -i_{\rm Lavg}(t), & v_{\rm cin}(t) > |v_{\rm in}(t)| \end{cases} \tag{3}$$

where $\omega = 2\pi f_{\rm line}$ is the line angular frequency and $f_{\rm line}$ is the line frequency.

The input voltage sampling is needed to implement VOT control with the explicit VOT expression. Usually, the input voltage can be sampled before or after the rectifier, that is sampling $v_{\rm in}$ or $v_{\rm cin}$. According to (3), when $v_{\rm cin} > |v_{\rm in}|$, $i_{\rm Lavg} = -i_C = -C_{\rm in}dv_{\rm cin}/dt$; thus, $v_{\rm cin}$ during Φ is related to $i_{\rm Lavg}$ and the larger the $i_{\rm Lavg}$, the faster the $v_{\rm cin}$ decreases. In other words, $v_{\rm cin}$ during Φ is related to $T_{\rm on}$ and is sensible to the sampling methods since $T_{\rm on}$ during Φ is different with different sampling methods.

The calculating process of $v_{\rm cin}$ during Φ with different sampling methods is shown in Fig. 6. It is noted that the only difference during the calculating process of $v_{\rm cin}$ under two different sampling methods is the calculated $T_{\rm on}$. According to the calculating process, Fig. 7 shows the waveforms of $v_{\rm cin}$, $|i_{\rm in}|$, $i_{\rm Lavg}$, and i_C with different sampling methods (calculating circuit parameters: $L_b = 100\,\mu$H, $U_{\rm rms} = 115$ V, $P_o = 40$ W, $V_o = 270$ Vdc, $C_{\rm in} = 470$ nF, $f_{\rm line} = 400$ Hz). In Fig. 7, $v_{\rm cin}$ starts deviating from $|v_{\rm in}|$ at Point A and $|i_{\rm in}| = i_{\rm Lavg} + i_C = 0$ during

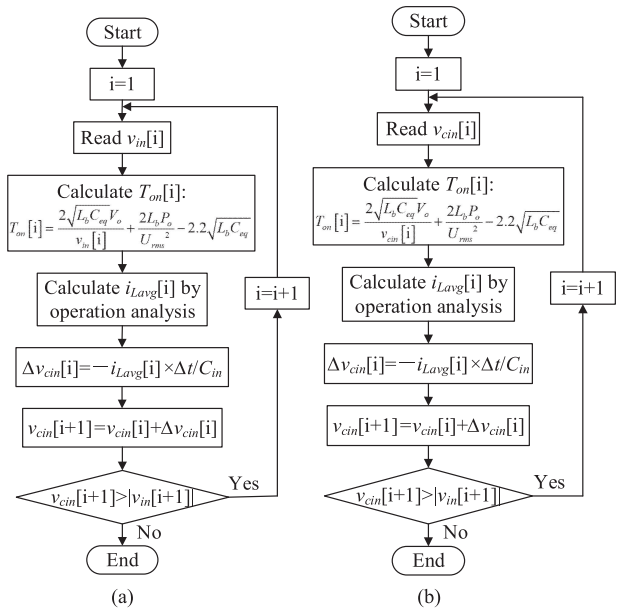

Fig. 6. Calculating process of $v_{\rm cin}$ during Φ with different sampling methods. (a) Sampling before the rectifier (sampling $v_{\rm in}$). (b) Sampling after the rectifier (sampling $v_{\rm cin}$).

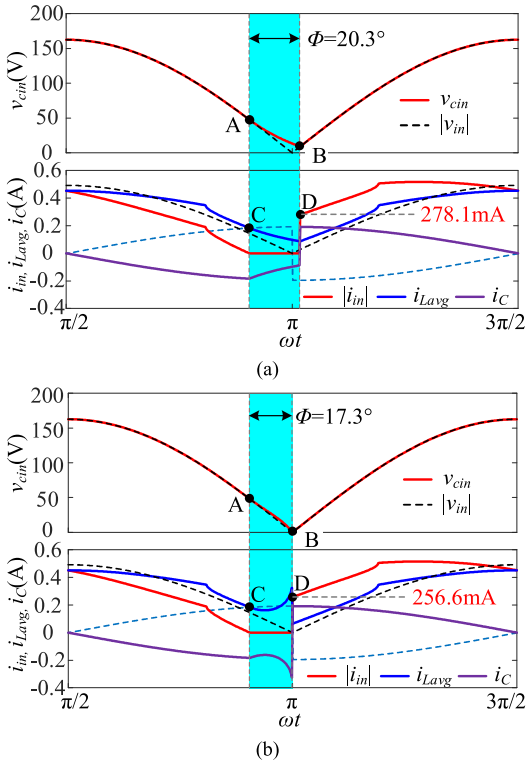

Fig. 7. Waveforms of $v_{\rm cin}$, $|i_{\rm in}|$, $i_{\rm Lavg}$, and i_C with different sampling methods. (a) Sampling after the rectifier. (b) Sampling before the rectifier.

the dead angle Φ, which results in the zero-crossing distortion and phase leading of $i_{\rm in}$. Compared with sampling after the rectifier, sampling before the rectifier can achieve a smaller Φ (from 20.3° to 17.3°), and thus a lower $i_{\rm in}$ THD. This is because

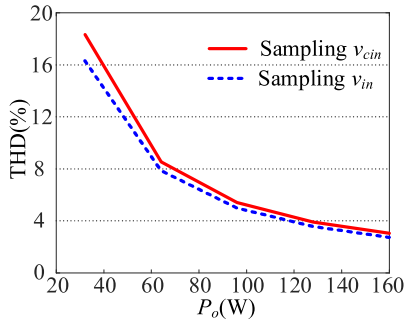

Fig. 8. Calculated $i_{\rm in}$ THD with different sampling methods at different loads.

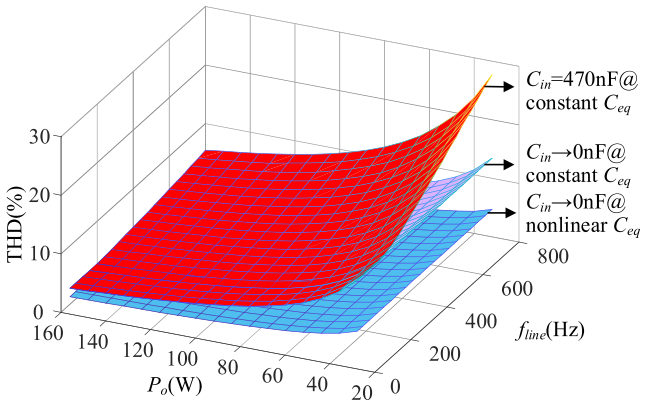

Fig. 9. Calculated $i_{\rm in}$ THD.

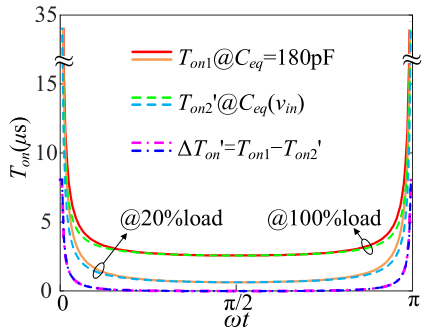

Fig. 10. Calculated $T_{\rm on}$ with or without $C_{\rm eq} = p|v_{\rm in}|+q$.

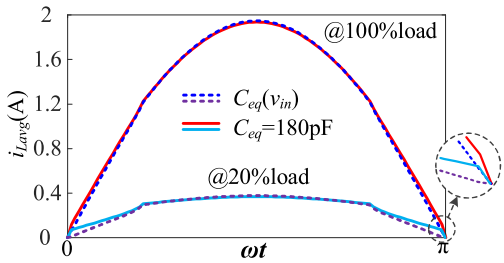

Fig. 11. Waveforms of $i_{\rm Lavg}$ at 20% or 100% load with constant $C_{\rm eq}$ and varying $C_{\rm eq}$ control when considering the effect of nonlinear $C_{\rm eq}$.

that, compared with sampling after the rectifier, the calculated $T_{\rm on}$ is larger and thus $i_{\rm Lavg}$ is larger during Φ when sampling before the rectifier, which makes $v_{\rm cin}$ decrease more quickly, accelerating the convergence of $v_{\rm cin}$ and $v_{\rm in}$. Besides, rectifier conducts suddenly at Point D and $i_{\rm in}$ increases rapidly, which will result in a severe spike of input current in actual experiments and thus deteriorate $i_{\rm in}$ THD. By comparison, sampling before the rectifier can obtain a smaller $i_{\rm in}$ at Point D and, thus, a smaller spike of input current in actual experiments and a lower $i_{\rm in}$ THD. Fig. 8 shows the calculated $i_{\rm in}$ THD with different sampling methods with above circuit parameters. From Fig. 8, with sampling before the rectifier (sampling $v_{\rm in}$), $i_{\rm in}$ THD is improved, especially at light load since the effect of IFC current becomes severer and thus Φ is larger at light load than that at full load.

Fig. 9 shows the $i_{\rm in}$ THD under different line frequency and different load condition when sampling before the rectifier and considering the nonlinearity of $C_{\rm eq}$ (calculating circuit parameters: $L_b = 100\,\mu$H, $U_{\rm rms} = 115$ V, $V_o = 270$ Vdc). In Fig. 9, $i_{\rm in}$ THD is deteriorated with constant $C_{\rm eq}$ and as P_o decreases, $i_{\rm in}$ THD increases, which is theoretically irrelevant to $f_{\rm line}$, if the effect of IFC is ignored ($C_{\rm in}$ is approximately equal to zero). When the effect of IFC is further considered, the deterioration of $i_{\rm in}$ THD becomes severer. Moreover, as $f_{\rm line}$ increases and P_o decreases, $i_{\rm in}$ THD increases. Thus, in order to improve the $i_{\rm in}$ THD under wide variable line frequency and light load condition, this article focuses on the compensation for the effect of IFC current and the nonlinear $C_{\rm eq}$.

III. Compensation Methods of Capacitance Effects

A. Varying C_{eq} Control

In order to improve the overcompensation of $i_{\rm Lavg}$ with $T_{\rm on}$ in (1) caused by nonlinear $C_{\rm eq}$, it is necessary to reduce $T_{\rm on}$, and as $|v_{\rm in}|$ increases, the reduction decreases. Obviously, it is difficult to establish the explicit expression of $T_{\rm on}$ with nonlinear $C_{\rm eq}$. Therefore, this article constructs a varying $C_{\rm eq}$ with $|v_{\rm in}|$ to compensate the distorted $i_{\rm Lavg}$. The varying $C_{\rm eq}$ must be smaller than the linear equivalent value (Equivalent linear value of parasitic capacitance is obtained by the linear charge-equivalent capacitance model which is illustrated and calculated in Appendix A) and as $|v_{\rm in}|$ increases, $C_{\rm eq}$ increases. For simple implementation, this article makes $C_{\rm eq}$ vary linearly with $|v_{\rm in}|$ as follows:

$$C_{\rm eq}\left(v_{\rm in}\right) = p\left|v_{\rm in}\right| + q \tag{4}$$

where p and q are the slope and intercept, respectively, and $C_{\rm eq}(v_{\rm in\_peak})$ is the linear equivalent value.

Fig. 10 shows the calculated $T_{\rm on}$ based on (1) with or without varying $C_{\rm eq}$ control. From Fig. 10, $T'_{\rm on2}$ is smaller than $T_{\rm on1}$ during entire half-line cycle and $\Delta T'_{\rm on}$ decreases as $|v_{\rm in}|$ increases. Fig. 11 calculates the waveforms of $i_{\rm Lavg}$ when considering the effect of nonlinear $C_{\rm eq}$ with $T_{\rm on1}$ and $T'_{\rm on2}$ in Fig. 10. The distortion of $i_{\rm Lavg}$ with varying $C_{\rm eq}$ control is improved, especially near the zero-crossing input voltage.

In order to obtain optimal p and q, making q varies from 0 pF to $C_{\rm eq}(v_{\rm in\_peak})$, and correspondingly, $p = (C_{\rm eq}(v_{\rm in\_peak}) - q)/v_{\rm in\_peak}$, calculate the input current THD with varying $C_{\rm eq}$ and find the optimal p and q where better input current THD can be obtained. It is noted that the expression of $T_{\rm on}$ in (1) is a

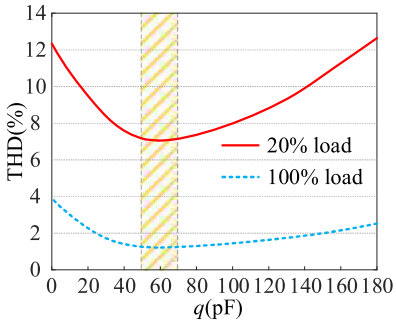

Fig. 12. Calculated $i_{\rm in}$ THD with different p and q.

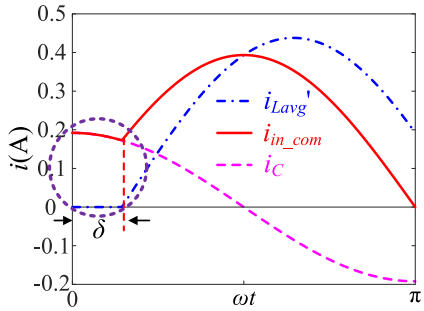

Fig. 13. Waveforms of $i_{\rm in\_com}$, $i'_{\rm Lavg}$, and i_C.

generalized expression suitable for CRM boost PFC converters to obtain sinusoidal input current, which is deduced by the iterative algorithm and numerical fitting method [8]. Fig. 12 gives the calculated input current THD with q from 0 to 180 pF (Calculating process is presented in Appendix A) under circuit parameters: $U_{\rm rms} = 115$ V, $V_o = 270$ Vdc, $P_{o\max} = 160$ W, and $L_b = 100\,\mu$H. It can be seen that $i_{\rm in}$ THD is improved as q decreases and p increases. However, if q continues to decrease, $T_{\rm on}$ is reduced too much near the zero-crossing input voltage and $i_{\rm Lavg}$ will be undercompensated, which will also result in the deterioration of $i_{\rm in}$ THD. In Fig. 12, when $q = 50$–70 pF, input current THD is lower and almost unchanged. Therefore, in order to compensate the effect of nonlinear $C_{\rm eq}$, $q = 50$–70 pF, and correspondingly, $p = 0.7993$–0.6764 pF/V can be adopted to obtain better input current THD.

B. Compensation for IFC Current

In order to compensate the effect of IFC and obtain sinusoidal and in-phase input current, $i_{\rm Lavg}$ in (1) should be corrected to $i'_{\rm Lavg}$ and $i'_{\rm Lavg}$ satisfies

$$|i_{\rm in}(t)| = i'_{\rm Lavg}(t) + i_C(t) = \frac{\sqrt{2}P_o}{U_{\rm rms}}\sin(\omega t). \tag{5}$$

Therefore, $i'_{\rm Lavg}$ can be expressed as follows:

$$i'_{\rm Lavg}(t) = \frac{\sqrt{2}P_o}{U_{\rm rms}}\sin(\omega t) - \sqrt{2}\omega U_{\rm rms}C_{\rm in}\cos(\omega t). \tag{6}$$

Fig. 13 shows the waveforms of compensated $i_{\rm in}$ and corrected $i_{\rm Lavg}$. Obviously, for the unidirectional characteristics of diodes, $i'_{\rm Lavg}$ cannot be negative and will be clamped to zero during δ, which means that the effect of IFC current can hardly be compensated totally. δ can be expressed as follows:

$$\delta = \arctan\left(\frac{\omega U_{\rm rms}^2 C_{\rm in}}{P_o}\right). \tag{7}$$

According to (7), as $f_{\rm line}$, $C_{\rm in}$ increases and P_o decreases, δ increases, which will also result in the distortion of $i_{\rm in}$. Therefore, it can be concluded that without IFC current compensation or compensating i_C will cause the distortion of $i_{\rm in}$, even the deterioration of $i_{\rm in}$ THD. Since the effect of IFC current can hardly be compensated totally, it can only be minimized. Theoretical analysis reveals that less compensation for IFC current can achieve better $i_{\rm in}$ THD. Once the prototype is determined, $C_{\rm in}$ is determined. The capacitance of compensation for IFC current is decided by the researchers. Define the compensated IFC current as $i_{\rm com}$ and $i_{\rm com}$ can be expressed as follows:

$$i_{\rm com}(t) = \sqrt{2}\omega U_{\rm rms}C_{\rm com}\cos(\omega t) \tag{8}$$

where $C_{\rm com}$ represents the compensated IFC.

In this case, $i'_{\rm Lavg}$ is corrected and $T_{\rm on}$ with IFC current compensation can be expressed as follows:

$$i'_{\rm Lavg}(t) = \frac{\sqrt{2}P_o}{U_{\rm rms}}\sin(\omega t) - i_{\rm com}(t) \tag{9}$$

$$T_{\rm on} = \frac{2\sqrt{L_bC_{\rm eq}}V_o}{v_{\rm in}} - 2.2\sqrt{L_bC_{\rm eq}} + \frac{2L_bP_o}{U_{\rm rms}^2} - \frac{2L_b}{v_{\rm in}}i_{\rm com}. \tag{10}$$

Ideally, $|i_{\rm in}|$ with IFC current compensation is supposed to be

$$|i_{\rm in}(t)| = i'_{\rm Lavg}(t) + i_C(t) = \begin{cases} A\cos(\omega t) & 0 < \omega t < \delta' \\ C\sin(\omega t) + B\cos(\omega t) & \delta' < \omega t < \pi - \Phi' \\ 0 & \pi - \Phi' < \omega t < \pi \end{cases} \tag{11}$$

where

$$A = \sqrt{2}U_{\rm rms}\omega C_{\rm in} \tag{12}$$

$$B = \sqrt{2}U_{\rm rms}\omega(C_{\rm in} - C_{\rm com}) \tag{13}$$

$$C = \frac{\sqrt{2}P_o}{U_{\rm rms}} \tag{14}$$

$$\delta' = \arctan\left(\frac{\omega U_{\rm rms}^2 C_{\rm com}}{P_o}\right) \tag{15}$$

$$\Phi' = \arctan\left(\frac{\omega U_{\rm rms}^2(C_{\rm in} - C_{\rm com})}{P_o}\right). \tag{16}$$

As $C_{\rm com}$ increases, δ' increases and Φ' decreases, which can also be seen in Fig. 14. In other words, as $C_{\rm com}$ increases, the effect of IFC current is reduced. However, $i_{\rm in}$ distortion derived from the IFC current compensation is deteriorated. Therefore, there exists an optimal $C_{\rm com}$ where the effect of $C_{\rm in}$ is reduced

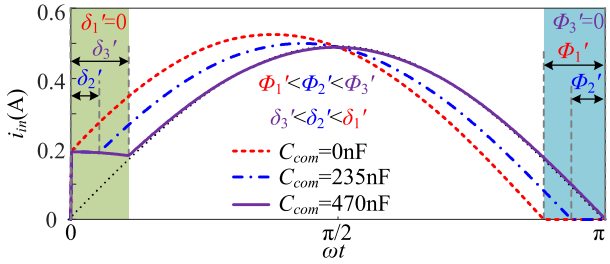

Fig. 14. Waveforms of $i_{\rm in}$ with different $C_{\rm com}$.

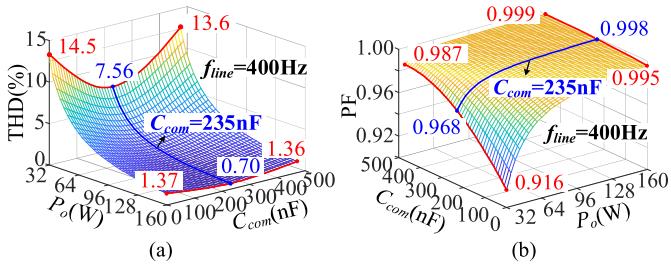

Fig. 15. $i_{\rm in}$ THD and PF with different $C_{\rm com}$ at 400 Hz. (a) THD. (b) PF.

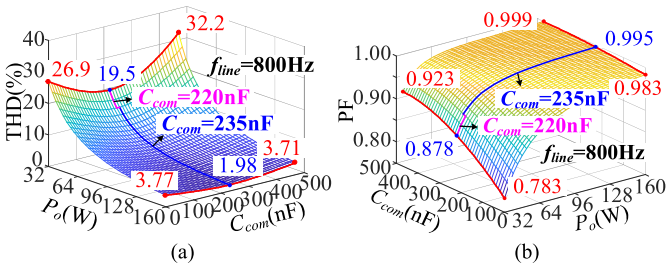

Fig. 16. $i_{\rm in}$ THD and PF with different $C_{\rm com}$ at 800 Hz. (a) THD. (b) PF.

while input current distortion derived from IFC current compensation is minor; therefore, lower input current THD can be obtained.

Based on (11), calculate the rms value $I_{\rm rms}$ and the fundamental component I_1 of $|i_{\rm in}|$ by Fourier Series Expansion, as shown in (17), (18), (21)–(23)

$$|i_{\rm in}(t)| = \frac{a_0}{2} + \sum_{k=1}^{\infty}\left(a_k\cos(k\omega t) + b_k\sin(k\omega t)\right) \tag{17}$$

$$I_1 = \sqrt{\frac{a_1^2+b_1^2}{2}} \tag{18}$$

where a_0, a_k, and b_k are coefficients.

According to (21)–(24) shown at the bottom of this page, THD and PF can be calculated as follows:

$$\text{THD} = \sqrt{\frac{I_{\rm rms}^2 - I_1^2}{I_1^2}} \tag{19}$$

$$\text{PF} = \frac{P_{\rm in}}{I_{\rm rms}U_{\rm rms}}. \tag{20}$$

Figs. 15 and 16 show the $i_{\rm in}$ THD and PF at 400/800 Hz with different $C_{\rm com}$. It can be seen that as $C_{\rm com}$ increases, THD decreases first and then increases while PF increases all the time with a certain P_o. At 800 Hz, when $C_{\rm com} = 470$ nF, $i_{\rm in}$ THD is deteriorated even with IFC current compensation. However, with about 235 nF compensation, lower $i_{\rm in}$ THD can be obtained, in which case, PF is still improved and acceptable although PF improvement is sacrificed marginally.

However, the expression of $i_{\rm in}$ THD is complicated and contains many complex operations and variables. Therefore, it is of great difficulty to find the explicit expression of optimal $C_{\rm com}$. On the other hand, in Figs. 15 and 16, optimal $C_{\rm com}$ is within 220–235 nF under different $f_{\rm line}$ and P_o when $C_{\rm in} = 470$ nF, which means that optimal $C_{\rm com}$ is about

$$I_{\rm rms} = \sqrt{\frac{1}{T}\int_0^T i_{\rm in}(t)^2dt} = \sqrt{\frac{1}{\pi}\left(\begin{array}{r} A^2\left(\frac{\sin(2\delta')}{4}+\frac{\delta'}{2}\right)+B^2\left(\frac{\pi-\delta'-\Phi'}{2}-\frac{\sin(2\delta')}{4}-\frac{\sin(2\Phi')}{4}\right) \\ +C^2\left(\frac{\pi-\delta'-\Phi'}{2}+\frac{\sin(2\delta')}{4}+\frac{\sin(2\Phi')}{4}\right)+BC\left(\frac{\cos(2\delta')}{2}-\frac{\cos(2\Phi')}{2}\right)\end{array}\right)} \tag{21}$$

$$a_1 = \frac{2}{T}\int_0^T i_{\rm in}(t)\cos(\omega t)\,dt = \frac{1}{\pi}\left(A\left(\frac{\sin(2\delta')}{2}+\delta'\right)+B\left(\pi-\delta'-\Phi'-\frac{\sin(2\delta')}{2}-\frac{\sin(2\Phi')}{2}\right)\right.$$
$$\left.+C\left(\frac{\cos(2\delta')}{2}-\frac{\cos(2\Phi')}{2}\right)\right) \tag{22}$$

$$b_1 = \frac{2}{T}\int_0^T i_{\rm in}(t)\sin(\omega t)\,dt = \frac{1}{\pi}\left(A\left(\frac{1-\cos(2\delta')}{2}\right)+B\left(\frac{\cos(2\delta')-\cos(2\Phi')}{2}\right)\right.$$
$$\left.+C\left(\pi-\delta'-\Phi'+\frac{\sin(2\delta')}{2}+\frac{\sin(2\Phi')}{2}\right)\right) \tag{23}$$

$$P_{\rm in} = \frac{1}{T}\int_0^T i_{\rm in}(t)\,v_{\rm in}(t)\,dt = \frac{\sqrt{2}U_{\rm rms}}{\pi}\left(A\left(\frac{1-\cos(2\delta')}{4}\right)+B\left(\frac{\cos(2\delta')-\cos(2\Phi')}{4}\right)\right.$$
$$\left.+C\left(\frac{\pi-\delta'-\Phi'}{2}+\frac{\sin(2\delta')}{4}+\frac{\sin(2\Phi')}{4}\right)\right) \tag{24}$$

TABLE I
OPTIMAL $C_{\rm com}$ UNDER DIFFERENT $C_{\rm in}$

C_{in}	Optimal C_{com}	$(C_{com}/C_{in})\times 100\%$
100 nF	50 nF	50%
200 nF	100 nF	50%
300 nF	150 nF	50%
400 nF	190-200 nF	47.5%-50%
470 nF	220-235 nF	46.8%-50%
600 nF	270-300 nF	45%-50%

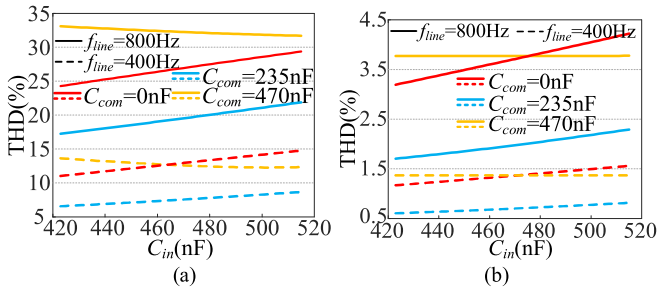

Fig. 17. $i_{\rm in}$ THD with $\pm 10\%$ $C_{\rm in}$ tolerance. (a) At 20% load. (b) At 100% load.

50%$C_{\rm in}$. The largest deviation of optimal $C_{\rm com}$ (220 nF) from 50%$C_{\rm in}$ (235 nF) appears at 800 Hz and light load, in which input current THD increases from 19.50% ($C_{\rm com}$ = 220 nF) to 19.54% ($C_{\rm com}$ = 235 nF). That is, the maximum sacrifice of input current THD is 0.04% within entire input and output range, when $C_{\rm com}$ = 50%$C_{\rm in}$ is adopted. Table I shows the optimal $C_{\rm com}$ under different $C_{\rm in}$ with the same analysis process, as shown in Figs. 15 and 16. The same conclusion can be obtained that the optimal $C_{\rm com}$ is about 50%$C_{\rm in}$ and the largest deviation of optimal $C_{\rm com}$ from 50%$C_{\rm in}$ appears at 800 Hz and light load. The maximum sacrifice of input current THD with $C_{\rm com}$ = 50%$C_{\rm in}$ is only 0.03% when $C_{\rm in}$ = 400 nF and 0.14% when $C_{\rm in}$ = 600 nF, compared with optimal $C_{\rm com}$. Therefore, it can be induced that optimal $C_{\rm com}$ is around 50%$C_{\rm in}$.

According to the aforementioned analysis, the proposed IFC current compensation is dependent on the $C_{\rm in}$ value. Unfortunately, the $C_{\rm in}$ value exists tolerance which is usually within $\pm 10\%$. Theoretically, the tolerance of $C_{\rm in}$ deteriorates the accuracy of the proposed IFC compensation. Fig. 17 shows the input current THD with $\pm 10\%$ $C_{\rm in}$ tolerance when $C_{\rm com}$ = 0 nF, 235 nF, and 470 nF with circuit parameters: $U_{\rm rms}$ = 115 V, V_o = 270 Vdc, $P_{\rm omax}$ = 160 W, L_b = 100 μH, and $C_{\rm in}$ = 470 nF. It can be seen that even with $\pm 10\%$ $C_{\rm in}$ tolerance, the input current THD is still lower when $C_{\rm com}$ = 235 nF compared with that when $C_{\rm com}$ = 0 nF or $C_{\rm com}$ = 470 nF.

IV. IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

A. Implementation of the Proposed Methods

To verify the effectiveness of the proposed VOT methods, a 115-Vac 160-W/270-Vdc CRM boost PFC prototype has been built. Circuit parameters of the experimental prototype are shown in Table II. Fig. 18 gives the control diagram for the implementation of the proposed VOT methods and the photograph of the experimental prototype is given in Fig. 19. The input voltage is sampled before the rectifier, which only needs to add an operational amplifier and a dc voltage reference to make the sampling voltage of $v_{\rm in}$ positive during the entire line cycle when compared with sampling after the rectifier. The eCAP module is used to capture the zero-crossing point of $v_{\rm in}$ and the timer provides the query clock signal. The compensation for IFC current is obtained by cosine lookup table. $T_{\rm on}$ is calculated by (1) or (10). In (1) or (10), P_o and $U_{\rm rms}$ both kept unchanged during the entire half-line cycle when PFC is in the steady state. Therefore, the constant term $2L_bP_o/U_{\rm rms}^2$

TABLE II
CIRCUIT PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

AC Input Voltage v_{in}	115 VAC
Output Voltage V_o	270 VDC
Max Output Power P_{omax}	160 W
Line frequency f_{line}	360-800 Hz
Input Filter Capacitor C_{in}	470 nF
Boost Inductance L_b	100 μH
Power Switch Q_b	TPH3206PS
Boost Diode D_b	C3D02060A
Equivalent linear value of C_{eq}	180 pF
Output Capacitor C_{out}	180 μF/ 450 V
MCU	TMS320F28335

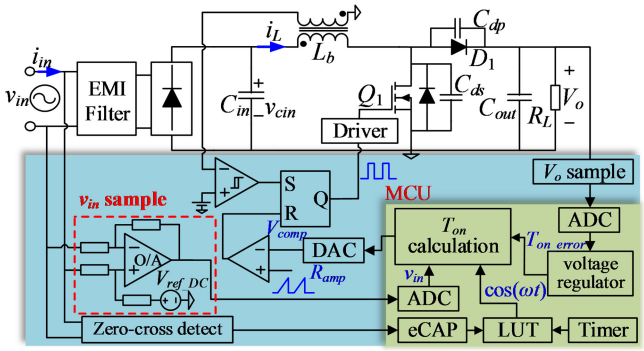

Fig. 18. Control diagram for the proposed methods.

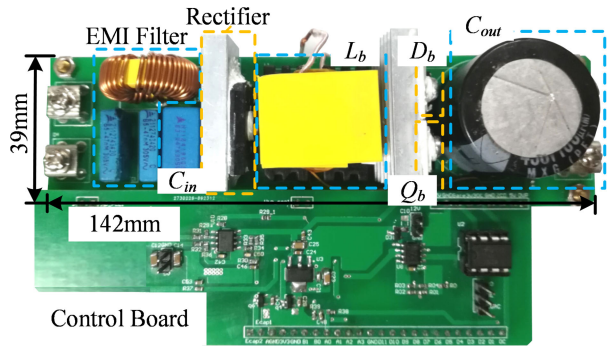

Fig. 19. Experimental CRM boost PFC prototype.

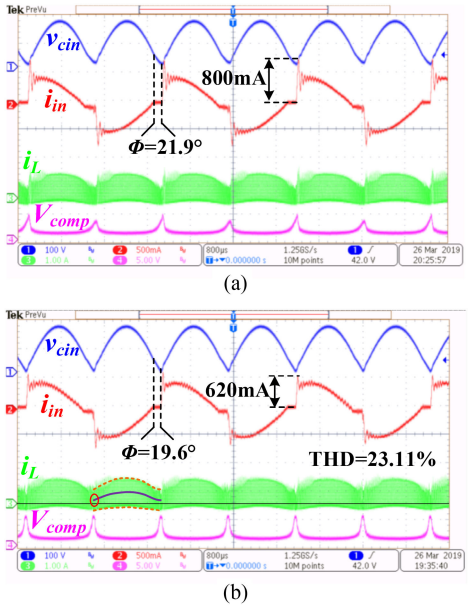

Fig. 20. Waveforms with different sampling methods at 400 Hz with 20% load. (a) Sampling after the rectifier. (b) Sampling before the rectifier.

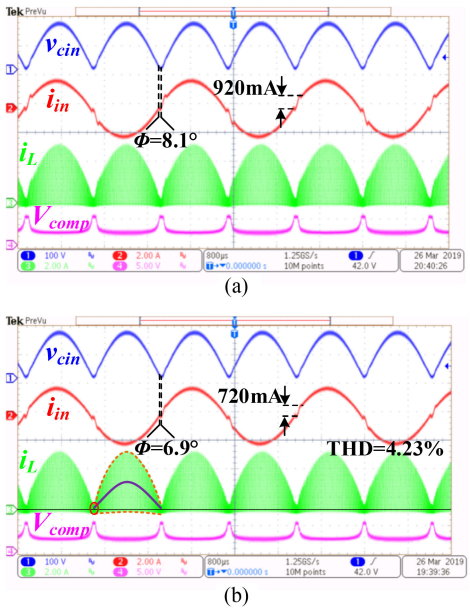

Fig. 21. Waveforms with different sampling methods at 400 Hz with full load. (a) Sampling after the rectifier. (b) Sampling before the rectifier.

can be provided directly and adjusted adaptively by the output of the voltage regulator $T_{\text{on\_error}}$, which is also almost constant since the bandwidth of voltage feedback loop of PFC is narrow. Calculated T_{on} and a D/A conversion generate the modulation signal V_{comp}. V_{comp} intersects with the ramp signal R_{amp} and proportionally controls T_{on}.

B. Experimental Results

Figs. 20 and 21 show the waveforms of v_{cin}, i_{in}, i_L and V_{comp} with different sampling methods at 400 Hz with 20%/full load. It is obvious that with sampling before the rectifier,

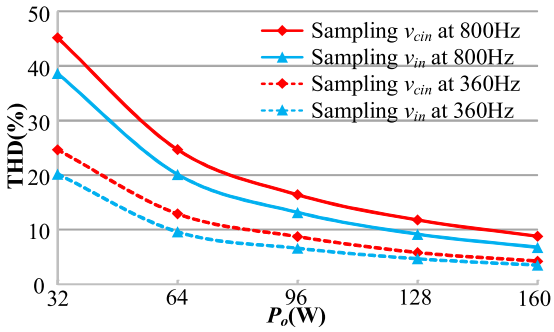

Fig. 22. Measured input current THD with different sampling methods at 360/800 Hz within entire load range.

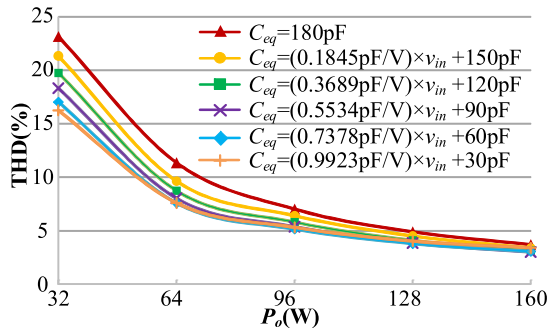

Fig. 23. Measured input current THD with different p and q.

minor Φ and smaller input current spike can be obtained. Fig. 22 gives the measured i_{in} THD with different sampling methods at 360/800 Hz within the entire load range. It can be seen that sampling before the rectifier can achieve a lower i_{in} THD with little sacrifice of circuit complexity and thus this article adopts sampling before the rectifier.

Based on the sampling before the rectifier, varying C_{eq} control is implemented to reduce the effect of nonlinear parasitic capacitance. Fig. 23 shows the measured i_{in} THD with several different p and q at 400 Hz. From Fig. 23, as p increases, the lower i_{in} THD can be obtained. However, the i_{in} THD deteriorates when q decreases to 30 pF. Thus, $C_{\text{eq}} = (0.7378\text{ pF/V}) \times v_{\text{in}} + 60\text{ pF}$ is finally selected to improve i_{in} THD in this article.

With optimal varying C_{eq}, Fig. 24 shows the waveforms of v_{cin}, i_{in}, i_L and V_{comp} at 400 Hz with 20%/full load. Compared with Figs. 20(b) and 21(b), the input current spike can be diminished with varying C_{eq} control and near the zero-crossing input voltage, i_L is obviously reduced. Although reduced i_L results in early deviation of v_{cin} and v_{in} and thus a larger Φ, varying C_{eq} control improves the distortion of i_{Lavg}. Fig. 25 further gives the measured i_{in} THD with or without varying C_{eq} control at 360/800 Hz within the entire load range. With varying C_{eq} control, i_{in} THD can be improved to 13.75% at 360 Hz and to 34.11% at 800 Hz with 20% load while i_{in} THD is reduced to 2.77% at 360 Hz and to 6.25% at 800 Hz with full load.

Based on sampling before the rectifier and the varying C_{eq} control above, in order to further improve the i_{in} THD at high line frequency, IFC compensation is implemented. Experimental waveforms with or without IFC compensation at 400 Hz with 20%/full load are shown in Figs. 26 and 27. With IFC

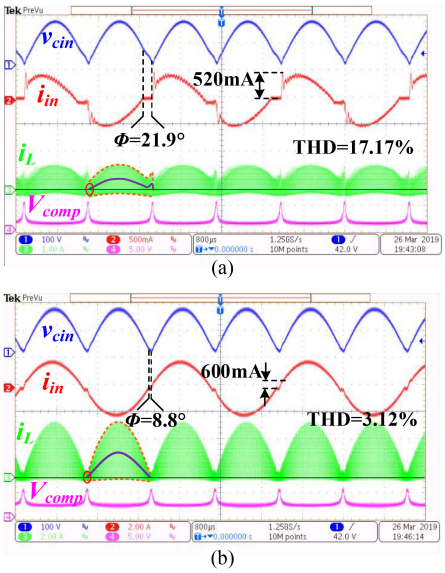

Fig. 24. Waveforms with optimal varying C_{eq} at 400 Hz. (a) 20% load. (b) Full load.

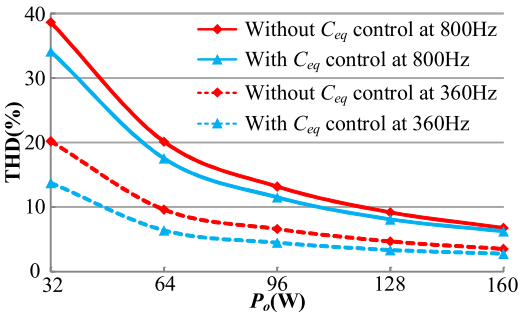

Fig. 25. Measured input current THD comparison at 360/800 Hz.

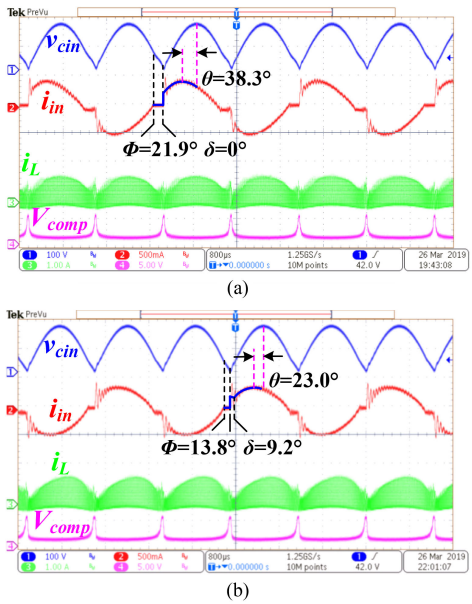

Fig. 26. Waveforms at 400 Hz with 20% load. (a) Without IFC compensation. (b) With IFC compensation ($C_{\text{com}} = 235$ nF).

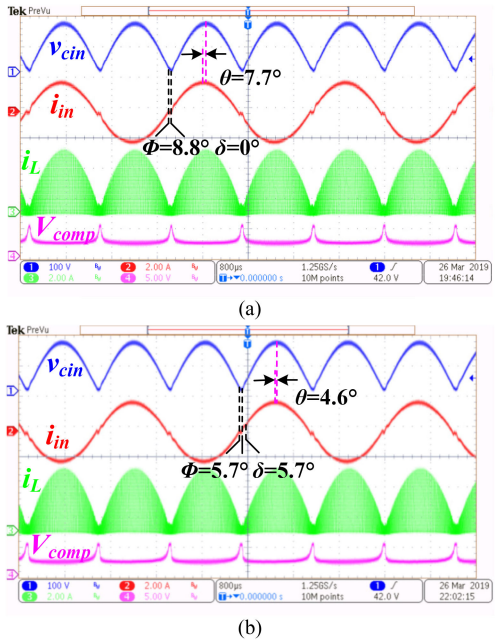

Fig. 27. Waveforms at 400 Hz with full load. (a) Without IFC compensation. (b) With IFC compensation ($C_{\text{com}} = 235$ nF).

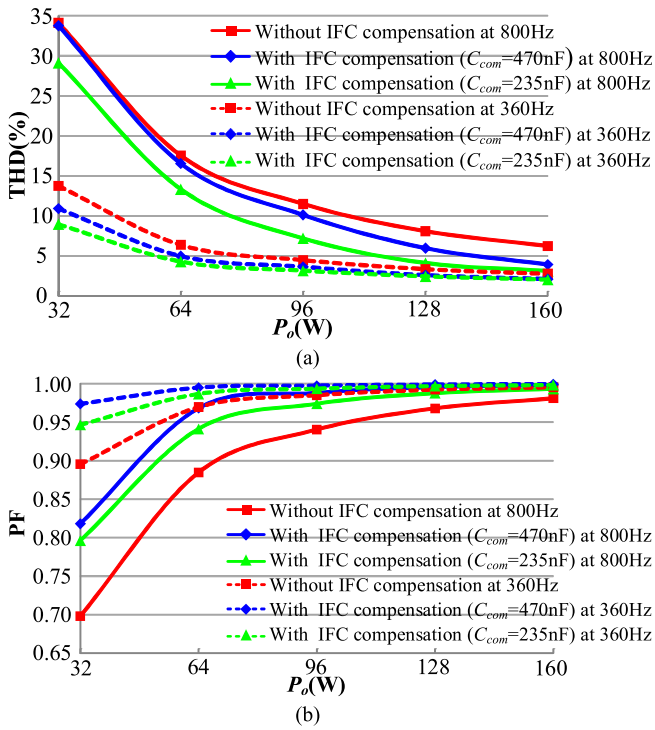

Fig. 28. Measured input current THD and PF comparison. (a) THD. (b) PF.

compensation ($C_{\text{com}} = 235$ nF), Φ decreases while δ increases. Besides, the leading phase angle θ is reduced with IFC compensation and thus a better PF is obtained.

Fig. 28 illustrates the measured i_{in} THD and PF with or without IFC compensation at 360/800 Hz. From Fig. 28, with

TABLE III
PERFORMANCE COMPARISON BETWEEN PROPOSED METHODS AND [10], [11]

	This paper	[10]	[11]
Input voltage v_{in}	115 VAC	90 VAC	230 VAC
Output voltage V_o	270 VDC	390 VDC	390 VDC
Output power P_o	160 W	195 W	195 W
Line frequency f_{line}	360 Hz	50 Hz	50 Hz
Input current THD	8.97% @360 Hz, 32 W 2.04% @360 Hz, 160 W	12.94% @50 Hz, 39 W 5.72% @50 Hz, 195 W	--
Input current PF	0.947 @360 Hz, 32 W 0.998 @360 Hz, 160 W	0.988 @50 Hz, 39 W 0.998 @50 Hz, 195 W	0.932 @50 Hz, 39 W 0.994 @50 Hz, 195 W
Control method	Real time cal. + Look-up table	Real time cal.	Analog

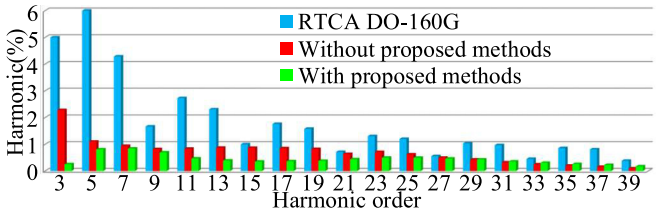

Fig. 29. Measured $i_{\rm in}$ harmonic contents at 400 Hz with full load.

IFC compensation, $i_{\rm in}$ THD and PF can be improved within the entire load range. Moreover, compared with $C_{\rm com} = 470$ nF, $i_{\rm in}$ THD is lower when $C_{\rm com} = 235$ nF. As a result, $i_{\rm in}$ THD can be improved to 2.04% at 360 Hz and to 3.14% at 800 Hz with full load. Fig. 29 compares RTCA DO-160G Std and measured input current harmonic contents at 400 Hz with full load. It can be seen that proposed methods can reduce the harmonic contents and meet the RTCA DO-160G Std.

Table III compares the performance of proposed methods with [10] and [11]. It should be noted that the experimental results in [10] or [11] are based on 50 Hz. From Table III, it can be seen that the proposed compensation method performs better THD at 360 Hz compared with that at 50 Hz in [10] and better PF at 360 Hz compared with that at 50 Hz in [11].

V. CONCLUSION

This article presents the compensation for the nonlinear parasitic capacitance of power switches and the IFC based on VOT control to reduce the effect of capacitances in CRM boost PFC converters, especially at high line frequency. The nonlinearity of parasitic capacitance leads to the inaccuracy of on time and thus the distorted average inductor current. In order to suppress the effect of nonlinear parasitic capacitance, varying $C_{\rm eq}$ control is proposed. Besides, due to the distortion of rectified input voltage deriving from the IFC, sampling before the rectifier can obtain minor dead angle and minor input current spike compared with sampling after the rectifier. The effect of IFC also leads to the input current distortion, especially under high line frequency and light load condition. The compensation for IFC current is further implemented and the appropriate IFC current compensation is also realized. Experimental results show that with compensation for nonlinear parasitic capacitance and the IFC current, input current THD and PF can be effectively improved within the entire input and load condition.

APPENDIX A
CALCULATION OF EQUIVALENT LINEAR VALUE OF $C_{\rm eq}$

The parasitic capacitances of power semiconductor devices $C_{\rm oss}$ and $C_{\rm dp}$ are both nonlinear and voltage dependent. For simplicity, nonlinear $C_{\rm eq}$ can be replaced by a linear-equivalent capacitance with enough accuracy. Generally, the common equivalent models of nonlinear capacitances are linear charge-equivalent capacitance model (as (A1)) and linear energy-equivalent model (as (A2))

$$C_{\rm ce}\left(V_o\right) = \frac{1}{V_o}\int_0^{V_o} C_{\rm eq}\left(v_{\rm ds}\right) dv_{\rm ds} \tag{A1}$$

$$C_{\rm ee}\left(V_o\right) = \frac{2}{V_o^2}\int_0^{V_o} C_{\rm eq}\left(v_{\rm ds}\right) v_{\rm ds} dv_{\rm ds}. \tag{A2}$$

According to [22], the linear charge-equivalent model has a much higher accuracy than the linear energy-equivalent model because it can accurately describe resonant current from the perspective of time domain. Thus, this article adopts the linear charge-equivalent capacitance model to calculate the equivalent value of $C_{\rm eq}$. Below are given the detailed calculation process.

1) Based on the $C(V_R)$ curve of C3D02060A [24], calculate $C_{\rm dp}(v_{\rm ds})$ curve (the green dot-dashed line as shown in Fig. 3) as follows:

$$C_{\rm dp}\left(v_{\rm ds}\right) = C\left(V_o - v_{\rm ds}\right). \tag{A3}$$

2) Calculate $C_{\rm eq}(v_{\rm ds})$ curve (the blue solid line, as shown in Fig. 3) by adding $C_{\rm oss}(v_{\rm ds})$ curve (the red-dashed line, as shown in Fig. 3) of TPH3206PS to $C_{\rm dp}(v_{\rm ds})$ curve.
3) The linear charge-equivalent capacitance is calculated by (A1) and its result is 180 pF.

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