A Novel Interleaved Nonisolated Bidirectional DC–DC Converter With High Voltage-Gain and Full-Range ZVS

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***Abstract*—A nonisolated soft-switching bidirectional dc–dc converter (BDC) with interleaved technique and built-in transformer (BT) is proposed for the interface between the energy storage system and dc microgrid bus in this article. A T-type neutral-point-clamped circuit is integrated into an interleaved conventional buck–boost BDC to obtain a high voltage-gain ratio and decrease voltage stresses of power switches effectively. Compared with the couple-inductor, BT allows for a small magnetic core size, owing to its inherent saturation avoidance. The interleaved structure is employed to reduce the current ripple in the low-voltage side and helps to achieve voltage matching on both sides of the BT under pulsewidth modulation control. Thus, the circulating current can be lowered to improve efficiency. Phase-shift control is adopted to regulate the power flows of the proposed BT-BDC. Moreover, the optimal design is given for the component parameters to accomplish zero-voltage switching in a wide voltage range, which can reduce the switching losses. The operational principles and characteristics of the proposed BT-BDC are presented in detail. The analysis and performance have been fully validated experimentally on a 40–60 V/400 V 1-kW prototype. The accordance between the analysis and the experimental results further testifies the advantages.**

***Index Terms*—Bidirectional dc–dc converter (BDC), built-in transformer (BT), interleaved technique, high voltage-gain, zero voltage switching (ZVS).**

NOMENCLATURE

Abbreviation List

BDC	Bidirectional dc–dc converter.
VGR	Voltage-gain ratio.
LVS	Low-voltage side.
HVS	High-voltage side.
SC	Switched-capacitor.
CI	Coupled-inductor.
BT	Built-in transformer.
SC-BDC	Switched-capacitor BDC.
CI-BDC	Coupled-inductor BDC.
BT-BDC	Built-in transformer BDC.
MB	Magnetic-based.
MB-BDC	Magnetic-based BDC.
ZVS	Zero voltage switching.
RMS	Root-mean-square.
V_L	LVS voltage.
V_H	HVS voltage.
φ	Phase-shift angle.
D	Duty cycle.
u_{ab}	Voltage of the primary side.
u_{cd}	Voltage of the secondary side.
u_{Lr}	Leakage inductance voltage.
i_{Lr}	Leakage inductance current.
i_{Lm}	Magnetizing current.
$P_{\rm base}$	Power base.
I_L	LVS current.
I_H	HVS current.
$P_{\rm ref}$	Power reference.
$i_{Lm\ \max}$	Maximum magnetizing current.
T_s	Periodic time.
T_{dz}	Dead time.
C_{oss}	Parasitic capacitance.

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I. INTRODUCTION

RECENTLY, energy storage systems have been widely used in electric vehicles, uninterrupted power supplies, renewable energy systems, and microgrids to compensate the power imbalance between the power generations and power consumptions [1]–[4]. As an interactive interface between the energy storage elements and the high-voltage dc bus, bidirectional dc–dc converters (BDCs), which have bidirectional power conversion capabilities, are indispensable for the applications of energy conversion. The voltage ratings of the energy storage elements are generally low. Thus, the series connection of the storage cells has been used commonly to increase the voltage ratings with the reducing reliability. Meanwhile, those of the high-voltage dc buses are up to 400 V [5]. Therefore, a BDC with a high voltage-gain ratio (VGR) is required to connect

the low-voltage side (LVS) with the high-voltage side (HVS) for energy storage systems. BDCs with high VGR are mainly divided into isolated and nonisolated categories. Among isolated topologies, the shortcomings of the large current ripple and insufficient voltage regulation exist in the voltage-fed type [6]. Meanwhile, the coupling of regulation variables leads to a complex control in the current-fed type [7], [8].

Compared with the isolated BDCs, nonisolated BDCs have the advantages of high efficiency, low cost, and simple control [9]. The conventional buck–boost BDC is the simplest bidirectional topology but it suffers from the reverse-recovery problem, which limits its VGR [10]. For nonisolated topologies, switched-capacitor (SC), coupled-inductor (CI), and built-in transformer (BT) are widely used in BDCs with high VGR [11]–[15]. Because capacitors replace inductors as the main energy storage elements, SC-BDCs have the advantages of lightweight, high power density, low voltage stress, and high VGR. Nevertheless, SC-BDCs are merely suitable for low-power applications because of the current overshoot in the LVS and large size components [13]. Meanwhile, CI-BDCs store energy in inductors in one cycle and power the load in the other cycles [16]. High VGR can be achieved in CI-BDCs by the proper windings design [14]. Compared with the CI type, the advantage of the BT type is that the balanced magnetic flux exists in the magnetic core, which allows a small core owing to its inherent saturation avoidance [17]. Therefore, magnetic-based (MB) BDCs (CI-BDCs and BT-BDCs) with high VGR have been extensively studied recently [17]–[22].

On the other side, the current in the LVS is much higher than the current in the HVS among BDCs with high VGR. The high current ripple in the MB-BDCs with high VGR affects the lifetime of energy storage in the LVS [23], [24]. Consequently, the multiphase interleaving structure is recommended in MB-BDCs to decrease the current ripples [13], [22], [25]–[29]. Simultaneously, the size of the LVS filter can be reduced along with the decline of ripple current. A novel CI-BDC is proposed with a good performance by adopting interleaved CIs in the LVS, as well as SCs in series with an inductor as charge pumps [13]. The CIs design is complicated because the coupling coefficient is 0.3. Moreover, an interleaved BT-BDC, containing the interleaved buck–boost BDC and the half-bridge converter, is proposed to simplify the design of CIs [22]. Although this topology has inherent zero voltage switching (ZVS), low LVS current ripple, and high VGR, it has poor voltage regulation ability. When the LVS voltage changes, the ZVS feature is failed and the efficiency is decreased due to the increase of the circulating current. A hybrid CI-BDC is proposed to improve efficiency [27]. However, the power flow control becomes complex. Therefore, a nonisolated BDC with low LVS ripple, high VGR, wide LVS voltage range ZVS, and simple control is significant for the applications of the bidirectional power conversions.

Based on the aforementioned analysis, a novel interleaved nonisolated BT-BDC is proposed with high VGR and full-range ZVS. Due to the canceling effect by using interleaving technology, the current ripple in the LVS can be reduced extremely. The drawbacks of the conventional buck–boost BDC and isolated BDCs are overcome. Meanwhile, the advantages of these BDCs

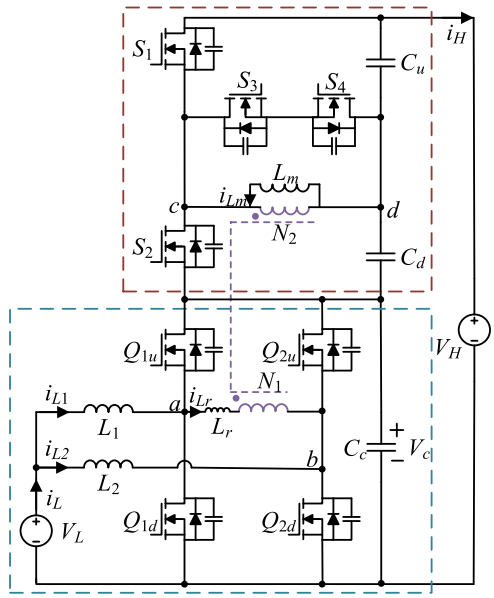


Fig. 1. Circuit diagram of the proposed converter.

are guaranteed by the combination of the interleaved conventional buck–boost BDC and the T-type neutral-point-clamped circuit. Due to the series connection of the two outputs, the high VGR can be achieved and the voltage stresses across the main switches can be reduced. The voltages on both sides of the BT are always matched, thus simple control and high efficiency.

This article is further organized as follows. An introduction is given in Section I. The operation mode and performance analysis are described in Section II, including topology principles, modulation scheme, operating modes, and calculation of transferred power. The soft-switching condition and parameter design are examined in Section III. The stress analysis and design guidelines are presented in Section IV. The comparative study against other interleaved MB-BDCs is shown in Section V. The extension of the proposed topology is given in Section VI, including magnetic components and generalized topologies. The waveforms of the experimental prototype and the corresponding descriptions are presented in Section VII. Finally, the conclusions have been drawn in Section VIII.

II. Operation Modes and Performance Analysis

The circuit diagram of the proposed interleaved nonisolated BDC is demonstrated in Fig. 1. The converter contains the interleaved buck–boost BDC and the T-type neutral-point-clamped circuit. Since both the circuits are in series to increase the VGR, the high voltage V_H is divided into two parts and shared by them. Thus, the voltage stresses on the active switches are less than V_H. The primary side of the transformer is located between two phases of the interleaved buck–boost BDC, while the secondary side is located inside the T-type neutral-point-clamped circuit by turns ratio $n = N_1/N_2$. L_1 and L_2 are the same dc inductors and C_c is the clamp capacitor. The ac inductor L_r represents the sum of the external inductor and the leakage inductor of the high-frequency transformer. L_m is the magnetizing inductance

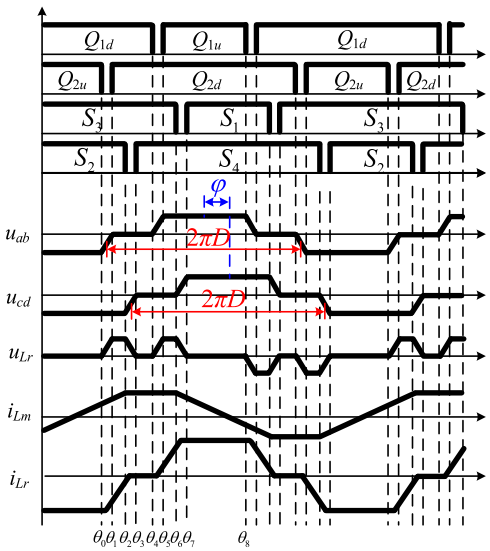


Fig. 2. Steady-state waveforms when $0 < \varphi < 2\pi(D\text{-}0.5)$.

of the secondary side. C_u and C_d are the clamp capacitors. Both primary voltage u_{ab} and secondary voltage u_{cd} have the waveform of three level. Due to the capability of bidirectional power flow, the boost mode is defined as the power flowing from LVS to HVS. The reversed power flow is defined as the buck mode.

A. Operational Principle

D denotes the duty cycle of the switch Q_{1d} (or Q_{2d}). The drive signal of Q_{1d} lags behind the drive signal of Q_{2d} by 180°. Meanwhile, the drive signals of Q_{1d} and Q_{2d} are complementary with those of Q_{1u} and Q_{2u}. S_3 (or S_4) and Q_{1d} (or Q_{2d}) share the same duty cycle D. The drive signal of S_3 also lags behind the drive signal of S_4 by 180°. Meanwhile, the drive signals of S_3 and S_4 are complementary with those of S_1 and S_2. The phase-shift angle φ is the angle difference between the voltages of the primary side and the secondary side of the transformer.

Despite the variation of V_L, the adjustment of D can ensure voltage matching of $V_C = n(V_H - V_C)/2$, which means the circulating current is minimized, thus the highest efficiency [30]. The transferred power P changes along with the variations of the duty cycle D or the phase-shift angle φ. The steady-state waveforms in boost mode during one period are shown in Fig. 2. It should be noted that the waveforms in the case of $0 < \varphi < 2\pi(D\text{-}0.5)$ during one cycle are chosen as an example. The voltage of the primary side u_{ab}, the voltage of the secondary side u_{cd}, the leakage inductance voltage u_{Lr}, the leakage inductance current i_{Lr}, and the magnetizing current i_{Lm} are demonstrated for analysis. The corresponding operation modes of a half cycle are shown in Fig. 3. The detailed analysis is described as follows.

Stage 1 (Before θ_0): Q_{1d}, Q_{2u}, S_2, and S_3 are in conducting state and the others are not. The power flows from the LVS to HVS. The slew rate of i_{Lr} maintains zero, thus voltage matching is achieved.

Stage 2 (θ_0–θ_1): Q_{2u} turns OFF. The sum of i_{L2} and i_{Lr} discharges C_{2d} and charges C_{2u} until D_{2d} begins to conduct. The drain–source voltage of Q_{2d} falls to zero and Q_{2d} is waiting for the driving signal.

Stage 3 (θ_1–θ_2): Q_{2d} turns ON with ZVS. u_{ab} is equal to 0 and u_{cd} is equal to $-(V_H - V_C)/2$. Therefore, u_{Lr} is equal to $n(V_H - V_C)/2$ and the current i_{Lr} is given as

$$i_{Lr}(\theta) = i_{Lr}(\theta_0) + \frac{T_s}{2\pi} \times \frac{\frac{1}{2}n(V_H - V_C)}{L_r}(\theta - \theta_0), \quad \theta \in [\theta_0, \theta_2]. \tag{1}$$

Stage 4 (θ_2–θ_3): S_2 turns OFF. The difference between i_{Lm} and ni_{Lr} discharges C_{s4} and charges C_{s2} until D_{s4} begins to conduct. The drain–source voltage of S_4 falls to zero and S_4 is waiting for the driving signal.

Stage 5 (θ_3–θ_4): S_4 turns ON with ZVS. u_{ab} is equal to 0 and u_{cd} is equal to 0. Therefore, u_{Lr} is 0 and the current i_{Lr} is

$$i_{Lr}(\theta) = 0, \quad \theta \in (\theta_2, \theta_4]. \tag{2}$$

Stage 6 (θ_4–θ_5): Q_{1d} turns OFF. The difference between i_{L1} and i_{Lr} discharges C_{1d} and charges C_{1u} until D_{1u} begins to conduct. The drain–source voltage of Q_{1u} falls to zero and Q_{1u} is waiting for the driving signal.

Stage 7 (θ_5–θ_6): Q_{1u} turns ON with ZVS. u_{ab} is equal to V_C and u_{cd} is equal to 0. Therefore, u_{Lr} is equal to V_C and the current i_{Lr} is given as

$$i_{Lr}(\theta) = i_{Lr}(\theta_4) + \frac{T_s}{2\pi} \cdot \frac{V_C}{L_r}(\theta - \theta_4), \quad \theta \in (\theta_4, \theta_6]. \tag{3}$$

Stage 8 (θ_6–θ_7): S_3 turns OFF. The sum of i_{Lm} and ni_{Lr} discharges C_{s1} and charges C_{s3} until D_{s1} begins to conduct. The drain–source voltage of S_1 falls to zero and S_1 is waiting for the driving signal.

Stage 9 (θ_7–θ_8): S_1 turns ON with ZVS. The current i_{Q1u} flows from source to drain first. Then it begins to flows from drain to source when $i_{L1} = i_{Lr}$. u_{ab} is equal to V_C and u_{cd} is equal to $(V_H - V_C)/2$. Therefore, u_{Lr} is equal to 0 and the current i_{Lr} is given as

$$i_{Lr}(\theta) = i_{Lr}(\theta_6) \quad \theta \in (\theta_6, \theta_8]. \tag{4}$$

The slew rate of i_{Lr} maintains zero, thus voltage matching is achieved. The steady-state waveforms and the operation modes in buck mode are similar to those in the boost mode.

B. VGR and Transferred Power Expressions

Since the analysis is similar for different modes, the analysis is done under the condition of $0 < \varphi < 2\pi(D\text{-}0.5)$. Due to the interleaved buck–boost BDC, the primary side of the transformer voltage u_{ab} can be calculated by

$$u_{ab} = V_c = \frac{V_L}{1 - D}. \tag{5}$$

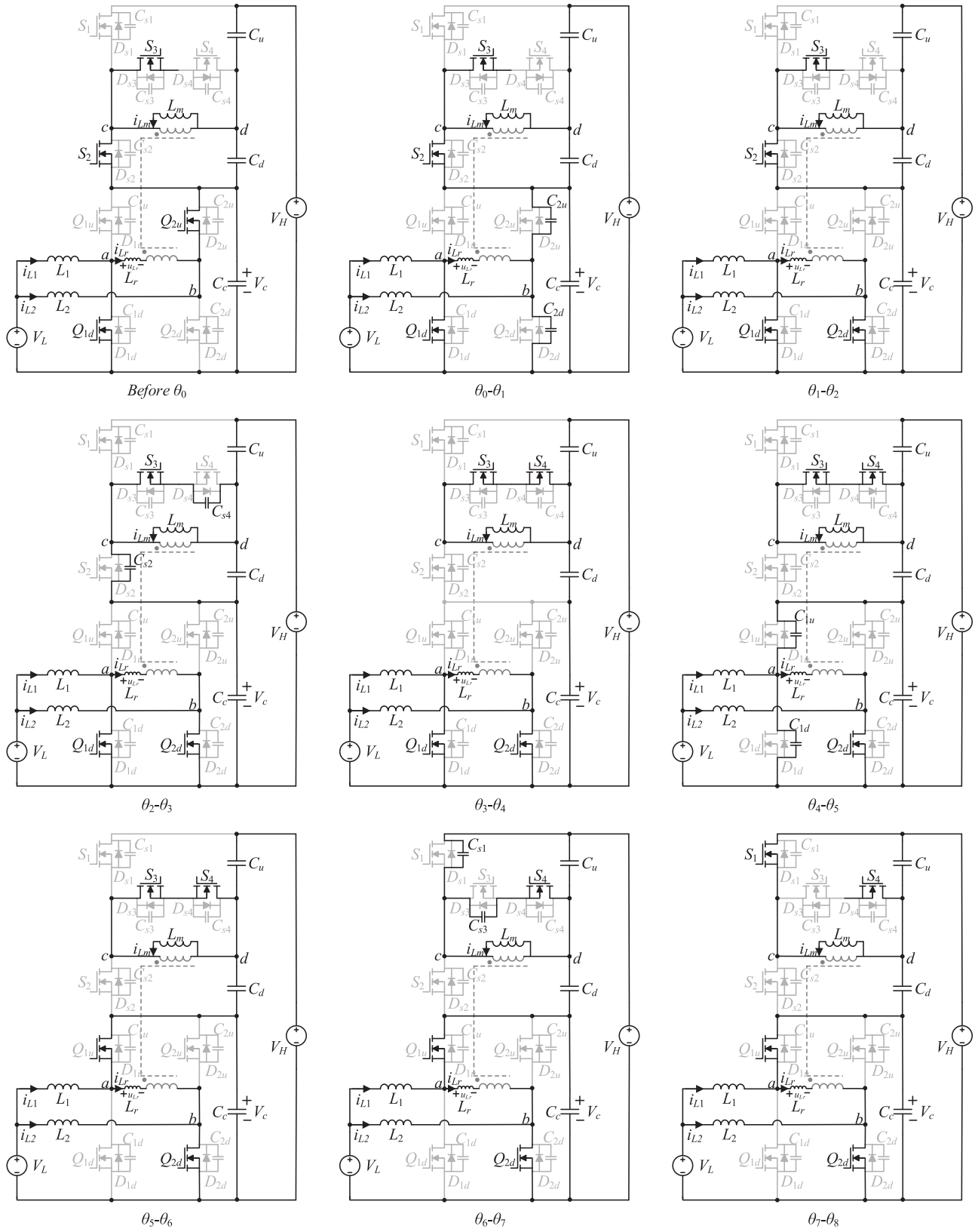


Fig. 3. Operation modes of a half cycle when $0 < \varphi < 2\pi(D\text{-}0.5)$.

Due to the T-type neutral-point-clamped circuit, the u_{cd} can be derived by

$$u_{cd} = \frac{V_H - V_C}{2}. \tag{6}$$

According to (5) and (6), the VGR can be derived as

$$G = \frac{V_H}{V_L} = \frac{n+2}{n(1-D)}. \tag{7}$$

Thus, the duty cycle D can be selected as follows:

$$D = 1 - \frac{(n+2)V_L}{nV_H}. \tag{8}$$

According to Fig. 2, phase angles θ_0, θ_2, θ_4, θ_6, θ_8 can be expressed by D as

$$\begin{cases} \theta_0 = 0 \\ \theta_2 = \varphi \\ \theta_4 = 2\pi D - \pi \\ \theta_6 = 2\pi D - \pi + \varphi \\ \theta_8 = \pi. \end{cases} \tag{9}$$

The primary voltage of transformer u_{ab} is

$$u_{ab}(\theta) = \begin{cases} 0, & \theta \in [0, 2\pi D - \pi] \\ \frac{V_L}{1-D}, & \theta \in (2\pi D - \pi, \pi] \\ -u_{ab}(\theta - \pi), & \theta \in (\pi, 2\pi] \end{cases}. \tag{10}$$

Therefore, according to (1)–(4), (9), (10) and the symmetry of one cycle, the transferred power expression can be expressed as follows:

$$P = P_{\text{base}}[-\varphi^2 + 4\pi(1-D)\varphi] \tag{11}$$

where P_{base} is the power base

$$P_{\text{base}} = \frac{n^2 V_H^2 T_s}{8(n+2)\pi^2 L_r}. \tag{12}$$

Likewise, the transferred power expressions can be summarized as follows:

$$P = \begin{cases} P_{\text{base}}[2\varphi^2 + 2\pi\varphi + 4\pi^2(D^2 - D) + \pi^2] \\ \quad \varphi \in [-0.5\pi, 2\pi(0.5 - D)] \\ P_{\text{base}}[\varphi^2 + 4\pi(1-D)\varphi] \\ \quad \varphi \in (2\pi(0.5 - D), 0] \\ P_{\text{base}}[-\varphi^2 + 4\pi(1-D)\varphi] \\ \quad \varphi \in (0, 2\pi(D - 0.5)] \\ P_{\text{base}}[-2\varphi^2 + 2\pi\varphi - 4\pi^2(D^2 - D) - \pi^2] \\ \quad \varphi \in (2\pi(D - 0.5), 0.5\pi] \end{cases}. \tag{13}$$

As indicated by (13), the transferred power versus the duty cycle D and the phase-shift angle φ is shown in Fig. 4. It shows that the transferred power P only increases monotonously along with the increasing of phase-shift angle φ when D is fixed to achieve voltage matching. The control block diagram is demonstrated in Fig. 5. It is composed of voltage-matching control and power flow control. V_L and V_H are the LVS voltage and the HVS voltage, respectively. I_H is the HVS current and P_{ref} is the power reference. Since D is determined by V_L and V_H

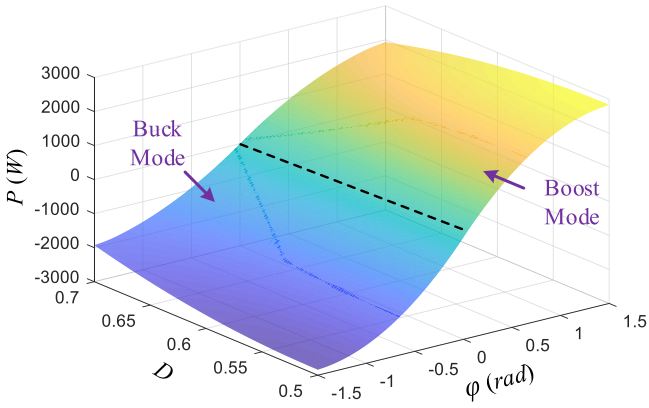


Fig. 4. Surface of power P versus duty cycle D and phase-shift angle φ.

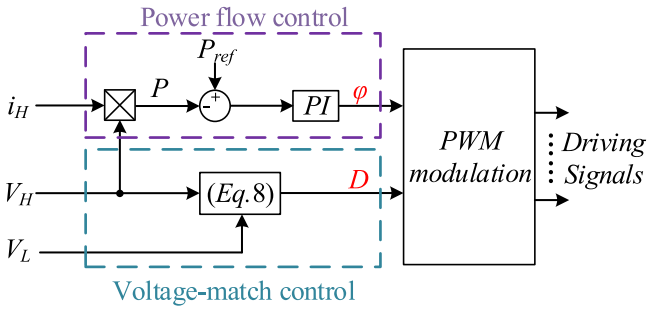


Fig. 5. Control block diagram.

based on (8) to achieve voltage matching, the transferred power P is regulated only by φ using the PI regulator. Meanwhile, the direction of the power flow is only determined by the sign of φ, which means the direction of the power flow is not sensitive to D. Therefore, the voltage matching is achieved by D while the transferred power flow is controlled by φ. It can be found that the control block is very simple and easy to implement.

Based on (7) and the battery voltage V_L range, the turns ratio n and the range of D can be selected reasonably. According to (12) and (13), the maximum transferred power, proportional to the P_{base} and inversely proportional to L_r, can be obtained by L_r reasonably. Thus, P_{ref} and the range of φ can be selected by the maximum transferred power.

III. Discussion of the Soft-Switching Performance

If junction capacitances of the power switches are neglected, a switch can turn ON with ZVS when there is a current flowing from the source to drain of the switch before the arrival of the driving signal. From the mode analysis shown in Section II, the junction capacitances of Q_{1u} and Q_{1d} (or Q_{2u} and Q_{2d}) are discharged and charged by the difference between i_{Lr} and i_{L1} (or i_{L2}), while ni_{Lr} and i_{Lm} on the secondary side help to achieve ZVS of S_1–S_4. The ZVS conditions for switches can be summarized as given in Table I.

The soft-switching performances in the boost mode and buck mode are similar. Therefore, the conditions can be analyzed together. For the interleaved conventional buck–boost BDC, there are many references for detailed analysis of its full-range

TABLE I
ZVS CONDITIONS FOR SWITCHES

Switches	Current
Q_{1u}&Q_{2u}	$i_{L1}(\theta_4)$-$i_{Lr}(\theta_4)$>0
Q_{1d}&Q_{2d}	-$i_{L2}(\theta_0)$-$i_{Lr}(\theta_0)$>0
S_1&S_2	$ni_{Lr}(\theta_6)$+$i_{Lm}(\theta_6)$>0
S_3&S_4	$ni_{Lr}(\theta_2)$+$i_{Lm}(\theta_2)$>0

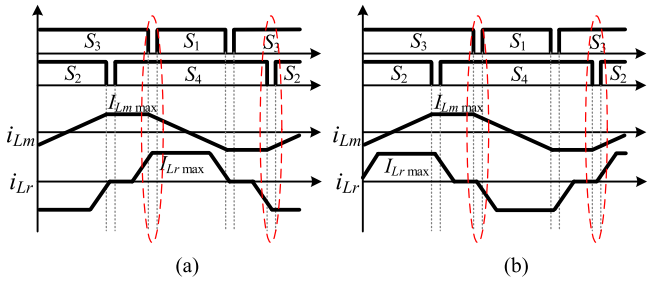


Fig. 6. Key waveforms of S_1–S_4. (a) Boost mode. (b) Buck mode.

ZVS condition [22]. In this section, the soft-switching condition of S_1–S_4 is analyzed in detail.

The waveforms of S_1–S_4 are shown in Fig. 6. S_1 and S_2 are taken as an example to analyze the ZVS performance. According to the detailed analysis in Fig. 3, the sum of i_{Lm} and ni_{Lr} charges the junction capacitance of the switch that has been turned OFF and discharges the junction capacitance of the switch that is about to be turned ON within the dead time to achieve complete ZVS [31]. Therefore, the ZVS condition for S_1–S_4 in the boost and buck modes can be calculated as follows:

$$\int_0^{T_{dz}} |ni_{Lr}+i_{Lm}|\,dt \geq 2C_{oss}\frac{V_C}{n} \tag{14}$$

where T_{dz} is the dead time of S_1–S_4 and C_{oss} is the parasitic capacitance of S_1–S_4.

As seen in Fig. 6(a), before S_1 turns ON, i_{Lm} is the maximum with the value of $i_{Lm\,\max}=V_LT_s/(2nL_m)$, and i_{Lr} begins to decrease. According to (14), the ZVS condition for S_1 and S_2 in boost mode can be expressed as follows:

$$\begin{cases} \frac{V_LT_s}{2nL_m}+\frac{nV_C}{2L_r}\left(\frac{\varphi}{2\pi}T_s-T_{dz}\right)\geq\frac{2C_{oss}V_C}{nT_{dz}}, & \frac{\varphi}{2\pi}T_s\geq T_{dz} \\ \frac{V_LT_s}{2nL_m}+\frac{nV_C}{2L_rT_{dz}}\left(\frac{\varphi}{2\pi}T_s\right)^2\geq\frac{2C_{oss}V_C}{nT_{dz}}, & \frac{\varphi}{2\pi}T_s<T_{dz} \end{cases}. \tag{15}$$

Equation (15) can be deduced as follows:

$$\begin{cases} \frac{V_LT_s}{L_m}+\frac{n^2V_C}{L_r}\left(\frac{\varphi}{2\pi}T_s-T_{dz}\right)\geq\frac{4C_{oss}V_C}{T_{dz}}, & \frac{\varphi}{2\pi}T_s\geq T_{dz} \\ \frac{V_LT_s}{L_m}+\frac{n^2V_C}{L_rT_{dz}}\left(\frac{\varphi}{2\pi}T_s\right)^2\geq\frac{4C_{oss}V_C}{T_{dz}}, & \frac{\varphi}{2\pi}T_s<T_{dz} \end{cases}. \tag{16}$$

It can be seen from (16) that the ZVS condition of S_1 and S_2 becomes more difficult with the decrease of phase-shifted angle φ and ZVS is easy to fail when there is no power transmission ($\varphi=0$). Therefore, L_m to achieve ZVS can be derived as follows:

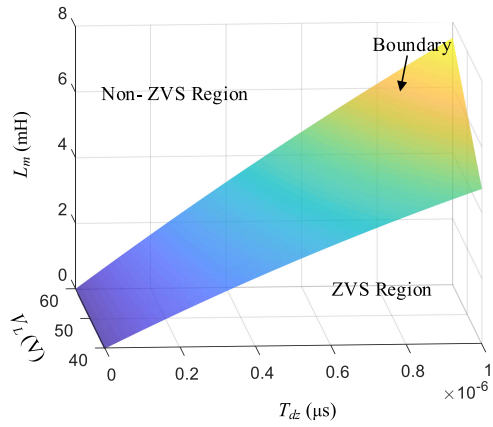


Fig. 7. Surface of the maximum magnetizing inductance L_m versus the LVS voltage V_L and the dead time T_{dz}.

$$\begin{aligned} L_m &\leq \frac{V_LT_sT_{dz}}{4C_{oss}V_C} \\ &= \frac{(1-D)V_CT_sT_{dz}}{4C_{oss}V_C} \\ &= \frac{(1-D)T_sT_{dz}}{4C_{oss}}. \end{aligned} \tag{17}$$

It can be proved that L_m in (17) is independent of the output power. In the same way, the ZVS condition for S_3 and S_4 in the buck mode is the same as (17). Similarly, the ZVS condition for S_1 and S_2 in buck mode and the ZVS condition for S_3 and S_4 in boost mode can be derived as

$$L_m \leq \frac{(1-D)T_s-T_{dz}}{4C_{oss}}T_{dz}. \tag{18}$$

From (17) and (18), it is obvious that the ZVS condition for S_1–S_4 in the boost and buck modes can be guaranteed when L_m satisfies (18). Based on (18), the maximum L_m curve versus the LVS voltage V_L and the dead time T_{dz} of S_1–S_4 is shown in Fig. 7. Fig. 7 indicates that the ZVS can be achieved when L_m is less than the value of the boundary.

To minimize the magnetizing loss, L_m should be designed as large as possible. The large inductance of L_m reduces the magnetizing loss but increases the copper loss. Therefore, the magnetizing loss and copper loss of the transformer need to be comprehensively debated [32]. As seen in Fig. 7, the inductance of L_m increases along with the ascend of dead time T_{dz}. However, the longer dead time causes more conduction time for the switches body diode when i_{Lr} is large enough at heavy loads. Therefore, L_m is designed to be 800 μH and dead time T_{dz}=600 ns.

IV. STRESS ANALYSIS AND DESIGN GUIDELINES

A 1-kW prototype with $V_L=40$–60 V and $V_H=400$ V operating at 50-kHz switching frequency is adopted as an example to illustrate the design considerations.

A. Stress Analysis

1) Duty cycle range: The duty cycle D ought to be closed to 0.5 when the battery voltage is maximum. In this case, according to (5), V_C is set as 120 V. Therefore, D is in the range of 1/3–0.5.

2) Turns ratio of the BT: Because of $V_H = 400$ V and $V_C = 120$ V, according to (5) and (7), turns ratio n is derived to be 6/7.

3) Voltage stress: The voltage stress of the interleaved conventional buck–boost BDC can be obtained as

$$V_{Q1u} = V_{Q1d} = V_{Q2u} = V_{Q2d} = V_C = 120\,\text{V}. \tag{19}$$

Due to the T-type neutral-point-clamped circuit, the voltage stress in the HVS can be derived as

$$V_{S1} = V_{S2} = V_H - V_C = 280\,\text{V} \tag{20}$$

$$V_{S3} = V_{S4} = \frac{V_H - V_C}{2} = 140\,\text{V}. \tag{21}$$

4) Current stress: The current ripples of two dc inductors are neglected for analysis simplification. The currents of L_1 and L_2 are expressed as

$$i_{L1} = i_{L2} = \frac{P}{2V_L}. \tag{22}$$

The peak current of the magnetizing inductance L_m can be obtained as

$$i_{Lm\,\max} = \frac{V_L T_S}{2nL_m}. \tag{23}$$

The current stress of the interleaved conventional buck–boost BDC can be obtained as

$$I_{Q1u} = I_{Q2u} = i_1 \tag{24}$$

$$I_{Q1d} = I_{Q2d} = i_1 + i_{Lr\,\max}. \tag{25}$$

The current stress in the HVS can be derived as

$$I_{S1} = I_{S2} = I_{S3} = I_{S4} = ni_{Lr\,\max} + i_{Lm\,\max}. \tag{26}$$

B. Design Guidelines

1) *AC inductor L_r:* Based on (12) and (13), the maximum power point, proportional with P_{base} and inversely proportional with L_r, can be changed by L_r reasonably. Therefore, the value of 18.1 μH is adopted. The transferred power versus the duty cycle D and the phase-shift angle φ is shown in Fig. 4.
2) *DC inductor L_1 and L_2:* The dc inductors are used to reduce the current ripple in the LVS. By using interleaving technology, the current ripple Δi can be expressed as

$$\Delta i = \frac{\left(\frac{V_L}{D} - 2V_L\right) DT_s}{2L_1}. \tag{27}$$

It is obvious that Δi is equal to 0 when $D = 0.5$. And Δi increases with the decrease of V_L. In order to limit the ripple rate within 10%, $L_1 = L_2 = 79$ μH are implemented.
3) *Capacitors:* The ripple voltages of the capacitors are designed to be 1% of the average voltages. According to the operation principles, the desired value of capacitors under 1-kW condition is calculated reasonably [22]. The values $C_C = 50$ μF and $C_u = C_d = 30$ μF are implemented.
4) *Power switches selection:* According to (19)–(21), the voltage stress on Q_{1u}, Q_{1d}, Q_{2u}, and Q_{2d} is 120 V; the voltage stress on S_1 and S_2 is 280 V; the voltage stress on S_3 and S_4 is 140 V. According to (24)–(26), the current stress on Q_{1u} and Q_{2u} is 12 A; the current stress on Q_{1d} and Q_{2d} is 19 A; the current stress on S_1, S_2, S_3, and S_4 is 8.2 A. Consequently, IRFP4668 and IRFP360 are selected.

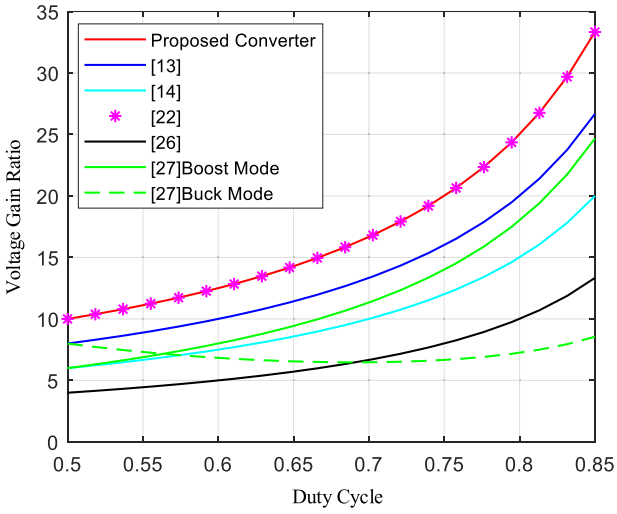
V. Comparative Analysis

In order to evaluate the performance, the comparisons can be conducted among the proposed conventional BDCs and the other similar MB-BDCs. As seen in Table II, the BDCs presented in [2], [6], [7], [13], [14], [22], [26], and [27] are compared with the proposed converter. The conventional buck–boost BDC is the simplest bidirectional topology, which is attractive for low-voltage applications due to simple control and low cost but it is not suitable for high VGR applications due to hard switching, the extreme duty cycle, and the severe reverse-recovery problem. High-frequency isolated BDCs are recommended as its VGR can be adjusted easily through the turns ratio of the transformer. Among isolated BDCs, the shortcomings of large current ripple and insufficient voltage regulation exist in the voltage-fed isolated BDC. Meanwhile, the coupling of regulation variables leads to a complex control in the current-fed isolated BDC. Comparatively speaking, the proposed converter has the advantages of flexible VGR, low current ripple, and simple control.

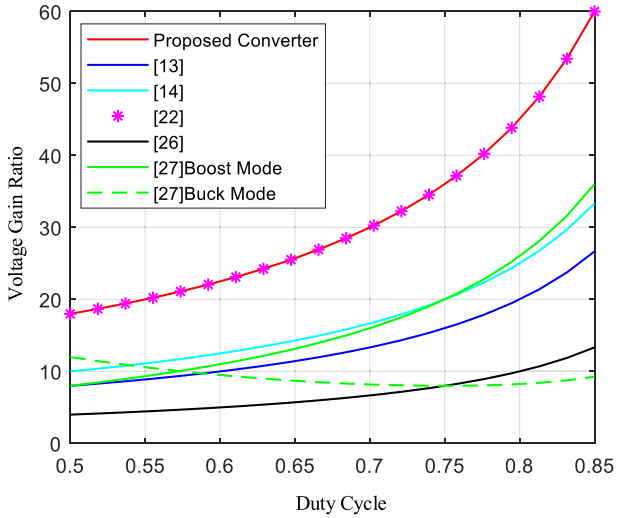
Similarly, it can be observed that the proposed converter with voltage matching has the better performance than the other MB-BDCs due to the less current ripple in the LVS, full soft-switching range, LVS voltage regulation capability, and the bidirectional symmetrical power flow capability. Moreover, Fig. 8 compares the theoretical VGR versus duty cycle. It can be seen that the VGR of the proposed can be adjusted flexibly through the turns ratio and the proposed BT-BDC can achieve high VGR without a high turns ratio. Furthermore, it can be found that the proposed converter and that in [22] possess the highest VGR. The proposed converter and that in [22] both contain the interleaved buck–boost BDC in the LVS, which can reduce current ripple extremely. The two circuits included in the proposed and [22] are in series to increase the VGR and V_H is shared by them. Thus, the voltage stresses on the active switches are less than V_H. Meanwhile, the difference between them is that the T-type neutral-point-clamped circuit is in the proposed converter while the half-bridge circuit is in [22]. Topology in [22] theoretically can bring less conduction loss due to fewer switches but it is difficult to realize a wide range of voltage regulation while maintaining high efficiency. The only optimal operation condition in [22] is matching the voltages on the two sides of the converter, whose duty cycle D is fixed to 0.5. Therefore, once the voltages on the two sides of the converter are not matched, a high circulating current and losing of soft switching will decrease the conversion efficiency

TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER SIMILAR CONVERTERS

Items	Proposed converter	[2] Conventional buck-boost BDC	[6] Voltage-fed isolated BDC	[7] Current-fed isolated BDC	[13]	[14]	[22]	[26]	[27]
Number of semiconductor devices	8	2	8	8	8	4	6	8	6
Number of phases in the LVS	2	1	2	2	4	1	2	2	2
Theoretical voltage gain	$\frac{n+2}{n(1-D)}$	$\frac{1}{1-D}$	$\frac{1}{n}$	$\frac{2}{n(1-D)}$	$\frac{4}{1-D}$	$\frac{n+1}{n(1-D)}$	$\frac{n+2}{n(1-D)}$	$\frac{2}{1-D}$	$\frac{2n+D}{n(1-D)} \Big/ \frac{nD(1-D)}{2(1-D)^2+n}$
LVS voltage regulation capability	Yes	Yes	No	Yes	Yes	Yes	No	Yes	Yes
Theoretical ZVS range	Full-range	Not	Limited	Full-range	Not	Limited	Full-range	Limited	Limited
Current ripple in the LVS	Low	High	High	Low	Low	High	Low	Low	Moderate



(a)



(b)

Fig. 8. Comparison of VGR versus duty cycle between converters presented in [13], [14], [22], [26], [27], and the proposed converter. (a) $n = 1/2$. (b) $n = 1/4$.

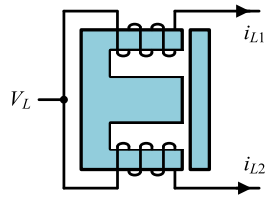


Fig. 9. Physical structure of the magnetic-integrated dc inductors using EI core.

dramatically. However, the proposed converter has the LVS voltage regulation capability, whose duty cycle D can change along with the variations of the LVS voltage. Moreover, the voltages on both sides are always matched. When D is not equal to 0.5, the proposed converter has higher conversion efficiency than [22]. Therefore, the proposed converter is more suitable than [22] for energy storage applications.

VI. EXTENSION OF THE PROPOSED TOPOLOGY

A. Magnetic Components

1) Magnetic-integrated dc inductors: Since L_1 and L_2 are designed with the same inductance and are subjected to the same operation conditions, they can be constructed with ferrite EI core with air gap to improve the power density. As seen in Fig. 9, two windings are wound on the outer legs with adding polarity to allow flux ripple cancellation in the center leg [33]. Furthermore, the magnetic-integrated inductor is used to eliminate the magnetic flux ripples, which can reduce the magnetic loss so as to improve the efficiency.

2) The ac inductor: The ac inductor L_r can be partly or fully implemented with the leakage inductance of the BT. Therefore, the power density can be improved effectively by the utilization of parasitic parameters. In addition, it can be found from (12) and (13) that the maximum power is proportional to the P_{base} and inversely proportional to L_r; therefore, the power range can be designed by the regulation of the leakage inductance L_r reasonably.

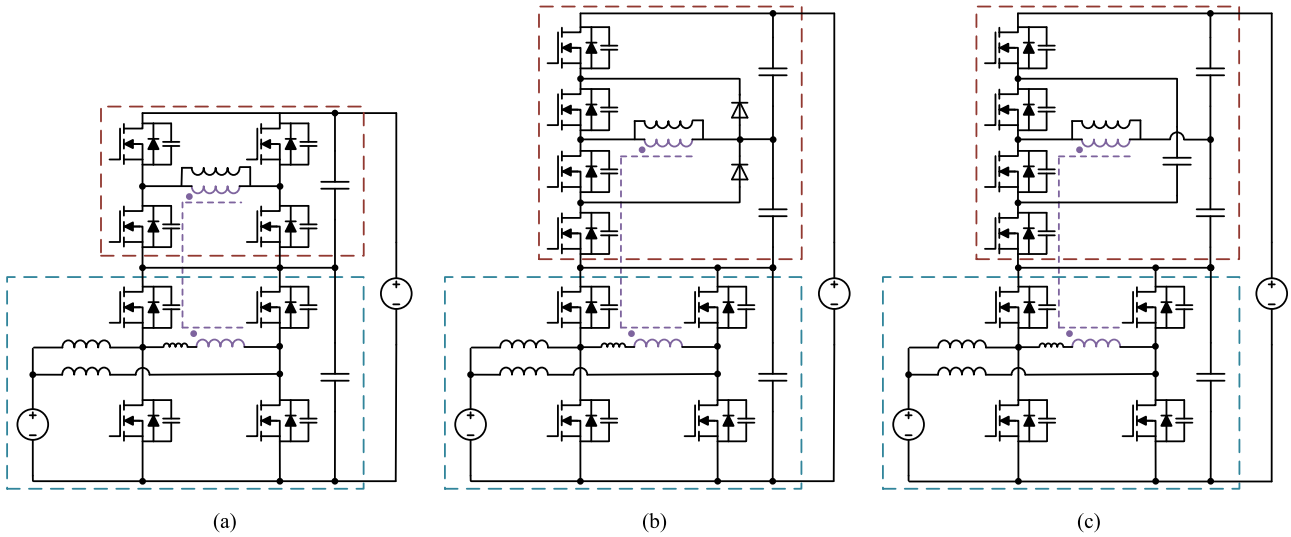


Fig. 10. Generalized three-level BT-BDCs topologies. (a) Full-bridge type. (b) Diode-clamped type. (c) Flying-capacitor type.

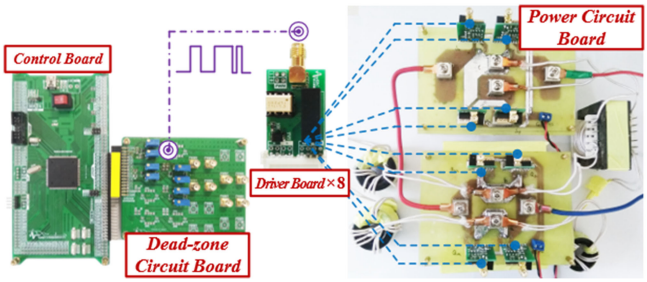


Fig. 11. Photo of the prototype.

TABLE III
MAIN PARAMETERS OF THE PROTOTYPE

Symbol	Parameter	Symbol	Parameter
V_L	40-60 V	L_r	18.1 μH
V_H	400 V	L_m	800 μH
P	1-kW	C_C	50 μF
f_s	50-kHz	C_u, C_d	30 μF
n	6/7	t_{dz}	600 ns
L_1, L_2	79 μH		
Q_{1u}, Q_{1d}, Q_{2u}, Q_{2d}, S_3, S_4	IRFP4668	S_1, S_2	IRFP360
P	0.00005	I	500

B. Generalized Three-Level Topologies

The idea, achieving interleaving technology and high VGR by employing two three-level structures on both sides of the BT, is also valid for other three-level circuits. Therefore, a family of three-level BT-BDCs with interleaving technology can be derived in Fig. 10. Similarly, the primary side of the BT is located between two phases of the interleaved conventional buck–boost BDC, while the secondary side is located in different three-level circuits.

The topology in Fig. 10(a) is the full-bridge type, which can achieve three levels on the secondary side of the BT by phase-shift control. Similarly, low LVS ripple, high VGR, wide LVS voltage range ZVS, and simple control can be achieved. Moreover, diode-clamped circuit and flying capacitor circuit in Fig. 10(b) and (c) can reduce voltage stresses of switches by half.

VII. EXPERIMENTAL RESULTS

A 1-kW experimental prototype has been built with 50-kHz switching frequency to verify the effectiveness of the proposed BT-BDC. It is illustrated in Fig. 11 with its parameters given in Table III.

For the performance evaluation at different voltage conversion ratios, the LVS voltage V_L is 40–60 V and the HVS voltage V_H is clamped to 400 V. L_1 and L_2 are 79 μH [22], Q_{1u}, Q_{1d}, Q_{2u}, and Q_{2d} can achieve ZVS. From the above analysis, t_{dz} is selected around 600 ns that is achieved by the dead-zone circuit. The control is implemented with a TM320F28335 digital controller.

The experimental waveforms of the buck and boost modes are shown in Fig. 12(a)–(f) at the rated power of $P = 1$ kW. The waveforms shown in Fig. 12(a)–(c) are tested in boost mode and those in Fig. 12(d)–(f) are tested in buck mode. u_{ab} and u_{cd} are the voltages of the BT primary and secondary side, respectively. i_{Lr} is the current of the leakage inductor L_r. The voltage-matching waveforms can be clearly observed from Fig. 12(a)–(f) as the slew rate of i_{Lr} maintains zero when $u_{ab} = u_{cd}$. Thus, the voltages on both sides of BT are matched to reduce the circulating current losses and ensure ZVS for all power switches. In addition, the duty cycle D is only determined by V_L. It can be found that the conversion power can be controlled independently by the adjustment of the phase-shift angle φ when the voltage

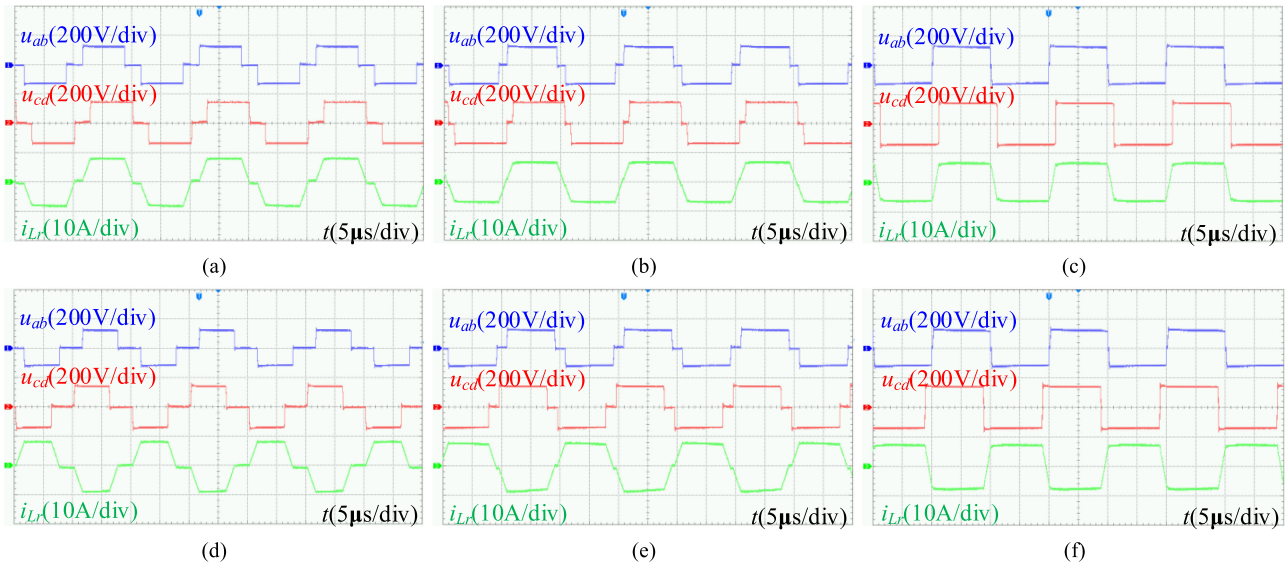


Fig. 12. Experimental waveforms for buck and boost modes at rated power. (a) $V_L = 40$ V in the boost mode. (b) $V_L = 50$ V in the boost mode. (c) $V_L = 60$ V in the boost mode. (d) $V_L = 40$ V in the buck mode. (e) $V_L = 50$ V in the buck mode. (f) $V_L = 60$ V in the buck mode.

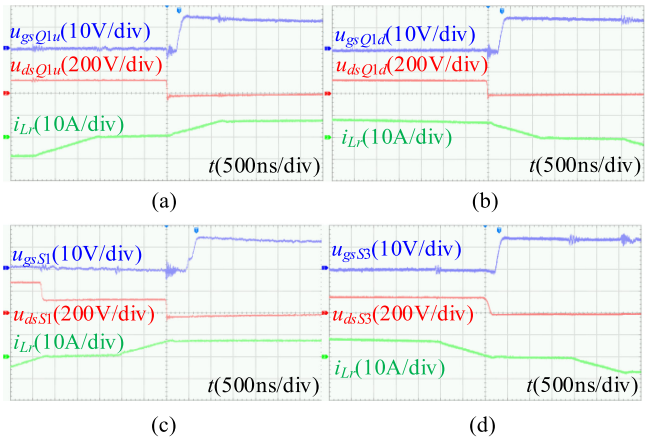


Fig. 13. Experimental waveforms of soft switching for boost mode at the rated power with $V_L = 40$ V. (a) ZVS of Q_{1u}. (b) ZVS of Q_{1d}. (c) ZVS of S_1. (d) ZVS of S_3.

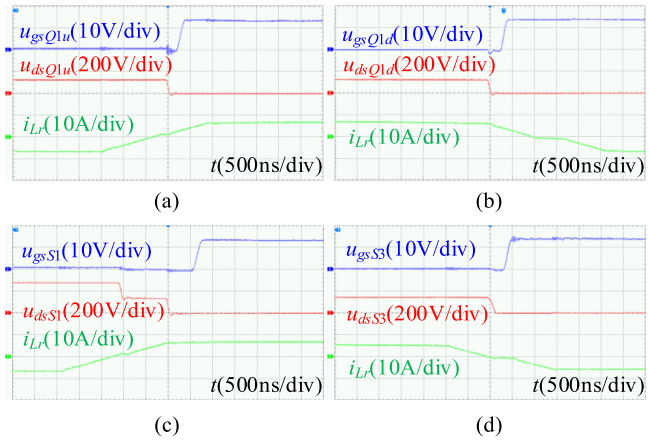


Fig. 14. Experimental waveforms of soft switching for boost mode at the rated power with $V_L = 50$ V. (a) ZVS of Q_{1u}. (b) ZVS of Q_{1d}. (c) ZVS of S_1. (d) ZVS of S_3.

matching is achieved by D. The experimental results agree well with the theoretical analysis.

The waveforms of soft switching are shown in Figs. 13–18. The waveforms in Figs. 13–15 are tested in the boost mode in $V_L = 40$, 50, and 60 V, respectively. The waveforms in Figs. 16–18 are tested in the buck mode in $V_L = 40$, 50, and 60 V, respectively. Figs. 14 and 17 are taken as an example to analyze ZVS performance. Because of the symmetry of the topology, the waveforms of half-power switches are shown. Fig. 14(a)–(d) shows the waveforms of soft switching in boost mode in Q_{1u}, Q_{1d}, S_1, and S_3, respectively. Fig. 17(a)–(d) shows the waveforms of soft switching in buck mode in Q_{1u}, Q_{1d}, S_1, and S_3, respectively. The gate voltage, the drain-to-source voltage, and the leakage inductor current are captured. As illustrated in Figs. 14 and 17, ZVS can be achieved for all the power switches. Meanwhile, it can be seen from Figs. 14 and 17 that the voltage

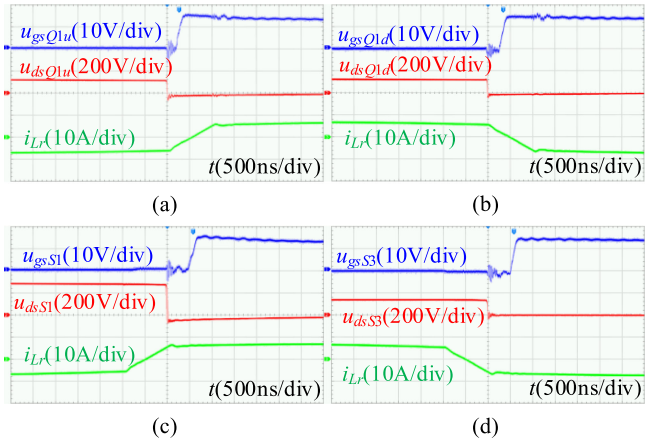


Fig. 15. Experimental waveforms of soft switching for boost mode at the rated power with $V_L = 60$ V. (a) ZVS of Q_{1u}. (b) ZVS of Q_{1d}. (c) ZVS of S_1. (d) ZVS of S_3.

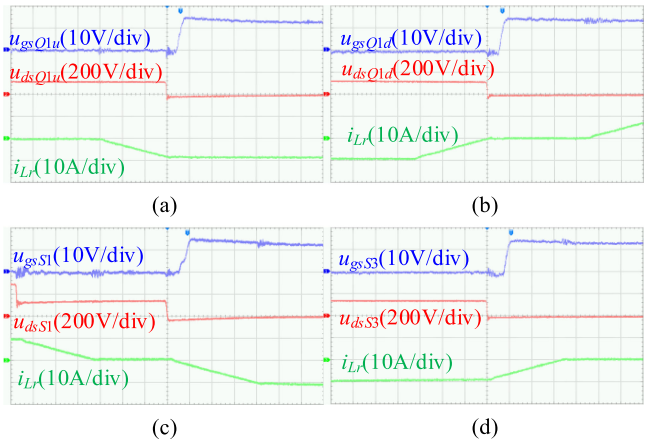


Fig. 16. Experimental waveforms of soft switching for buck mode at the rated power with $V_L = 40$ V. (a) ZVS of Q_{1u}. (b) ZVS of Q_{1d}. (c) ZVS of S_1. (d) ZVS of S_3.

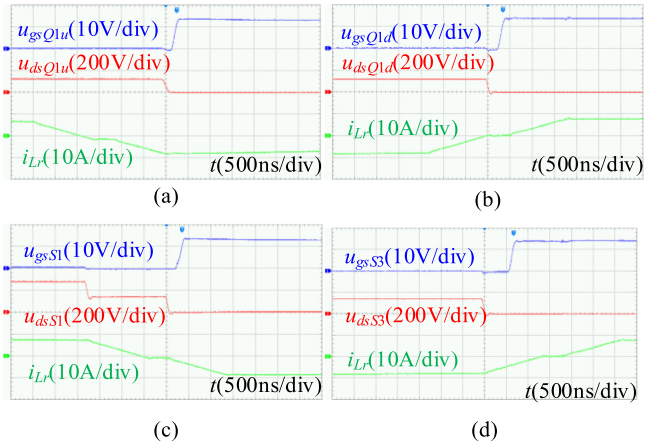


Fig. 17. Experimental waveforms of soft switching for buck mode at the rated power with $V_L = 50$ V. (a) ZVS of Q_{1u}. (b) ZVS of Q_{1d}. (c) ZVS of S_1. (d) ZVS of S_3.

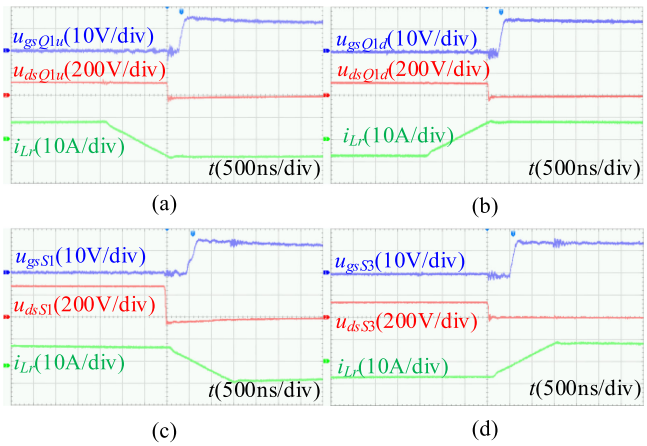


Fig. 18. Experimental waveforms of soft switching for buck mode at the rated power with $V_L = 60$ V. (a) ZVS of Q_{1u}. (b) ZVS of Q_{1d}. (c) ZVS of S_1. (d) ZVS of S_3.

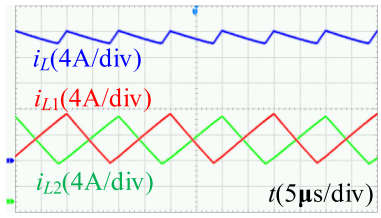


Fig. 19. Experiment waveform of high-frequency current ripple in the LVS at the rated power with $V_L = 50$ V.

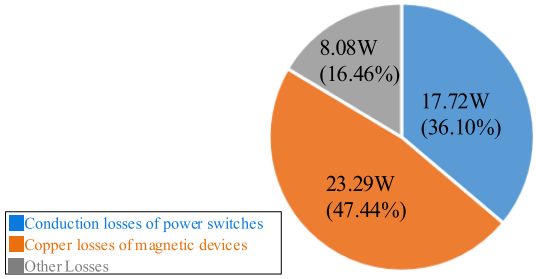


Fig. 20. Pie chart of losses in the proposed converter.

stresses on Q_{1u} and Q_{1d} are 120 V, while the voltage stress on S_1 and S_3 is 140 V and 280 V, respectively. The waveforms indicate that the 400 V high voltage is divided into two parts and shared by the two circuits. Thus, the voltage stresses on power switches are reduced.

The experimental waveforms of the high-frequency current ripple in the LVS at rated power with $V_L = 50$ V are shown in Fig. 19. Under the condition of interleaving control, the amplitude of the current ripple in the LVS is greatly reduced and the frequency is doubled, which can reduce the size of the filter and prolong the lifetime of the energy storage device.

The pie chart of losses in the boost mode is shown in Fig. 20, where V_L is 40 V and V_H is 400 V. The switching losses are taken as zero due to the soft switching. As seen in Fig. 20, the losses include conduction losses of power switches, copper losses of magnetic devices, and other losses. Conduction losses of power switches can be written as

$$P_{\text{con,loss}} = 2 \times (I^2_{\text{RMS},Q1u} \times R_{\text{on},Q1u} + I^2_{\text{RMS},Q1d} \times R_{\text{on},Q1d} + I^2_{\text{RMS},S1} \times R_{\text{on},S1} + I^2_{\text{RMS},S3} \times R_{\text{on},S3}) \quad (28)$$

where I_{RMS} is the root-mean-square (RMS) current of the power switch and R_{on} is the static drain-to-source ON-resistance of the power switch.

Copper losses of magnetic devices can be written as

$$P_{\text{mag,loss}} = I^2_{\text{RMS},L1} \times r_{L1} \times 2 + I^2_{\text{RMS},Lr} \times r_{Lr} \quad (29)$$

where r_{L1} is the equivalent series resistance of L_1 and r_{Lr} is the equivalent series resistance of L_r.

Fig. 21 shows the measured efficiency curves of the proposed converter under different voltages in the boost mode and the buck mode. The overall conversion efficiency is high, whose maximum efficiency is 96.5%. It can be seen that the efficiencies

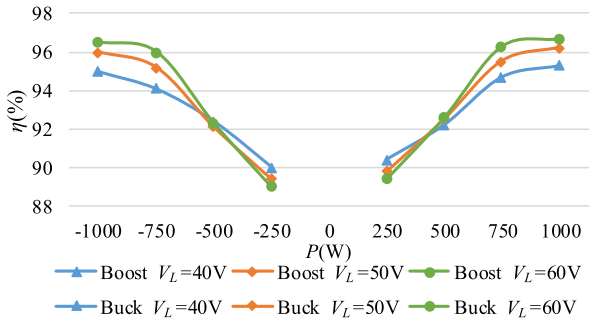


Fig. 21. Measured efficiency curves under different voltages.

of the boost mode and the buck mode are similar, which means the power flow direction is not sensitive to the efficiency. Furthermore, the efficiency of the proposed BT-BDC is insensitive to the variation of the LVS voltage V_L. Thus, the proposed BT-BDC is a good candidate for the interface between the energy storage system with a wide voltage range and the high-voltage dc bus in dc microgrid, renewable generation systems, electric vehicles, and uninterrupted power supplies.

VIII. Conclusion

In this article, a novel interleaved soft-switching BT-BDC with high VGR and low current ripple has been proposed by integrating a T-type neutral-point-clamped circuit into an interleaved conventional buck–boost BDC. By series connection of two circuits, there are lower voltage stresses of power switches and higher VGR. Voltage-matching control is achieved by the adjustment of the duty cycles. Thus, the voltages on the both sides of BT are always matched to reduce the circulating current losses and improve the soft-switching performance. Power flow can be regulated by employing phase-shift control. Moreover, the parameter optimization is analyzed in detail to achieve ZVS for all the power switches within a wide voltage range, thus reducing the switching losses. The comparative study against other MB-BDCs is conducted, demonstrating the merits of the proposed converter, such as low LVS ripple, high VGR, wide LVS voltage range of ZVS, and simple control. Furthermore, a family of three-level BT-BDCs with interleaving structure has been derived. Finally, the effectiveness of the proposed BT-BDC and control strategy is verified by a prototype of 1-kW, 40–60 to 400 V. Experimental results testify that the proposed topology and control are effective for the interface between the energy storage system and the dc bus.

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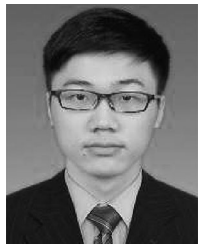

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