Systematic Synthesis and Derivation of Multilevel Converters Using Common Topological Structures With Unified Matrix Models

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***Abstract*—Multilevel converters (MLCs) have been increasingly adopted in both low-power low-voltage systems and high-power high-voltage applications. In recent years, many new topologies have been proposed, and a few of them have been successfully implemented in industry. While searching for new topologies, synthesis and derivation principles of multilevel topologies are critical for converter design. In this article, a generalized synthesizing approach of multilevel topologies is proposed and analyzed with the considerations of the voltage source, current source, and matrix-type MLCs. Based on the proposed method, the topological relationship among these three types MLCs is revealed through the stage-based common circuit structure. In addition to the graphic-based approach, a mathematical approach is proposed for representing the MLC topologies in this work. The matrix-based model is utilized to unify and verify the derivation and simplification process in a systematic way through many MLC examples in this article. Finally, demonstration examples are presented to show how the proposed principles can be used to derive new topologies covering five-level to nine-level converters. With the ever-increasing research efforts on MLCs, it is hoped that this article can provide a new approach that inspires the development of more interesting and practical MLC topologies for various applications.**

***Index Terms*—Current-source converter (CSC), matrix converter, multilevel converter (MLC), voltage-source converter (VSC).**

Nomenclature

Abbreviation

ac	Alternating current.
ANPC	Active neutral point clamped.
CHB	Cascaded H-bridge.
CSC	Current-source converter.
DC	Direct current.
DMC	Direct matrix converter.
DPP	Differential power processor.
DSCC	Double-star chopper cell.
EMI	Electromagnetic interference.
EV	Electric vehicle.
FC	Flying capacitor.
FCC	Flying capacitor converter.
HBBB	H-bridge building blocks.
HV	High voltage.
IC	Integrated circuit.
IMC	Indirect matrix converter.
LED	Light-emitting diode.
LS	Level selector.
LG	Level generator.
MLC	Multilevel converter.
MMC	Modular multilevel converter.
MV	Medium voltage.
NBD	Node-branch diagram.
NPC	Neutral point clamped.
NNPC	Nested neutral point clamped.
NNPP	Nested neutral point piloted.
PV	Photovoltaic.
PWM	Pulsewidth modulation.
SMC	Stacked multicell converter.
SM	Submodule.
TNPC	T-type NPC.
VSC	Voltage-source converter.

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I. Introduction

PWM converters are essential in many applications. New converters and devices keep emerging, which promotes the innovation in the power electronics field and enables new applications such as renewable energy integration, electric vehicles, smart grids, wireless power transfer, etc. [1].

Conventionally, the converter design is an iterative process which requires repetitive synthesis, derivation, and evaluation of converter topology if available candidates cannot completely satisfy the requirements. This could easily lead to non-optimal results and extend the development cycle with repetitive efforts [2]–[6]. A comprehensive converter database can potentially reduce the repetitive design process and break the conventional design loop by providing a large set of converter topologies. To build this converter database, continuous research efforts

have been put on this topic resulting in the increasingly profound and systematic understanding of topological synthesis and derivation [7]–[18]. However, compared with conventional two-level topologies, the database establishment of MLCs is much more challenging due to their complicated structures and a high number of possible topologies [11]–[43]. To date, the topology synthesis and derivation approaches of MLCs are mainly focused on specific types MLCs and rarely discussed in a systematic way, especially when it comes to all three kinds of MLCs: voltage-source MLCs, current-source MLCs, and multilevel matrix converters [38]–[49].

Generalized from existing concepts and approaches, the topology synthesis and derivation approach based on common structures of MLCs with unified matrix models is proposed in this paper. It provides a different perspective covering voltage-source MLCs, current-source MLCs, and matrix MLCs through the commonness of their topological structures. The concept of the stage is proposed to demonstrate the inherent topological and mathematical structural features of voltage-source MLC and current-source MLC. While the concept of the virtual dc link is introduced to decompose a multilevel matrix converter into stages.

The contributions of this article are briefly summarized as follows.

1) The common topological structures of voltage-source MLCs, current-source MLCs, and multilevel matrix converters are investigated and unified in the matrix model forms.
2) Through the proposed general methodology, all three types of MLCs can be synthesized and derived systematically.
3) The method is more intrinsic as it reveals the functional characteristics of an MLC topology (i.e., generating and selecting voltage/current levels), not only the circuit appearance.
4) The matrix representation of MLC topologies can be developed and utilized as mathematical verification of topology derivation process.
5) Various existing MLC topologies can be derived and modeled through this general methodology. Extensive examples are given in this article for demonstration.
6) Finally, with the proposed topology derivation and synthesis principles, a number of newly published topologies are obtained. Case study results of these new topologies are also presented in this article.

The rest of the article is organized as follows: Section II reviews the existing synthesis and derivation approaches, Section III investigates the common structures of MLCs, Section IV introduces the stage-based concept and its unified matrix models, Sections V to VIII are the synthesis of single-stage topologies (Section V), the deduction of multiple stages topologies (Section VI), the simplification of circuits (Section VII), and the topological synthesis and derivation for matrix MLCs (Section VIII), respectively. In Section IX, the implementation of the proposed method is discussed, and several emerging topologies are derived with discussions and experimental verifications. Finally, Section X concludes the paper.

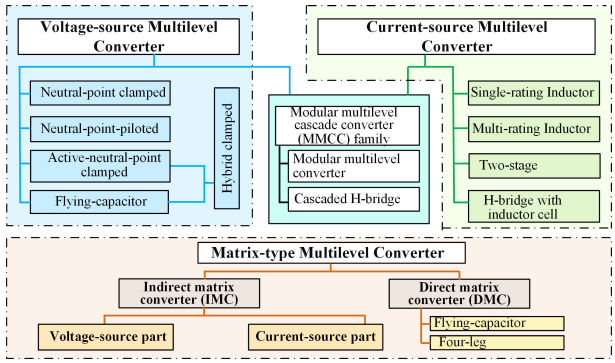


Fig. 1. Categories of existing MLC topologies.

II. Overview of Synthesis and Derivation Approaches of Existing Multilevel Converters

As of today, various MLCs have been widely applied in the industry owing to their merits like high-quality output, reduced voltage/current stress on semiconductor devices, reduced device switching frequency, low EMI, and so on [11]–[18]. The MLCs can be classified as three types, namely the voltage-source MLCs [14], the current-source MLCs [15], and the matrix MLCs [16]. A more detailed classification of existing topologies is summarized in Fig. 1.

For medium- and high-voltage applications, voltage-source CHB converter has been commercialized successfully because of its modular structure, utilization of low power rating devices, and low cost [2], [19], [20]. Such topologies with multiple isolated dc links normally consist of single/shared dc-link topology as basic modules. With the knowledge of a single/shared dc-link topology database, each element inside the database could be utilized to derive multi-dc-link topologies. Therefore, in this article, topologies with a single/shared dc link are chosen to be discussed first.

In a single-phase or multiple-phase system, an MLC with single/shared dc link is referred to as the converter with 1) only one dc source; 2) with several non-isolated and series/parallel connected dc sources that are shared by all phase-legs simultaneously. Some of this kind of voltage-source MLCs have been applied in industry, e.g., NPC converter [21], FCC [22], five-level ANPC [23], MMC [24], NNPP converter (also called SMC) [25], etc. Current-source MLCs and matrix MLCs with shared dc link can also be found in the literature, e.g., multicell current-source MLC [26], diode-clamped indirect matrix MLC [27], just to name a few.

Besides conventional applications, MLCs with single/shared DC link have also been widely accepted in low voltage/current applications. Topologies like three-level ANPC, FCC, TNPC have become increasingly popular in applications like PV inverters and EV drives [28]–[33]. In applications with even lower voltage, e.g., power supply and LED driver, MLCs are also gaining their popularity [34]. Recent technology can even integrate MLC into ICs [35]–[37]. Different from the medium- and high-voltage applications, low-voltage scenario enables the use of a wide range of topologies, including those originally unfavorable in medium- and high-voltage applications. For

example, topologies with difficulty in dc voltage balancing are more practical in low-voltage applications, where balancing circuit becomes a feasible solution. As the demand for MLCs keeps increasing, seeking new topologies becomes a critical task, and systematic topology synthesis and derivation approach can greatly facilitate this task.

Many studies have been reported in the literature focusing on voltage-source MLCs and current-source MLCs [38]–[49]. A generalized self-balancing MLC is proposed in [38], from which several existing voltage-source topologies, e.g., diode-clamped and capacitor-clamped topologies, can be derived. In [38], the concept named level line is used to explain the output voltage level based on the natural structural division of this self-balancing topology. Though the generalized topology is composed of minimal cells (such as half-bridge or three-level cells), systematic topology derivation is difficult to be realized based on the suggested procedure. More importantly, some topologies (such as SMC, switched capacitor MLC) are hard to be explained or analyzed based on this generalized self-balancing MLC. In [39] and [40], a concept that divides a specific hybrid voltage-source multilevel topology into two functional parts, named level generation and polarity generation, is proposed to establish the link between the topological structure and its operation. However, this concept cannot be generalized to other kinds of voltage-source MLCs as 1) it requires the relationship between the two parts to be low-frequency coupling and 2) it can only represent one fixed structure for a specific type of MLC.

Recently several voltage-source topology derivation methods are summarized in [41], which can cover a large number of topologies and can be considered as a good extension to the generalized topology in [38]. However, conventional sophisticated methods are not easy to follow which are normally dependent on very skilled expertise (e.g., adequate familiarity with the operation principles of a certain type of converters). On the other hand, it is possible to use basic circuit theory (e.g., *Kirchhoff*'s laws under lumped parameter circuits) and the help of an algorithm for autonomously synthesizing and deriving topologies [50]–[52]. While the effective implementation of the algorithm and its interpretability of the results could be quite challenging. Another way is to develop a rule-based method balancing the operational complexity and comprehensibility [6]. It is expected to be broad enough to cover most types of topologies while having clear rules for manual implementation or algorithm implementation and is also easy to understand.

To derive current-source MLCs, dual principles are normally utilized to facilitate the topological derivation process [12], [47], [48]. In [47], the duality principle is utilized to construct the current-source MLCs topologies based on the existent voltage-source MLCs topologies. In [12], such duality principle is utilized for MMC derivation considering both the SMs and cell connections. While it is true that duality principles are powerful tools toward topology derivation, it still requires the existent voltage-source MLCs topologies to realize VSC to CSC mapping process. In this article, instead of mapping specific VSC topologies to CSC versions, we establish the synthesis and derivation principles of current-source MLCs directly based on their common structures.

In fact, some research works summarize the common structure of certain types of MLCs which can help the derivation process of new topologies [41]–[43]. For example, in [41], two types of derivation methods are reviewed: 1) generalized-topology method; 2) basic-cell method. Based on the former type, the structure of general topology is needed first, and then simplify it according to various requirements. However, the general principles of topology deduction can hardly be obtained in this way. While the second one limits the basic cells must be self-balanced, which in fact makes the topology deduction lose generality. Although the self-voltage balancing capability is appreciated in some applications, there are other applications when topologies requiring external balancing force can be reasonable, e.g., low-voltage scenario. In [43], five main SMs are introduced as the basic structures covering a large number of voltage-source MLC structures. The common structures are shown in specific types of circuit connection forms, e.g., series connection and parallel connection. While the structure properties among different topologies are still ambiguous due to the lack of universal representation models in a mathematical point of view. In general, the common structures of MLCs are still unclear and have never been investigated in a systematic way.

III. Investigation of The Common Structures of Existing Multilevel Topologies

In this section, the structures of all three types of MLCs are thoroughly investigated, i.e., voltage-source MLC, current-source MLC, and matrix-type MLC. To cover mainstream converters, five typical topologies (e.g., generalized MMC with half-bridge SM, generalized self-balance MLC, general multilevel CSCs, three-level, and five-level matrix converters) are presented with associated mathematical representations to demonstrate the common topological features of all three types of MLCs. First, two general voltage-source topologies are selected and discussed as follows.

Voltage-Source Example 1: Circuit form of MMC with half-bridge SM (also can be referred to as DSCC converter in [14]) is shown in Fig. 2(a).

The output voltage w.r.t. potential $A1$ of each SM is related to its switching states, the dc capacitor voltage, and the input voltage levels. Equation (1) is for the rightmost two SMs, which can be expanded to cover all the SMs information through iterative substitution.

The matrix model of Stage *n-1* of MMC is as follows:

$$\begin{bmatrix} V_{o(n-1)1} \\ V_{o(n-1)2} \end{bmatrix} = \begin{bmatrix} S_{(n-1)4} & S_{(n-1)3} & & \\ & & S_{(n-1)2} & S_{(n-1)1} \end{bmatrix} \times \begin{bmatrix} L_{(n-1)22} \\ L_{(n-1)21} \\ L_{(n-1)12} \\ L_{(n-1)11} \end{bmatrix}. \quad (2)$$

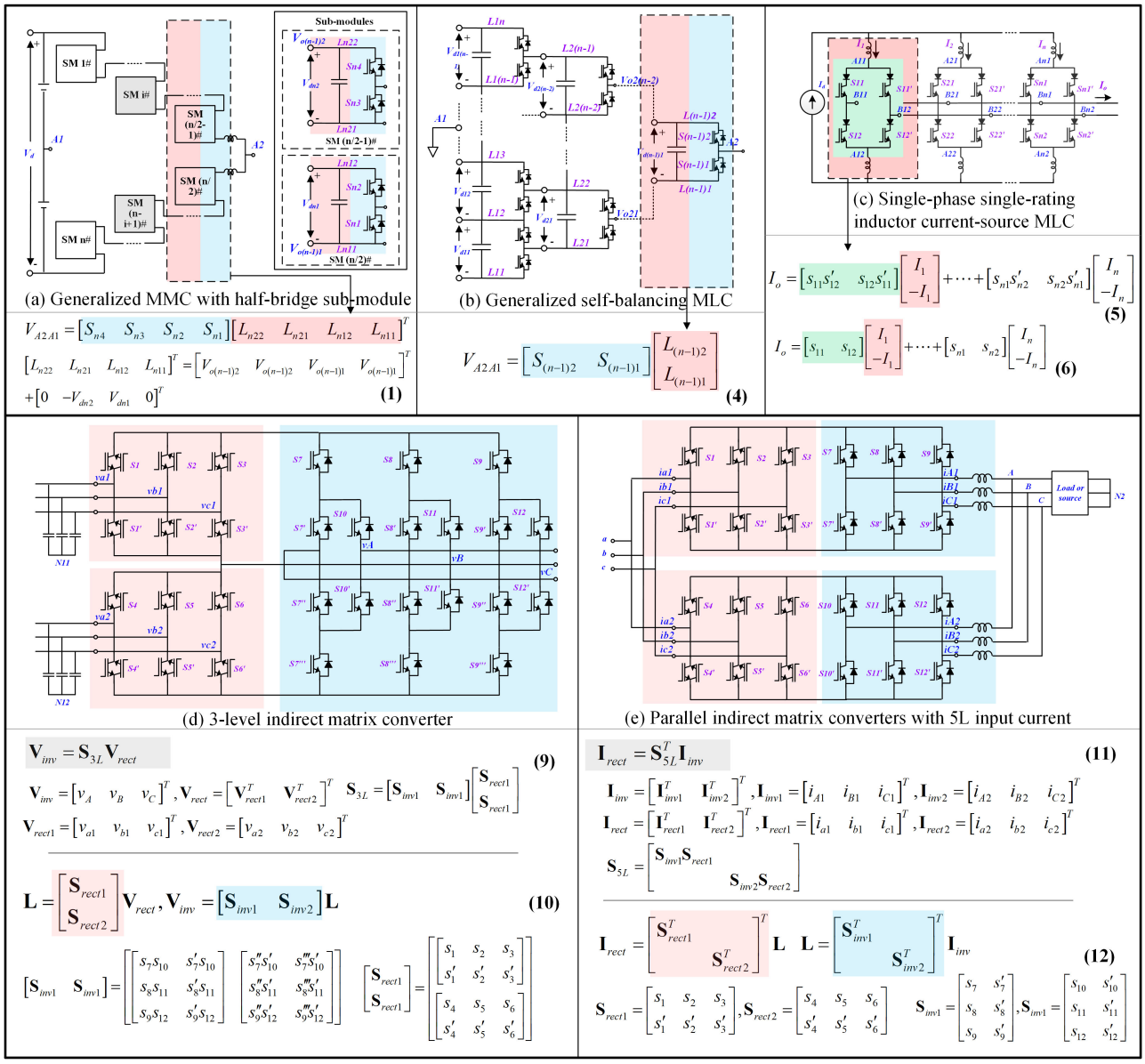


Fig. 2. Investigation of mainstream converters. (a) Generalized MMC with half-bridge sub-module. (b) Generalized self-balance MLC. (c) General multilevel CSCs. (d) 3-level (voltage) and (e) 5-level (current) matrix converters are presented with associated mathematical representations to demonstrate the common topological features of all three types of MLCs.

Substitute (2) into (1), we have the extended model of V_{A2A1}

$$V_{A2A1} = \begin{bmatrix} S_{n4} & S_{n3} & S_{n2} & S_{n1} \end{bmatrix} \times \left\{ \begin{bmatrix} S_{(n-1)4} & S_{(n-1)3} & & \\ S_{(n-1)4} & S_{(n-1)3} & & \\ & & S_{(n-1)2} & S_{(n-1)1} \\ & & S_{(n-1)2} & S_{(n-1)1} \end{bmatrix} \times \begin{bmatrix} L_{(n-1)22} \\ L_{(n-1)21} \\ L_{(n-1)12} \\ L_{(n-1)11} \end{bmatrix} + \begin{bmatrix} 0 \\ -V_{dn2} \\ V_{dn1} \\ 0 \end{bmatrix} \right\}. \quad (3)$$

If the stage $n-2$ of MMC is considered, (3) will be extended with the information of next neighboring SMs (associated with $[S_{(n-2)4}\, S_{(n-2)3}\, S_{(n-2)2}\, S_{(n-2)1}]$ and $[L_{(n-2)22}\, L_{(n-2)21}\, L_{(n-2)12}\, L_{(n-2)11}]^T$). In such a way, V_{A2A1} can contain all SMs information.

Voltage-Source Example 2: Circuit form of generalized self-balancing MLC in [38] is shown in Fig. 2(b).

Equation (4) is for the rightmost half-bridge and can also be expanded with all the clamping capacitors and associated switch networks through iterative substitution.

Next, a general current-source MLC example is presented to illustrate the common structure of this type of MLC.

Current-Source Example: Circuit form of single-phase single-rating inductor current-source MLC is shown in Fig. 2(c) [48].

Normally, the upper switches are complementary (e.g., $S11$ and $S'11$), which simplifies (5) into (6).

Note that two types of vectors are implemented: one represents the switching states, and another one represents the available input currents.

The same structure can also be found in H-bridge current-source inverter in [49]. It can be considered as the counterpart of a conventional VSC with floating capacitor H-bridge cells [53] and shares similar modulation schemes and control strategies.

Through the above examples, it is straightforward to summarize the common structure of a voltage-source MLC as the dot product of two vectors

$$v = S \cdot L \tag{7}$$

where v denotes the output voltage, S denotes the switching state vector, L denotes the voltage level vector. Such equation can also be written for any intermediate output voltages inside the voltage-source MLCs. In such a unified way, all topologies discussed in [43] can be systematically represented.

While the common structure of a current-source MLC is the dot product of two vectors

$$i = S \cdot I \tag{8}$$

where i denotes the output current, S denotes the switching state vector, I denotes the current vector. Such an equation can also be written for any SM output currents inside the MLCs.

Finally, for matrix converters, two examples are presented to illustrate their topological features.

Matrix Converter Example 1: A three-level (voltage) matrix MLC is shown in Fig. 2(d). The detailed analysis of a similar 3L matrix MLC using NPC was given in [27].

Assume there is an intermediate voltage vector such as $L = [L_3\ L_2\ L_2\ L_1]^T$, the voltage relationship between rectifier parts and inverter part can be expressed as (10), where the equations of the two parts have the same structures of voltage-source MLC and current-source MLC as shown before, respectively.

Matrix Converter Example 2: In Fig. 2(e), input current with 5 levels can be generated by the parallel indirect matrix converters system, while only 3 levels can be expected if two converters are synchronized as described in [54].

Assume the intermediate current vector is $L = [L_1\ -L_1\ L_2\ -L_2]^T$, the current relationship between rectifier parts and inverter part can be expressed as (12), which has the same structure of current-source MLC.

This section investigates the common structures among all three kinds of MLCs with associated matrix representations. It is demonstrated that the outputs of MLCs can be represented in a unique dot product of two matrices. For complex circuits, the models can be developed iteratively. In such way, the similarity and difference of various MLCs can be exhibited in a mathematical way, and the derivation method for one topology can be mathematically transformed into another one which will greatly facilitate the derivation process.

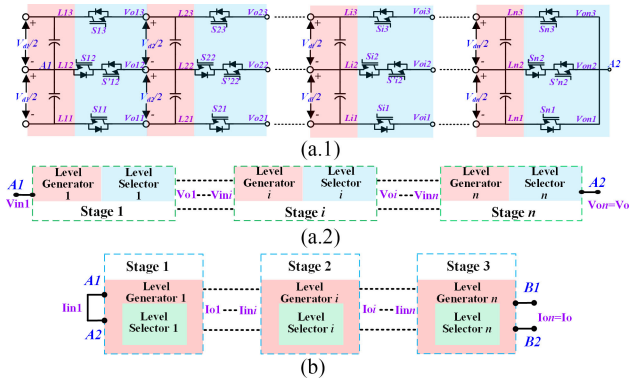


Fig. 3. (a.1) Generalized SMC with clear division of stages, and the representation of multilevel topology based on the concept of the stage for (a.2) voltage-source MLC, (b) current-source MLC.

IV. Representing Multilevel Converters Through Stage and Node-Branch Diagram With Unified Matrix Models

In the literature, similar concepts toward the MLC structure have been developed, e.g., level lines, layers [38]–[41], which easily leads to confusions under different semantics toward different types of topologies. Based on the summary of common structures of MLC topologies in the previous section, all three types of MLCs can be represented in a unified mathematical form. In this section, such a concept is defined more precisely and will be discussed thoroughly with demonstration examples to help better understand the mathematical models and the topological relationships of various MLC topologies.

A. Proposed Concept of Stage

To represent voltage-source and current-source MLC in a generalized manner, the concept of the stage is introduced in this section. In the proposed concept, a multilevel topology is composed of several stages, as the general SMC shown in Fig. 3(a.1). It can be naturally divided into several cascaded structures and each of the structure consists of a stacked capacitor bank for level generation, and a switch network linked this bank to select the generated voltages. And such structure is defined as the stage which can be utilized to represent all kinds of voltage-source MLCs as the conceptual diagram shown in Fig. 3(a.2).

In the same way, a current-source MLC is considered as a composition of several consecutively connected stages as shown in Fig. 3(b). Each stage can have single or multiple inputs and single or multiple outputs with different circuit appearance. A stage can be further decomposed into a combination of LGs and LSs:

1) An LG is a circuit responsible for generating or retaining the desired voltage/current levels.
2) An LS is a circuit responsible for selecting the proper voltage/current levels that generated from the previous LG.

The typical structure of a stage is composed of an LG and an LS as shown in dotted circuits in Fig. 2(a)–(c). While a matrix

MLC can be considered as a combination of voltage-source MLC with a virtual voltage source and current-source MLC with a virtual current source.

For all three types of MLCs, the physical switches are abstracted into the NBD. The topology synthesis and derivation are realized by designing and manipulating the stages with NBD. Details on the proposed concepts and an NBD will be presented in Section IV-B.

The stage-based common structure of MLC with shared dc link shows that a stage has a complete voltage/current level output capability, which can be considered as the smallest unit of functional circuits in a topology. Two-level topologies can be considered special cases from the stage-based point of view.

The connection rule of LG and LS in a stage is that the number of input terminals of an LS and the number of output terminals of an LG must be the same when they are to be connected. After connection, the generated levels (from an LG) can be selected by the subsequent LS. By coordinating the behaviors of all the LSs, desired output levels can be obtained. The procedure is also known as modulation. Since there is no restriction on the switching frequency of the LSs, the coupling between an LG and an LS can be either high frequency or low frequency in the proposed concept. Examples are given in following sections for better understanding of the concept of stage and the NBD.

B. Node-Branch Diagram and Unified Matrix Models of MLCs

The NBD has been a useful tool to represent the electrical topologies [52], [55]–[57]. It provides a general way to present the multilevel topologies. However, conventionally, the NBD cannot reveal the structural synthesis of a multilevel topology. In this article, this diagram is combined with the concept of the stage, providing an efficient and generalized approach to represent and derive topologies. The definitions of node and branch are as follows.

1) *Node:* A node is an abstract point in an NBD. For a physical circuit, a node can represent the terminal of electrical components or any chosen positions in a lumped circuit.
2) *Branch:* A branch is a line segment joining two nodes. While a branch represents the conductor connecting two chosen points in a lumped circuit. All the branches in NBD are not directed, such that all the associated nodes have equal rights.

In a multilevel circuit, the power electronic switch is abstracted as a special NBD that can be controlled. From the signal flow point of view, it can have two states. One is the state of signal transmission, one is the state of the signal block. Furthermore, the switching functions can also be developed for each NBD as following matrix representation:

$$X = S * L \tag{13}$$

where X denotes the output voltage/current matrix of an arbitrary stage, S denotes the LS matrix of this stage through basic bi-logic representation (value 1 for switch "ON," value 0 for switch "OFF"), L denotes the LG matrix of the same stage, $*$ represents the most basic matrix multiplication. With that, the topological synthesis and derivation process can be considered as basic linear equation calculation. While the topology simplification process is the transformation of equations.

For each topology, the NBD can be drawn based on the concept of the stage. To better explain the concept of stage and the NBD, examples are given in the following sections.

C. Commonly Used Level Generators, Level Selectors of Voltage-Source MLCs

Considering the generality of multilevel topologies, the basic LGs and LSs of voltage-source MLC are first introduced in both circuit form and node-branch form in the following context.

First, the circuit form of n-input-n-output (n-to-n) LG is shown in Fig. 4(a). Such a LG is the most basic component of a voltage-source multilevel topology. Each input terminal A_j can be chosen as the reference point ($j = 1, 2, \ldots, n$), which can be arbitrarily selected. Voltage levels are generated by the linked dc source which is named as V_{di} for the ith dc source. In general, the dc sources can either be the outputs of dc–dc converters, or simply ideal voltage sources, or capacitor buffered voltages from the front ends. LEVELi means the generated voltage of the ith output terminal relative to the reference point, $i = 1, 2, \ldots, n$. Node-branch form of the n-to-n LG is also shown in Fig. 4(a). When drawing an NBD, the sources are neglected while only levels remain, and the level must be labeled using the term LEVELi or Li to indicate the voltage level information. The associated LG vector is expressed as (14).

The arbitrarily selected input terminal is served as a reference to simplify the representation of circuit voltages and will not change the difference between adjacent terminal voltage potentials. In Fig. 4(b), a 1-to-n LG is shown, while A1 is the reference point (usually chosen as the mirror symmetry point of the circuit, also known as a neutral point).

Second, the n-input-($n - 1$)-output (n-to-(n-1)) LS is shown in Fig. 4(c). This type of LS, which is commonly used as a part of the generalized voltage-source MLC [38], is composed of connected half bridges. The associated LS matrix is written as (15).

The input nodes of an LS can be connected to an LG or an LS with compatible output terminals (i.e., to form an n-to-m LS, in which $n > m$, one can link ($n - m$) LS with input-output terminals following such order: n-to-(n-1) LS, (n-1)-to-($n - 2$) LS, …, ($m + 1$)-to-m LS. If $m = 1$, the connected LGs form the main topology of a general ANPC [58]).

In literature, the LS with redundant switches called switching cell arrays can be found in [59]. Another type of voltage LS using active bidirectional switches is shown in Fig. 4(d). The associated LS matrix is written as (16).

Practically, to achieve the same function, whether the polarity of the internal switch of the selector is unidirectional or bidirectional can be determined by considering the designer's requirements based on the principle of simplification (details will be presented in Section VI). The simplest example is the three-level TNPC converter shown as in Fig. 4(h) [60].

Note that only single-phase topologies are considered here. The derivation of multiphase converters can be treated as a

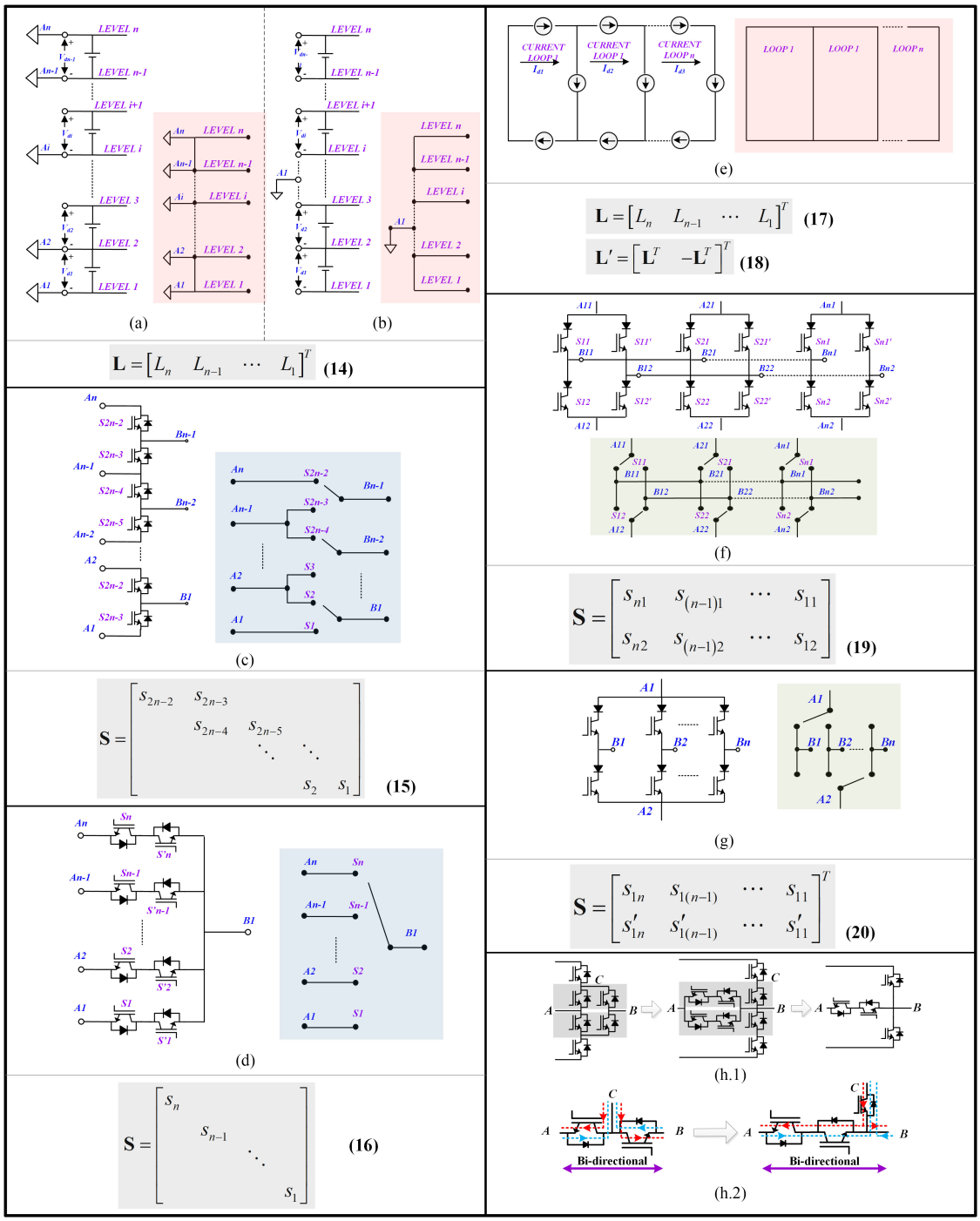


Fig. 4. Commonly used level generators, level selectors of MLCs. (a) n-to-n level generator. (b) 1-to-n level generator. (c) n-to-(n-1) level selector. (d) n-to-1 level selector. (e) 1-to-n level generator for current-source MLC. (f) n-to-1 level selector for current-source MLC. (g) 1-to-n-level selector for current-source MLC. (h) 3-level TNPC.

permutation and combination of the data of the derived phase-leg "topology database." For the multiphase converter design, the derivation is still a step-by-step process. One can decide to use: 1) identical phase-leg topology, 2) different phase-leg topology. While the topology of each leg is still needed to be derived before the combination of them to form a converter, which means the proposed method should be carried out first to form the database of possible topologies of single-phase leg.

For example, if a four-leg converter for four-wire application is to be designed, either identical phase legs or different phase legs can be utilized. Such a hybrid combination of legs will result in various multiphase topologies. There can be 16 possible solutions, e.g., 4 same legs, 3 same legs with 1 different leg, 2 same legs with 2 different legs, …. Assume four identical phase legs are utilized to form a converter toward four-wire application. Next step is to choose a topology for each phase

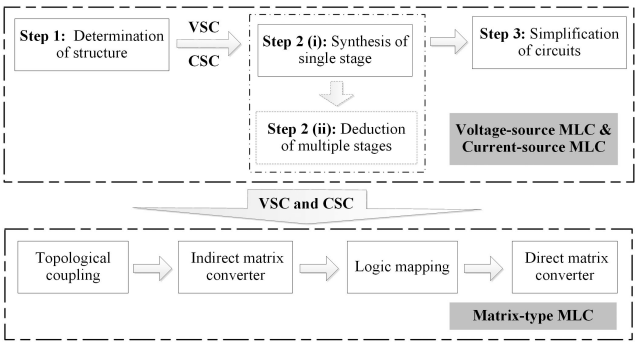


Fig. 5. Unified method of synthesis and derivation of MLCs.

leg, e.g., two-level phase leg. In this case, this derived converter is the conventional four-leg two-level converter.

To summarize, derivation of phase-leg topology is needed to be completed before the multiphase converter derivation process. This article is intended to be focused on the phase-leg derivation since such work will lay the fundamentals of multiphase scenarios.

D. Commonly Used Level Generators, Level Selectors of Current-Source MLCs

The basic LGs and LSs of current-source MLC are introduced in both circuit form and node-branch form in the following context.

First, the 1-input-*n*-output (1-to-*n*) current LG is shown in Fig. 4(e). This type of LG is normally expected as the general element of current-source MLCs, which can be found in [46]. The LG vector is expressed as (17).

The output current level, however, could be $2n + 1$ for such LG, which is different from its voltage counterpart. Therefore, the LG vector is normally expanded into (18).

Each current loop is generated by the linked dc source which is named as I_{di} for the *i*th dc source. In general, the dc sources can either be the outputs of dc-dc- converters, or simply ideal current sources, or inductors buffered current from the front end. Similarly, in an LG, the sources are neglected while only loops remain. The loop must be labeled using the term LOOPi or Li to indicate the current loop information.

Second, the *n*-input-1-output (*n*-to-1) current LS is shown in Fig. 4(f). This type of LS is composed of parallel connected full bridges [47], [48]. Each full bridge has a two-terminal input port and a two-terminal output port, which are expected to be linked with either LG or LS with compatible terminals. The associated LS matrix is written as (19).

Third, the 1-input-*n*-output (1-to-*n*) current LS is shown in Fig. 4(g). The associated LS matrix is written as (20).

When $n = 3$, this type of LS is a three-phase bridge of CSC, which is very common in practical application.

E. Proposed Topological Synthesis and Derivation Method

Based on the concept of the *stage*, the unified method of synthesis and deduction for various multilevel topologies is proposed and summarized as in Fig. 5.

The first step is to determine the structure of MLC topology, i.e., voltage-source type, current-source type. As for voltage-source MLC, one needs to choose the structure and the number of output levels which is N_V for the required topology to be generated. The following two situations are considered: 1) single-stage structure and 2) multiple-stage structure. For the desired single-stage voltage-source MLC, the number of output levels of the desired stage is N_V, which means a 1-to-N_V LG and an N_V-to-1 LS are needed.

Once the structure is determined, each stage can be considered based on the concept of LG and LS. If the multiple-stage topology is desired, one can determine how a variety of single-stage structures reasonably form a complete voltage-source MLC in accordance with the proposed principles. At last, through the proposed circuit simplification principles, one can get various modified topologies. The details will be presented in Sections V and VI.

The proposed methodology is also valid for current-source MLC. The structure determination is slightly different from voltage-source MLC due to the indirect relationship between desired current levels and current loops

$$N_C = f\left(N'_C\right) \tag{21}$$

in which N_C is the desired count of current levels, $N_C\prime$ is the corresponding count of current loops.

Normally, the function is expected as follows:

$$N_C = 2 \times N'_C + 1. \tag{22}$$

Both single-stage structure and multiple-stage structure of current-source MLCs are considered. For the desired single-stage current-source MLC, the number of output levels of the layer is N_C, which means a 1-to-N'_C LG and an N'_C-to-1 LS are needed. For arbitrary current-source MLC structures with more than one stage, it is more straightforward to determine the levels of each stage than voltage-source MLC. When increasing the stage number, the parallel structure can be used [61]. The superposition principle of the paralleled current outputs of each stage ensures that the output current levels meet the requirements.

For the simplest case, one can connect identical N'_C stages in parallel (only a single loop is generated in each one) to form a current-source MLC with N_C output current levels as shown in Fig. 2(c) ($N'_C = 3$). More details will be presented in Sections V and VI.

As for matrix type MLC, the derived current-source stage and voltage-source stage will be merged into IMC through the concept of virtual dc link. And then the logic mapping will be carried out to convert IMC into associated DMC. The details will be presented in Section VIII.

In general, the unified method can facilitate the design process. For example, if we want to find out an optimal topology for application requirement set $\{R\}$, the conventional method will easily result in repetitive derivation loops. The existing topologies forms a "topology database" set $\{T\} = \{T_1 \bigcup T_2\}$, where subset $\{T_1\}$ satisfies $\{R\}$, while subset $\{T_2\}$ does not. If the new topology set $\{N\}$ can be derived and added into the set $\{T\}$ to form a new database set $\{NT\} = \{N \bigcup T\}$, then, we can verify if optimal topology $o \in \{N\} \subset \{NT\}$. In a conventional way, we can only add a set $\{NT\}$ with a small

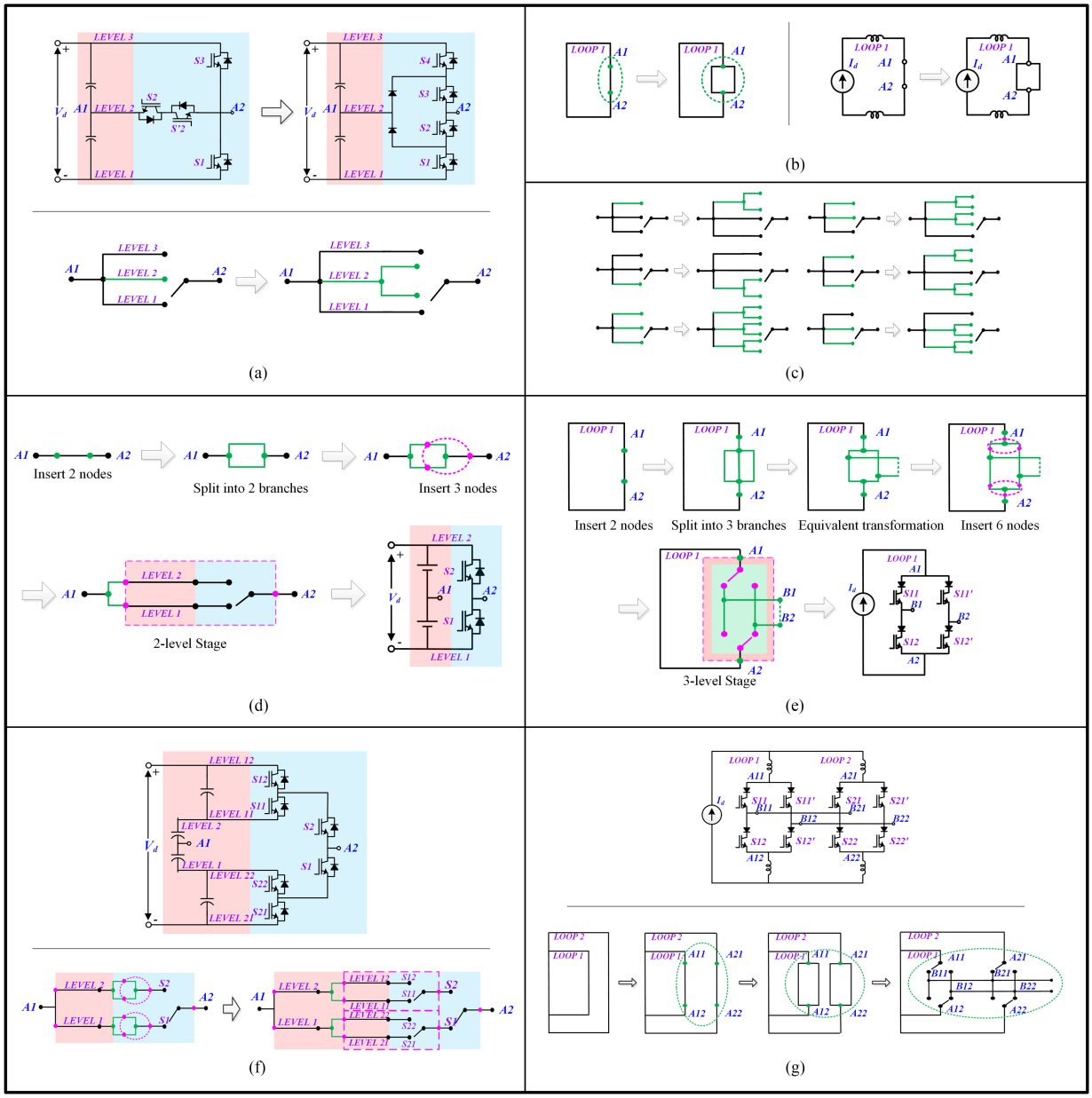


Fig. 6. Examples of synthesis of single-stage topologies through principle 1.1–1.3. (a) The process of branch split for the voltage-source circuit. (b) The process of branch split for the current-source circuit. (c) Other possible synthesis results of (a). (d) The process of circuit expansion for the voltage-source converter. (e) The process of circuit expansion for the current-source converter. (f) 4L ANPC stage with six switches. (g) 5L single-rating inductor current-source MLC stage.

number of topologies due to the lack of systematic derivation approach. Once $o \in \{N\} \subset \{NT\}$ is not satisfied, the whole process will have to go through again. Alternatively, if the derivation approach covers as many topologies as possible, we will have a set $\{NT\}$ as large as possible. Such that, the possibility of finding $o \in \{N\} \subset \{NT\}$ is increased and the unnecessary iterative process is avoided.

In summary, the proposed concept of the stage can unite all three types of MLCs in a common form. It is envisaged that the new perspective on the MLCs topology derivation presented in this paper can be a useful tool for researchers when designing topologies. In particular, the MLC topologies are represented in a mathematical manner, therefore, systematic synthesis and derivation can be realized not only in the circuit level but also in the abstract level. It can greatly facilitate the manual design process and provide the potential for computer-aided design and analysis with clear rules.

V. Synthesis of Single-Stage Topologies

A. Basic Principles of General Synthesis Process

Principle 1.1: Nodes can be inserted into the same voltage level/current loop.

Principle 1.2: Branches of the same voltage level/current loop can be split into multiple ones.

The split branches can change both the structure and operation of the stage, but the output is equivalent as shown in Fig. 6(a) and (b). Based on principle 2, there are seven possible synthesis

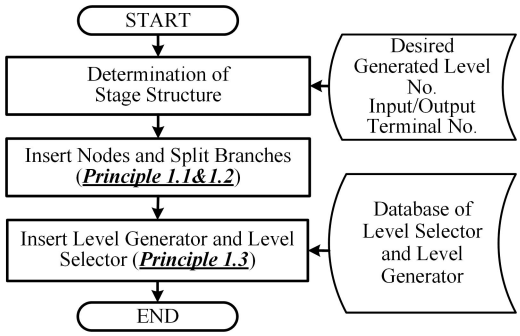


Fig. 7. Synthesis procedure of a single-stage circuit.

results in total which are associated with seven possible topologies [see Fig. 6(c)]. While Fig. 6(a) shows one possible synthesis process from 3L TNPC topology to NPC topology.

Principle 1.3: Circuit composed of insert nodes and split branches based on Principle 1 and 2 can be expanded into LGs and/or LSs with consistent terminals and compatible polarity.

After the process of node insertion and branch split, the expanded circuit changes both the structure and operation of the original stage and forms a new one as shown in Fig. 6(d) and (e). Theoretically, circuits with any count of terminals can be synthesized based on Principle 1.1 and 1.2, which will lead to the synthesis of any single-stage topologies.

B. Synthesis Flow Chart

The synthesis procedure of a single-stage circuit is summarized in Fig. 7. One can arbitrarily select the desired level number and input/output terminal number, and utilize the commonly used LGs, LSs of MLCs to develop a large number of single-stage topologies.

C. Demonstration Examples

To provide a clear understanding of the proposed principles, a few examples using existing multilevel topologies are presented here.

Stage synthesis Example 1: The circuit form of the four-level ANPC stage with six switches is shown in Fig. 6(f) [62]. The synthesis process is also shown. Once three nodes are inserted into each branch of the 2-to-1 LS, the following process of each branch is just the repeat of Fig. 6(d).

Stage synthesis Example 2: The circuit form of 5L single-rating inductor current-source MLC stage with eight switches is shown in Fig. 6(g) [48]. The branches with inserted four nodes are split into four branches, then, 2-to-1 LS for current-source MLC is used to form the final topology.

VI. Deduction of Multiple Stages Topologies

A. Concepts of Base Stage and Extended Stage

Two concepts are introduced here for the general derivation process: 1) Base stage is chosen as the stage that is directly linked with power sources in a topology. 2) The extended stage is the stage that is used to extend the number of voltage/current levels in a topology.

For example, a shared dc-link MLC has normally only one isolated source (or potentially several non-isolated sources) and can have several extended stages but only one base stage.

B. Basic Principles of the General Derivation Process

Principle 2.1: Stages for voltage-source MLC with a consistent number of terminals can be docked with each other.

Fig. 8(a) shows three stages with different terminals waiting to be derived into a voltage-source MLC. The matrix representations are written as (23).

One can choose a 2-to-3 stage in Fig. 8(a.1) as the base stage to form a 3L bridge as shown in Fig. 8(b). Therefore, the voltage of the dc power supply can be doubled, which means that it has voltage step-up capability. The matrix representation of output voltage is shown as (24). While $[V_{o13}\ V_{o12}\ V_{o11}]^T$ can be solved based on [63] as shown in (25).

Principle 2.2: Stages for current-source MLC with a consistent number of terminals can be connected in parallel.

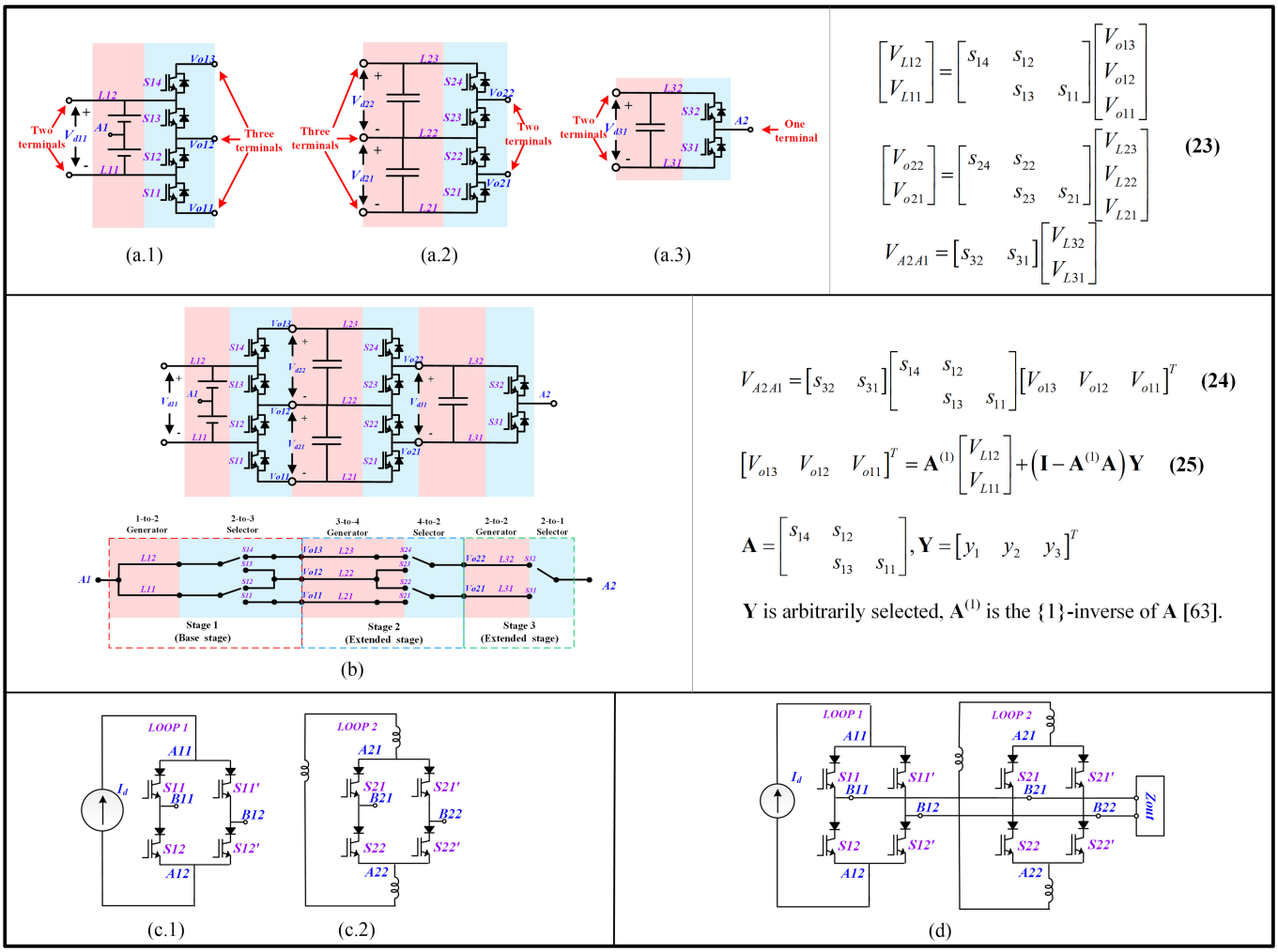
Fig. 8(c) shows two stand-alone stages with 3L current outputs. One can easily connect these two stages to form a 5L current-source MLC as shown in Fig. 8(d), which can be considered as the counterpart of voltage-source MLC with cascaded HBBBs [49], [64]. The matrix representation is the same as single-rating inductor current-source MLC shown in Fig. 6(g).

C. Derivation Flow Chart

The derivation process of the circuit with multiple stages is summarized in Fig. 9. One can arbitrarily select the desired number of total generated levels and choose a base stage and extended stage from the database of a single-stage generated as presented in Section V to form the multistage circuits. The deduction principles can be considered as the extension of topology conformation principles proposed in [42], while the similar modularization is also addressed in the derivation process.

VII. Simplification of Multilevel Converters

After the initial topology obtained by previous steps, its internal redundant parts need to be identified before the process of simplification. The redundant circuit is normally symmetrical and functionally repetitive and can be identified from two perspectives: 1) structure and 2) function. One of the most straightforward approaches is to focus on whether the operation of a symmetric circuit with certain modulation schemes has redundant states in its switching table. This task can easily become cumbersome and unorderly when the level increases. However, with the proposed method, the matrix representations are established to facilitate the simplification process in this section. The equivalence between the original and simplified topologies can also be demonstrated through mathematical operations (for single-stage scenarios, refer to [65] which is for simplification of ANPC converters using matrix models.)



$$\begin{bmatrix} V_{L12} \\ V_{L11} \end{bmatrix} = \begin{bmatrix} s_{14} & s_{12} \\ & s_{13} \quad s_{11} \end{bmatrix} \begin{bmatrix} V_{o13} \\ V_{o12} \\ V_{o11} \end{bmatrix}$$

$$\begin{bmatrix} V_{o22} \\ V_{o21} \end{bmatrix} = \begin{bmatrix} s_{24} & s_{22} \\ & s_{23} \quad s_{21} \end{bmatrix} \begin{bmatrix} V_{L23} \\ V_{L22} \\ V_{L21} \end{bmatrix} \quad (23)$$

$$V_{A2A1} = \begin{bmatrix} s_{32} & s_{31} \end{bmatrix} \begin{bmatrix} V_{L32} \\ V_{L31} \end{bmatrix}$$

$$V_{A2A1} = \begin{bmatrix} s_{32} & s_{31} \end{bmatrix} \begin{bmatrix} s_{14} & s_{12} \\ & s_{13} \quad s_{11} \end{bmatrix} \begin{bmatrix} V_{o13} & V_{o12} & V_{o11} \end{bmatrix}^T \quad (24)$$

$$\begin{bmatrix} V_{o13} & V_{o12} & V_{o11} \end{bmatrix}^T = \mathbf{A}^{(1)} \begin{bmatrix} V_{L12} \\ V_{L11} \end{bmatrix} + \left(\mathbf{I} - \mathbf{A}^{(1)}\mathbf{A}\right)\mathbf{Y} \quad (25)$$

$$\mathbf{A} = \begin{bmatrix} s_{14} & s_{12} \\ & s_{13} \quad s_{11} \end{bmatrix}, \mathbf{Y} = \begin{bmatrix} y_1 & y_2 & y_3 \end{bmatrix}^T$$

Y is arbitrarily selected, $\mathbf{A}^{(1)}$ is the {1}-inverse of **A** [63].

Fig. 8. Examples of deduction of multiple stages topologies through principle 2.1–2.2.

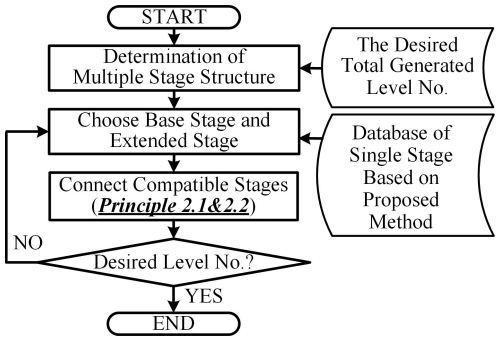


Fig. 9. Derivation procedure of a multiple-stage circuit.

Principle 3.1: Redundant circuits located between several interconnected stages can be simplified without changing the output level range.

Fig. 10(a) shows the simplification process of a nine-level (9L) converter proposed in [66]. Two circuits are identified as redundant circuits by red dotted lines and then simplified into the bottom topology of Fig. 10(a).

Assume intermediate variables V_{oX1}, V_{oX2}, V_{oY1}, V_{oY2} in original topology [see labels in Fig. 10(a)], then, the following two equations can be written:

$$V_{A2A1} = \mathbf{S}_3 \mathbf{V}_{XY2} \quad (26)$$

where $\mathbf{S}_3 = [\, s_{36} \quad s_{35} \,]$, $\mathbf{V}_{XY2} = [\, V_{oX2} \quad V_{oY2} \,]^T$ and

$$\mathbf{V}_{XY2} = \mathbf{S}_2 \mathbf{V}_{XY1} \quad (27)$$

where V_{XY2}, S_2, and V_{XY1} are as follows:

$$\mathbf{S}_2 = \begin{bmatrix} \mathbf{S}_{21} & \mathbf{O} \\ \mathbf{O} & \mathbf{S}_{22} \end{bmatrix}, \mathbf{S}_{21} = \begin{bmatrix} s_{28}s_{34} & s_{28}s_{33} & s_{27}s_{34} & s_{27}s_{33} \end{bmatrix},$$

$$\mathbf{S}_{22} = \begin{bmatrix} s_{26}s_{32} & s_{26}s_{31} & s_{25}s_{32} & s_{25}s_{31} \end{bmatrix},$$

$$\mathbf{V}_{XY1} = \begin{bmatrix} V_{oX1} & V_{oX1} & V_{oX1} & V_{oX1} & V_{oY1} & V_{oY1} & V_{oY1} & V_{oY1} \end{bmatrix}^T$$

$$+ \begin{bmatrix} 0 & -V_{d32} & V_{d32} & 0 & 0 & -V_{d31} & V_{d31} & 0 \end{bmatrix}^T.$$

Equation (26) shows that the terminal output voltage of the 9L converter before simplification is determined by both the output voltage of redundant circuits and the associated LS, while (27)

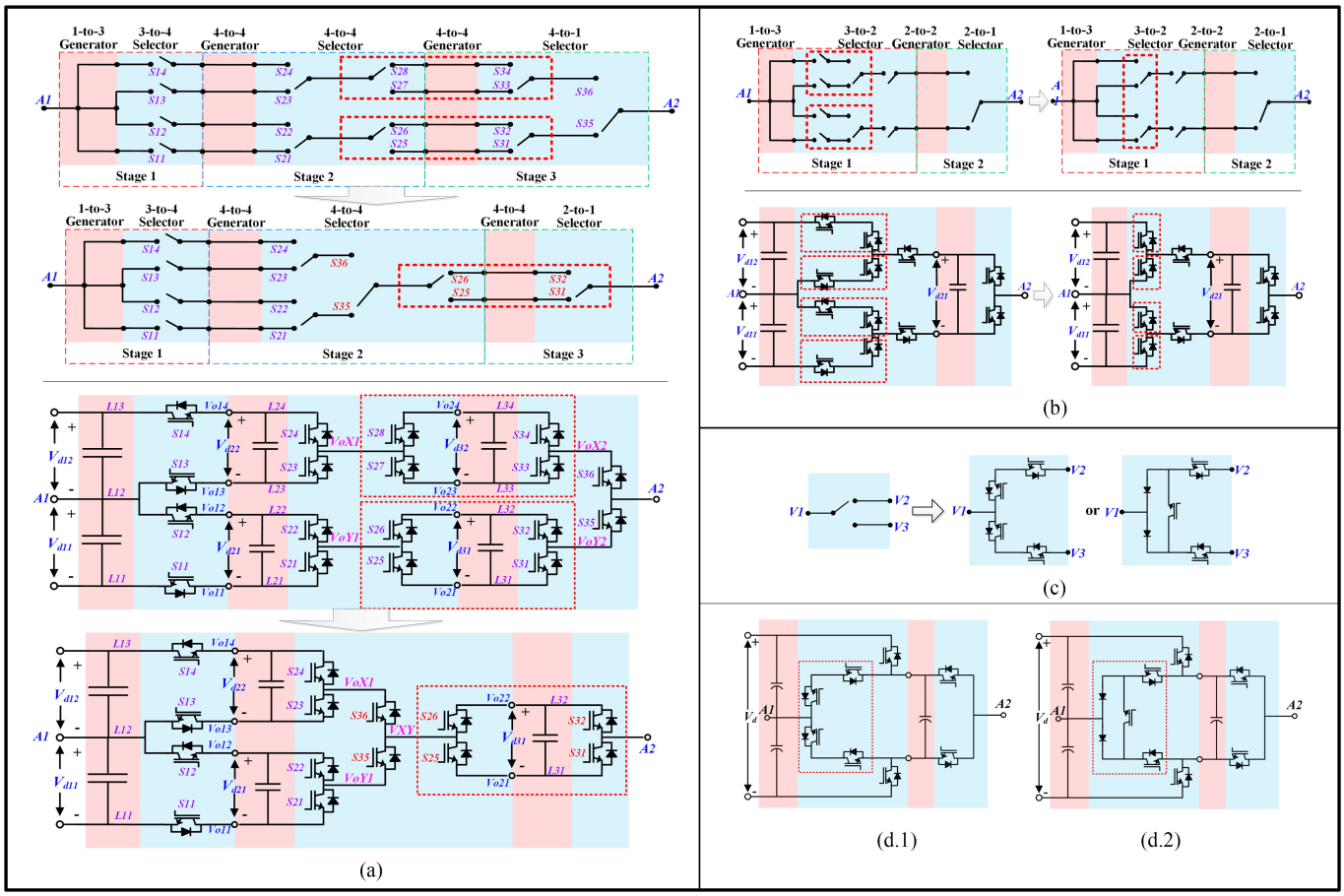


Fig. 10. Examples of simplification of topologies. (a) Simplification process of a 9L converter. (b) Simplification process of a 5L converter. (c) Circuits with same three-pole switching function. (d.1) Eight-switch 5L ANPC converter, (d.2) Seven-switch 5LANPC converter.

means the voltage of redundant circuits are determined by their input voltages and the associated LS.

Assume the switching states of each pair of (S_{28}, S_{26}), (S_{27}, S_{25}), (S_{34}, S_{32}), (S_{33}, S_{31}) are identical, and $V_{d32} = 0$, (26) and (27) can be simplified into the following:

$$V_{A2A1} = \mathbf{S}_{22}\mathbf{V}'_{XY1} \tag{28}$$

where

$$\mathbf{V}'_{XY1} = \left[\begin{bmatrix}\mathbf{V}''_{XY1} & \mathbf{V}''_{XY1} & \mathbf{V}''_{XY1} & \mathbf{V}''_{XY1}\end{bmatrix}^T \times \begin{bmatrix}s_{36} & s_{35}\end{bmatrix}^T + \begin{bmatrix}0 & -V_{d31} & V_{d31} & 0\end{bmatrix}^T\right],$$

$$\mathbf{V}''_{XY1} = \begin{bmatrix}V_{oX1} & V_{oY1}\end{bmatrix}.$$

As (28) indicates, the position of the LS (S_{36}, S_{35}) and redundant circuits can be exchanged when the above assumption is satisfied. The resulting structure of matrix representation will not affect the terminal output voltage V_{A2A1}. Since the intermediate variable $\mathbf{V}''_{XY1}$ can be expressed based on the virtual input voltage V_{XY}, (28) can be further simplified using$V_{XY} = \mathbf{S}_3\mathbf{V}''_{XY1}$, then, the simplified structure can be expressed as follows:

$$V_{A2A1} = \mathbf{S}_{22}\mathbf{V}_{XY} \tag{29}$$

where $\mathbf{V}_{XY} = [[V_{XY}\ V_{XY}\ V_{XY}\ V_{XY}]^T + [0\ -V_{d31}\ V_{d31}\ 0]^T]$.

As such, according to the simplified matrix representation, only one H-bridge is necessary for this topology and the whole circuit can be simplified into bottom topology form as shown in Fig. 10(a). Since the matrix representation demonstrates the fundamental operating principles of the circuit, one can utilize these matrix models to control the simplified topology and develop associated modulation schemes.

Principle 3.2: Redundant circuits within one stage can be simplified without changing the interstage properties.

Fig. 10(b) shows the simplification process of a 5L converter proposed in [23]. Redundant circuits are identified by red dotted lines and then simplified into the right-hand topology.

Inference 1: A pair of neighboring LG and LS (or we call it a stage in a general way) that does not increase the output voltage/current levels can be simplified into neighboring stages.

Inference 2: Circuits with the same function can be exchanged with each other without changing the input–output relationship of the substituted area.

Fig. 10(c) shows that two circuits have the same three-pole switching function [67]. While Fig. 10(d) shows that the existing eight-switch five-level ANPC converter is functionally equivalent to seven-switch five-level ANPC converter if the three-pole switch is substituted [68]. The matrix representations remain the same.

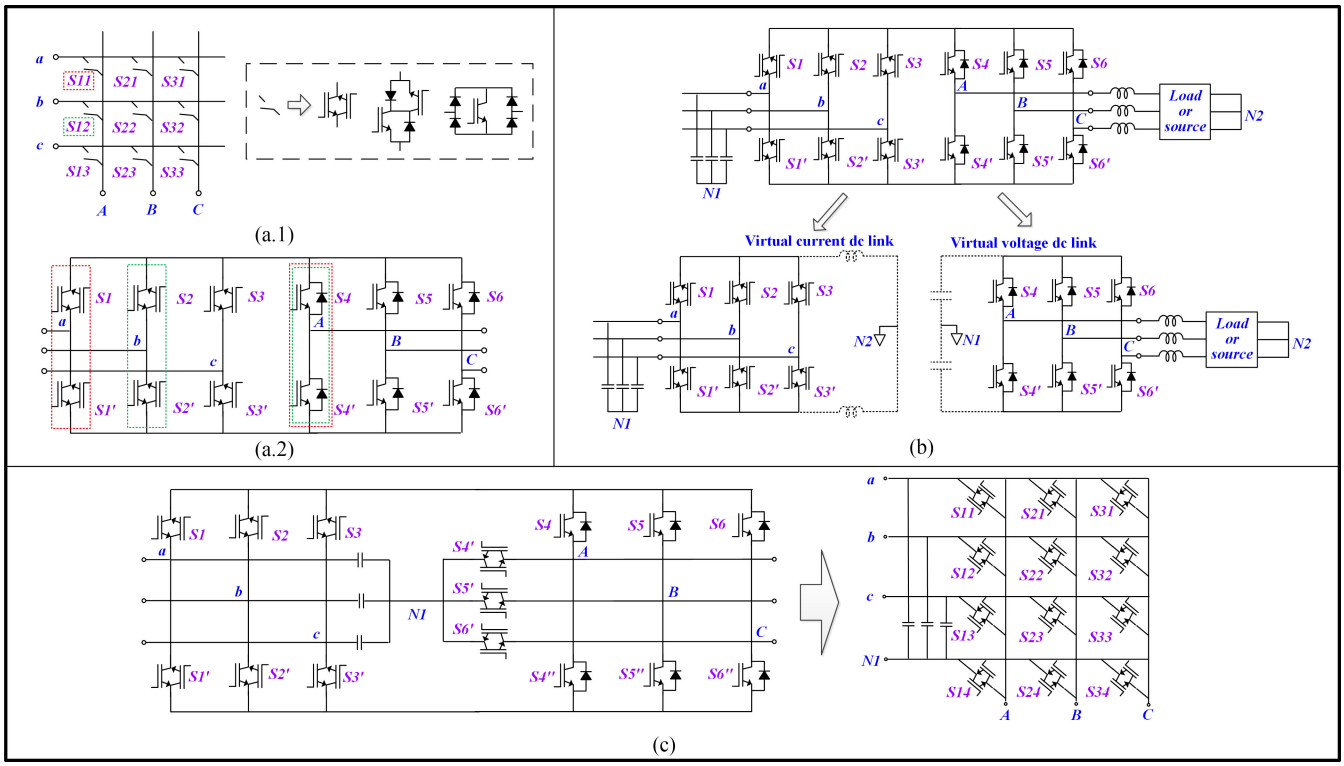


Fig. 11. Topological relationship between matrix converter and voltage/current-source converter and the derivation examples of multilevel matrix converter.

VIII. Topological Derivation for Multilevel Matrix Converters

In addition to VSCs and CSCs, both DMC and IMC [shown in Fig. 11(a)] have been studied for decades due to the attractive features such as minimization of dc energy storage components, improved compactness, direct ac-to-ac conversion with controllable input power factor and output frequency [69]. To improve the output waveform quality, the MLC concept has been applied to DMCs and IMCs [70]. However, one can hardly derive multilevel matrix converters based on the conventional methods due to the topological difference from voltage-source and current-source MLCs.

A. Topological Relationship Between Matrix Converter and Voltage/Current-Source Converter

The logic mapping relationship between DMCs and IMCs is briefly reviewed based on matrix converter theory [71], [72]. For a 2L DMC and IMC, the switching logic is straightforward as shown in (30) and (31), where *S* is the switching function matrix of DMC [see Fig. 11(b)], while the $S_{\rm inv}$ and $S_{\rm rect}$ are switching function matrix of inverter part (*S*1–*S*3, *S*1'–*S*3') and rectifier part (*S*4–*S*6, *S*4'–*S*6') in IMC, respectively

$$\mathbf{V}_{\rm inv} = \mathbf{S}\mathbf{V}_{\rm rect}, \quad \mathbf{I}_{\rm rect} = \mathbf{S}^T\mathbf{I}_{\rm inv} \tag{30}$$

$$\mathbf{S} = \mathbf{S}_{\rm inv}\mathbf{S}_{\rm rect} \tag{31}$$

where

$$\mathbf{S} = \begin{bmatrix} s_{11} & s_{12} & s_{13} \\ s_{21} & s_{22} & s_{23} \\ s_{31} & s_{32} & s_{33} \end{bmatrix}, \mathbf{S}_{\rm inv} = \begin{bmatrix} s_4 & s'_4 \\ s_5 & s'_5 \\ s_6 & s'_6 \end{bmatrix}, \mathbf{S}_{\rm rect} = \begin{bmatrix} s_1 & s_2 & s_3 \\ s'_1 & s'_2 & s'_3 \end{bmatrix}.$$

The gating signal of every single switch in DMC can be generated by combining signals of associated switches in IMC. For example, to drive s_{11}, one can use signals of the first leg switches of inverter part and rectifier part in IMC which are denoted as vectors A_1, a_1 as shown in (32), respectively. The same generation process can also be carried out for s_{12} as shown in (33). In such a way, a DMC can be considered as a virtual IMC with the same PWM logic

$$s_{11} = \mathbf{A}_1\mathbf{a}_1 = \begin{bmatrix} s_4 & s'_4 \end{bmatrix} \begin{bmatrix} s_1 \\ s'_1 \end{bmatrix} \tag{32}$$

$$s_{12} = \mathbf{A}_1\mathbf{a}_2 = \begin{bmatrix} s_4 & s'_4 \end{bmatrix} \begin{bmatrix} s_2 \\ s'_2 \end{bmatrix}. \tag{33}$$

In a given operating state, the rectifier and inverter parts of the IMC can be treated as a CSC and VSC as shown in Fig. 11(b). The virtually linked filters can be considered as the virtual dc link with time-varying values. As for the rectifier part, its dc side is always linked with the inverter-side filters (i.e., inductors) through the devices (*S*4–*S*6, *S*4'–*S*6') under certain switching pattern (same principle for inverter part operation). Through the virtual dc link concept (the virtual LG can also be implemented), derivation principles of voltage-source and

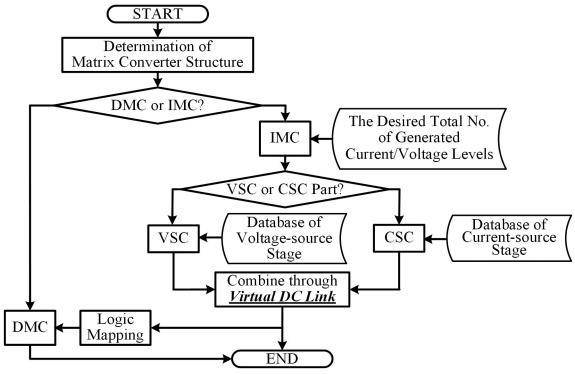


Fig. 12. Derivation procedure of a matrix type MLC through the proposed method.

current-source MLCs can be utilized for multilevel indirect matrix converters. Afterward, the associated direct matrix can also be derived based on the logic mapping relationship.

B. Derivation Based on Virtual DC Link Concept

The derivation process of matrix type MLC based virtual dc link concept is summarized in Fig. 12. Either DMC or IMC can be derived through the proposed method. For IMC topologies, both VSC part and CSC part can be derived respectively through the process introduced in Sections V–VII. Then, the chosen VSC and CSC parts can be combined through the virtual dc link to form the IMC topology. At the same time, the associated DMC topology can be obtained through logic mapping.

C. Demonstration Examples

To better understand the derivation process of matrix MLCs, a matrix MLC example is demonstrated below.

Matrix Converter Example: In Fig. 11(c), the derivation process of another 3-voltage-level matrix MLC based on the three-level voltage-source T-type NPC converter is demonstrated. The virtual three-level dc link is derived through the neutral point of rectifier-side filters. While the corresponding 3L DMC version can be derived based on the same logic mapping process of Fig. 11(b) which can be found in [73]

$$\mathbf{V}_{\text{inv}} = \mathbf{S}_{3L}\mathbf{V}_{\text{rect}} \tag{34}$$

where $\mathbf{V}_{\text{inv}} = [\,v_A\ v_B\ v_C\,]^T$, $\mathbf{V}_{\text{rect}} = [\,v_a\ v_b\ v_c\ v_{N1}\,]^T$.

To derive S_{3L}, assume the voltage vector of virtual dc link is $L = [L_3\,L_2\,L_2\,L_1]^T$, $L' = [L_3\,L_2\,L_1]^T$, then

$$\mathbf{L} = \mathbf{S}_{\text{rect}}\mathbf{V}_{\text{rect}}, \quad \mathbf{V}_{\text{inv}} = \mathbf{S}_{\text{inv}}\mathbf{L}' \tag{35}$$

$$\mathbf{S}_{3L} = \mathbf{S}_{\text{inv}}\mathbf{S}_{\text{rect}} \tag{36}$$

where

$$\mathbf{S}_{3L} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & s_{14} \\ s_{21} & s_{22} & s_{23} & s_{24} \\ s_{31} & s_{32} & s_{33} & s_{34} \end{bmatrix},$$

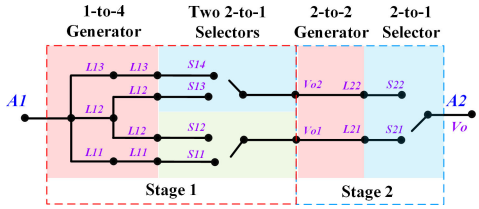


Fig. 13. NBD of 5L-ANPC topology.

$$\mathbf{S}_{\text{inv}} = \begin{bmatrix} s_4 & s'_4 & s''_4 \\ s_5 & s'_5 & s''_5 \\ s_6 & s'_6 & s''_6 \end{bmatrix}, \mathbf{S}_{\text{rect}} = \begin{bmatrix} s_1 & s_2 & s_3 & 0 \\ 0 & 0 & 0 & 1 \\ s'_1 & s'_2 & s'_3 & 0 \end{bmatrix}.$$

IX. Implementation of the Proposed Approach

A. Generated Level Number Estimation Through Matrix Model of MLC

One of the challenges during derivation is the estimation of generated level numbers of derived topologies. As discussed previously, MLCs can be represented as an ordered combination of matrix models through the concepts of the LG and LS. With the help of matrix representation, one can potentially investigate the mathematic properties of both existing and future topologies.

As presented in Sections III and IV, a LG can be considered as a vector, called level vector, noted as *L*. While a LS can be considered as a matrix, noted as *S*. Thus, the outputs of stages in a voltage-source MLC are as follows:

$$\mathbf{V}_{o1} = \mathbf{S}_1\mathbf{L}_1, \ldots, \mathbf{V}_{oi} = \mathbf{S}_i\mathbf{L}_i, \ldots, \mathbf{V}_{\text{on}} = \mathbf{S}_n\mathbf{L}_n. \tag{37}$$

The ith *level vector* ($i > 1$) is a function of neighboring stages:

$$\mathbf{L}_i = \mathbf{F}\left(\mathbf{V}_{o(i-1)}, \mathbf{S}_i, \mathbf{S}_{(i-1)}, \mathbf{V}_{fi}\right) \tag{38}$$

where V_{fi} is the voltages of flying capacitors in stages.

To represent the MLC topology, the full-stage matrix model can be established in accordance with the natural stage division of a given MLC.

Here the famous 5L ANPC topology is taken as an example. The main circuit is shown in Fig. 10(b), while its NBD is shown in Fig. 13.

The outputs of the first stage can be expressed as follows:

$$\mathbf{V}_{o1} = \mathbf{S}_1\mathbf{L}_1 \tag{39}$$

where

$$\mathbf{V}_{o1} = \left[\,V_{o2}\ V_{o1}\,\right]^T, \mathbf{S}_1 = \left[\,\mathbf{S}_{12}\ \mathbf{S}_{11}\,\right]^T,$$
$$\mathbf{S}_{12} = \left[\,S_{14}\ S_{13}\ 0\ 0\,\right]^T, \mathbf{S}_{11} = \left[\,0\ 0\ S_{12}\ S_{11}\,\right]^T,$$
$$\mathbf{L}_1 = \left[\,L_{13}\ L_{12}\ L_{12}\ L_{11}\,\right]^T.$$

The outputs of the second stage can be expressed as follows:

$$\mathbf{V}_{o2} = \mathbf{S}_2\mathbf{L}_2 \tag{40}$$

where

$$\mathbf{V}_{o2} = V_o, \mathbf{S}_2 = \left[\,\mathbf{S}_{22}\ \mathbf{S}_{21}\,\right]^T, \mathbf{L}_2 = \left[\,L_{22}\ L_{21}\,\right]^T.$$

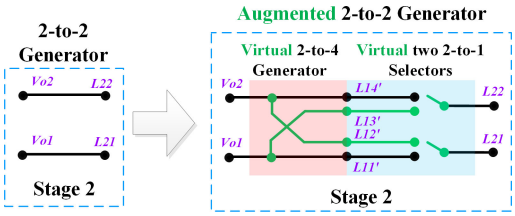


Fig. 14. Augmented level generator of the second stage of 5L-ANPC topology.

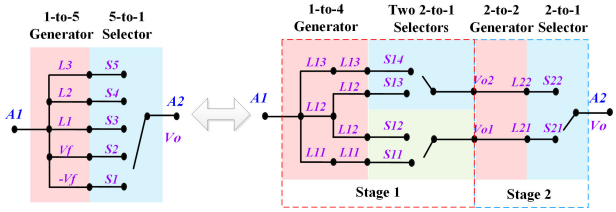


Fig. 15. Single-stage NBD of 5L-ANPC topology.

Based on (38), the level vector L_2 is a function of S_1, S_2, V_{o1}, V_f, which results in an augmented second stage with a virtual level vector $L'_1 = [L'_{14}\, L'_{13}\, L'_{12}\, L'_{11}]^T$ as shown in Fig. 14.

The outputs of the augmented second stage can be expressed as follows:

$$\mathbf{L}_2 = \mathbf{S'}_1\mathbf{L'}_1 \tag{41}$$

where

$$\begin{aligned}
&\mathbf{S}_1{}' = \left[\mathbf{S}'_{12}\ \mathbf{S}'_{11}\right]^T,\\
&\mathbf{S}'_{12} = \left[S'_{14}\ S'_{13}\ 0\ 0\right]^T, \mathbf{S}'_{11} = \left[0\ 0\ S'_{12}\ S'_{11}\right]^T,\\
&S'_{14} = (S_{14}\ \ or\ \ S_{13})\, S_{22}, S'_{13} = (S_{12}\ \ or\ \ S_{11})\, S_{22},\\
&S'_{12} = (S_{14}\ \ or\ \ S_{13})\, S_{21}, S'_{11} = (S_{12}\ \ or\ \ S_{11})\, S_{21},\\
&\mathbf{L}'_1 = \left[L'_{14}\ L'_{13}\ L'_{12}\ L'_{11}\right]^T,\\
&L'_{14} = V_{o2}, L'_{13} = V_{o1} + V_f, L'_{12} = V_{o2} - V_f, L'_{11} = V_{o1}.
\end{aligned}$$

Therefore, the output of the 5L-ANPC converter is as follows:

$$\begin{aligned}
V_o = &\left[(S_{14}\ \text{or}\ S_{13})\, S_{14}\right] L_{13}\\
&+ \left[(S_{14}\ \text{or}\ S_{13})\, S_{13} + (S_{12}\ \text{or}\ S_{11})\, S_{12}\right] L_{12}\\
&+ \left[(S_{12}\ \text{or}\ S_{11})\, S_{11}\right] L_{11}\\
&+ \left[(S_{12}\ \text{or}\ S_{11})\, S_{22}\right] V_f + \left[(S_{14}\ \text{or}\ S_{13})\, S_{21}\right](-V_f).
\end{aligned} \tag{42}$$

And (42) can be equivalently transformed into the following:

$$V_o = \mathbf{SL} \tag{43}$$

where

$$\begin{aligned}
&\mathbf{S} = \left[S_5\ S_4\ S_3\ S_2\ S_1\right],\\
&S_5 = (S_{14}\ \ \text{or}\ \ S_{13})\, S_{14},\\
&S_4 = (S_{14}\ \ \text{or}\ \ S_{13})\, S_{13} + (S_{12}\ \ \text{or}\ \ S_{11})\, S_{12},\\
&S_3 = (S_{12}\ \ \text{or}\ \ S_{11})\, S_{11},\\
&S_2 = (S_{12}\ \ \text{or}\ \ S_{11})\, S_{22},\\
&S_1 = (S_{14}\ \ \text{or}\ \ S_{13})\, S_{21},\\
&\mathbf{L} = \left[L_{13}\ L_{12}\ L_{11}\ V_f\ -V_f\right]^T.
\end{aligned}$$

Equation (43) can be called as the single-stage matrix model. And the single-stage NBD can be developed for 5L-ANPC converter as shown in Fig. 15. It indicates all potential output levels this topology can generate: L_{13}, $L_{13} - V_f$, $L_{12} - V_f$, L_{12}, $L_{12} + V_f$, $L_{11} + V_f$, L_{11}. Assume the input terminal potentials are: $L_{13} = 2\text{E}$, $L_{12} = 0$, $L_{11} = -2\text{E}$, and the flying capacitor voltages are $V_f = \text{E}$, then, the five-level outputs can be obtained: $\pm 2\text{E}$, $\pm\text{E}$, 0. If $V_f = 2\text{E}$, then, only three-level outputs can be generated: $\pm 2\text{E}$, 0. Such systematic estimation process can be utilized for any derived MLCs through the proposed method.

B. Systematic Way for Voltage Balance Analysis

Another great challenge of MLC derivation is the voltage/current balance of capacitors/inductors. Here the flying capacitor voltage balance analysis of 5L ANPC topology is discussed as an example through the matrix model. While such analysis can also be done for any MLC derived through the proposed method.

The model (43) can be transferred into the following form through elementary row transformation of L:

$$\mathbf{EL} = \mathbf{PL'} \tag{44}$$

where E is the five-dimension unit matrix

$$\mathbf{P} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0\\ 1 & 0 & 0 & 0 & 1\\ 0 & 1 & 0 & 0 & 0\\ 0 & 0 & 1 & 1 & 0\\ 0 & 0 & 1 & 0 & 0 \end{bmatrix}, \mathbf{L'} = \begin{bmatrix} L_{13}\\ L_{13} - V_f\\ L_{12}\\ L_{11} + V_f\\ L_{11} \end{bmatrix}.$$

Let $\mathbf{S'} = \mathbf{SP}$, then

$$V_o = \mathbf{SL} = \mathbf{SPP^{-1}L} = \mathbf{S'L'} \tag{45}$$

where $\mathbf{S'} = [(S_5 + S_4)\ S_3\ (S_2 + S_1)\ S_2\ S_4]$.

The general transformation can be expressed as follows:

$$V_o = \mathbf{SL} = \mathbf{SP}_{(i)}\left[\mathbf{P}_{(i)}\right]^{-1}\mathbf{L} = \mathbf{S}_{(i)}\mathbf{L}_{(i)} \tag{46}$$

where i is an integer, $\text{rank}(\mathbf{P}_{(i)}) = 5$. Note that the calculation of the matrix $P_{(i)}$ is offline.

The following equivalent single-stage matrix models can be developed based on (46):

$$\begin{aligned}
\mathbf{M}_{(1)} &= \mathbf{S}_{(1)}\mathbf{L}_{(1)}, \mathbf{L}_{(1)}\\
&= \left[L_{13}\ \ L_{13} - V_f\ \ L_{12}\ \ L_{11} + V_f\ \ L_{11}\right]^T\\
\mathbf{M}_{(2)} &= \mathbf{S}_{(2)}\mathbf{L}_{(2)}, \mathbf{L}_{(2)}\\
&= \left[L_{13}\ \ L_{12} + V_f\ \ L_{12}\ \ L_{11} + V_f\ \ L_{11}\right]^T\\
\mathbf{M}_{(3)} &= \mathbf{S}_{(3)}\mathbf{L}_{(3)}, \mathbf{L}_{(3)}\\
&= \left[L_{13}\ \ L_{13} - V_f\ \ L_{12}\ \ L_{12} - V_f\ \ L_{11}\right]^T\\
\mathbf{M}_{(4)} &= \mathbf{S}_{(4)}\mathbf{L}_{(4)}, \mathbf{L}_{(4)}\\
&= \left[L_{13}\ \ L_{12} + V_f\ \ L_{12}\ \ L_{12} - V_f\ \ L_{11}\right]^T.
\end{aligned} \tag{47}$$

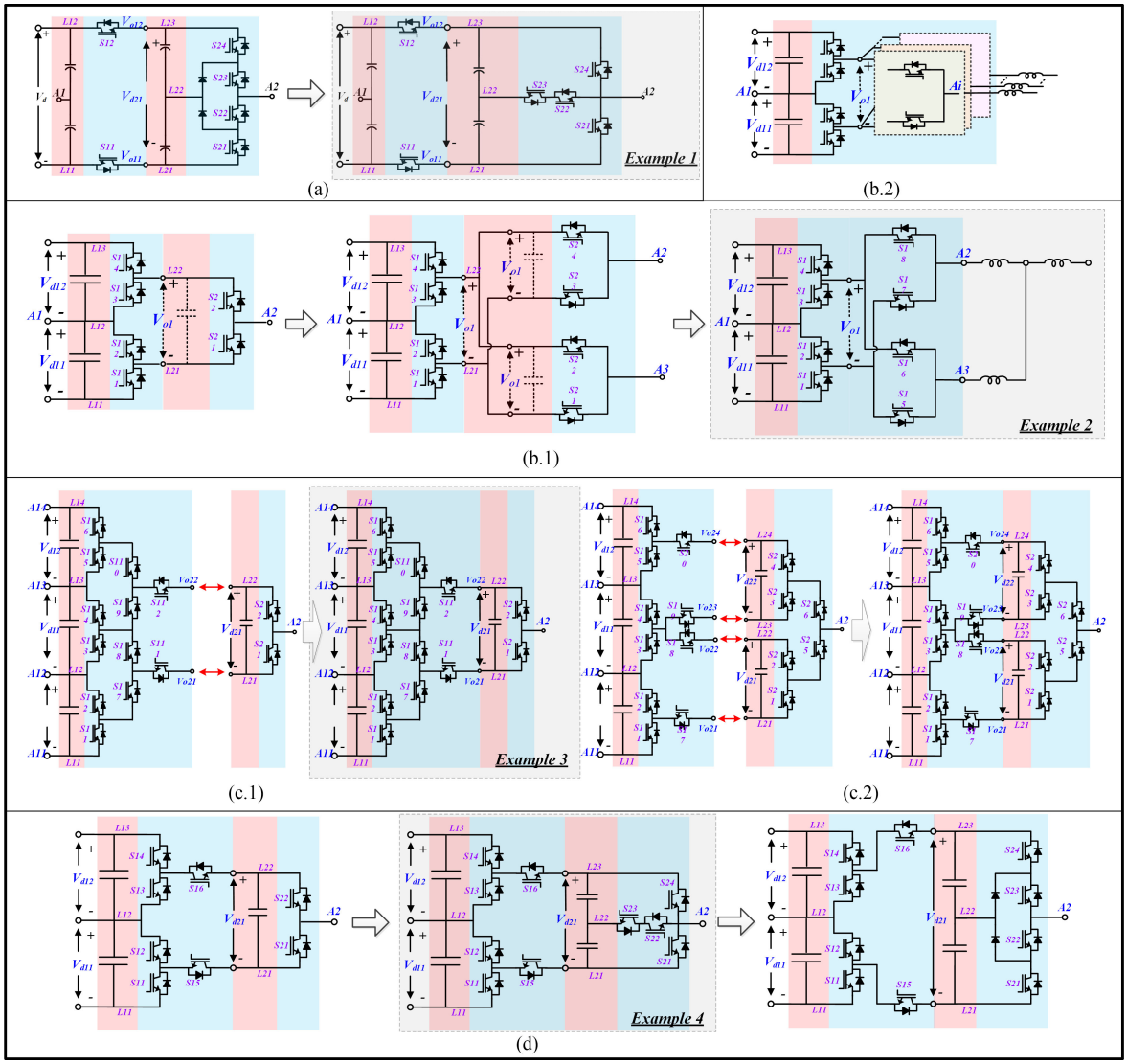


Fig. 16. Derivation examples covering 5 to 9 level topologies. (a) 4L T-type NNPC through new simplification of stages in existing topology. (b) Internal parallel 3L ANPC converter through new internal stage combinations. (c) and (d) Hybrid-clamped 7L/9L topologies through new combinations of different stages.

To balance the flying capacitors of the 5L-ANPC converter, these models can be utilized as different operation/modulation modes of the converter and be rotated based on the desired switching frequency. Such that, the output levels can maintain the same, while the voltage of the flying capacitor can be controlled.

C. Inspirations of New Topologies Through the Proposed Method

Based on the proposed synthesis methodology, derivation of a new topology can be considered in the following directions:

1) new simplification of stages in generalized topology;
2) new inter-stage combinations;
3) new combinations of different stage.

Besides, multilevel matrix converter can be derived through the logical mapping relationship between indirect-type and direct-type converter.

1) New Simplification of Stages in Existing Topology: Derived Topology Example 1: Fig. 16(a) shows the simplification process of a four-level converter proposed in [74]. The second stage of the NNPC topology is replaced by T-type NPC topology. The gating signal of PWM introduced in [74] can be implemented without modification, therefore, will not be covered in this section. Note that the voltage of each flying capacitor can be controlled as $1/3V_d$ or $1/4V_d$, resulting in four- or five-level output in theory [75].

2) New Combinations of Internal Stages: Derived Topology Example 2: Internal paralleled configuration is recently proposed in [76]. Fig. 16(b.1) shows the derivation process of the internal paralleled 3L ANPC topology. First, the 2-stage 3L ANPC is decomposed into two parts: high switching frequency part and low switching frequency part which is essentially the same with [76]. In steady state, the V_{o1} is maintained constant, and the basic half bridges (second stages) can be modularly connected in parallel without oscillation of input voltage. Based

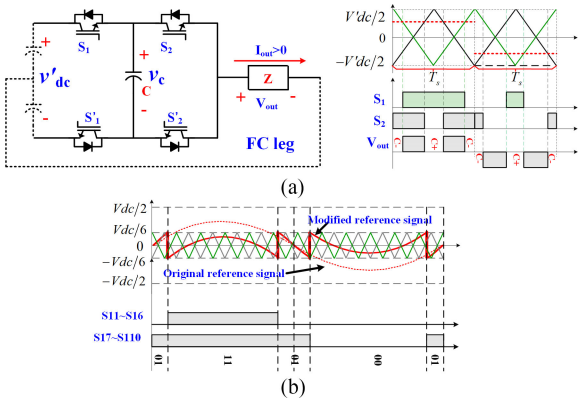


Fig. 17. (a) PS-PWM for 3L flying capacitor converter. (b) PWM for hybrid-clamped 7L topology 1#.

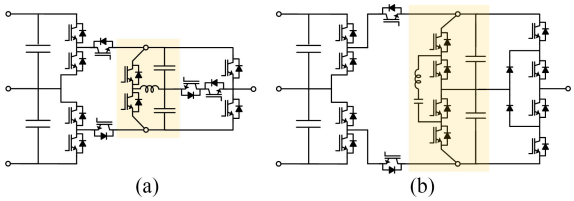


Fig. 18. Voltage balance of flying capacitors of hybrid-clamped 9L topology through (a) 2L balancing circuit for 9L 1# topology and (b) 3L balancing circuit for 9L 2# topology.

on the simplification principle, one can eliminate the capacitors of the second stage and finally obtain the simplified topology. During the derivation process, the number of paralleled stages can be greater than two and results in a modular structure shown in Fig. 16(b.2). Each module can share the same power rating and operate at a high switching frequency which is preferred for wide-bandgap semiconductor.

3) New Combinations of Different Stages: Derived Topology Example 3: In Fig. 16(c.1), two stages are shown: one is a 4L stage with two output terminals, the other one is a 2-to-1 stage. The combination of these two stages forms the hybrid-clamped seven-level topology 1# through the derivation principle. Same rules can be implemented to derive hybrid-clamped seven-level topology 2#. The operation principles are based on the carrier-based PWM of 4L ANPC designed in [77] with modification for FC balance to generate seven-level output.

For these presented hybrid-clamped 7L topologies, the conventional PS-PWM (see Fig. 17) can be utilized for the FC legs without modification. The FC voltage self-balancing can also be achieved [78]. A carrier-based PWM scheme of hybrid-clamped 7L topology 1# is given as demonstration to show the basic operation principle.

Derived Topology Example 4: In Fig. 16(d), two hybrid-clamped 9L topologies can be derived through the substitution of the second stage of hybrid-clamped five-level topology: the original 2-to-1 stage can be replaced by a T-type three-level stage or an NPC-based three-level stage. Since the three-level stages are not self-balancing, auxiliary circuits are mandatory for their FCs. Both two-level and three-level balancing circuits can be implemented as shown in Fig. 18. Note that the auxiliary

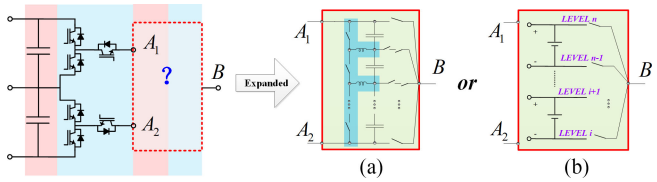


Fig. 19. Extended the second stage circuit into a generalized version to obtain higher output levels through (a) FCs with auxiliary circuit and (b) dc supplies.

circuits only need to deal with differential power of FCs, the working principles are basically the same as a DPP [37], [79], [80]. Thus, lower power rating devices can be implemented. Compared with 9L topology proposed in [81], the total power rating of active switches can be similar, while the conduction losses of the main topologies can be less due to the reduction of conducting switches. One can also extend the second stage circuit into a generalized version to obtain higher output levels as shown in Fig. 19. While the auxiliary circuit can be utilized to help balance the flying capacitor voltages. It provides another potential way to increase the output levels of MLCs by utilizing stages combined with auxiliary circuit instead of stages with self-balancing capability as presented in [41]. In fact, a similar way can be found in [82], where the extended commutation cell is used to realize eight-level output. Since each stage of the level generation is not limited to capacitors in proposed method, we can even use dc supplies to provide stable dc voltages in any stages. Typical examples can be found in [83] and [84].

D. Practical Considerations of Derived Multilevel Topologies

The proposed method is demonstrated through four derived examples. While it is also expected that the derivation results have certain practical values. To address such objective, in this section, the practical considerations of these topology examples are discussed.

The main reasons of utilizing MLCs in practical applications are to acquire: 1) reduced ac-side filter size due to a high number of output levels and reduced *dv/dt* or *di/dt*, 2) higher power ratings through the sharing blocking voltages or currents of devices.

This general derivation approach can cover a large number of various MLCs, from low-level ones to high-level ones. With a high number of output levels (voltage or current), the output power quality can be improved. While the complexity of the derivation process can significantly increase since the applicable LGs and selectors increases as well.

For single dc-link topology, a higher level MLC is possible as shown in Fig. 16(a). While the naturally unbalanced flying capacitors make the control and modulation schemes more challenging than conventional topologies [85].

With two dc links, a higher level MLC is also possible as shown in Fig. 16(b) and (d). While the auxiliary balancing circuit is preferable for 9L examples in Fig. 16(d) due to unbalanced flying capacitor voltages [86]. As mentioned in Section II, different applications require different applicable converters. Compared to MV or HV high-power scenarios, implementation

TABLE I
SUMMARIES OF DERIVED MLC TOPOLOGIES (PER PHASE)

	Example 1 Fig. 16(a) (T-NPC)	Example 2 Fig. 16(b.1)	Example 3 Fig. 16(c.1)	Example 4 Fig. 16(d) (T-NPC)
Level	4/5	3/5	7	9
No. of DC links	1	2	3	2
Total ratings of active devices	2Vdc/ 2.5Vdc	3Vdc/ 4Vdc	4Vdc	3.5Vdc
Total ratings of passive devices	2Vdc diode +2/3Vdc cap./ 2.5Vdc diode +1/2Vdc cap.	3Vdc diode/ 4Vdc diode	4Vdc diode + 1/3Vdc cap.	4Vdc diode + 1/4Vdc cap.
Naturally balanced dc cap. voltages?	N/A	Yes	Limited balance range	Yes
Naturally balanced flying cap. voltages?	Limited balance range	N/A	Yes	No
Auxiliary circuits preferred?	N/A	N/A	Yes (for low voltage)	Yes
Preferred voltage rating	Low/medium voltage	Low/medium voltage	Low/ medium voltage	Low voltage
Preferred power rating	Low/medium power	Medium/high power	Low/ medium power	Low power

of auxiliary circuits can be more reasonable in low-voltage low-power cases as in some single-phase PV system [87]. While a naturally balanced dc-link/flying/floating capacitor voltages are more attractive in MV/HV applications.

Three dc links can bring us the derived seven-level example as shown in Fig. 16(c). While the limited stable operation regions for such topology will make such topology less attractive for wide-range heavy-load high-power applications [88]. Recently, another seven-level topology is proposed with the capability of balancing both dc-link and flying capacitors, which can be implemented for MV drive system [89]. Such topology can also be synthesized through this method.

To summarize, the features of derived topologies are listed in Table I. While in practice, more compromises should be made to cope with various requirements, e.g., total costs, reliability, efficiency, power density, etc. [2]–[5], [90], [91].

E. Verifications of Derived Topology

In the previous section, four examples (1–4) are presented as the demonstration of how the proposed method can help inspire new topologies. All examples exhibit certain practical values for practical applications. Some of them are proposed in literature within one year of publication of this work. The detailed discussions and verifications of Example 1 topology in Fig. 16(a) can be found in [74]. While [86] shows Example 4 topology can operate as a five-/seven-/nine-level converter with thorough analysis and experiments. Example 3 topology in Fig. 16(c) is similar to the fifth figure in [66] without H-bridge cells. Example 2 topology in Fig. 16(b) can be considered as the extension of [92] since it can be operated with more than two modules, a different allocation of high switching frequency

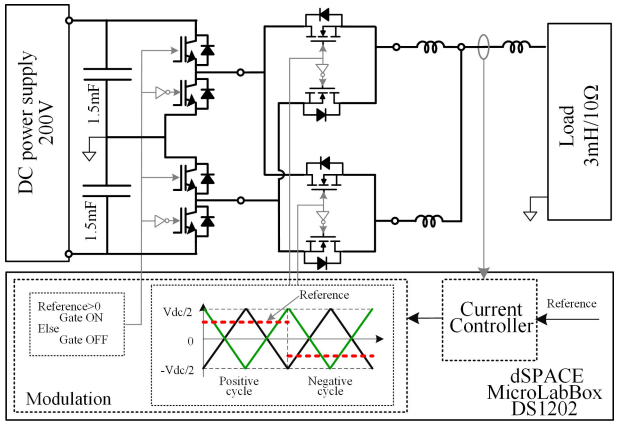


Fig. 20. Experimental setup.

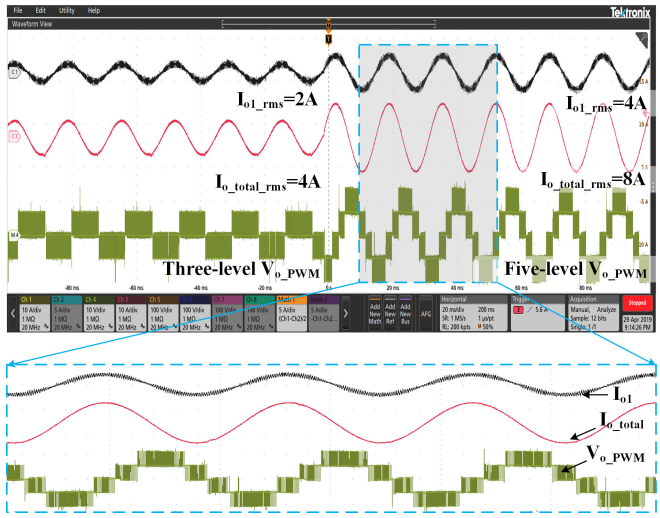


Fig. 21. Experimental results of 2# topology example. The waveforms from top to bottom: output current of the A2 terminal, the output current of the total current, output PWM voltage pulses. The RMS value of the current reference is changed from 4 to 8 A during the operation.

part and low switching frequency part and utilizes the shared dc links rather than multiple isolated dc supplies for multiphase applications.

To verify Example 2 topology, the experiments are carried out with the three-phase platform in the lab based on the circuit in Fig. 16(b.1). Each phase leg is composed of four IGBT devices (Infineon IKQ50N120CT2) for S_{11}–S_{14}, four GaN devices (GaN Systems GS66516) for S_{15}–S_{18}, as shown in experimental setup in Fig. 20. The digital controller is the dSPACE MicroLabBox DS1202. The conventional current-closed-loop control is implemented to track the reference current, while the carrier-based PWM with two 180° shifted carriers is used for the interleaved operation of this topology. The generalized operation principles are referred to [93]. The experimental results are shown in Fig. 21 with parameters listed in Table II. In [92], four switches (per phase) have to block the whole dc voltage. Compared to [92], one merit of the example 2 topology is the reduced device ratings for five-level output with all devices withstand half dc-link voltage.

TABLE II
EXPERIMENTAL PARAMETERS

DC voltage	200V	Device frequency	5kHz
AC current	4A/8A	Line frequency	60Hz
LR load	3mH/10Ω	DC capacitor	1.5mF

X. CONCLUSION

To systematically synthesize and derive multilevel voltage-source, current-source, and matrix converters, a general methodology is proposed in this article. With the stage-based common structure, the systematic design of MLCs can be realized. The node-branch forms are obtained for most commonly studied topologies, which not only demonstrate the common structures of both the voltage-source and current-source multilevel topologies, but also the logical equivalence of multilevel indirect and direct matrix converters. The matrix presentations of MLCs are derived from their node-branch forms, which provides an opportunity for systematic analysis of different MLCs. It can help the simplification process of derived various MLC topologies, and can also facilitate the modulation implementation for different MLCs, including matrix converters, through the logic mapping. Moreover, compared to the current approach of manual design and analysis, the design rules of the proposed method are more general and straightforward to follow even for researchers without a strong power electronics background. With the proposed method, a unified design platform could be established, which opens the potential for both manual synthesis and derivation and computer-aided design and analysis. Several emerging multilevel topologies are derived as examples, e.g., internal paralleled MLCs, seven-level hybrid MLCs, and 9L MLCs with auxiliary circuits. The discussions with practical considerations and experiments are given to further demonstrate the feasibility of the proposed method.

As the research of MLC getting more attention in recent years, it is hoped that this article can provide inspiration for researchers when looking for new topologies towards various applications, e.g., high-power conversion in smart grid, medium voltage system, emerging low-voltage power converter, etc. In future work, additional requirements can be further considered in the design, such as proper modulation design, active/passive device optimized selection, efficiency improvement, power density requirement, lifetime expectation, reliability, environmental impacts, etc.

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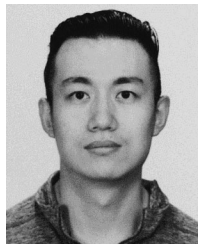

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