Series Chain-Link Modular Multilevel AC–DC Converter (SCC) for HVDC Applications

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***Abstract*—Introduction of the modular multilevel converter (MMC) has enabled the exploitation of voltage source converters (VSCs) in an increasing number of high-voltage direct current (HVdc) applications. Subsequently, some new topologies and solutions have been presented to tailor the MMC concept to specific uses. Particular attention has been paid to reduction of the converter footprint for applications where plant size is a critical economic aspect, for example, in offshore installations. This article introduces a new series-connected modular multilevel ac–dc converter, the series chain-link converter (SCC), which gives a significant reduction in the required number of submodules (SMs) and a more compact distribution of the energy storage, compared to an MMC. In this article, the operating principle of the converter and its design are discussed in detail; the SM count and energy storage requirement are also given. The basic control loops required for the practical operation of the converter are presented and designed. The SCC concept has been experimentally validated on a small-scale 450 V dc, 415 V ac, 4.5 kVA laboratory prototype, confirming the practical viability of the topology.**

***Index Terms*—High-voltage direct current (HVdc), modular multilevel converter (MMC), series chain-link converter (SCC).**

I. Introduction

HIGH-VOLTAGE direct current (HVdc) has proven to be a more convenient solution than conventional ac systems for long-distance power transmission since the 1950s. Recently, voltage source converters (VSCs) have been extensively investigated as a replacement for line-commuted converters (LCCs) in order to reduce the converter station footprint, provide independent control of the active and the reactive power, and enable black-start capabilities. VSC technology has been employed for a long time in medium-voltage (MV) applications, such as MV drives [1], [2]. However, the basic two-level VSC has severe drawbacks at higher voltages and power ratings because of the static and dynamic balancing required for series-connected semiconductors, the high switching loss, and high dv/dt, which impacts the insulation of transformers and inductors [3]. To overcome the limitations of the two-level VSC, multilevel conversion has been investigated since the 1980s, starting from the three-level neutral-point clamped converter (NPC) converter introduced by Nabae *et al.* in [4]. However, the nonmodular structure has limited the application of the NPC in high-voltage converters with more levels. Another solution, the cascaded H bridge was proposed in [5], where the multilevel voltages are obtained by the series connection of H bridges, each requiring an isolated dc source. The first multilevel converter targeted for HVdc applications was the flying capacitor converter [6], but the large number of capacitors, with progressively increasing voltage ratings, required to achieve suitable voltage levels has affected its practical exploitation.

A remarkable step forward in multilevel conversion was presented in [7], where a chain link of H bridges with floating capacitors was used in a three-phase static compensator (STATCOM). In the early 2000s, Lesnicar and Marquadt [8] introduced the first modular multilevel converter (MMC) for ac–dc conversion. The MMC has allowed the exploitation of VSC concepts in HVdc applications where compact converter size, black-start capability, and independent active and reactive power control are required. As highlighted in [9], the footprint of an MMC-VSC converter substation can potentially be between one-third and one-fourth of an equivalent LCC substation. In addition, the MMC features straightforward redundancy, modular structure, lower power losses than other VSCs, and low dv/dt impressed on magnetic components.

The MMC has been adopted in a number of HVdc installations from the main industrial leaders as in [9] and [10]. In offshore applications, the converter platform plays a key role in the final cost [11], and the advantage of the MMC is the significant reduction in filtering components and the absence of reactive power compensation components. However, improving the MMC power density is one of the most important targets for further developments of the topology. For example, a twin module could be used to compact three voltage levels in a single submodule (SM) unit [12].

The constant attention on the MMC concept has led to the introduction of new modular multilevel topologies. In [13] and [14], a hybrid modular multilevel VSC and its augmented version, the series bridge converter, have been presented. Due to the series connection of phase chain links on the dc side and the production of rectified ac waveforms, these topologies have a

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low number of SMs and reduced energy storage. However, three "unfolding bridges" are required and the control of the ac and dc sides is not completely decoupled. In the alternate arm converter (AAC) [15], the reduction of SMs is achieved by switching the ac current path from the upper to the lower arms of each phase leg. This also reduces the required energy storage. Despite these advantages, the converter balancing procedure is complicated when the converter is operated away from the "sweet spot." The active flying capacitor MMC [16] presents the operation similar to that of the AAC, but it uses only one chain link of SMs per phase, further reducing the required number of SMs. However, as in the AAC, it requires a capacitive filter on the dc side and additionally a series connection of basic commutation cells (insulated gate bipolar transistor (IGBT) + antiparallel diode) across the dc link, one per phase. A series-connected MMC (SC-MMC) is presented in [17]. As for the MMC, the SC-MMC retains decoupled control of the ac and dc sides, but it requires 12 arm inductors. An additional multilevel topology that uses the series connection of the phases is presented in [18]. Despite the interesting connection, this topology requires high energy stored in the chain links connected in the path of the ac current.

The introduction of the series chain-link converter (SCC) proposed in this article is motivated by the aim to reduce the number of required SMs and to achieve a more compact distribution of the energy within the converter with respect to an MMC, and for this reason, it is based on series connection of the converter phases on the dc side. At the same time, the converter is conceived to retain the important characteristics of the MMC, such as independent dc and ac control capability, low power losses, and similar total energy storage requirements. The design should also guarantee converter operation in abnormal grid scenarios, such as voltage imbalances and more onerous fault conditions.

The rest of this article is organized as follows. Section II describes the SCC in detail, including the different topological options and the considerations that led to the choice of the final topology of the converter. The basic steady-state equations governing the converter operation are presented, and sizing of the converter is discussed including the number of required SMs and energy storage. Section III discusses the control loops and their design. Section IV describes the experimental prototype used for the evaluation of the converter and Section V shows experimental results in steady state and during transients, confirming the practical feasibility of the topology.

II. Series Chain-Link Converter

The general schematic of the proposed converter is presented in Fig. 1. The SCC is obtained by connecting three longitudinal chain links (L-CH) of half-bridge (HB) SMs in series on the dc side. In normal steady-state conditions, each L-CH must generate one-third of the total dc voltage plus the ac voltage of the corresponding phase. The sum of the three L-CH voltages is equal to the total dc link voltage, since in steady state, the three ac components in each L-CH are a symmetrical set of voltages. The dc voltage can then be adjusted by a coordinated action on the dc component produced by each L-CH. On the ac side,

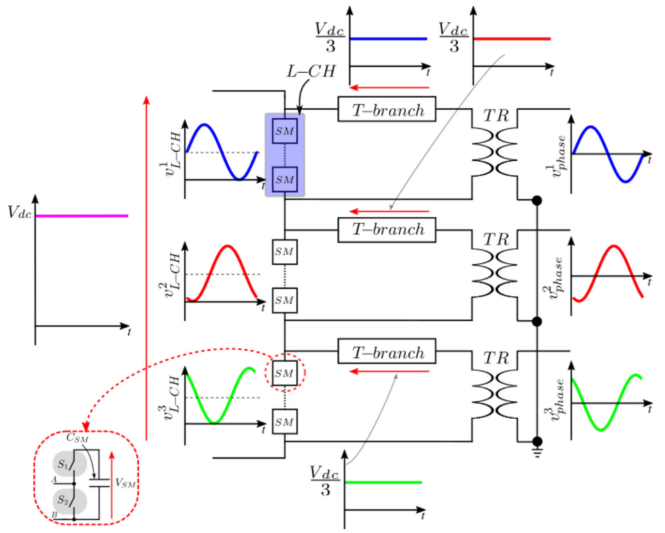

Fig. 1. Schematic of the SCC including ideal voltage waveforms on the ac and dc sides of the converter.

the phase voltage is derived from each L-CH by eliminating the dc "offset." This task is carried out, for each phase, by a transverse branch (T branch), and the methods proposed to eliminate the dc offset use a combination of either full-bridge (FB) or HB SMs and passive elements, such as inductors and capacitors. The resulting ac voltages are applied to the secondary windings of either three independent single-phase transformers or a three-phase transformer with all the individual winding terminals accessible on the converter side. The three transformer windings on the grid side may be arranged in a star or delta configuration. The need for a transformer is not generally a disadvantage since, although the MMC has been proposed as a transformerless solution [19], in practice, a transformer is nearly always used in HVdc applications to meet system requirements. A transformer is normally required in order to adjust the ac voltage on the converter side [20]. A delta connection of the transformer on the converter side also allows optimization of the output voltage capabilities of converter by using the third harmonic injection, as reported in [21]. The main benefits of using a transformer in an HVdc system are summarized in [22]. The transformer provides additional coupling reactance, adjusts the ac voltages at optimal levels, provides galvanic isolation, and prevents the flow of the zero sequence between the ac system and the converter.

A. Converter Description

Despite the different options for the realization of the T branch, which are discussed later, each of the proposed solutions has the same circuit configuration on the dc side, with HB SM L-CHs. To introduce the working principle of the converter, the dc side is considered first. The arrangement in Fig. 2, representing the most general realization of the T branch using a combination of passive and active elements, can be used as a reference for the analysis. For now, the T branches can be considered as ideal elements that perfectly remove the dc offset

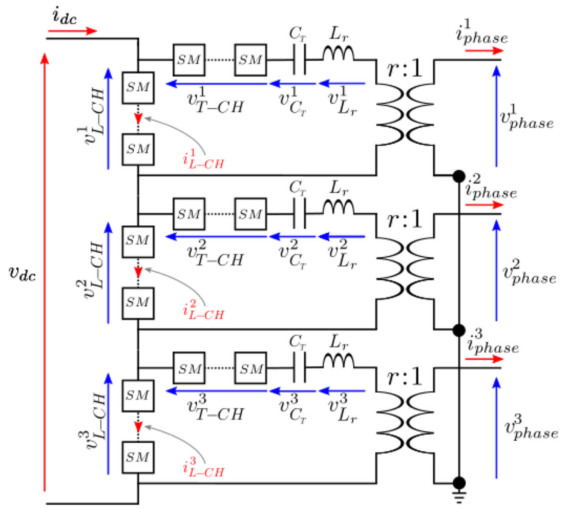

Fig. 2. Generalized representation of the SCC with inductors, capacitors, and chain links in the T branches. Note that the ac-line inductance is not shown and is assumed to be incorporated in the leakage inductance of the transformer in each phase.

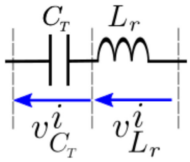

Fig. 3. Passive T branch. The series-connected inductor is selected to create a resonance tank, with the capacitor, at the line frequency.

produced by the corresponding L-CHs. Assuming that L-CHs are represented as ideal controllable voltage sources, the basic equations describing the converter can be formulated.

During normal operation, the voltage generated by each L-CH circuit is one-third of the total dc voltage plus the ac voltage component needed to regulate the power transfer between the converter and the ac grid. During normal operation, the *i*th ($i = 1, 2, 3$) L-CH produces a voltage of the form

$$v^i_{\text{L-CH}}(t) = \frac{V_{\text{dc}}}{3} + r \cdot \hat{V}_{\text{phase}} \sin\left(\omega_g \cdot t - \frac{i-1}{3}\pi\right). \quad (1)$$

The current flowing in the *i*th L-CH can be described by the following equation:

$$i^i_{\text{L-CH}}(t) = I_{\text{dc}} - \frac{1}{r}\hat{I}_{\text{phase}} \sin\left(\omega_g \cdot t - \varphi - \frac{i-1}{3}\pi\right) \quad (2)$$

where $\hat{V}_{\text{phase}}$ and $\hat{I}_{\text{phase}}$ are, respectively, the ac grid voltage and current amplitudes, ω_g is the angular frequency of the grid, φ is the phase shift between the ac voltage and the ac current, and r is the secondary to primary transformer turns ratio, as shown in Fig. 2. Since the dc voltage in each L-CH is $V_{\text{dc}}/3$, the modulation index m can be defined as

$$m = \frac{3 \cdot r \cdot \hat{V}_{\text{phase}}}{V_{\text{dc}}}. \quad (3)$$

Note that $m = 1$ corresponds to the maximum ac-side voltage that can be generated with conventional modulation. When the dc power matches the ac power, the power balance equation holds

$$V_{\text{dc}} \cdot I_{\text{dc}} = \frac{3}{2}\hat{V}_{\text{phase}} \cdot \hat{I}_{\text{phase}} \cos(\varphi) \quad (4)$$

and then, the relation between the dc current and the ac current assumes the following expression

$$I_{\text{dc}} = \frac{1}{2} m \frac{\hat{I}_{\text{phase}}}{r} \cos(\varphi). \quad (5)$$

As for the MMC, control of the dc and ac sides can be completely decoupled. The decoupling in the SCC is evident, since the sum of the dc voltage components of each L-CH controls the dc-side power transfer, whereas the ac components control the ac-side power.

The number of required SMs in each L-CH can be obtained using (1) and is given as

$$N_{\text{SM}_{\text{L-CH}}} = \left\lceil \frac{\left|\hat{v}^i_{\text{L-CH}}\right|}{V_{\text{SM}}} \right\rceil \quad (6)$$

where $\hat{v}^i_{\text{L-CH}}$ is the maximum voltage produced by each L-CH and V_{SM} is the nominal SM voltage. Equation (6) can be rearranged and expressed as a function of the ac grid voltage. To do so, some assumptions are necessary. First, it is assumed that there is no voltage generated across the T branches at the line frequency. To further simplify the analysis, the transformers are considered to be ideal and the voltage drop across the leakage inductance is neglected. In order to adjust the voltage levels during the normal converter operation, regulation margins must be guaranteed on both the dc and ac voltages. By defining the dc regulation margin RM_{dc}, the dc-link voltage range can be expressed as

$$V_{\text{dc}} = (1 \pm \text{RM}_{\text{dc}})\, V_{\text{dc},N} \quad (7)$$

where $V_{\text{dc},N}$ is the dc-link nominal voltage.

A similar expression can also be derived for the ac voltages

$$\hat{V}_{\text{phase}} = (1 \pm \text{RM}_{\text{ac}}) \cdot r \cdot \hat{V}_{\text{phase},N} \quad (8)$$

where RM_{ac} is now the ac voltage regulation margin and $\hat{V}_{\text{phase},N}$ is the nominal ac phase voltage. To produce the desired L-CH voltage with HBs, the ac voltage must always be smaller than the minimum dc voltage produced by each L-CH

$$(1 - \text{RM}_{\text{dc}})\frac{V_{\text{dc},N}}{3} \geq (1 + \text{RM}_{\text{ac}}) \cdot r \cdot \hat{V}_{\text{phase},N}. \quad (9)$$

For given nominal ac and dc system voltages, and having fixed the regulation margins, (9) can be used to identify the transformer turns ratio r. In addition to RM_{dc} and RM_{ac}, a redundancy factor k_r should be included. Taking into account the constraint (9), (6) can be used to determine the N_{SM} in each L-CH, having fixed the design factors (RM_{dc}, RM_{ac}, and k_r), the transformer turns ratio, and the nominal V_{SM}. The resulting expression to determine the number of SMs of the L-CH ($N_{\text{SM}_{\text{L-CH}}}$) is given in Appendix.

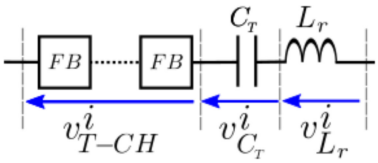

Fig. 4. Hybrid transverse T branch, obtained with the series connection of a transverse FB chain-link (T-CH), a capacitor C_T, and an inductor L_r.

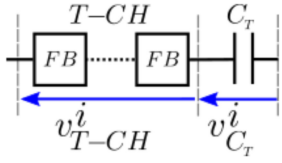

Fig. 5. Hybrid T branch with a capacitor C_T and a transverse FB chain-link T-CH.

B. T-Branch Options

As highlighted earlier, the series connection of L-CHs on the dc side provides no path to eliminate the dc component (offset) from the ac side. Consequently, this must be removed by adding the T branches. An important design aspect is the choice of the most convenient topology for the T branches. Additionally, the T branch can be designed to cooperate with L-CHs in dealing with unbalanced and fault conditions in the grid. Intuitively, it may be convenient to use the additional degree of freedom on the T branch to guarantee, throughout the converter operating range, the constraint of a ripple-free dc side

$$\sum_{i=1}^{3} v^i_{\text{L-CH}}(t) = V_{\text{dc}}. \tag{10}$$

If (10) is not respected, ac components may appear on the dc side, leading to deteriorated operation of the converter.

The minimum circuit configuration to block the dc offset on the ac side is a series capacitor. However, the dc blocking function should be performed with the following:

1) minimum size of the dc blocking circuit; and
2) minimum impact on the ac voltage generation capability.

These two objectives conflict, since with just a capacitor in the T branch, it alone must be sized to guarantee negligible ac voltage drop. This leads to high values of capacitance and makes the solution impractical.

1) Passive T Branch: The limitations of a purely capacitive T branch can be overcome by replacing the blocking capacitor with an *LC* (inductor L_r and blocking capacitor C_T) series resonant tank, resonating at the line frequency (Fig. 3). Doing so, the size of the capacitor can be reduced, and the ac voltage drop across the capacitor will be eliminated by the antiphase voltage across the resonant inductor. Note that this resonating inductor is separate from the ac-line inductance. The total impedance as seen from the grid is still inductive, assuming that the transformers are designed for a specific value of leakage inductance [23]. This solution is denoted as the *passive* T-branch SCC.

Although dc offset elimination is achieved, an additional passive component is required (the inductor) and furthermore no "active" control of the T branch can be achieved. Whilst it introduces a useful concept, the lack of flexibility in this solution is a serious limitation and we do not consider it in any further detail here.

2) Hybrid T Branch: The scheme proposed in Fig. 2 uses a combination of active components (chain link of SMs—T-CH) and passive elements in the T branches and will be referred to as a *hybrid* T-branch SCC. In the hybrid T branch in Fig. 4, the passive components are generally not chosen to resonate at the grid frequency. For this reason, the T-CH SMs are FBs, since during normal operation, the T-CH must produce an ac voltage able to cancel out the residual ac voltage drop across the passive components. This ac voltage is in quadrature with the line current and, neglecting loss, energy balance is naturally achieved in the T-CH SMs. In this sense, assuming $L_r < C_T$, the T-CH can be seen as an equivalent inductive reactance that makes the T branch operate as a virtual resonant circuit where part of the inductance is passive and part is electronically emulated by the T-CH. The voltage produced by the ith T-CH can be generally expressed as follows:

$$v^i_{\text{T-CH}}(t) = \omega_g \cdot L_{\text{eq}} \cdot \frac{1}{r} \hat{I}^i_{\text{phase}} \sin\left(\omega_g \cdot t + \frac{\pi}{2} - \varphi - \frac{i-1}{3}\pi\right) \tag{11}$$

where the equivalent inductance emulated by the T-CH in order to achieve resonance at ω_g is given by

$$L_{\text{eq}} = \frac{1}{\omega_g^2 \cdot C_T} - L_r. \tag{12}$$

As a result, the ac voltage drop at the grid frequency across the T branch is zero. The passive resonant inductor cooperates with the T-CH in eliminating the ac voltage drop across the blocking capacitor C_T. However, the retention of L_r in the circuit could significantly impact the volume occupied by the converter. For this reason, the hybrid T branch may be reduced to a T-CH and a blocking capacitor C_T, with the T-CH emulating all the required inductance (see Fig. 5).

The equivalent inductance emulated by the T-CHs is then given by

$$L_{\text{eq}} = \frac{1}{\omega_g^2 \cdot C_T}. \tag{13}$$

It is now necessary to determine the value of C_T. This could be driven by an economic optimization of the number of SMs in the T-CHs and the size of the blocking capacitors C_T. However, at this stage, the capacitor is simply selected in order to limit the ac voltage drop, due to the nominal ac current on the converter side, to a value equal to half of the ac voltage produced by each L-CH

$$X_{C_T} \cdot \frac{I_{\text{phase},N}}{r} = r \cdot \frac{V_{\text{phase},N}}{2} \tag{14}$$

where $I_{\text{phase},N}$ and $V_{\text{phase},N}$ are, respectively, the nominal values of the current and phase voltage on the grid side. Using

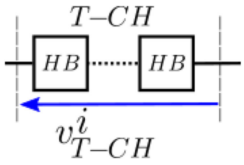

Fig. 6. Active transverse T branch. The connection features only a transverse HB chain link (T-CH).

(14), the required capacitance can be obtained as

$$C_T = 2 \cdot \frac{I_{\text{phase},N}}{r \cdot \omega_g \cdot V_{\text{phase},N}} = \frac{1}{\pi f_g} \frac{S}{(rV_{\text{LL}})^2} \tag{15}$$

where S is the rated apparent power and V_{LL} is the grid line-to-line voltage. The number of T-CH SMs can be determined according to voltage drop on C_T that needs to be canceled (half the converter side ac voltage in this case). However, extra voltage capability could be useful to cover all the contingencies [24], [25]. For this reason, it has been assumed that each T-CH must be able to produce three-fifths of the nominal phase voltage

$$\max\left(V_{\text{T-CH}}\right) = \frac{3}{5} \cdot r \cdot \hat{V}_{\text{phase},N} \tag{16}$$

and the number of required SMs can be determined according to (39) given in Appendix.

3) Active T Branch: Finally, Fig. 6 illustrates another possible arrangement of the T branch, which is realized only using HB SMs controlled to produce one-third of the dc voltage

$$V^i_{\text{T-CH}} = \frac{V_{\text{dc}}}{3}. \tag{17}$$

This is the most intuitive solution, as the dc offset is removed by placing an equivalent controllable voltage source such that the polarity opposes the corresponding dc component of the $v^i_{\text{L-CH}}$. As derived for the hybrid T-CH and the L-CH, an expression to identify the required minimum number of SMs in the active T-CHs $N^{\text{active}}_{\text{SM}_{\text{T-CH}}}$ can be obtained and is given in Appendix.

C. Selection of the Optimal Converter Topology

In this section, some considerations are presented to choose the most suitable solution between the hybrid and the active SCC. As highlighted, the main aim of this new topology is to reduce the number of SMs in the converter, as a higher number increases the control system complexity and, in turn, the overall converter complexity. The main operating differences between the options have been presented and now a comparison in terms of the ratings of the T-CHs is given.

1) Current Rating: In both solutions, the currents flowing in the two T-CHs are the same, and the semiconductors will have the same current ratings.

2) Number of SMs: The number of required SMs can be determined via (39) and (40) given in Appendix, and the relative requirement between the two options can be obtained as

$$\frac{N^{\text{Hybrid}}_{\text{SM}_{\text{T-CH}}}}{N^{\text{active}}_{\text{SM}_{\text{T-CH}}}} \approx 0.6. \tag{18}$$

For simplicity, the RM_{dc} and RM_{ac} have been assumed equal to 1. Note that if an ac regulation margin RM_{ac} less than unity is used (it is sensible to assume so as otherwise no ac regulation margin would be available), the relative SM requirement of (18) decreases and becomes even more favorable to the hybrid SCC.

From (18), it can be concluded that the active SCC requires at least 40% more SMs than that by the hybrid SCC. However, the hybrid SCC requires FB modules, whereas the active SCC requires only HBs. As consequence, the semiconductor count for the two options is similar.

3) Energy Storage: To provide a basic evaluation of the different energy storage requirements, the instantaneous power $p_{\text{CH}}(t)$ absorbed by each chain link can be integrated over time (for the power balance condition with zero average power exchanged by the chain links) and the energy variation $\Delta e(t)$ can be derived as follows:

$$\Delta e(t) = \int p_{\text{CH}}(t)\, dt = v_{\text{CH}}(t) \cdot i_{\text{CH}}(t)\, dt. \tag{19}$$

Also, assuming perfect energy sharing among the SMs within a chain link, the time-dependent energy stored in the chain link can be described by

$$E_{\text{CH}}(t) = \frac{1}{2} C_{\text{SM}} N_{\text{SM}} v^2_{\text{SM}}(t). \tag{20}$$

The instantaneous voltage in each SM $v_{\text{SM}}(t)$ can be decomposed into a dc component V_{SM} and an ac component $\Delta v_{\text{SM}}(t)$. By assuming power balance conditions and small ripple in $v_{\text{SM}}(t)$, the expression of the energy fluctuation as a function of the ac component of the SM voltage becomes

$$\Delta e(t) \approx C_{\text{SM}} \cdot N_{\text{SM}} \cdot V_{\text{SM}} \cdot \Delta v_{\text{SM}}(t). \tag{21}$$

Knowing the expression of the energy fluctuation, the peak-to-peak ac voltage component can be limited by selecting an appropriate value of C_{SM} according to

$$C_{\text{SM}} \geq \frac{\Delta e_{\text{pp}}}{N_{\text{SM}} \cdot \delta_{v_{c,\text{pp}}} \cdot V^2_{\text{SM}}} \tag{22}$$

where $\delta_{v_{c,\text{pp}}}$ is the per unit peak-to-peak voltage fluctuation, normalized with respect to the nominal SM voltage V_{SM}. The minimum energy storage in each chain link can be calculated as

$$E_{\min} = \frac{\Delta e_{\text{pp}}}{2 \cdot \delta_{v_{c,\text{pp}}}} [J]. \tag{23}$$

Also, the minimum specific energy required H [26] to guarantee the per-unit peak-to-peak voltage fluctuation $\delta_{v_{c,\text{pp}}}$ can be written as

$$H_{\min} = \frac{\Delta e_{\text{pp}}}{2 \cdot \delta_{v_{c,\text{pp}}} \cdot S} \left[\frac{\text{J}}{\text{W}} = \text{s}\right]. \tag{24}$$

In the literature, H is generally expressed in kJ/MW or ms. Equations (23) and (24) can be used for a comparison of the two T branch solutions. It is first necessary to evaluate the energy fluctuation in the individual T-CHs. During normal operation, the amplitude of the voltage produced by the hybrid T-CH can be approximated by

$$\hat{V}^i_{\text{T-CH}} = \omega_g \cdot L_{\text{eq}} \cdot \frac{1}{r} \hat{I}^i_{\text{phase}} \approx r \cdot \frac{\hat{V}^i_{\text{phase}}}{2} \approx \frac{V_{\text{dc}}}{6}. \tag{25}$$

To explain the above expression, some remarks are required. The T-CH is controlled, as already discussed, to "resonate" with the blocking capacitor C_T, and at nominal operating conditions, it produces an amplitude that is half of the amplitude of the nominal ac voltage, that in turn is roughly half the dc voltage produced by each L-CH. The peak-to-peak energy fluctuation can be estimated by

$$\Delta e_{\text{pp}}^{\text{Hy}} = 2\frac{V_{\text{dc}}\hat{I}^i_{\text{phase}}}{24\omega_g r} \approx \frac{S}{6\omega_g}. \tag{26}$$

The energy fluctuation in the active T-CH of the *i*th phase can be evaluated as

$$\Delta e_{\text{pp}}^{\text{Act}} = 2\frac{V_{\text{dc}}\hat{I}^i_{\text{phase}}}{3\omega_g r} \approx \frac{4}{3}\frac{S}{\omega_g}. \tag{27}$$

The relative energy storage requirement can now be evaluated as follows:

$$\frac{\Delta e_{\text{pp}}^{\text{Act}}}{\Delta e_{\text{pp}}^{\text{Hy}}} = 8. \tag{28}$$

The energy storage in the active T-CH is eight times greater than the energy storage in the hybrid T-CH solution. This result comes about because of the different energy fluctuation ripple and the different amplitude of the voltage produced by the two solutions. The hybrid chain link produces approximately half the voltage of the active T-CH and the ripple frequency is double than that of the active T-CH.

The smaller energy storage requirement of the hybrid solution makes it the most attractive option for the T-branch configuration. Consequently, the hybrid option is only one taken forward for further study, and for simplicity, we remove the hybrid designation and just refer to it as the SCC.

D. Discussion on Energy Storage and Number of SMs of the Selected Topology

Using (1) and (2), it is possible to determine the total energy fluctuation in the L-CH SMs. It is easily shown that the total energy fluctuation is equal to the energy fluctuation of an equivalent MMC. Consequently, the energy storage in the L-CHs is approximately the same as that by an equivalent MMC. To evaluate the additional storage required by the T-CHs, (26) can be used. As $V_{\text{dc}}/3 \approx r \cdot V^i_{\text{phase}}$, (26) can be rewritten as

$$\Delta e_{\text{pp}}^{\text{Hy}} \approx 2\frac{V^i_{\text{phase}}\hat{I}^i_{\text{phase}}}{4\omega_g}. \tag{29}$$

The specific energy storage for the T-CHs can be written in the form of

$$H^{\text{Hy}} = \frac{\Delta e_{\text{pp}}^{\text{Hy}}}{S} \approx 2 \cdot \frac{S}{4\omega_g}\frac{1}{S} = \frac{1}{2\pi f_g}. \tag{30}$$

For example, a system with a line frequency $f_g = 50$Hz requires an additional specific energy of approximately 3 kJ/MVA. Hence, the additional energy stored in the T-CHs is not significant since it is, for example, less than 10% of the typical total energy storage in an MMC [27].

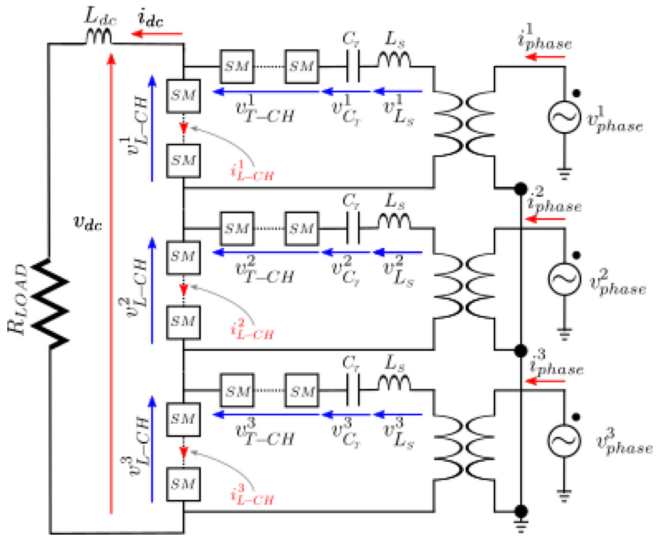

Fig. 7. Schematic of the simplified SCC HVdc system for comparison study.

TABLE I
HVDC SCALED-DOWN SYSTEM PARAMETERS

Symbol	Quantity	Value
V_{dc}	dc voltage	20 kV
V_{LL}	line to line voltage	11 kV
f_g	line frequency	50 Hz
P	Active power	20 MW
Q	Reactive power	8.5 $MVAr$

The number of SMs required by an MMC can be identified according to the system voltage levels and the available semiconductor devices. However, a simplified comparative analysis to identify the relative SM requirement between two MMCs can be determined by approximating the available voltage in each chain link of SMs of the complete converter, in terms of the dc voltage. Thus, the total requirement for the SCC is $\approx 2V_{\text{dc}} + 3 \cdot V_{\text{dc}}/6$, whereas for an equivalent MMC, it is $\approx 6V_{\text{dc}}$. This means that an SCC requires approximately the same energy storage as an equivalent MMC and the number of SMs required is reduced by $\approx 60\%$. This result can be seen also from a different perspective: the SCC has the potential to compact the energy storage of an MMC into a converter that requires only 40% of the number of SMs of an MMC.

III. HVDC SIMULATION AND COMPARISON

In order to prove the viability of the SCC topology introduced in this article, the results of a full switching simulation are presented in this section. The voltage and power ratings of a scaled-down industrial HVdc (MMC) demonstrator [28] have been used as reference for this study. Fig. 7 shows the simplified schematic of the SCC HVdc system considered.

The converter operates as an interface between an MV ac grid and a dc system. For simplicity, the dc system is replaced by a resistive load R_{LOAD}. The parameters of the two systems are summarized in Table I and Table II.

TABLE II
SCC PARAMETERS

Symbol	Quantity	Value
$C_{SM_{L-CH}}$	L-CH SM capacitance	19 mF
$C_{SM_{T-CH}}$	T-CH SM capacitance	12 mF
C_T	Transverse capacitance	2.3 mF
$N_{SM_{L-CH}}$	Number of L-CH SM per phase	11
$N_{SM_{T-CH}}$	Number of T-CH SM per phase	5
V_{SM}	SM operating voltage	1.5 kV
f_{PWM}	PWM frequency	500 Hz
f_{sort}	Sorting frequency	500 Hz

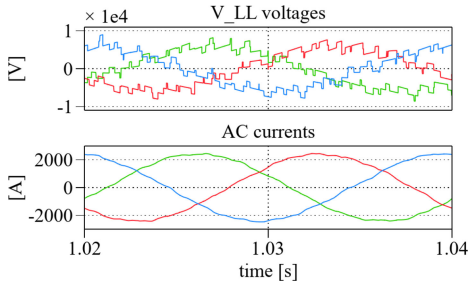

Fig. 8. Line-to-line voltages and ac currents on the converter side of the transformer.

On the ac side, each converter phase is connected to the corresponding grid phase via a single-phase transformer, as shown in Fig. 7. It is very important to note that L_s shown in Fig. 7 is not the same as L_r shown previously in Fig. 4. The function of L_r is taken up entirely by the chain links as explained previously, whereas L_s represents the ac-line interface reactance required by any HVdc converter to allow for power control. It includes the transformer leakage reactance and is common to both the SCC and MMC implementations and it is not therefore included in the comparison tables. A value of 18% is used according to the value reported in [28]. The transformer turns ratio is identified by using (9) having fixed both the dc voltage regulation margin and an ac voltage regulation margin ($\mathrm{RM_{dc}}$, $\mathrm{RM_{ac}}$) equal to 0.05 ($\pm 5\%$ voltage regulation). On the dc side, the system is modeled as a resistive load of 20Ω, which is connected to the converter via an inductor $L_{\mathrm{dc}} = 22$ mH.

The capacitance values of the SMs have been selected according to (22) in order to limit the voltage oscillation to around $\pm 10\%$ of the average value (i.e., 20% peak-to-peak voltage fluctuation $\delta_{v_{c,\mathrm{pp}}}$) [29]. The numbers of SMs for the L-CHs and T-CHs are calculated, respectively, according to (38) and (39) assuming 10% ($k_r = 0.1$) SMs redundancy. The SM operating voltage is 1.5 kV [28] and IGBT modules with 3.3 kV voltage ratings are considered. The full-load losses for this basic design, assuming typical 3.3-kV devices, has been calculated at 1.3%—a figure that could be further optimized by examining tradeoffs between losses and fault-handling capabilities [24].

In Fig. 8, the waveforms of the ac voltages and currents are shown. This figure shows the ac quantities measured on the converter side of the transformer. The ac current has total harmonic distortion (THD) of 2.5%.

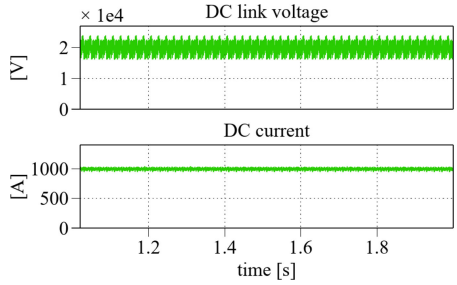

Fig. 9. Top waveform shows the dc-side voltage produced by the converter. The bottom waveform shows the dc current flowing into the dc load.

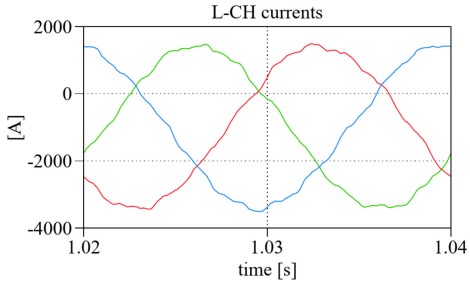

Fig. 10. Waveforms of L-CH currents.

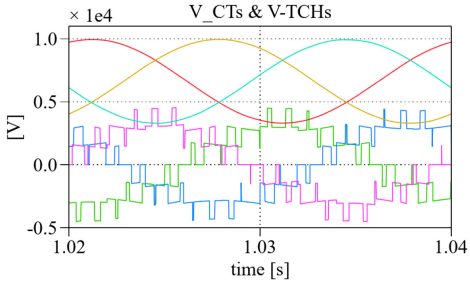

Fig. 11. Converter VTCH and VCT voltages.

On the dc side, the voltage V_{dc} of the converter is the sum of the three voltages produced by the L-CHs according to (10). The dc voltage illustrated in Fig. 9 shows a ripple at the switching frequency given by the instantaneous sum of the three L-CH SMs that are pulsewidth modulated (one for each L-CH). This voltage oscillation has a range of $\pm 2 \cdot V_{\mathrm{SM}}$.

The current flowing in each L-CH is given by the sum of the dc current and the ac current of the corresponding phase, as shown in Fig. 10.

The characteristic voltage waveforms of the transverse branches are shown in Fig. 11. This shows the voltages on the transverse capacitors C_T and the voltages produced by the T-CHs. As expected, each V_{C_T} voltage has a dc component approximately equal to $V_{\mathrm{dc}}/3$ and an ac component equal to the capacitive voltage drop. The T-CHs are modulated to produce a voltage that cancels this capacitive voltage drop.

The SM nominal voltages (V_{SM}) have been chosen to be 1.5 kV and the instantaneous waveforms are shown in Fig. 12. As expected, the fundamental period of the voltage ripple is 20 ms for the L-CH SMs (the same as in an MMC), whereas it is 10 ms for the T-CH SMs.

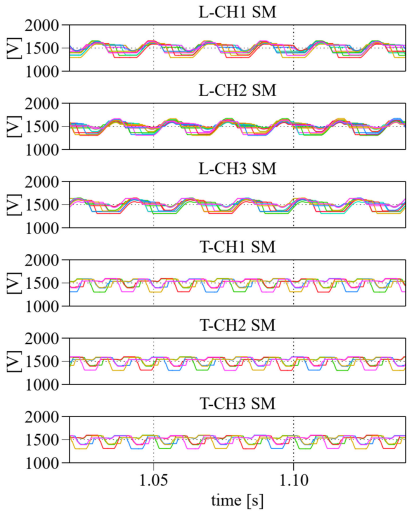

Fig. 12. Converter SM voltages.

TABLE III
COMPARISON

Quantity	MMC	SCC
r	1.05	0.7
N of chain-links	6	6
N_{SM} per chain-link	16	11*, 5**
N_{SM} per converter	96	48 = 33* + 15**
V_{SM}	1.5 kV	1.5 kV
$I_{ch\ (RMS)}$	0.7 kA	1.9* kA, 1.6** kA
I_{dc}	1 kA	1 kA
C_{SM}	7.5 mF	19* mF, 12** mF
H	36.3 ms	32.5* ms, 9.3** ms
C_T	-	2.3 mF
H_{C_T}	-	7 ms
L_{arm}	4.7 mH	-
N of arm inductors	6	-

*L-CH. **T-CH.

A. MMC Comparison

The SCC design used to simulate the scaled-down industrial HVdc system is used in this section for a comparison with an equivalent MMC. The MMC is assumed to be connected between the same dc system and ac grid. Equivalent design methods, already introduced for the SCC, have been used to determine the parameters of the MMC converter. In order to choose the transformer ratio used to interface the MMC with the ac grid, the same ac and dc regulation margins introduced for the SCC have been used. The average SM voltage is $V_{\rm SM} = 1.5$kV, the value of the SM capacitance is selected to limit the peak-to-peak voltage oscillation to 20% of the average SM voltage, and the number of SMs has been determined considering the same redundancy adopted for the SCC (i.e., 10%).

The results of the comparison are summarized in Table III. The main advantage of the topology is the reduction of number of SMs, indeed the SCC requires 50% fewer SMs than that by an MMC. This factor significantly impacts the required control apparatus and auxiliary elements to be installed. Also, the number of semiconductors is reduced. In addition, the inherent concentration of the energy storage, although a greater specific value is needed (15% more), could help to reduce the occupied volume since the energy is stored in less SMs. Three transverse capacitors C_T and one dc-side inductor $L_{\rm dc}$ are required, reducing the number of passive elements from six (one arm inductor for each MMC arm) to four. It can be seen from the table that the major drawback of the converter is the high current circulating in the semiconductors. This preliminary comparison shows that the SCC has the potential to reduce those factors that significantly impact the converter footprint, namely the number of SMs and the number of passive elements.

IV. CONTROL STRATEGY

The main objective of this section is to develop the control scheme for the SCC. This analysis focuses on the control of the small-scale laboratory prototype of the SCC that has been designed and built to validate the converter concept. Only the control loops that are strictly necessary for the operation of the laboratory demonstrator are presented, a more detailed analysis of the converter dynamics will be the object of the future work. The basic schematic of the laboratory prototype setup is the same as that used for the simulation study shown previously in Fig. 7, where it is worth noting that the inductors L_s on the ac side are the combination of interconnected inductors with the leakage inductance of the transformer, and they are not used "to cancel" the blocking capacitor ac voltage drops. This task is fully carried out by the T-CHs. For simplicity, control of the voltage on the dc side is performed in open loop. The dc voltage is shared equally among the three L-CHs and constitutes the constant component of the L-CH modulation signals. The power absorbed by the dc side is therefore defined by the resistive load. A slow outer total energy control (TEC) generates the active components of the ac current references in order to meet the power balance, and these are tracked by an inner current controller. A reactive current component $I_R^{\rm ref}$ can be directly added to the ac current references.

A. Current Control

Considering that the outer energy control loops will be designed to have dynamics at least an order of magnitude slower than the current loops, the T-CHs and the L-CHs can be considered as ideal controllable voltage sources. The current loops can then be analyzed referring to a generic *i*th phase, and the ac side equation can be derived from Fig. 7 as follows:

$$r \cdot v^i_{\rm phase}(t) = \frac{1}{C_r}\int i^i_{\rm phase}(t)\,dt + L_s\frac{d\,i^i_{\rm phase}(t)}{dt} + v^i_{\text{L-CH}}(t) - v^i_{\text{T-CH}}(t),\ i = 1,2,3. \quad (31)$$

For simplicity, the FB chain links in the hybrid T branches, discussed in Section II-B2, are controlled in open loop so that the generated ac voltages $v^i_{\text{T-CH}}(t)$ are "inductive" 50Hz voltages

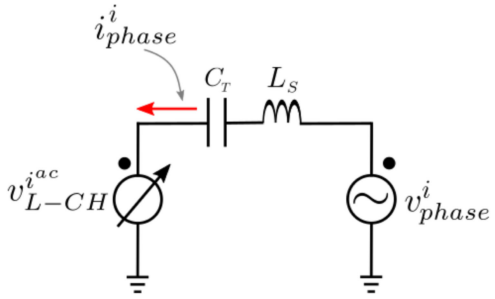

Fig. 13. Equivalent ac circuit of the *i*th converter phase ($i = 1, 2, 3$).

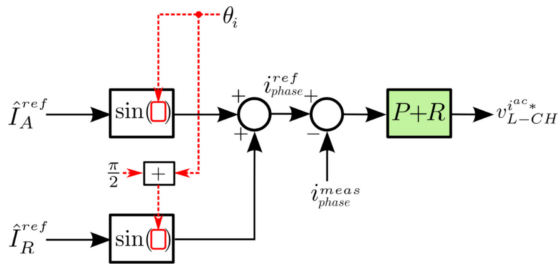

Fig. 14. Current control loops.

that cancel the ripple across C_T in each phase. The modulation signals for $v^i_{\text{T-CH}}(t)$ are derived from the ac current references and the values of the capacitors C_T. As a result, the voltages $v^i_{\text{T-CH}}(t)$ act as a 50–Hz disturbance for the small signal model of the current control. For this reason, the chain link that controls the current of the *i*th phase is only the corresponding $v^i_{\text{L-CH}}$. In conclusion, the equivalent circuit of the ac side can be represented as in Fig. 13, where the disturbance introduced by the T-CH generator has been neglected for brevity.

The current control proposed in this article is realized in the *abc* frame and three single-phase PLLs based on quadrature signal generation and the Park transformation [30] are used for grid synchronization. In order to track the alternating current reference, a proportional–resonant controller, derived in [31], has been used for each phase, as shown in Fig. 14.

The output of the controller constitutes the ac modulation signal $v^{i^{ac_*}}_{\text{L-CH}}$ of the corresponding L-CH modulator.

B. Energy Control

The energy control should guarantee that the total energy stored in the converter is maintained at the reference value and that uniform energy distribution is achieved within each chain link. These needs are met via a three-level control structure that consists of the following: TEC, interphase control (IPC), and intrachain-link balancing (ICB).

The dynamics of the average voltage in each chain link are approximated by the *s*-domain transfer function that can be obtained via linearizing the nonlinear differential equation that describes the system

$$G_P = \frac{V_{C_{\text{eq}}}(s)}{P(s)} = \frac{1}{sV_{\text{SM}}C_{\text{SM}}}. \tag{32}$$

This transfer function describes the relationship between the input power $P(s)$ and the output voltage $V_{C_{\text{eq}}}(s)$ of a generic chain link of SMs about the quiescent working point.

1) TEC Control: The TEC in Fig. 15 ensures that the total energy stored in converter SMs is maintained at the desired level. To do so, this control acts simultaneously on both the L-CHs and the T-CHs total energies. The reference voltage $V^{\text{ref}}_{C_{\text{eq}}\sum} = (3 \cdot N_{\text{SM}_{\text{L-CH}}} + 3 \cdot N_{\text{SM}_{\text{T-CH}}}) \cdot V^{\text{ref}}_{\text{SM}}$ is compared with a feedback of the total voltage "available" in the converter $V^{\text{meas}}_{C_{\text{eq}}\sum}$, i.e., the sum of all the SM voltages, and the error is processed by a proportional–integral (PI) controller that defines the peak of the active component of the grid current reference, thus defining the ac active power. However, a small part of this power must be "intercepted" by the T-CHs in order to maintain the local energy balance by compensating for semiconductor loss. To do so, a resistive voltage component is added to $v^i_{\text{T-CH}}$ of (11) via a controllable angle δ^i

$$v^i_{\text{T-CH}} = -\omega_g \cdot L_{\text{eq}} \cdot \frac{1}{r}\hat{I}_{\text{ref}} \sin\left(\omega_g \cdot t + \frac{\pi}{2} - \varphi - \frac{i-1}{3}\pi - \delta^i\right). \tag{33}$$

The measured "available voltage" in the T-CH of the *i*th phase $V^{\text{meas}}_{C_{\text{eq}}(\text{T-CH}^i)} = \sum_{j=1}^{N_{\text{SM}_{\text{T-CH}}}} v^j_{\text{T-CH}^i}$ is subtracted from the reference voltage $N_{\text{SM}_{\text{T-CH}}}V_{\text{SM}}$, and then the output of a PI controller defines the controllable angle δ^i of the corresponding T-CH. The modulation signal of the corresponding T-CH is defined by a voltage function according to (33).

2) IPC Control: During the converter operation, mismatches between the energy stored in the different phases can arise. It is then necessary to add another level of energy control to equalize the energy storage. This control acts on the net power exchange between different converter phases. However, it does not modify the power reference generated by the TEC, but it is designed to distribute the power reference differently between the converter phases to reach energy equalization. It is worth noting that only the differential energy of two pairs of phases are required since the third is a combination of the other two. The implementation of this additional level of control is shown in Fig. 16.

Considering that the dc power is imposed by the load and V_{dc}, by adjusting the contribution of each L-CH to the dc voltage, it is possible to modify the net power exchanged by the chain link. Each L-CH dc component is modified via the corresponding ΔV^*_{dc}. It is important to remark that the IPC does not affect the power exchanged on the dc side and the sum of the three dc components $\Delta V^*_{\text{dc}_{1,2,3}}$ is always zero. The parameters of the controllers are selected in order to obtain a dynamic response slower than the TEC loops to guarantee decoupling.

3) Modulation and ICB Control: The control loops generate the modulation signals for the converter chain links; however, they are generated assuming ripple-free SM voltages. If no additional action is taken, the interaction between the modulation signals and the SM voltage ripple will introduce chain-link voltage components at multiples of the line frequency. To avoid this, the modulation index $\text{Mod}(t)$ is compensated with the available

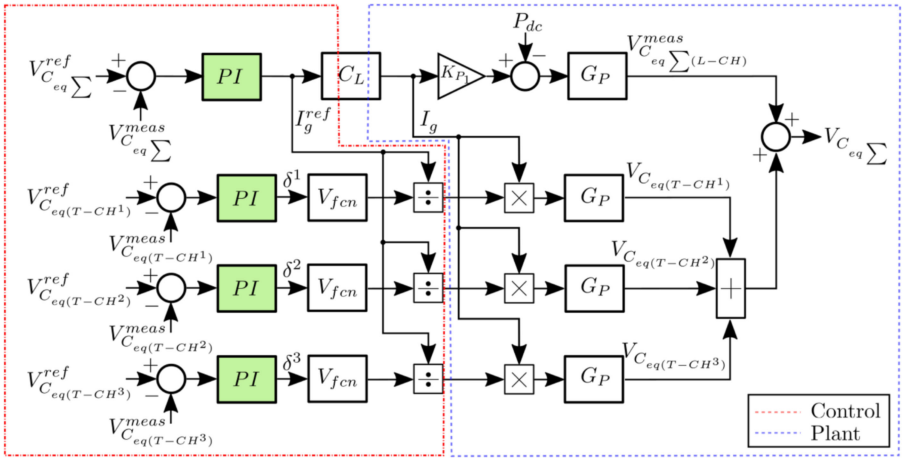

Fig. 15. TEC control loops. K_{P_1} is the power constant and it is equal to the rms value of the ac grid voltage. The TEC includes the PI that controls the voltage in the L-CHs (top PI) and the three PIs that control the voltage in the T-CHs. C_L is the closed-loop transfer function of the current control. The voltage function V_{fcn} is implemented according to (33).

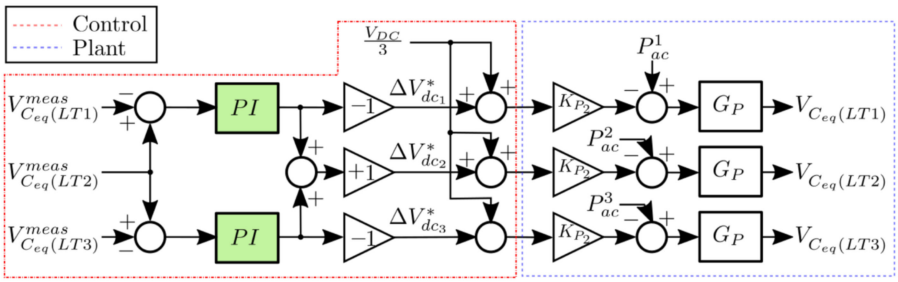

Fig. 16. IPC control loops. K_{P_2} is the power constant, which, in this control loop, is the value of the dc current. G_P is the transfer function between the voltage in the phase chain links and the input power. The sign of the $\Delta V^*_{\text{dc}_{1,2,3}}$ depends on the direction of the power flow. $V_{C_{\text{eq(LTi)}}}$ is the available voltage in the L-CH and the T-CH of the ith phase.

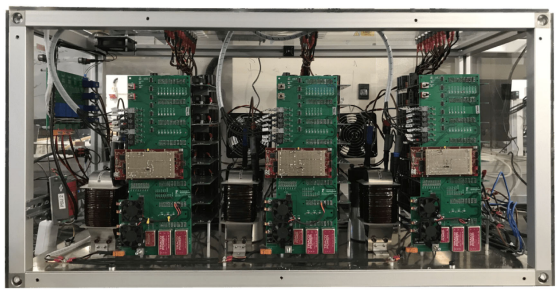

Fig. 17. Photograph of the experimental rig.

voltage in the corresponding chain link $V_{C_{\text{eq}}}(t)$ according to

$$\text{Mod}^c(t) = \frac{\text{Mod}(t)}{V_{C_{\text{eq}}}(t)} \cdot N_{\text{SM}} \cdot V_{\text{SM}} \tag{34}$$

where $\text{Mod}^c(t)$ is the compensated modulation signal of a generic chain link of SMs. The modulation technique used to produce the gate signals for the SM switches is based on the phase disposition pulsewidth modulation (PD-PWM) technique.

The ICB is used to equalize the SM voltages with a canonical sorting procedure [32], [33] and the algorithm implemented to sort the SMs is the so-called "bubble sort"—although it should be noted that any previously reported sorting method could be used. The submodulation signals will be sorted according to the sign of the current in order to equalize the voltage sharing within each chain link.

V. Experimental Setup

To validate the converter, a flexible modular multilevel prototype for laboratory purposes, shown in Fig. 17, has been designed and built. The control system is based on a master–slave architecture designed to achieve high control flexibility.

A. Laboratory Prototype

The converter has been designed for a nominal ac rms line-to-line voltage of 400 V and a dc voltage of 450 V. The total power rating is equal to 4.5 kVA with a power factor of 0.8. It is worth noting that each L-CH should be able to reproduce one-third of the dc voltage plus the corresponding ac voltage on the converter

side, as indicated in the following equation:

$$V_{\text{MAX}} = \frac{V_{\text{dc}}}{3} + r\hat{V}_{\text{phase}}. \tag{35}$$

With this assumption, the maximum peak value of the ac voltage produced by the converter cannot exceed 150 V (when the converter is operated at 450 V on the dc side): as a consequence, the transformer turns ratio has been selected to be equal to 240/90. This will leave, in nominal operating conditions, at least 10% ac voltage margin.

With the power rating defined, a sensible number of SMs should be selected to produce the multilevel waveforms output by the converter. Accordingly, five HB SMs ($N_{\text{SM}_{\text{L-CH}}}$) are used for each L-CH and the nominal voltage of each L-CH SM is 60 V according to the following equation:

$$V_{\text{SM}_{\text{L-CH}}} = \frac{V_{\text{MAX}}}{N_{\text{SM}_{\text{L-CH}}}} \simeq \frac{V_{\text{dc}}}{3}\frac{2}{N_{\text{SM}_{\text{L-CH}}}}. \tag{36}$$

To simplify the design, the T-SMs have also been chosen with the same voltage rating and three FB SMs have been adopted in each T-CH. The switching devices are Infineon IPB072N15N3 MOSFET, rated 150 V and 100 A. The capacitor in each SM is 5 mF, giving an equivalent H constant [26] of 50 ms. Two series-connected resistors are connected across the terminals of the "SM floating dc link" for discharging and measurement purposes. It is worth noting that less energy storage ($H = 38$ ms) is actually required to achieve the 10% voltage ripple in all SM because the SM in the T-CHs could have a lower capacitance. However, the same capacitance has been used in all the SMs for ease of manufacturing. Each phase of the converter is realized by stacking eight SMs (five L-CHs and three T-CHs) and connecting them to the same backplane, which interfaces a local slave controller with the control and sensing signals in each SM.

B. Control System

In this application, the control system has been implemented using off-the-shelf microcontroller units (MCUs). Monitoring all the SM voltages to ensure control of the energy stored in the SMs requires a number of analogue to digital converter (ADCs) that are not typically available in commercial MCUs. However, it is worth noting that SM voltage control is performed on the total voltage of each chain link and not on the single SM. This allows a control based on a master–slave architecture to be used, where a local slave MCU monitors each SM in the chain link and communicates to the master only the sum of the available voltages. In the SCC prototype, the central control board hosts a Texas Instruments F28379D controlCARD, acting as master (see Fig. 18). The master is connected to the local controllers via optical channels and to a measurement board via coaxial cables. In each SM stack, a F28377S LaunchPad sits on a local controller backplane (see Fig. 19).

VI. Experimental Results

In order to initially validate the new topology and the associated control scheme implemented in the experimental rig (see Table IV), full switching simulations have been performed

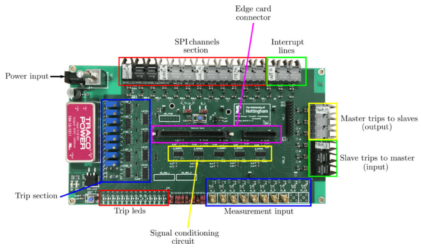

Fig. 18. Central controller docking board.

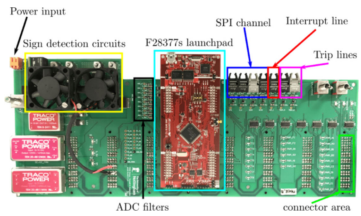

Fig. 19. Local control board.

TABLE IV
System Parameters

Symbol	Quantity	Value
V_{dc}	dc voltage	450 V
V_{LL}	line to line voltage	415 V
f_g	line frequency	50 Hz
r	transformer turns ratio	90/240
L_s	line inductance	1.7 mH
R_s	line resistance	0.3 Ω
L_{dc}	dc inductance	11.7 mH
R_{LOAD}	Load resistance	120 Ω
$N_{SM_{L-CH}}$	number of SMs for each L-CH	5
$N_{SM_{T-CH}}$	number of SMs for each T-CH	3
V_{SM}	SM nominal voltage	60 V
C_{SM}	SM capacitance	5 mF
R_{SM}	SM resistance	39.1 $k\Omega$
C_T	blocking capacitance	880 uF
f_{PWM}	PWM frequency	8 kHz
f_{SORT}	sorting frequency	2 kHz

in the MATLAB/Simulink environment in conjunction with the PLECS blockset. However, due to space, the experimental results are presented in preference in the following paragraphs. However, to illustrate the match between the simulation study and the experimental tests, the dynamic responses of the system are compared. For the experimental results, the converter has been used as a rectifier connected to a resistive load on the dc side, as shown in Fig. 7. On the ac side, the converter is connected to a three-phase auto transformer via three single-phase transformers. The parameters of the system are summarized in Table IV. Due to the large amount of waveforms to be recorded simultaneously, two different acquisition methods have been used. The results are recorded via the use of oscilloscopes and the master control board. Two oscilloscopes have been used to measure the following:

1) the L-CH voltages and the T-CH voltages;
2) the dc voltage; and

TABLE V
PARAMETERS OF THE IMPLEMENTED CONTROL LOOPS

Symbol	Bandwidth [Hz]	Parameter	Value
TEC L-CH	≈ 3.5	k_p	0.1
		k_i	1.0
TEC T-CH	≈ 3.5	k_p	0.1
		k_i	1.0
IPC	≈ 0.35	k_p	0.1
		k_i	0.1
PLL	≈ 3	k_p	0.2
		T_i	0.05
P+R	≈ 50.0	k_p	0.1
		k_R	0.1
		ω_c	1.0
		ω_c	$2\pi 50$
T-CH notch	–	ω_0	$2\pi 100$
		Q	10.0

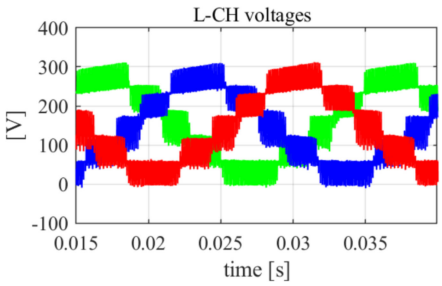

Fig. 20. Voltage waveforms produced by the L-CHs.

3) the voltages on the blocking capacitors C_T.

The first oscilloscope is a Yokogava DCM2024 with 200 MHz bandwidth and 2.5 GSa/s sample rate, and the second is Tektronix DP0 2024 with the same bandwidth and 1 GSa/s sample rate.

In addition, the master board stores the converter-side ac voltages/currents, the SM voltages, and the energy/current transients. The waveforms recorded via the master are sampled at 2 kHz—a quarter of the switching frequency (8 kHz).

The parameters of the control loops adopted have been obtained employing standard linear control design tools and are given in Table V. The notch filters included in the table are designed to reduce the voltage ripple on the feedback of the SM voltages of the T-CHs. The transfer function of the adopted filter is

$$H(s) = \frac{s^2 + \omega^2}{s^2 + \frac{\omega_0^2}{Q} s + \omega_0} \tag{37}$$

where ω_0 is the frequency to be canceled and Q is the quality factor of the filter.

A. Steady-State Converter Operation

These tests are mainly needed to verify if the controllers drive the system state variables to the reference values. In Fig. 20, the voltage produced by the three L-CHs are shown.

Fig. 21 shows the waveforms produced by the three T-CHs. Even though each T-CH is able to produce seven voltage levels,

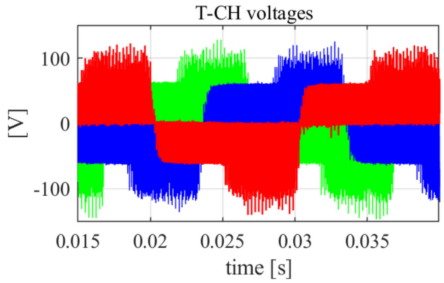

Fig. 21. Voltage waveforms produced by the T-CHs.

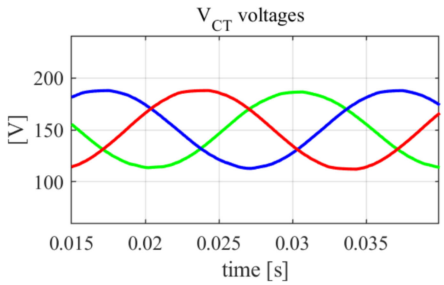

Fig. 22. Blocking capacitor C_T voltages.

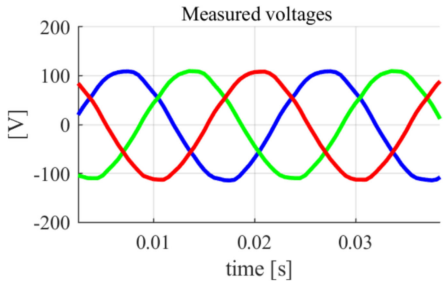

Fig. 23. AC voltages. The currents are measured on the converter side of the transformer.

only three levels are used in this operating condition. This is due to the fact that the amplitude of the voltage produced by this chain link is directly proportional to the phase currents, and in this experiment, the currents are below the nominal value. The appearance of extra levels in this figure is due to very short "error" pulses created by an interaction of the bridge dead-time delay and cycling of the zero state between upper and lower device pairs in each bridge to equalize losses. Due to their short duration, they have an insignificant effect on the overall operation. The voltage drops across the blocking capacitors C_T are presented in Fig. 22. The small differences in ac amplitude are mainly due to mismatches in the blocking capacitor values C_T. The voltages and currents on the ac side of the converter are shown in Fig. 23 and Fig. 24 respectively. The small distortion present in the current waveforms can be justified by the noncompensated dead times and by the fact that the network voltages feeding the auto transformer have some distortion.

Fig. 25 presents the SM voltages including both the L-CH and T-CH SMs. As expected, the SM working voltages match the reference value $V_{\mathrm{SM}}^{\mathrm{ref}} = 60\,\mathrm{V}$. The L-CH SMs have a

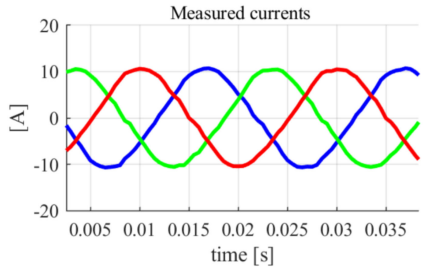

Fig. 24. AC currents. The currents are measured on the converter side of the transformer.

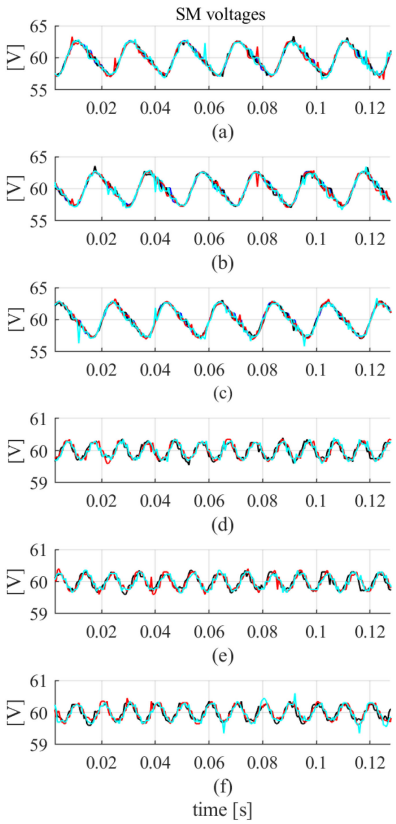

Fig. 25. SM voltages of the converter chain links. (a) L-CH SM voltages of the first phase. (b) L-CH voltages of the second phase. (c) L-CH voltages of the third phase. (d) T-CH SM voltages of the first phase. (e) T-CH voltages of the second phase. (f) T-CH voltages of the third phase. The colors used to mark the SMs of the L-CHs are, respectively, blue, green, black, red, and cyan. The colors used to mark the SMs of the T-CHs are, respectively, black, red, and cyan.

fundamental voltage ripple at 50 Hz, whereas, as expected, the T-CH SM voltages have a fundamental ripple at 100 Hz. The peak-to-peak voltage fluctuations are smaller in the T-CHs than in the L-CHs. Clearly, the T-CHs could have a smaller capacitance for the same peak-to-peak voltage ripple as the L-CHs. However, the same value of C_{SM} is used in both to unify and simplify the design.

B. Reactive Reference Variation

To test the functionality of the current control loops, independently from the dynamics of the energy control, a 6-A amplitude step in the reactive component of the current is imposed. The dc

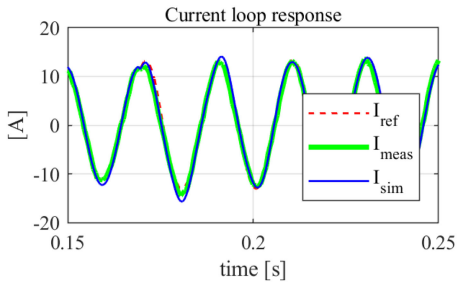

Fig. 26. Dynamic response of the current control loop to a variation of the reactive component set point.

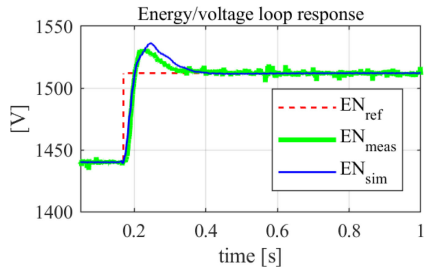

Fig. 27. Dynamic response of the total energy/voltage control loop to a variation of the energy/voltage reference value.

load during this test is $R_{\mathrm{LOAD}} = 90\,\Omega$. The dynamic response of the ac current control loops is shown in Fig. 26. This figure also shows a corresponding simulation result, illustrating the match between the modeling and the experimental results.

The phase current takes approximately one fundamental period to settle.

C. Energy Variation

In order to validate the dynamic response of the TEC, a 5% energy reference step was applied. In Fig. 27, the dynamics of the total energy controller are shown. The settling time of the energy loop is approximately 0.3 s according to the design bandwidth of the TEC loops. This result confirms the effectiveness of the analytical design and again the match between modeling and experiment is illustrated.

D. 32% Load Variation

To further verify the TEC response to perturbations, a 32% load variation has been applied. Initially, the converter operates with a dc load R_{LOAD} of 60 Ω, requiring an active power flow from the grid to the dc side of 3.3 kW. After a certain period, the network is switched to a resistor of 90 Ω, for an equivalent power flow of 2.25 kW. Despite the different load conditions, the controllers are still tuned according to Table V. The response of the TEC is shown in Fig. 28. After the load step, the system requires approximately 0.3 s to settle as expected according to the bandwidth of the TEC. A good match between the experimental results and the simulation model is demonstrated again.

VII. Conclusion

An innovative modular multilevel SCC has been presented. The proposed solution takes advantage of the inherent property

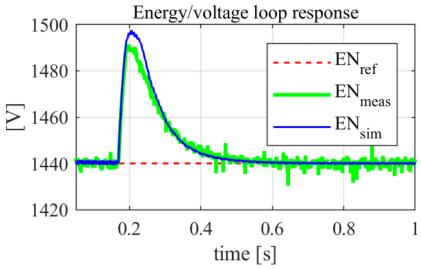

Fig. 28. Dynamic response of the energy/voltage control loop to load variation.

of a symmetric set of voltages in order to reduce the required number of SMs and to achieve a more concentrated energy storage than in a traditional MMC. As such, it is expected to be interesting where converter footprint is at a premium, for example, in offshore applications. The blocking capacitor C_T fulfills the task of removing the dc offset produced by the corresponding L-CH, and a T-CH is adopted "to cancel" the ac voltage drop across the blocking capacitors and also to provide an additional degree of freedom to deal with different converter operating conditions. The converter has the potential to reduce the number of required SMs by 60% while maintaining approximately the same energy storage of an equivalent MMC. In addition, the number of passive elements are reduced since the converter needs only three blocking capacitors. The experimental results from a laboratory-scale prototype prove the viability of this new solution.

APPENDIX

The minimum number of HB SMs for the L-CHs can be evaluated according to

$$N_{\mathrm{SM_{L\text{-}CH}}} = \left\lceil \left\lceil \sqrt{\frac{2}{3}} \frac{\left(\frac{(1+\mathrm{RM_{ac}})\cdot(2-\mathrm{RM_{dc}})}{1-\mathrm{RM_{dc}}}\right) r \cdot V_{\mathrm{LL}}}{V_{\mathrm{SM}}} \right\rceil \cdot k_r \right\rceil. \quad (38)$$

The minimum number of FB SMs of the T-CHs in the active configuration can be evaluated according to

$$N_{\mathrm{SM_{T\text{-}CH}}}^{\mathrm{Hybrid}} = \left\lceil \left\lceil \frac{\sqrt{6}}{5} \cdot \frac{(1+\mathrm{RM_{ac}}) \cdot r \cdot V_{\mathrm{LL}}}{V_{\mathrm{SM}}} \right\rceil \cdot k_r \right\rceil. \quad (39)$$

The minimum number of HB SMs of the T-CHs in the hybrid configuration can be evaluated according to

$$N_{\mathrm{SM_{T\text{-}CH}}}^{\mathrm{active}} = \left\lceil \left\lceil \sqrt{\frac{2}{3}} \frac{\frac{(1+\mathrm{RM_{ac}})\cdot(1+\mathrm{RM_{dc}})}{1-\mathrm{RM_{dc}}} \cdot r \cdot V_{\mathrm{LL}}}{V_{\mathrm{SM}}} \right\rceil \cdot k_r \right\rceil. \quad (40)$$

The energy fluctuation in the T-CH SMs of the hybrid configuration can be evaluated by

$$E(t) = \int \hat{V}_{\mathrm{T\text{-}CH}}^{i} \sin\left(\omega_g \cdot t + \frac{\pi}{2} - \varphi - \frac{i-1}{3}\pi\right) \cdot \frac{1}{r} \hat{I}_{\mathrm{phase}}^{i} \sin\left(\omega_g \cdot t - \varphi - \frac{i-1}{3}\pi\right) dt,\ i = 1,2,3 \quad (41)$$

where $\hat{V}_{\mathrm{T\text{-}CH}}^{i}$ is assumed to be approximately $V_{\mathrm{dc}}/6$. With a similar approach, the energy fluctuation in the T-CH SMs of the active configuration can be calculated by

$$E(t) = \int \frac{V_{\mathrm{dc}}}{3} \cdot \frac{1}{r} \hat{I}_{\mathrm{phase}}^{i} \sin\left(\omega_g \cdot t - \varphi - \frac{i-1}{3}\pi\right) dt. \quad (42)$$

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