Optimized SVM and Remedial Control Strategy for Cascaded Current-Source-Converters-Based Dual Three-Phase PMSM Drives System

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***Abstract*—In this article, the switching strategy and the remedial control scheme are studied for the cascaded current-source converters (CSCs) fed dual three-phase permanent-magnet synchronous motor (PMSM) variable-speed drives. An optimized space vector modulation (SVM) strategy is proposed to reduce the DC-link current ripple for the proposed drives system. In particular, this switching strategy can work effectively for motor drives under low speed with low back EMF, where there exists a large voltage difference between peak voltage values on the grid side and the motor side. Apart from that, a hybrid fault-tolerant control scheme is also designed for the open-phase fault in dual three-phase PMSM drives system, aiming at achieving small DC-link current ripple and torque ripple, low copper loss, and machine-friendly waveform quality. With the proposed optimized SVM and the hybrid fault-tolerant control strategy, the DC-link current ripple of the cascaded CSCs system can be effectively reduced and good operational performance can be obtained under both normal operation condition and open-phase fault condition. Experimental results are provided to verify the effectiveness of the proposed methods.**

***Index Terms*—Current-source converter (CSC), DC-link current ripple, dual three-phase permanent-magnet synchronous motor (PMSM), remedial control, space vector modulation (SVM).**

I. Introduction

NOWADAYS, electric drives with multiphase machines have drawn great attention in some modern industry applications, such as elevator traction system, electric and hybrid electric vehicles, electric ship propulsion, and more-electric aircrafts [1], [2]. Multiphase machines are regarded as suitable candidates for high-power and high-reliability applications, offering some potential advantages over their three-phase counterparts in these applications, such as high power rating, low torque ripple, and high fault-tolerant capability [3]. Dual three-phase motor drives, which are aimed at dual three-phase winding stator machines, six-phase machines, and open-end windings machines, are one kind of multiphase drives systems [9]. The symmetrical windings with a 60° phase-shift angle and the asymmetrical windings with a 30° phase-shift angle are two widely studied categories of dual three-phase permanent-magnet synchronous motors (PMSMs). Between them, the asymmetrical dual three-phase PMSM drives have advantages of eliminating the sixth-harmonic pulsating torque component due to the opposition of these components produced by two sets of three-phase windings [4]. Moreover, dual three-phase windings could be designed in one stator with no magnetic coupling. Therefore, faults in one winding will have little impact on the operation of the other winding. The reliability and the fault-tolerant ability of the drive system are thus increased [5].

Many previous studies have been carried out for multiphase drives, where multiphase machines are usually supplied by two or more modular VSIs [5]–[8]. The technique of vector space decomposition has been proposed for modeling and control of dual three-phase motor drives, where three two-dimensional orthogonal subspaces are decoupled, and thereby modeling and control of machines are simplified [6]. A simple but effective two-step voltage vector synthesis method was proposed for parallel T-type neutral-point-clamping (T-NPC) inverters fed double-stator-winding PMSM drives with closed-loop controllers on harmonic subspace in [5]. With this method, good dynamic response and harmonic performance are obtained in the drives. In [7] and [8], the suppression of low-order harmonics and unbalanced currents between dual three-phase windings are studied for the dual three-phase induction motor drives and dual three-phase PMSM drives, respectively.

However, to the best of the authors' knowledge, all of the previous multiphase drives are focused on voltage-source converters fed drives. On the other hand, the current-source converters (CSCs) technology, employing an inductor choke as the DC link, has been widely applied for high-power drives. The CSCs based high-power drive offers advantages of motor-friendly waveforms, low *du/dt*, and reliable overcurrent and short-circuit protection [9]–[11]. So far, there have been some works focusing on applying the series CSCs to wind power generation system [12], [13], [27], [28]. An interconnecting structure has been proposed for an offshore wind farm high-voltage DC transmission to eliminate the need of offshore transformers, where PWM CSCs

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are connected in series at the generator side for more power transmission [12]. In [13], the offshore wind farm employed the cascaded PWM CSCs configuration, which has some advantages of simple system topology and operation, as well as eliminating the bulky central offshore converter platform that usually used in a VSC-based counterpart. In addition, an optimized strategy is proposed to reduce cost and improve the operation efficiency of series-connected CSCs based offshore wind conversion systems without extra components or auxiliary circuits [27]. Lee and Sul [28] introduced a series-connected CSCs typology for the variable speed wind turbine generation system as a promising alternative to conventional VSCs based parallel connected system. Such a series typology can be connected to multiphase PMSM, so that the medium voltage system can be easily achieved even applying low-voltage switching devices to CSCs. However, only ordinary control scheme and PWM strategy were discussed.

For a CSCs system, the large DC-link current ripple is always regarded as a challenging issue since it may result in output current harmonics, electromagnetic interference, additional power losses, and system instability [14]. Conventionally, one solution for mitigating DC-link current ripple is to increase the DC-link inductor, but with the cost of bulky size, high cost, and slow dynamic response of the system. In [14], a method was proposed to adjust the pulse patterns of space vector modulation (SVM) between the rectifier and the inverter in a back-to-back CSCs system, and the DC-link current ripple was mitigated significantly. In [15], the reduction of DC-link current ripple was achieved in paralleled back-to-back CSCs by proper selection of redundant switching states and sequence design with the steady-state current balancing control principle. In [16], the DC-link current ripple was suppressed for paralleled current-source grid-connected converters under unbalanced grid conditions by designing the hybrid current controller. By this way, the double-frequency oscillations in active power at AC side can be suppressed effectively. However, those works are investigated for paralleled CSCs based energy conversion systems. In [17], Liu *et al*. propose an optimized SVM strategy to reduce the DC-link current ripple in the cascaded CSCs system and give experiments with the *RL* load. However, the collaborative modulation and control of cascaded CSCs based multiphase PMSM drives system are still absent and need further investigation.

On the other hand, multiphase drives system can offer higher fault-tolerant capability compared with their three-phase counterparts. A lot of existing surveys have been focused on fault analysis and fault-tolerant control of drives system [18]–[20]. However, those methods are only considered with VSCs technology. The fault-tolerant control of multiphase machine based on CSCs is still rare. The short-circuit faults in power switches of CSCs are usually tolerated by forcing shoot-through operation in the converter leg comprising the faulty switch. Thus, the total three-phase converter module can be bypassed and there is no impact on other modules. In [21], a fault ride-through strategy for CSC-based offshore wind farm was proposed, where the inherent short-circuit operating capability of CSC is applied to isolate the faulty three-phase PMSG without influencing other cascaded wind turbines. On the other hand, the open-circuit fault

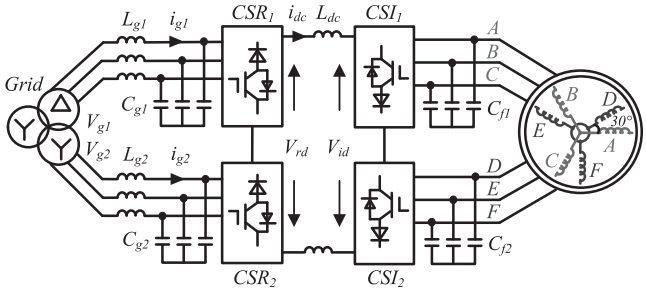

Fig. 1. Configuration of cascaded CSCs fed dual three-phase PMSMs system.

is more challenging for CSCs drive system since the DC-link choke will excite a large voltage spike due to open-circuit fault. In [22], the mapping sinusoidal pulsewidth modulation (SPWM) technique has been deduced for five-phase current source inverter (CSI) system under both the healthy and the open-circuit fault conditions. However, it indicates that the smaller current conduction time is distributed for each phase leg compared with the three-phase CSCs system such that larger DC-link current will be required. In addition, only the static *RL* load is employed in the simulation to explore the specified cases. Therefore, fault-tolerant controls of CSCs based multiphase drives, in particular for the open-circuit faults, need further investigation.

In this article, a cascaded CSCs based dual three-phase PMSM drives system will be proposed, which could not only inherit advantages of multiphase drives but also make full of techniques of three-phase CSCs. Since the cascaded configuration is adopted, the proposed CSCs system is suitable for medium-voltage motor drives. In addition, the dual bridge CSCs on the grid side and the motor side of this drives system offer more control freedoms in suppressing the DC-link current ripple under normal and open-circuit fault conditions. Therefore, optimized gate patterns of SVM are investigated and proposed to reduce DC-link current ripple in the cascaded CSCs drives system with variable speeds and loads under normal condition. For open-phase fault in dual three-phase PMSM, a fault-tolerant control scheme and a modified SPWM strategy are applied to cascaded CSIs, aiming at achieving smaller DC-link current ripple and torque ripple.

II. Configuration and Control Schemes

A. Configuration and Modeling

The configuration of the cascaded CSCs fed dual three-phase PMSM drives system is shown in Fig. 1. In this drives system, power suppliers are two AC voltage sources from the phase-shifting transformer, which has a 30° shifted phase angle on the secondary output ports. By using the phase-shifted transformer, the harmonic performance of grid line currents of primary side can be improved [23]. The cascaded CSIs are applied to supply power for motor drives on the inverter side. Three-phase filter capacitors are needed on both the rectifier side and the inverter side to assist phase commutation of power switches and suppressing current harmonics. However, the inductor–capacitor (*LC*) resonance, which is caused by filter capacitors and filter inductors on the grid side or filter capacitors and stator inductors

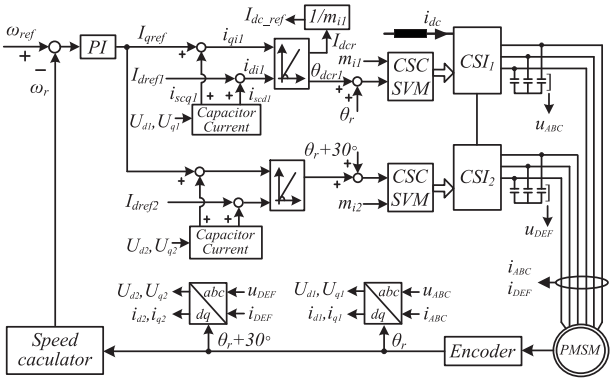

Fig. 2. Block diagram of control scheme of CSIs on the motor side.

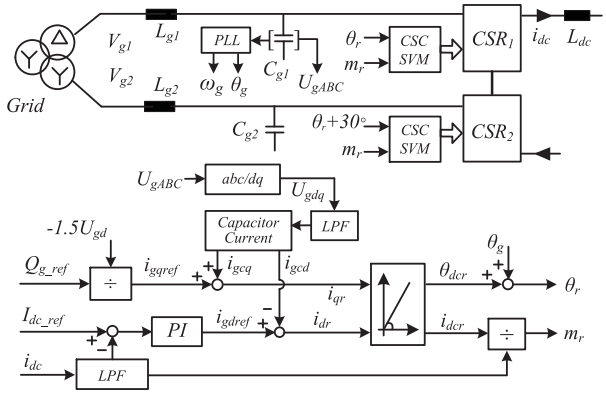

Fig. 3. Block diagram of control scheme of CSRs on the grid side.

on the load side, is always considered as the challenging issue for the CSCs energy conversion system. Therefore, proper control methods such as hybrid combination approach and dynamic voltage control are needed to damp the *LC* resonance [23], [24].

As aforementioned, the asymmetrical winding distributions machines have the advantage of better torque ripple performance. Therefore, a non-salient dual three-phase PMSM with a 30° shifted phase angle between two adjacent phase windings is adopted in this article. Supposed that the magnetic saturation, the mutual leakage inductance, and core losses are neglected, while assuming sinusoidal distribution of phase windings, the voltage, flux, and back EMF models of a non-salient dual three-phase PMSM can be expressed as follows [5]:

$$u_s = R_s i_s + p\psi_s \tag{1}$$

$$\psi_s = L_s i_s + \psi_f \phi(\theta_r)_s \tag{2}$$

$$e_s = p\left[\psi_f \phi\left(\theta_r\right)\right] \tag{3}$$

where *s* is associated to six phases of dual three-phase PMSM (*s* = *A, B, C, D, E,* and *F*), and *p* denotes the differential operator. u_s is the phase terminal voltage, i_s is the phase current, R_s is the stator resistance, ψ_s is the stator flux, and L_s is the self-inductance. $\psi_f \phi(\theta_r)_s$ is the rotor flux related to motor phase, where θ_r is the electrical angle of the motor, ψ_f is the magnitude of rotor magnetic flux produced by PM, $\phi(\theta_r)_s$ is respect to motor phases from *A* to *F* [$\varphi(\theta_r)_s = \cos(\theta_r)$, $\cos(\theta_r - 2\pi/3)$, $\cos(\theta_r + 2\pi/3)$, $\cos(\theta_r - \pi/6)$, $\cos(\theta_r - 5\pi/6)$, $\cos(\theta_r + \pi/2)$, $s = A \ldots F$]. The electrical torque of the dual three-phase PMSM drives is given as follows:

$$T_e = 3/2 N_P \psi_f \left(i_{q1} + i_{q2}\right) \tag{4}$$

where N_p is the rotor pole-pairs, i_{q1} and i_{q2} are the *q*-axis currents of two sets of three-phase windings (namely phases *A*, *B*, *C* and phases *D*, *E*, *F*) under *dq*-axis reference frame, respectively.

B. Control Schemes

As shown in Fig. 2, a simple field-oriented-control (FOC) scheme with dual three-phase SVM is employed in the cascaded CSIs on motor side to regulate the dual three-phase PMSM drives. Since the configuration of two sets of CSIs drives is identical, control schemes of CSI_1 and CSI_2 are almost the same except for the only difference of the feedback electrical angle from the motor, as shown in Fig. 2. Take the control scheme of CSI_1 as an example, the speeds ω_r of machine is fed back with a speed regulator to track the speed reference value ω_{ref}. The *dq*-axis current references for CSI_1 are generated with the compensation of filter capacitor currents i_{scd} and i_{scq}, which are expressed as

$$\begin{aligned} i_{di1} &= I_{\text{dref1}} + i_{scd} = -\omega_r U_{q1} C_f \\ i_{qi1} &= I_{\text{qref}} + i_{scq} = I_{\text{qref}} + \omega_r U_{d1} C_f \end{aligned} \tag{5}$$

where I_{qref} is the torque producing current given by output of speed regulator. The *d*-axis current reference I_{dref1} is normally set as zero for maximum torque per current (MTPA) in non-salient dual three-phase PMSM drives. The U_{d1} and U_{q1} are the *d*-axis and the *q*-axis voltages of filter capacitor, respectively. Since this article mainly focuses on the cascaded CSCs drive under low speed with low back EMF, the differential terms of capacitor currents can be neglected to reduce the sensitivity and noise and only the steady-state terms are calculated in (5) [11].

The power-factor angle θ_{dcr1} and the CSI_1 output current commands I_{dcr} are calculated with the polar coordinate conversion module and then switching pulses for the CSI_1 are generated with CSC SVM. Finally, the DC-link current reference I_{dc_ref} for the CSCs based drive can be obtained as

$$I_{dc\_\text{ref}} = \frac{I_{dcr}}{m_{i1}} = \frac{\sqrt{{i_{di1}}^2 + {i_{qi1}}^2}}{m_{i1}} \tag{6}$$

where m_{i1} is the modulation index of CSI_1, which ranges from 0 to 1. It is clear from (6) that with a given CSI output current command, the DC-link current has a reverse relationship with the CSI modulation index. Under a given power condition, the lower DC-link current leads to smaller DC-link current ripples as well as lower losses on the DC-link inductance and switching devices. The minimum DC-link current control is achieved when the modulation index m_{i1} is set to 1 [25]. Therefore, a unity modulation index strategy is applied to calculate the DC-link current reference on the motor side, whereas the DC-link current is controlled by CSRs on grid side according to the DC-link current reference.

As shown in Fig. 3, the voltage-oriented control scheme is developed for cascaded CSRs on the grid side. The main purpose of

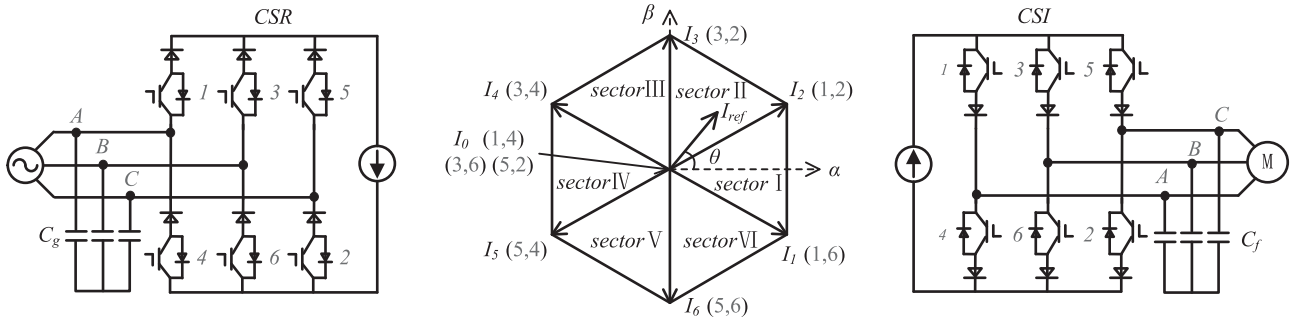

Fig. 4. Traditional SVM scheme for CSRs and CSIs.

grid-side control is the DC-link current and reactive power regulation. The DC-link current control is implemented to meet the motor-side requirement, whereas the reactive power regulation is employed to satisfy the grid code [11]. The DC-link current reference $I_{\text{dc\_ref}}$ is determined by the current requirement from the motor side. The DC-link current i_{dc} of CSRs is controlled with a DC-link current regulator, which generates the *d*-axis grid current $i_{g\text{dref}}$. Reactive power of the grid can be independently controlled by setting the desired reactive power reference Q_{g_ref}, which is used to generate the *q*-axis grid current $i_{g\text{qref}}$. Normally, the Q_{g_ref} is set as zero to implement the unity power factor control on the grid side. The *dq*-axis current references for CSRs can be calculated with the compensation of the filter capacitor currents i_{gcd} and i_{gcq} as

$$\begin{aligned} i_{dr} &= i_{gd\_\text{ref}} + i_{\text{gcd}} = i_{gd\_\text{ref}} - \omega_g U_{gq} C_g \\ i_{qr} &= i_{gq\_\text{ref}} + i_{gcq} = \omega_g U_{gd} C_g \end{aligned} \tag{7}$$

where ω_g is the electrical angular velocity of the grid obtained from *PLL*, and U_{gd} and U_{gq} are the *d*-axis and the *q*-axis voltages of the filter capacitor, respectively. Similarly, the differential terms of capacitor currents are neglected and only the steady-state current are used in (7). Finally, switching pulses for each CSR are produced with CSC SVM according to the different vector angle and the modulation index, as shown in Fig. 3.

III. Proposed Optimized SVM Strategies

Normally, mitigation of DC-link current ripple can be achieved by increasing the DC-link inductor choke. However, this method results in bulky size, high cost, and slow dynamic response of the system. In this article, instead of adding the physical damping inductor, a collaborative SVM pulse patterns adjustment technique among the cascaded CSRs and the cascaded CSIs is investigated to reduce the DC-link current ripple significantly.

A. Previous Modulation Scheme

The SVM, which offers better dynamic adjustment ability, is adopted in this article. The SVM can be implemented with three-, five-, or seven-segment switching sequences [26]. The modulation with more segments can bring benefits to the DC-link current ripple reduction, but also result in more switching commutations and losses. In particular, more segments would bring more algorithm complexity when collaborative control among cascaded CSCs is designed. Therefore, only typical three-segment switching sequences are discussed in this article.

As presented in Fig. 4, the SVM scheme for CSCs has six active vectors (I_1–I_6) and three zero vectors (I_0). The reference I_{ref} can be synthesized by three nearest vectors, namely two active vectors and one zero vector. According to ampere–second balancing principle, the dwell time T_1, T_2, and T_0 for three vectors can be calculated as

$$\begin{aligned} T_1 &= m_a \sin(\pi/6 - \theta)\, T_s \\ T_2 &= m_a \sin(\pi/6 + \theta)\, T_s \\ T_0 &= T_s - T_1 - T_2 \\ m_a &= I_{\text{dc\_ref}}/i_{\text{dc}} \end{aligned} \tag{8}$$

where T_s denotes the sampling period, m_a stands for the modulation index, and θ is the vector angle ($-\pi/6 < \theta < \pi/6$). More details of SVM strategy for CSCs can be inferred in [23].

Basically, when the DC-link inductor is fixed, the DC-link current ripple Δi is determined by both the voltage-drop ΔV across the inductors and the dwell time Δt, illuminated as

$$\Delta i = \frac{\Delta V}{L}\Delta t = \frac{V_{rd} - V_{id}}{L}\Delta t \tag{9}$$

where V_{rd} and V_{id} are the DC-link voltages of the cascaded CSRs and CSIs, respectively. The DC-link current ripple can be reduced by decreasing ΔV and Δt. However, for a specified current space vector, the dwell time Δt is constant and the voltage-drop ΔV is the main influence factor of DC-link current ripple [14]. So, only voltage-drop reduction is considered in this article.

As investigated in [14], there are six possible arrangements for pulse pattern in one sector, and there are much more possible pulse patterns if they are considered in different six sectors of both the rectifier and the inverter. To reduce the DC-link current ripple, the voltage-drop on DC inductor should be controlled as small as possible. Fig. 5(a) shows the optimized pulse pattern arrangement of current space vector diagram for the back-to-back CSCs in [14].This pulse pattern is defined as the (L-M-S)–(L-M-S) type since the corresponding rectifier voltage amplitude of current vectors I_{r1}, I_{r2}, and I_{r0} are $V_{r1} > V_{r2} > V_{r0}$ and the corresponding inverter voltage amplitude of current vectors I_{i1}, I_{i2}, and I_{i0} are $V_{i1} > V_{i2} > V_{i0}$, where L, M, and S mean large, middle, and small, respectively. This method does not cause any

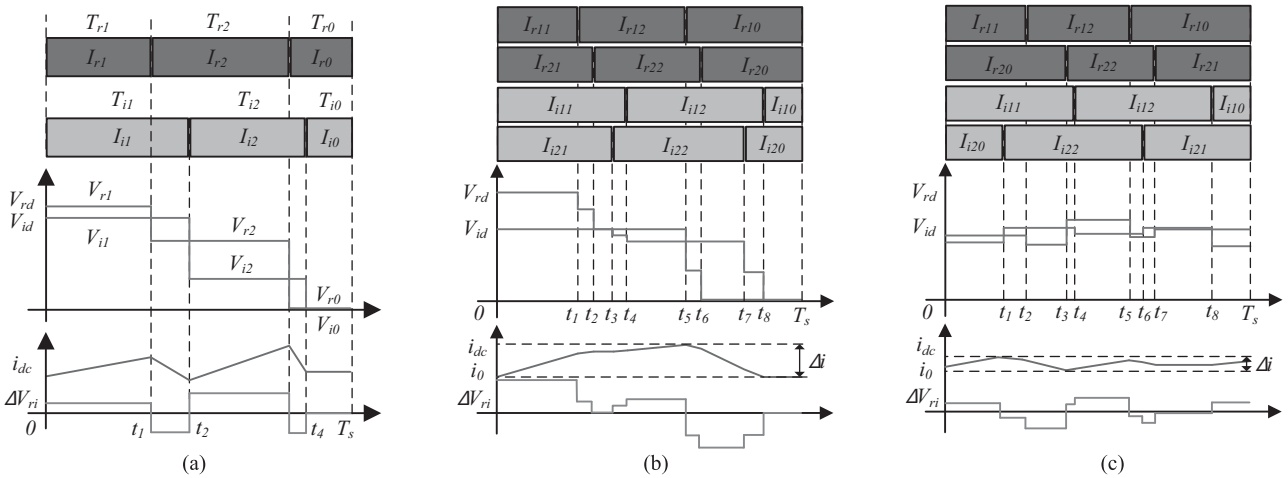

Fig. 5. Pulse pattern arrangements for current vectors and the corresponding DC-link current and voltages. (a) Previous proposed SVM strategy in [14]. (b) Exemplified SVM strategy. (c) Proposed optimized SVM strategy.

additional commutations loss compared with the conventional SVM method. Unfortunately, this method is out of discussion in applications where the voltage on one AC side is much lower than that on the other side (e.g., for a motor drive system working at low speed).

B. Proposed Modulation for Cascaded CSCs

Different from [14], a cascaded CSCs fed dual three-phase PMSM variable-speed drives system is considered in this article, where the motor may operate with low speeds. Under these conditions, the AC voltage on motor side is much lower than that on the grid side. As shown in Fig. 1, the DC-link voltage of the cascaded CSRs V_{rd} is the sum of DC-link voltages of CSR_1 and CSR_2, and the DC-link voltage of the cascaded CSIs V_{id} is the sum of DC-link voltages of CSI_1 and CSI_2. Therefore, there are more flexible arrangements of pulse patterns among the rectifier sides and inverter sides.

Assumed that I_{r11}, I_{r12}, and I_{r10} are the current vectors of CSR_1, and their corresponding DC-link voltage voltages are V_{r11}, V_{r12}, and V_{r10}, whereas the corresponding DC-link voltages of CSI_1 vectors I_{i11}, I_{i12}, and I_{i10} are V_{i11}, V_{i12}, and V_{i10}, respectively. For the simplicity of analysis, only the relationship of $V_{r11} > V_{r12} > V_{r10}$ and $V_{i11} > V_{i12} > V_{i10}$ is used for exemplification in this article. The current vectors and the corresponding DC-link voltage voltages of CSR_2 and CSI_2 are defined as I_{r21}, I_{r22}, I_{r20}, and I_{i21}, I_{i22}, I_{i20}, and $V_{r21} > V_{r22} > V_{r20}$, and $V_{i21} > V_{i22} > V_{i20}$, respectively. The definitions of DC-link voltages V_{kxy} in corresponding of six sectors are noted in Table I while the dwelling time of those current vectors are named as $T_{kxy}(k = r,\ i;\ x = 1,\ 2;\ y = 0,\ 1,\ 2)$. The subscripts $k = r/i$ denote the rectifier/inverter sides, $x = 1,\ 2$ stands for CSC_1 and CSC_2, and $y = 0,\ 1,\ 2$ presents the three current vectors. Noted that the variables appeared in the following figures are the same definition as those in Table I.

Take Fig. 5(b) for the example, i_{dc} stands for the DC-link current, Δi is the DC-link current ripple, ΔV_{ri} is the voltage difference between the rectifier and inverter side, V_{rd} and V_{id} are DC-link voltages of rectifier and inverter side, respectively. For the simplicity of analysis, the DC-link voltages are regarded as constant values in every sampling period. It is illustrated in Fig. 5(b) that the DC-link inductor current acts as a piecewise function because night segments are presented in one sampling period T_s. The DC-link current increases or decreases according to the positive and negative signs of the voltage difference ΔV_{ri} between the rectifier and inverter sides during the sampling period T_s. Furthermore, the increasing and decreasing amplitudes of DC-link current are determined by voltage drops in each time interval.

TABLE I
DEFINITION OF DC-LINK VOLTAGES

Sector	V_{kx1}	V_{kx2}	V_{kx0}
sector Ⅰ	V_{kab}	$-V_{kca}$	0
sector Ⅱ	$-V_{kca}$	V_{kbc}	0
sector Ⅲ	V_{kbc}	$-V_{kab}$	0
sector Ⅳ	$-V_{kab}$	V_{kca}	0
sector Ⅴ	V_{kca}	$-V_{kbc}$	0
sector Ⅵ	$-V_{kbc}$	V_{kab}	0

In the case of Fig. 5(b), the DC-link current mainly increases during time interval $0{\sim}t_5$ and decreases during time interval $t_5{\sim}t_8$, so the DC-link current ripple Δi can be approximately considered as the increasing amplitude during time interval $0{\sim}t_5$. This pulse pattern is defined as $(I_{r11} - I_{r12} - I_{r10},\ I_{r21} - I_{r22} - I_{r20})$–$(I_{i11} - I_{i12} - I_{i10},\ I_{i21} - I_{i22} - I_{i20})$. It should be noted that this kind of pulse pattern is the optimized pulse pattern arrangement of current space vector proposed in the literature [14]. Namely, all current vectors of both CSRs and CSIs are arranged from large to small. However, there still exists large DC-link current ripple, as can be observed in Fig. 5(b). The reason lies in that the AC voltage on grid side is much larger than the AC voltage on motor side under low speed operation.

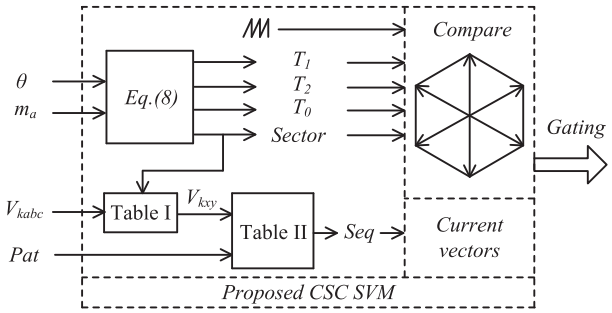

Fig. 6. Generation of pulses patterns for cascaded CSRs and CSIs.

To keep voltage balance on two sides of DC-link, the dwell time of zero current vectors I_{r10} and I_{r20} on grid side are much longer than the dwell time of I_{i10} and I_{i20} on motor side. On the other hand, the dwell time of active current vectors on grid side are much smaller than the dwell time of active current vectors on motor side. So, there still exists a certain period with large voltage drops between two sides of DC link during the switching interval $T_{\rm s}$.

To solve this problem, a collaborative arrangement of pulse patterns is proposed for cascaded CSCs in this article, considering not only the cooperation between CSRs on grid side and CSIs on load side, but also the coordinated cooperation of the series CSRs and the series CSIs. Take the CSRs side for example, assumed that rectifier voltages are $V_{r11} > V_{r12} > V_{r10}$ of $\rm CSR_1$, and $V_{r21} > V_{r22} > V_{r20}$ of $\rm CSR_2$. When the current vectors of $\rm CSR_1$ are arranged as $(I_{r11} - I_{r12} - I_{r10})$, the current vectors of $\rm CSR_2$ is arranged as $(I_{r20} - I_{r22} - I_{r21})$. Namely, the sequence of current vectors of $\rm CSR_1$ is arranged in the opposite sort compared to that of $\rm CSR_2$ regarding to their corresponding voltages on DC link. By this way, the DC-link voltage peaks can be mitigated by cascaded CSRs on the grid side. The similar arrangement of switching sequence can be applied to the CSIs on the motor side. Therefore, voltage drops between two sides can be reduced effectively, and the DC-link current ripple can be mitigated naturally, as shown in Fig. 5(c).

The generation of pulse patterns in series CSRs and CSIs sides are presented in Fig. 6, where definitions of the pulse pattern and determination of current vectors sequence are listed in Table II. Pattern P_0 means that the voltages of current vectors are arranged from large to small, whereas pattern P_1 denotes that the voltages of current vectors are arranged from small to large. The subscripts *k*, *x,* and *y* are defined the same as that shown in Table I. Different from conventional SVM strategy, the generation of switching pulses with the proposed optimized SVM in Fig. 6 can be summarized as following: first, after the vector angle θ and modulation index m_a are obtained, the sector and the dwell time T_1, T_2, and T_0 are calculated by (8). The DC-link voltage V_{kxy} is defined according to the measured voltage V_{kabc} and the sector number in Table I. Second, the sequences for each CSC module are determined by different relationships of V_{kxy} and the given pulse pattern in Table II. For example, when the pulse pattern P_0 is applied to one of the series CSC modules, the pattern P_1 should be applied to another module. Finally, current vectors are arranged to generate the specialized gating signals by comparing the calculated dwell time with the saw-tooth carrier. The generation principle is adopted in both the grid side and the motor side. In summary, not only the cooperation between the grid side and the motor side, but also the coordinated cooperation between the series CSCs are considered in the proposed collaborated SVM strategy during design of pulse patterns for CSCs.

TABLE II
DEFINITION AND DETERMINATION OF CURRENT VECTORS

Pattern	*Relations of V_{kxy}*	*Sequence*	*Current vectors*
P_0	$V_{kx1} > V_{kx2} > V_{kx0}$	1	I_{kx1}-I_{kx2}-I_{kx0}
	$V_{kx1} > V_{kx0} > V_{kx2}$	2	I_{kx1}-I_{kx0}-I_{kx2}
	$V_{kx2} > V_{kx1} > V_{kx0}$	3	I_{kx2}-I_{kx1}-I_{kx0}
	$V_{kx2} > V_{kx0} > V_{kx1}$	4	I_{kx2}-I_{kx0}-I_{kx1}
	$V_{kx0} > V_{kx1} > V_{kx2}$	5	I_{kx0}-I_{kx1}-I_{kx2}
	$V_{kx0} > V_{kx2} > V_{kx1}$	6	I_{kx0}-I_{kx2}-I_{kx1}
P_1	$V_{kx1} > V_{kx2} > V_{kx0}$	6	I_{kx0}-I_{kx2}-I_{kx1}
	$V_{kx1} > V_{kx0} > V_{kx2}$	4	I_{kx2}-I_{kx0}-I_{kx1}
	$V_{kx2} > V_{kx1} > V_{kx0}$	5	I_{kx0}-I_{kx1}-I_{kx2}
	$V_{kx2} > V_{kx0} > V_{kx1}$	2	I_{kx1}-I_{kx0}-I_{kx2}
	$V_{kx0} > V_{kx1} > V_{kx2}$	3	I_{kx2}-I_{kx1}-I_{kx0}
	$V_{kx0} > V_{kx2} > V_{kx1}$	1	I_{kx1}-I_{kx2}-I_{kx0}

IV. FAULT-TOLERANT SCHEME FOR OPEN-CIRCUIT FAULT

As aforementioned, the open-circuit fault is a challenging issue in CSCs based motor drives. Therefore, a fault-tolerant control scheme and a modified SPWM strategy are proposed for the cascaded CSIs fed dual three-phase PMSM drives under one-phase open-circuit condition. For clarity of analysis, the set of three-phase winding with open-circuit fault is defined as the faulty winding, whereas the other set is defined as the healthy winding. The key of the proposed hybrid fault-tolerant control strategies are to make full use of the reminding phase legs of faulty winding to produce electrical torque while employing the healthy winding to compensate the torque fluctuation.

A. Proposed Hybrid Fault-Tolerant Strategies

Fig. 7 shows the system structure with one-phase open-circuit fault in the dual three-phase PMSM drives. Take the open-circuit fault in phase D as the example, the two remaining phases E and F in the faulty winding have to carry the currents in opposite directions due to isolated neutrals of dual windings. In order to ensure the maximum torque at given current amplitudes, the current of phase *E* should maintain the same phase as the back EMF of phases *E* to *F* [18]. According to the model in (3), the back EMF e_{EF} and the current references of phases *E* and *F* (i_E and i_F) in the faulty winding can be obtained as

$$e_{EF} = \sqrt{3}\omega_r \psi_f \cos(\theta_r - \pi/6) \tag{10}$$

$$i_E = -i_F = I_m \cos(\theta_r - \pi/6) \tag{11}$$

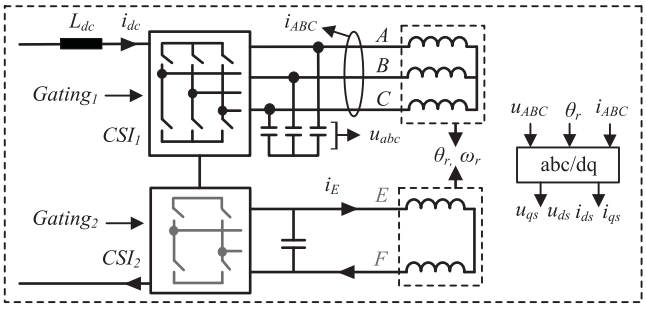

Fig. 7. System structure with phase D open-circuit fault.

where ω_r is the motor electrical angular speed, and I_m is the magnitude of i_E and i_F, which could be determined according to the following optimization of power losses. By applying coordinate rotation transformation, currents of phases *E* and *F* under *dq*-axis synchronous reference frame can be obtained as

$$i_{d2} = \sqrt{3}/3 I_m \left(\sin 2\left(\theta_r - \pi/6\right)\right) \tag{12}$$

$$i_{q2} = \sqrt{3}/3 I_m \left(1 + \cos 2\left(\theta_r - \pi/6\right)\right). \tag{13}$$

To compensate the torque fluctuation produced by faulty winding, the healthy winding should generate the opposite torque oscillation. Since the torque is produced by the *q*-axis currents of stator windings for the non-salient dual three-phase PMSM, the total *q*-axis current reference for the faulty winding and the healthy winding need to be controlled as a constant value. Therefore, the *q*-axis current reference i_{q2} of the healthy winding can be derived in (15), where $2I_{\text{qref}}$ is the total torque producing current under normal condition and I_{qref} can be obtained by $T_e/3N_p\psi_f$ from (4). Considering minimizing the copper losses, the *d*-axis current reference for the healthy winding should be forced to zero [18]. However, this method may result in distorted currents in the healthy winding, which should be avoid for the CSC module due to the *LC* resonance. Therefore, a sine-function with the same magnitude and frequency as the periodic component in i_{q1} is adopted in the *d*-axis current reference, as shown in (14) [4], in such a way that three-phase currents of the healthy winding still maintain sinusoidal in the healthy winding.

$$i_{d1} = -\sqrt{3}/3 I_m \left(\sin 2\left(\theta_r - \pi/6\right)\right) \tag{14}$$

$$i_{q1} = 2I_{\text{qref}} - \sqrt{3}/3 I_m \left(1 + \cos 2\left(\theta_r - \pi/6\right)\right). \tag{15}$$

On the other hand, in order to minimize the machine losses for a given torque, phase E current amplitude I_m should be deliberately considered. According to *dq*-axis current references of both the faulty winding and the healthy winding from (12)–(15), the total copper losses equation can be derived as (16). Considering periodic quantities in (16), the mean value of the copper losses at steady state is derived in (17), shown as follows:

$$P_{Cu} = (3/2)\left(\left(i_{d1}^2 + i_{d2}^2\right) + \left(i_{q1}^2 + i_{q2}^2\right)\right) R_s \tag{16}$$

$$P_{Cu\_m} = \left[\left(\sqrt{2}I_m - \sqrt{3/2}I_{\text{qref}}\right)^2 + (9/2)\left(I_{\text{qref}}\right)^2\right] R_s. \tag{17}$$

Therefore, the minimum copper loss $P_{Cu\_m} = 9(I_{qref})^2 R_s/2$ is achieved when $I_m = \sqrt{3}I_{\text{qref}}/2$, where the I_{qref} is determined by the output of speed regulator, as shown in Fig. 8. When the three-phase faulty winding is completely removed from the drives system, the copper loss of machine is calculated to be $P_{cu2} = 6{I_{\text{qref}}}^2 R_s$. The copper loss of the dual three-phase PMSM with the proposed method in [18] is calculated as $P_{cu3} = 30{I_{\text{qref}}}^2 R_s/7$. The relationship of three copper losses is $P_{cu3} < P_{cu\_m} < P_{cu2}$. It should be noted that the setting of *d*-axis current reference in this article may slightly increase the copper losses compared with control scheme in [18]. However, this is a tradeoff between the power efficiency and the waveform quality. With the setting of *d*-axis current in the proposed fault-tolerant method, only fundamental component is included in three-phase currents of the healthy winding. However, the setting of *d*-axis current reference of method in [18] will impose third-order harmonic to motor currents. Thus, optimized *dq*-axis current references of both faulty winding and healthy winding is obtained with the proposed method.

B. Healthy-Winding Control

The block diagram of the proposed hybrid fault-tolerant control scheme is shown in Fig. 8. Since *dq*-axis current references in healthy winding are periodic fluctuation quantities superimposed by constant component, proportional-integral-resonant controllers are used to track the *dq*-axis current references, namely i_{ds}^* and i_{qs}^* of the healthy winding. Capacitor voltage regulators are employed to generate the *dq*-axis capacitor current references, namely i_{cds}^* and i_{cqs}^*, which are added to current references of the health winding to obtain converter current references, namely i_{wds}^* and i_{wqs}^*. Finally, the CSI output current command I_{dcr} is obtained, which are expressed as

$$I_{dcr} = \sqrt{{i_{wds}^*}^2 + {i_{wqs}^*}^2} = \sqrt{\left(i_{ds}^* + i_{cds}^*\right)^2 + \left(i_{qs}^* + i_{cqs}^*\right)^2}. \tag{18}$$

Normally, a simple FOC control scheme is applied to CSIs, as discussed in Section II. The modulation index is set to 1 and the minimum DC-link current reference calculated from CSIs side can be regarded as a constant value under normal condition. However, the CSI output current command I_{dcr} will be a periodic variation due to the periodic fluctuation in *dq*-axis current references of CSI_1 under one-phase open-circuit fault condition. If the CSI modulation index is set to 1, the *dq*-axis currents of CSI_1 cannot be adequately controlled and the fault-tolerant control cannot be achieved successfully. To solve this problem, the modulation index m_1 control is proposed in the fault-tolerant control scheme, as shown in Fig. 8. As can be seen, different from the constant modulation index in FOC control scheme, the modulation index m_1 is obtained by dividing the CSI output current command i_{dcr} by actual DC-link current i_{dc}.

On the other hand, the electrical torque of dual three-phase PMSM is produced by two set of windings. When the open-circuit fault occurs in phase D, the electrical torque provided by the faulty winding is reduced, and the healthy winding has to increase the *q*-axis current reference to keep balance

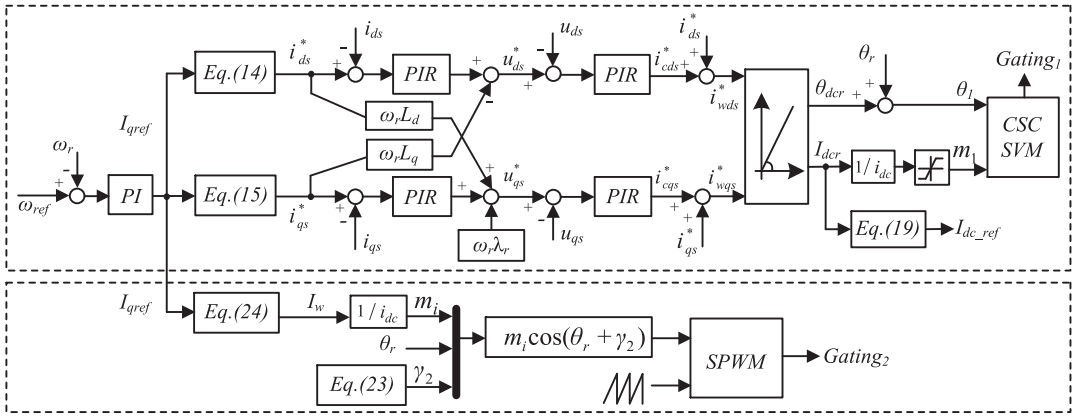

Fig. 8. Block diagram of the proposed hybrid fault-tolerant control scheme.

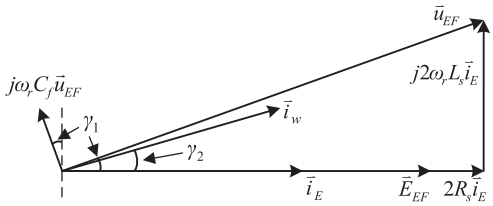

Fig. 9. Faulty winding vector diagram.

with the load torque. Consequently, the actual DC-link current $i_{\rm dc}$ should be maintained as a constant at its highest value to avoid the saturation of modulation index calculation in $\rm CSI_1$ $(0 \le m_1 \le 1)$. Thus, the DC-link current reference $I_{\rm dc\_ref}$ given to CSR side should be set bigger than the maximum CSI output current command, shown as follows:

$$I_{\rm dc\_ref} \ge (I_{dcr})_{\max}. \tag{19}$$

It should be noted that the cascaded CSIs use the conventional FOC control scheme at first and then change to the hybrid fault-tolerant control scheme. The centralized grid-voltage orientation control scheme applied in cascaded CSRs on the grid side does not change during the whole operation process.

C. Faulty-Winding Control

The faulty inverter, namely $\rm CSI_2$, can work as a single-phase CSI under open-circuit fault in phase D. Thus, a simple SPWM technique is designed to modulate the single phase CSI. However, it should be noted that filter capacitor currents of $\rm CSI_2$ need to be carefully compensated since motor currents are obtained by subtracting capacitor currents from converter currents.

Fig. 9 gives the vector diagram of related electrical variables of the faulty winding under the stationary reference frame. The current vector of phase E $\vec{i}_E$ maintains the same phase of the generated back EMF vector $\vec{e}_{EF}$, whose magnitude equals $\sqrt{3}\omega_r\psi_f$ in the steady state. The motor terminal voltage $\vec{u}_{EF}$ of faulty winding can be obtained by $(\vec{u}_{EF} = \vec{u}_E - \vec{u}_F = j2\omega_r L_s \vec{i}_E + \vec{e}_{EF} + 2R_s \vec{i}_E)$, according to (1) and (2). The filter capacitor current is derived using terminal voltage as $(\vec{i}_{\rm cap} = j\omega_r C_f \vec{u}_{EF})$. Thus, the current reference $\vec{i}_w$ of single phase CSI could be obtained by adding the capacitor current $\vec{i}_{\rm cap}$ to the phase E current $\vec{i}_E$. The formula derivation of the magnitude I_w and angle γ_2 of the current reference $\vec{i}_w$ of single phase $\rm CSI_2$ could be listed as

$$U_{EF} = \sqrt{(2\omega_r L_s I_m)^2 + \left(\sqrt{3}\omega_r\psi_f + 2R_s I_m\right)^2} \tag{20}$$

$$I_{\rm cap} = \omega_r C_f U_{EF} \tag{21}$$

$$\gamma_1 = \sin^{-1}\left(2\omega_r L_s I_m / U_{EF}\right) \tag{22}$$

$$\gamma_2 = \tan^{-1}\left(I_{\rm cap}\cos\gamma_1 / \left(I_m - I_{\rm cap}\sin\gamma_1\right)\right) \tag{23}$$

$$I_w = \sqrt{\left(I_{\rm cap}\cos\gamma_1\right)^2 + \left(I_m - I_{\rm cap}\sin\gamma_1\right)^2} \tag{24}$$

where U_{EF} is the magnitude of the motor terminal voltage $\vec{u}_{EF}$, and $I_{\rm cap}$ is the capacitor current $\vec{i}_{\rm cap}$. γ_1 stands for the power factor angle of the motor terminal voltage $\vec{u}_{EF}$ and phase current $\vec{i}_E$ in faulty winding.

V. Experiment Verification

The experiments have been carried out on a low-power prototype system to verify the effectiveness of the proposed optimized SVM and the hybrid fault-tolerant control scheme. The experimental setup is shown in Fig. 10. The load of the dual three-phase PMSM is a three-phase PMSG that coupled with a three-phase resistance. The main system parameters are listed in the Table III and the sampling frequency is set to be 5 kHz. The modulation and control algorithm are implemented on a platform, consisting of a digital signal processor (DSP) and a field-programmable gate array (FPGA). The DSP (TMSF28335) collects feedback signals and performs the control algorithm, whereas the FPGA (SPARTAN-6) is used to generate the PWM signals for four CSC modules in the drives system. In the fault-tolerant experiments, the open-phase faults are implemented by disabling one relay of a specific phase leg. The experimental results measured from the laboratory prototype are shown in Figs. 11–13. The

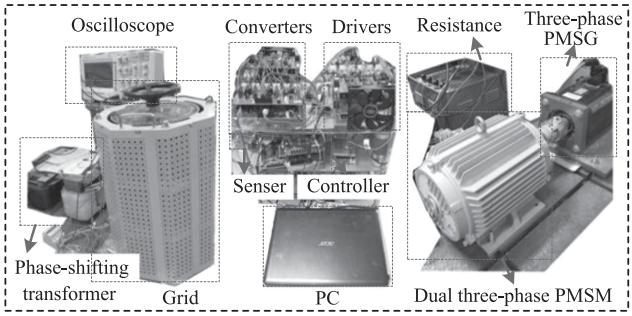

Fig. 10. Experimental low-power prototype set up.

TABLE III
SYSTEM PARAMETERS OF EXPERIMENT

	Parameter	Experiment
Rectifier Sides	Grid line voltage(rms, base)	70 V
	Grid current(rms, base)	7A
	Frequency(base)	50Hz
	Input filter inductor	0.25 pu
	Input filter capacitor	0.25 pu
DC Side	DC-link inductor	0.25 pu
Inverter Sides	Output filter capacitor	0.27 pu
	Synchronous inductance	0.25 pu
	Stator resistance	0.05 pu
	Flux	0.12 Wb
	Pole pairs	4
	Switching frequency	2.5 kHz

comparisons of different SVM strategies for DC-link current ripple mitigation are shown in Figs. 11, whereas Figs. 12 and 13 show the measured performances of the fault-tolerant control. It should be noted that the DC-link current, and phase currents are measured by current probe, whereas the torque is estimated by (4) and is shown on oscilloscope through DA module in DSP.

A. Experiments of DC-Link Current Ripple Mitigation

In the experiment, the dual three-phase PMSM rotates at a low speed of 300 r/min (namely 20 Hz). Fig. 11(a)–(c) shows DC-link current ripples and corresponding cascaded rectifiers/inverters voltages. Fig. 11(d) and (e) shows phase currents (i_A and i_D) of the dual three-phase PMSM and FFT analysis results of i_A with three different SVM strategies. It is observed that there is a 30° shifted phase angle between two phase currents (i_A and i_D) due to the asymmetrical distributions of two set of windings.

The system performances with traditional SVM pulse pattern are shown in Fig. 11(a) and (d). It can be observed that during the time interval (200 μs) of a sampling period, the DC-link voltage on the rectifier side varies from 0 to 90 V, whereas the DC-link voltage varies from 0 to 60 V on the inverter side. Consequently, the DC-link current ripple is large since there is no specific arrangement of pulse pattern for current ripple mitigation. It can be measured from Fig. 11(a) that the average DC-link current is 4.5 A, and the DC-link current ripple is up to 1.12 A during a sampling period. Define the current ripple coefficient as $D_{idc} = \Delta i_{\rm dc}/i_{\rm dc}$, and the value of D_{idc} with the traditional SVM pulse pattern is 0.25. The output current waveforms still maintain sinusoidal and the total harmonic distortion (THD) of i_A is 1.61%, as shown in Fig. 11(d).

Fig. 11(b) and (e) shows the experimental results of the method in [14]. The DC-link voltages on CSRs and CSIs sides in Fig. 11(b) are arranged from large to small in one sampling period and have the same variation range as that of Fig. 11(a). The average DC-link current is 4.5 A and the DC-link current ripple in Fig. 11(b) is slightly smaller compared with that of traditional SVM pulse pattern in Fig. 11(a). But the DC-link current ripple is not reduced effectively. The ripple value is still up to 1.08 A, and the current ripple coefficient D_{idc} with the method in [14] is 0.24. The reason is that there still exists high voltage difference between two sides of DC link under low speed operation. The THD value of i_A is 1.34% with the pulse pattern proposed in [14].

Fig. 11(c) and (f) illustrate the measured performances of the proposed optimized pulse pattern. The average DC-link current is 4.5 A, which is the same as that in previous experiments. Regardless of voltage ripples, which are caused by commutation overlap time and have little impact on the DC-link current ripple, the DC-link voltage of the cascaded CSRs varies from 40 to 90 V and the DC-link voltage of the cascaded CSIs varies from 30 to 60 V. Thus, the DC-link current benefits from smoother DC-link voltages. The current ripple is 0.6 A and the DC-link current ripple coefficient D_{idc} is only 0.13, which are much smaller than that with traditional pulse pattern and the pulse pattern between rectifier and inverter sides in [14]. The current waveforms maintain sinusoidal and the THD of i_A is 1.71%. The THD result of the proposed method is slightly higher than that of other two methods. The reason lies in that the current vector sequences are changed dynamically, and the harmonic performance is changed accordingly [26]. Since the increase of THD values using the proposed strategy is within an acceptable region, it is a good choice by reducing the DC-link current ripple effectively under different working conditions.

B. Experiments of the Fault-Tolerant Control

The experimental verification of the fault-tolerant control is carried out on the same prototype system and the system structure with phase D open-circuit fault is shown in Fig. 7. Experimental results of the drive system with occurrence of open-circuit fault and with fault-tolerant control are given in Figs. 12 and 13, where Figs. 12(a) and 13(a) are the overall process, Fig. 12(b) and (c) and Fig. 13(b) and (c) show the detailed transient response. As shown in Fig. 12(a), the cascaded CSRs maintain the implementation of the centralized grid-voltage orientation control during the whole process, while the FOC control scheme and fault-tolerant control scheme are used for CSIs within different periods.

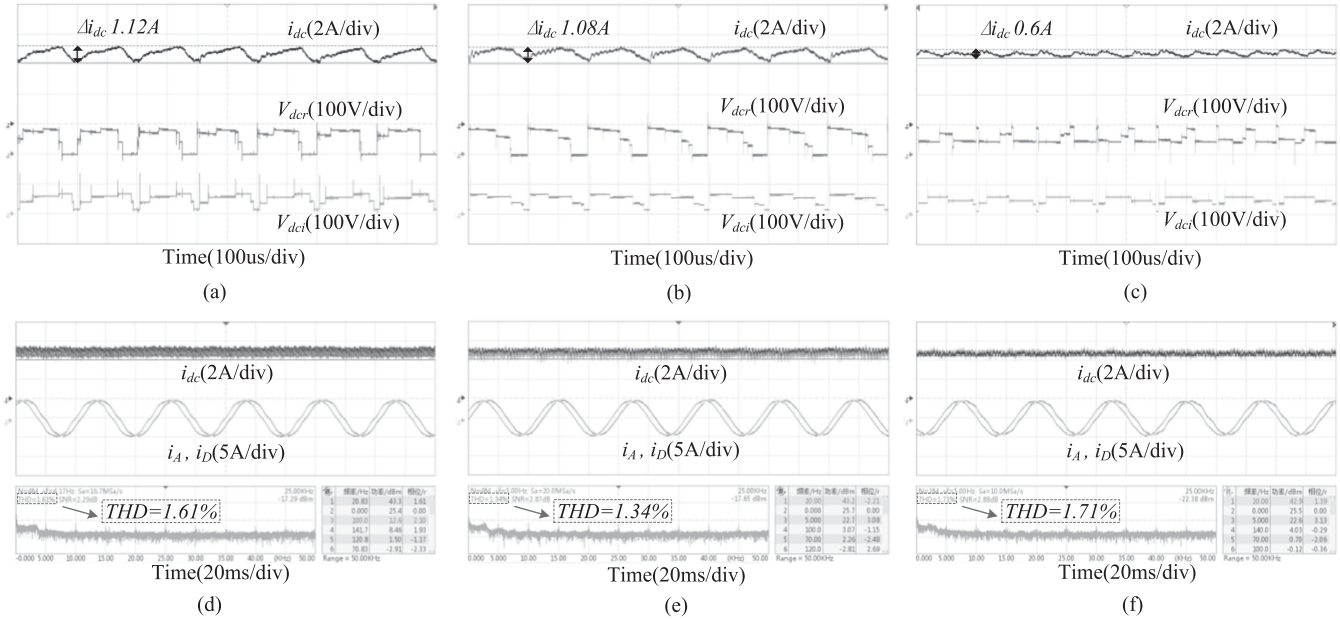

Fig. 11. Experimental results of different SVM strategy. (a) DC-link current, phase currents, and DC-link voltages of traditional pulse pattern. (b) DC-link current, phase currents, and DC-link voltages of previous pulse pattern in [14]. (c) DC-link current, phase currents, and DC-link voltages of proposed optimized pulse pattern. (d) Phase currents and phase A current FFT analysis of traditional pulse pattern. (e) Phase currents and phase A current FFT analysis of previous pulse pattern in [14]. (f) Phase currents and phase A current FFT analysis of proposed optimized pulse pattern.

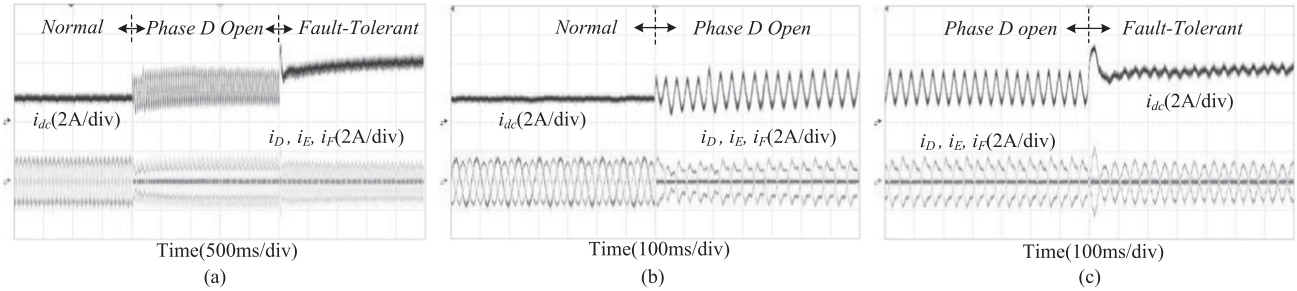

Fig. 12. Experimental results of the proposed fault-tolerant strategy (DC-link current and faulty winding currents). (a) Overall process of experimental result. (b) Transient result from normal to phase D open. (c) Transient result from phase D open to fault-tolerant.

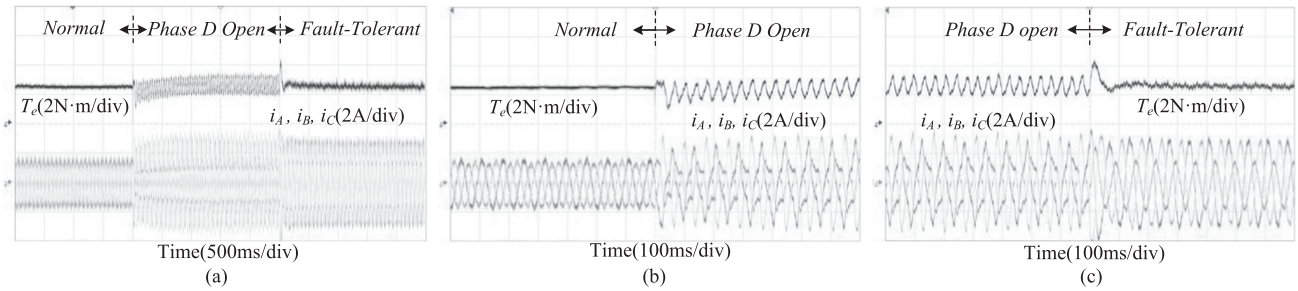

Fig. 13. Experimental results of the proposed fault-tolerant strategy (electrical torque and healthy winding currents). (a) Overall process of experimental result. (b) Transient result from normal to phase D open. (c) Transient result from phase D open to fault-tolerant.

In the experiment, the dual three-phase PMSM operates under 210 r/min (namely 14 Hz) and 2.5 N·m, as shown in Figs. 12(b) and 13(b). The steady state of system is achieved under normal condition and all phase currents are controlled symmetric and sinusoidal. The minimum DC-link current is obtained when the unity modulation index based FOC control scheme is applied to the cascaded CSIs. When the open-circuit fault occurs in phase D, two remaining phases E and F in the faulty winding have to carry the currents in opposite directions due to isolated neutrals of two set of windings, while asymmetric phase currents appear

in the healthy winding. It also can be observed that healthy winding currents increase with the increasing of the DC-link current, so as to keep balance with load torque. However, without fault-tolerant control, a distinct double-frequency oscillation appears in the DC-link current and the total electrical torque. At the same time, phase currents in two set of windings suffer from severe distortion.

On the other hand, the large fluctuation in DC-link current and electrical torque can be mitigated effectively after the proposed fault-tolerant control and the modified SPWM scheme are applied to the cascaded CSIs, as shown in Figs. 12(c) and 13(c). The DC-link current is set at its highest value to avoid the saturation of modulation index, which is the reason why the DC-link current with the proposed fault-tolerant control is larger than that under normal condition. Moreover, all the remainding current waveforms of the dual three-phase PMSM are improved and controlled sinusoidal with the proposed hybrid fault-tolerant control scheme. Therefore, the operational performance of the dual three-phase PMSM is improved.

VI. Conclusion

A coordinated SVM strategy and a hybrid fault-tolerant control scheme have been proposed for DC-link current regulation in cascaded CSCs fed dual three-phase PMSM drives system. The optimized SVM strategy has been designed and proposed to reduce the DC-link current ripple when PMSM works below the rated speed with low back EMF. On the other hand, a hybrid fault-tolerant control for the open-phase fault in dual three-phase PMSM drives system have been studied and analyzed in this article. All the research works aim to achieve small DC-link current ripple, low copper loss, and machine-friendly waveform quality for the CSCs fed dual three-phase PMSM drives system. The detailed design criteria of the optimized SVM strategy and the hybrid fault-tolerant control scheme are presented in this article. The experimental results have been given to verify that both the DC-link current and the phase currents of PMSM can be controlled well for the cascaded CSCs fed dual three-phase PMSM drives systems by applying the proposed optimized SVM scheme and the hybrid fault-tolerant control scheme.

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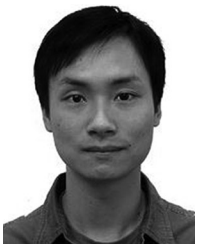

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