Modeling and Analysis of DC Terminal Impedance of Voltage-Source Converters With Different Control Modes

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***Abstract*—A dc terminal impedance model of voltage-source converter (VSC) is required to analyze the stability of multiterminal high-voltage direct current system. This article proposes a comprehensive dc terminal impedance model for conventional three-phase two-level VSC under different control modes. The control strategy includes inner decoupled current control and outer control, the latter contains dc voltage control, active/reactive power control, and droop control for grid-connected VSC and ac voltage control for VSC connected to a load. When a VSC is connected to the ac grid, the phase-locked loop (PLL) is also taken into account. The influences of PLL dynamics, control time delay and dead time on the dc-side impedance are explained. Also, how the parameters of the inner current control and outer control affect the characteristics of dc terminal impedance is analyzed in detail. Finally, experimental measurements verify the proposed impedance models and analysis.**

***Index Terms*—Frequency-domain analysis, impedance modeling, terminal characteristics, voltage-source converters (VSCs).**

I. Introduction

VOLTAGE-SOURCE converters (VSCs) have been extensively applied in high-voltage direct current (HVdc) systems in recent decades. Many HVdc transmission systems have been built or planned worldwide, including not only point-to-point HVdc links, but also multiterminal HVdc (MTdc) networks [1]–[6]. Many studies including topology, modeling, control, stability, and fault have been published in the past few years [7]–[11]. The small-signal stability analysis method has become more important because of the instability problems of MTdc systems caused by interactions among the converters.

The state-space average model and the eigenvalue analysis method are often used in multiterminal dc and ac systems [12]–[14]. A detailed state-space model of a four-terminal VSC–HVdc system is presented in [12]. However, the state-space matrix has a dimension of 56, and the model would become more elaborate with an increase in modules. Although the stability of the whole system has been well analyzed, the state-space model is not suitable for MTdc systems. In those cases, the impedance-based criterion is widely used for analyzing the stability of the dc and ac buses [15]–[20]. In a dc or ac distributed power system, each converter connected to the dc or ac bus can be regarded as a subsystem. Only if the terminal impedance of each subsystem is known, the stability of the whole system can be determined by applying the stability criterion. In that case, the stability of the VSC–MTdc network can also be based on the impedance criterion if each VSC station that is connected to the dc bus can be considered as a submodule. Therefore, the dc terminal impedance model of a single VSC station is essential.

The control strategy of VSCs usually includes inner current control and outer control in direct–quadrature (d–q) frame. The outer controllers depend on the control objectives of VSC stations [1]. When a VSC is connected to the ac grid, the tasks of VSC–HVdc systems include controlling the dc-link voltage and the active/reactive power flows. Simultaneously, a phase-locked loop (PLL) is required to make the control system synchronize with the ac grid. For dc voltage control, the converter is controlled as a voltage source on the dc side. If a perturbation current is injected into the dc current and the response voltage is obtained at the corresponding frequency, the dc terminal impedance can be calculated. For active power control, the converter is controlled as a current source on the dc side. In this case, the dc terminal admittance is obtained by injecting perturbation voltage into dc voltage source and obtaining the response current at the corresponding frequency. Another task of VSC–HVdc systems is controlling the magnitude and frequency of ac voltage when a VSC is connected to an offshore wind farm or some other loads instead of ac grid on the ac side. In that case, the VSC is controlled as a voltage source on the ac side. A dc terminal admittance model is required for that situation. Besides, the droop control is also popular in the coordinated control of MTdc system. Therefore, a dc terminal impedance model is needed to analyze the droop characteristic.

Various studies about modeling of VSC–HVdc systems have been published [21]–[25]. A dc-link impedance model of grid-connected VSC is derived using the power balance method in

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[21], which analyzes the influence of filter inductor, dc capacitor, and power flow on the stability of a two-terminal VSC–HVdc system, but the study ignores the behavior of inner current and the influence of outer controllers. The case of ac voltage control is not considered either. Hence, the impedance model is insufficient for analyzing the stability and dynamic behavior of VSC–HVdc systems. Shah and Parsa [22] described impedance models of VSCs in *dq*, sequence, and phasor domains but focused mainly on the coupling effects of dc and ac networks. It considers only inner current control and ignores the outer controllers. Wu *et al.* [23] presents a dc-side impedance model for a specific VSC and proposed a virtual resistive–inductive impedance active stabilization method to improve stability of the VSC–HVdc system, so the impedance model is not universal for VSCs with different control tasks. The stability of a two-module HVdc system is analyzed by impedance-based Nyquist criterion, which considers effect of factors on the stability [24], [25]. Although a model for different control structures is developed, the focus is on the stability. The effect of parameters of controllers still needs to be analyzed in detail. Therefore, a comprehensive dc terminal impedance model of VSCs with inner current control and four kinds of outer control modes is beneficial, and influences of key parameters on the impedance must be analyzed in detail.

This article proposes a dc terminal impedance model of VSCs with inner current control and different outer controllers. The outer controllers are dc voltage control, power control, droop control, and ac voltage control. The effects of inner current control and outer control on the impedance are considered. When the VSC is connected to the ac grid, the PLL is also taken into account. The control time delay and dead-time effect are also addressed in the model and discussed. The parameters influencing the impedance model, especially the proportional and integral gains of each controller, are analyzed in detail. The rest of this article is organized as follows. Section II describes the studied system. Section III presents small-signal models for power stage, PLL, and inner current control and then gives the derivations of dc impedance models for different outer controllers. Section IV analyzes the effect of parameters on the impedance. Section V shows the experimental verification of the proposed model and the analysis results. Finally, Section VI concludes this article.

II. System Description

Each VSC station is able to work as an independent module in the MTdc system. A three-phase, two-level VSC is discussed in this article instead of a modular multilevel converter (MMC) which is used more in engineering applications to simplify the model. Except for the internal circulating current suppression control for the MMC, the external converter control comprising inner current control and outer control is the same as the control structure for two-level converters. Therefore, the model and analysis of the two-level converter can also reflect the dc terminal characteristics of a VSC station.

The system studied in this article is shown in Fig. 1. From the power stage, the converter equipped with an *L* filter on the ac side can be connected to either ac grid or a load. A capacitor

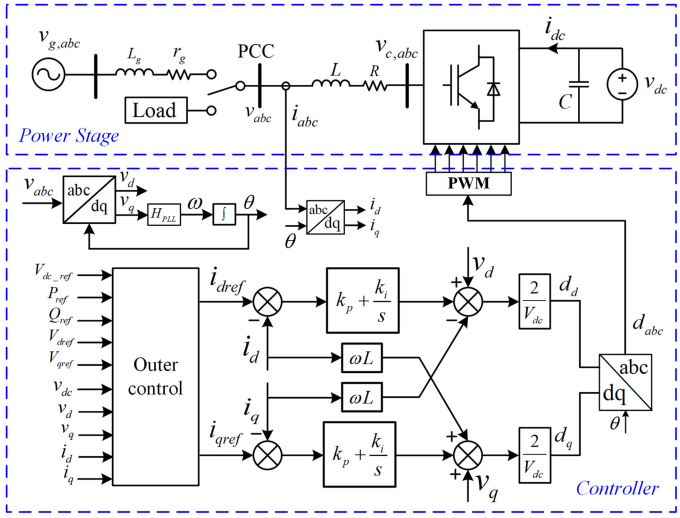

Fig. 1. VSC with current control and outer controllers.

and a dc source are connected to the VSC on the DC side. In the control part, the converter is controlled in the synchronous rotating reference frame, and the phase angle θ is from point of common coupling (PCC) voltage. When the converter is connected to the ac grid, a PLL is used to make the control system synchronize with the PCC voltage. Otherwise, when the converter is connected to a load, the PLL is not required. The control system comprises mainly inner current control and outer control.

The inner current control is a common part for VSC with different control modes. The inner control contains decoupled current control and voltage feedforward control. A proportional–integral (PI) compensator is used to regulate the inductor current on the *D*- and *Q*-axis to track the current reference. There are four kinds of outer controllers. In the dc voltage control, the dc voltage $v_{\rm dc}$ is regulated by the PI compensator to track the dc voltage reference $V_{\rm dc\_ref}$. The output is the *D*-axis current reference $i_{\rm dref}$, and the *Q*-axis current reference $i_{\rm qref}$ is 0. For power control, active power and reactive power, which are calculated by inductor current i_{dq} and PCC voltage v_{dq}, are also regulated by PI compensators to track the power references $P_{\rm ref}$ and $Q_{\rm ref}$, respectively. For droop control, the dc voltage $v_{\rm dc}$ gets through droop control to output active power references $P_{\rm ref}$. Then, the active power and reactive power are regulated by PI compensators like power control. For ac voltage control, the voltages of PCC, v_d and v_q, are controlled by PI regulators to track the voltage references $V_{\rm dref}$ and $V_{\rm qref}$.

III. Impedance Model Derivation

A. Power Stage Model

The small-signal circuit of the power stage in *d–q* frame is shown in Fig. 2, where the expressions are the same as those in (1) and (2). Each variable can be written in vector form; for example, PCC voltage $\hat{v}_{dq} = [\hat{v}_d\ \hat{v}_q]^T$, where the symbol ^ means small-signal form of the variable. The uppercase of variable denotes the steady-state operation point of itself. For

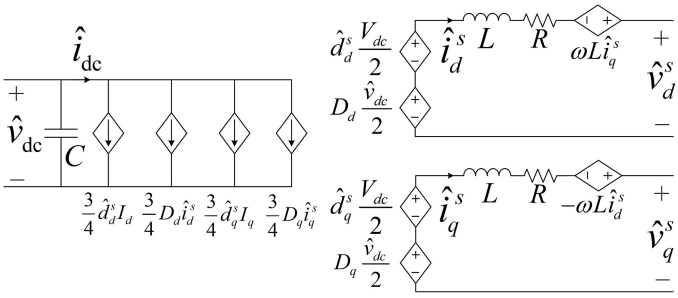

Fig. 2. Small-signal circuit of power stage in the *d–q* frame.

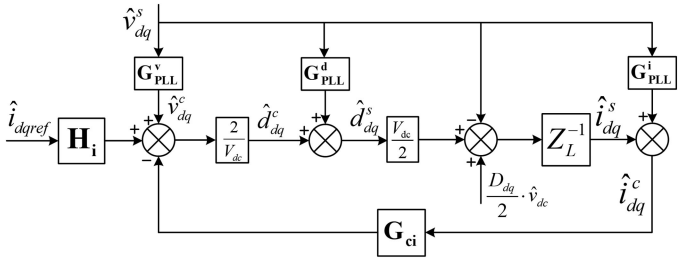

Fig. 3. Small-signal model of current control loop with PLL.

example, D_{dq} is the operating point of duty cycle. The variables are all phase variables.

$$\hat{v}_{dq}^s = -Z_L\hat{i}_{dq}^s + \hat{d}_{dq}^s\frac{V_{\rm dc}}{2} + D_{dq}\frac{\hat{v}_{\rm dc}}{2} \tag{1}$$

$$\hat{i}_{\rm dc} = \frac{3}{4}\left(I_{dq}^T\hat{d}_{dq}^s + D_{dq}^T\hat{i}_{dq}^s\right) \tag{2}$$

where

$$Z_L(s) = \begin{bmatrix} sL+R & -\omega L \\ \omega L & sL+R \end{bmatrix}.$$

B. PLL Model

When the converter is connected to the ac grid, the control system is aligned with the PCC voltage through the output angle generated by PLL. In this case, the influence of PLL must be considered. In a steady state, the angle produced by PLL is the same as the angle of the PCC voltage. However, when the PCC voltage has a perturbation, the two angles are different. Therefore, the PCC voltage, the inductor current, and the duty cycle in the control system are different from the corresponding variables in the power stage. A superscript is added to the variables to distinguish between them in the equations. The superscript s denotes the power stage and the c denotes the control system. According to existing work on the PLL model [26], the transfer function of PLL output angle to q channel voltage is

$$G_{\rm PLL} = \frac{\Delta\hat{\theta}}{\hat{v}_q^s} = \frac{H_{\rm PLL}}{s + V_d^s H_{\rm PLL}} \tag{3}$$

where the PI controller of PLL is $H_{\rm PLL} = k_{\rm pllp} + k_{\rm plli}/s$. For PCC voltage, inductor current, and duty cycle, the relations are given as follows:

$$\hat{v}_{dq}^c \approx \mathbf{G_{PLL}^v}\cdot\hat{v}_{dq}^s = \begin{bmatrix} 1 & V_q G_{\rm PLL} \\ 0 & 1 - V_d G_{\rm PLL} \end{bmatrix}\hat{v}_{dq}^s \tag{4}$$

$$\hat{i}_{dq}^c \approx \mathbf{G_{PLL}^i}\cdot\hat{v}_{dq}^s + \hat{i}_{dq}^s = \begin{bmatrix} 0 & I_q G_{\rm PLL} \\ 0 & -I_d G_{\rm PLL} \end{bmatrix}\hat{v}_{dq}^s + \hat{i}_{dq}^s \tag{5}$$

$$\hat{d}_{dq}^s \approx \mathbf{G_{PLL}^d}\cdot\hat{v}_{dq}^s + \hat{d}_{dq}^c = \begin{bmatrix} 0 & -D_q G_{\rm PLL} \\ 0 & D_d G_{\rm PLL} \end{bmatrix}\hat{v}_{dq}^s + \hat{d}_{dq}^c. \tag{6}$$

C. Inner Current Control Loop

Combining the decoupled current control and the PCC voltage feedforward control shown in Fig. 1, the expression for inner current control written in vector form is

$$\hat{d}_{dq}^c\frac{V_{\rm dc}}{2} = \mathbf{H_i}\hat{i}_{dq\rm ref} - \mathbf{G_{ci}}\hat{i}_{dq}^c + \hat{v}_{dq}^c \tag{7}$$

where

$$\mathbf{H_i} = \begin{bmatrix} k_p + \frac{k_i}{s} & 0 \\ 0 & k_p + \frac{k_i}{s} \end{bmatrix} \text{ and } \mathbf{G_{ci}} = \begin{bmatrix} k_p + \frac{k_i}{s} & \omega L \\ -\omega L & k_p + \frac{k_i}{s} \end{bmatrix}.$$

The inner current control loop is formed by power stage and current control, i.e., (1) and (7). Fig. 3 shows the small-signal model of the inner current control loop with PLL, where the inputs are $\hat{i}_{dq\rm ref}$, $\hat{v}_{dq}^s$, and $\hat{v}_{\rm dc}$, and the output is $\hat{i}_{dq}^s$ [27]. The relationship between $\hat{i}_{dq}^s$, $\hat{i}_{dq\rm ref}$, $\hat{v}_{dq}^s$, and $\hat{v}_{\rm dc}$ is

$$\begin{aligned}\hat{i}_{dq}^s = {} & (Z_L + \mathbf{G_{ci}})^{-1}\mathbf{H_i}\hat{i}_{dq\rm ref} + (Z_L + \mathbf{G_{ci}})^{-1}\frac{D_{dq}}{2}\hat{v}_{\rm dc} \\ & + (Z_L + \mathbf{G_{ci}})^{-1}\mathbf{G_{PLL\_V}}\hat{v}_{dq}^s\end{aligned} \tag{8}$$

where

$$\mathbf{G_{PLL\_V}} = \mathbf{G_{PLL}^v} - \mathbf{G_{ci}}\mathbf{G_{PLL}^i} + \frac{V_{\rm dc}}{2}\mathbf{G_{PLL}^d} - \mathbf{I}. \tag{9}$$

The d- and q-axis current are decoupled, so the transfer function of inner current loop is

$$\frac{\hat{i}_d}{\hat{i}_{d\rm ref}} = \frac{sk_p + k_i}{s^2L + (R + k_p)s + k_i}. \tag{10}$$

When k_p increases, the bandwidth becomes wider. The gain of the transfer function remains flat, and the phase shift is small within the bandwidth.

Obviously, the influence of PLL dynamic is produced by the perturbation of PCC voltage. The grid voltage is ideal grid, so $\hat{v}_{gdq}^s = 0$. For PCC voltage,

$$\hat{v}_{dq}^s = Z_g\hat{i}_{dq}^s \tag{11}$$

where grid impedance is

$$Z_g = \begin{bmatrix} sL_g + r_g & -\omega L_g \\ \omega L_g & sL_g + r_g \end{bmatrix}.$$

To derive dc-side admittance, by combining (1), (2), and (11), the following yields

$$\hat{i}_{\rm dc} = \left(\frac{3}{2V_{\rm dc}} I_{dq}^T \left(Z_g + Z_L\right) + \frac{3}{4} D_{dq}^T\right) \hat{i}_{dq}^s - \frac{3}{4V_{\rm dc}} I_{dq}^T D_{dq} \hat{v}_{\rm dc}. \tag{12}$$

Obviously, if the relation between $\hat{i}_{dq}^s$ and $\hat{v}_{\rm dc}$ is known, the transfer function from $\hat{v}_{\rm dc}$ to $\hat{i}_{\rm dc}$ would be obtained, that is, dc-side admittance.

For a VSC with only current control and no outer control, the reference value of the inductor current is constant, so

$$\hat{i}_{dq\rm ref} = 0. \tag{13}$$

Substituting (13) and (11) into (8), the relation between $\hat{i}_{dq}^s$ and $\hat{v}_{\rm dc}$ is given as

$$\hat{i}_{dq}^s = \left(\mathbf{G_{ci}} + Z_L - \mathbf{G_{PLL\_V}} Z_g\right)^{-1} \frac{D_{dq}}{2} \hat{v}_{\rm dc}. \tag{14}$$

Therefore, the dc-side admittance can be derived as

$$Y_{{\rm dc}\_i_{dq}} = \frac{\hat{i}_{\rm dc}}{\hat{v}_{\rm dc}} = \left(\frac{3}{2V_{\rm dc}} I_{dq}^T \left(Z_g + Z_L\right) + \frac{3}{4} D_{dq}^T\right) \cdot \left(Z_L + \mathbf{G_{ci}} - \mathbf{G_{PLL\_V}} Z_g\right)^{-1} \frac{D_{dq}}{2} - \frac{3}{4V_{\rm dc}} I_{dq}^T D_{dq}. \tag{15}$$

D. Outer Controllers

The power stage and the current controller are the common parts of the VSC under different control modes. However, the outer controllers are determined by the tasks of VSC stations in engineering. This article also focuses on the characteristics of outer controllers according to the application.

For dc voltage control, the converter is controlled as a voltage source on the dc side. The output of the dc voltage controller is

$$i_{d\rm ref} = \left(v_{\rm dc} - V_{\rm dc\_ref}\right) \left(k_{vp} + \frac{k_{vi}}{s}\right). \tag{16}$$

Therefore, the small-signal relation between the dc voltage and the reference inductor current is

$$\hat{i}_{dq\rm ref} = \mathbf{H_v} \hat{v}_{\rm dc} \tag{17}$$

where

$$\mathbf{H_v} = \begin{bmatrix} k_{vp} + \frac{k_{vi}}{s} \\ 0 \end{bmatrix}.$$

Substituting (11) and (17) into (8), we obtain the following

$$\hat{i}_{dq}^s = \left(Z_L + \mathbf{G_{ci}} - \mathbf{G_{PLL\_V}} Z_g\right)^{-1} \left(\mathbf{H_i H_v} + \frac{D_{dq}}{2}\right) \hat{v}_{\rm dc}. \tag{18}$$

Then the dc-side admittance is

$$Y_{{\rm dc}\_V_{\rm dc}} = \left(\frac{3}{2V_{\rm dc}} I_{dq}^T \left(Z_g + Z_L\right) + \frac{3}{4} D_{dq}^T\right) \left(Z_L + \mathbf{G_{ci}} - \mathbf{G_{PLL\_V}} Z_g\right)^{-1} \left(\mathbf{H_i H_v} + \frac{D_{dq}}{2}\right) - \frac{3}{4V_{\rm dc}} I_{dq}^T D_{dq}. \tag{19}$$

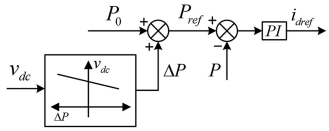

Fig. 4. Droop control.

For power control, the outputs of outer controllers are given as (20), and the small-signal relation is given as (21)

$$\begin{cases} i_{d\rm ref} = \left(P_{\rm ref} - 1.5 v_d^c i_d^c\right) \left(k_{pp} + \frac{k_{pi}}{s}\right) \\ i_{q\rm ref} = \left(Q_{\rm ref} - 1.5 v_d^c i_q^c\right) \left(k_{pp} + \frac{k_{pi}}{s}\right) \end{cases} \tag{20}$$

$$\hat{i}_{dq\rm ref} = \mathbf{H_p} \left(\mathbf{G_{pv}} \hat{v}_{dq}^c + \mathbf{G_{pi}} \hat{i}_{dq}^c\right) = \begin{bmatrix} H_p & 0 \\ 0 & H_p \end{bmatrix} \left(\begin{bmatrix} -1.5 I_d & 0 \\ -1.5 I_q & 0 \end{bmatrix} \hat{v}_{dq}^c + \begin{bmatrix} -1.5 V_d & 0 \\ 0 & -1.5 V_d \end{bmatrix} \hat{i}_{dq}^c\right) \tag{21}$$

where $H_p = k_{pp} + k_{pi}/s$. Substituting (21) into (8), and then combining them with (4), (5), and (11), the dc-side admittance of power control is given as

$$Y_{\rm dc\_PQ} = \left(\frac{3}{2V_{dc}} I_{dq}^T \left(Z_g + Z_L\right) + \frac{3}{4} D_{dq}^T\right) \left(Z_L + \mathbf{G_{ci}} - \mathbf{G_{PLL\_V}} Z_g - \mathbf{H_i H_p} \left(\mathbf{G_{pv}} \mathbf{G_{PLL}^v} Z_g + \mathbf{G_{pi}} \left(\mathbf{G_{PLL}^i} Z_g + \mathbf{I}\right)\right)\right)^{-1} \frac{D_{dq}}{2} - \frac{3}{4V_{\rm dc}} I_{dq}^T D_{dq}. \tag{22}$$

For droop control, the control diagram is shown in Fig. 4. In this article, the power flow direction from dc side to ac side is defined positive, and therefore, the reference power is

$$P_{\rm ref} = P_0 + \Delta P = P_0 + \frac{1}{k_{\rm dc}} \left(v_{\rm dc} - V_{\rm dc0}\right) \tag{23}$$

where P_0 and $V_{\rm dc0}$ are operating points of power and dc voltage, and $k_{\rm dc}$ is the slope of the droop control. A rise in the dc voltage indicates surplus power in the system, so the controller need to increase inversion to make power balance. If $v_{\rm dc}$ is higher, the ΔP will be higher. Thus, $P_{\rm ref}$ will increase, which means the output power increases.

Unlike power control, the reference power also has a perturbation

$$\hat{P}_{\rm ref} = \frac{1}{k_{\rm dc}} \hat{v}_{\rm dc}. \tag{24}$$

Thus

$$\hat{i}_{dq\rm ref} = \mathbf{H_p} \left(\mathbf{G_{pv}} \hat{v}_{dq}^c + \mathbf{G_{pi}} \hat{i}_{dq}^c + \mathbf{G_{droop}} \hat{v}_{\rm dc}\right) \tag{25}$$

where $\mathbf{G_{droop}} = \left[\begin{smallmatrix} 1/\mathbf{k_{dc}} \\ \mathbf{0} \end{smallmatrix}\right]$.

In a similar way, the dc-side admittance is

$$Y_{\rm dc\_droop} = \left(\frac{3}{2V_{\rm dc}} I_{dq}^T \left(Z_g + Z_L\right) + \frac{3}{4} D_{dq}^T\right) \times \left(Z_L + \mathbf{G_{ci}} - \mathbf{G_{PLL\_V}} Z_g\right.$$

$$- \mathbf{H_i H_p}(\mathbf{G_{pv}} \mathbf{G^v_{PLL}} Z_g + \mathbf{G_{pi}}(\mathbf{G^i_{PLL}} Z_g + \mathbf{I})))^{-1} \times \left(\mathbf{H_i H_p G_{droop}} + \frac{D_{dq}}{2} \right) - \frac{3}{4V_{\rm dc}} I_{dq}^T D_{dq}. \tag{26}$$

For ac voltage control, the converter is connected to a load on the ac side, and the *d* and *q* channel components of PCC voltage are controlled as (27). There is no PLL in the system, so the PLL model does not need to be considered. The power stage model and the current control are the same as those of other cases. The relation among $\hat{i}_{dq}$, $\hat{i}_{dq\rm ref}$, and $\hat{v}_{\rm dc}$ is given as (28)

$$\begin{cases} i_{d\rm ref} = (V_{d\rm ref} - v_d)\left(k_{vp1} + \frac{k_{vi1}}{s}\right) \\ i_{q\rm ref} = (V_{q\rm ref} - v_q)\left(k_{vp1} + \frac{k_{vi1}}{s}\right) \end{cases} \tag{27}$$

$$\hat{i}_{dq} = (Z_L + \mathbf{G_{ci}})^{-1} \left(\mathbf{H_i} \hat{i}_{dq\rm ref} + \frac{D_{dq}}{2} \hat{v}_{\rm dc} \right). \tag{28}$$

The small-signal relation between the ac voltage and the reference inductor current is

$$\hat{i}_{dq\rm ref} = \mathbf{H_{v1}} \hat{v}_{dq} \tag{29}$$

where

$$\mathbf{H_{v1}} = \begin{bmatrix} -\left(k_{vp1} + \frac{k_{vi1}}{s}\right) & 0 \\ 0 & -\left(k_{vp1} + \frac{k_{vi1}}{s}\right) \end{bmatrix}.$$

Because the converter is connected to the load, the relation between $\hat{v}_{dq}$ and $\hat{i}_{dq}$ in PCC is

$$\hat{v}_{dq} = Z_{\rm load} \hat{i}_{dq}. \tag{30}$$

Combining (29), (30), and (28), the dc-side admittance of converter with ac voltage control can also be derived as

$$Y_{\rm dc\_V_{ac}} = \left(\frac{3}{2V_{\rm dc}} I_{dq}^T (Z_{\rm load} + Z_L) + \frac{3}{4} D_{dq}^T \right) \times (Z_L + \mathbf{G_{ci}} - \mathbf{H_i H_{v1}} Z_{\rm load})^{-1} \frac{D_{dq}}{2} - \frac{3}{4V_{\rm dc}} I_{dq}^T D_{dq}. \tag{31}$$

IV. Analysis of Parameters of DC-Side Impedance

The dc-side admittances of cases for current control, dc voltage control, power control, droop control, and ac voltage control are all modeled. Next, the influences of key parameters on impedance models need to be discussed, which include PI parameters of PLL, current controllers, outer controllers, digital control time delay, and dead time delay.

A. Influence of PLL

According to Fig. 3, there are three inputs, $\hat{i}_{dq\rm ref}$, $\hat{v}^s_{dq}$, and $\hat{v}_{\rm dc}$, and one output, $\hat{i}^s_{dq}$. The influence of PLL is caused mainly by the perturbation of $\hat{v}^s_{dq}$ and then moves to the current loop through the transfer functions of $\mathbf{G^v_{PLL}}$, $\mathbf{G^i_{PLL}}$, and $\mathbf{G^d_{PLL}}$. Therefore, the effect of PLL on the impedance depends on the PI regulator. It can be found that PLL actually adds a pair of conjugate zeros and a pair of conjugate poles to the dc-side admittances by analyzing the proposed impedance models. Also,

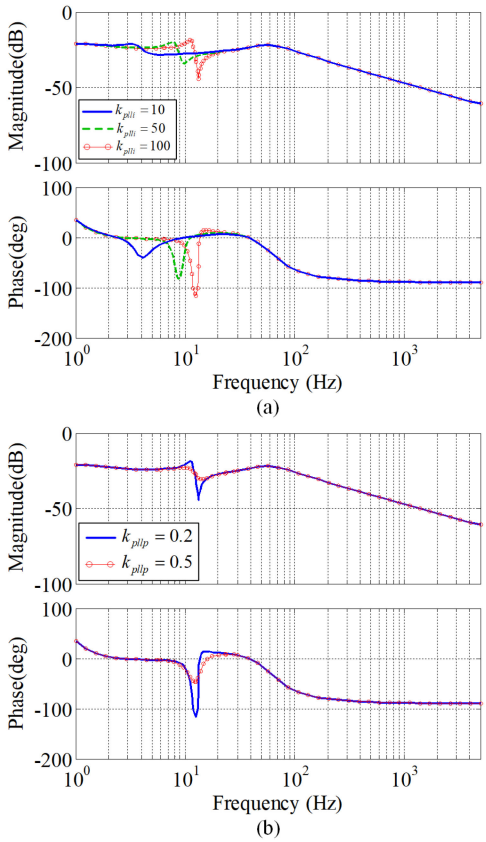

Fig. 5. DC impedance model of grid-connected inverter under current control with changing PLL parameters.

the zeros are rather close to the poles. Before studying the poles and zeros, the PLL dynamics need to be analyzed. The transfer function of PLL is

$$G_{\rm PLL} = \frac{\Delta\hat{\theta}}{\hat{v}^s_q} = \frac{s k_{{\rm pll}p} + k_{{\rm pll}i}}{s^2 + s V_d k_{{\rm pll}p} + V_d k_{{\rm pll}i}}. \tag{32}$$

It is clear that $G_{\rm PLL}$ has one zero and a pair of conjugate poles. The angular frequency of the conjugate poles is $\omega^{G_{\rm PLL}}_{p1,p2} = \sqrt{V_d k_{{\rm pll}i}}$. When $k_{{\rm pll}i}$ is larger, the frequency of the poles will increase as well, hence the bandwidth of PLL becomes larger. The log magnitude–frequency characteristic of $G_{\rm PLL}$ has a resonance peak when $k_{{\rm pll}p}$ is small, and if $k_{{\rm pll}p}$ is smaller, the peak becomes higher.

The bode plot of the dc admittance represents characteristics similar to those of $G_{\rm PLL}$. Fig. 5 depicts the bode plot of dc-side admittance of a grid-tied converter with current control by using the parameters of the VSC system shown in Table I. The adjacent zeros and poles caused by the PLL present a large jump in magnitude and phase of admittance. The location of the large jump moves to the right with increase in $k_{{\rm pll}i}$, as shown in Fig. 5(a). Furthermore, when $k_{{\rm pll}p}$ becomes smaller, the jump is larger, as shown in Fig. 5(b). The influence of PLL on the dc-side impedance of VSC with current control is obvious. However, when the converter is controlled with outer controllers, the impact of PLL is less. If a grid-tied converter is controlled under dc voltage control, the dc-side impedance may be influenced more by the outer controller or inner current controller, and thus

TABLE I
PARAMETERS OF VSC WITH CURRENT CONTROL

Parameter	Value
D channel grid voltage v_{sd}	70 V
Q channel grid voltage v_{sq}	0 V
D channel current reference i_{dref}	5 A
Q channel current reference i_{qref}	0 A
DC voltage reference V_{dcref}	200 V
Line frequency ω	$2\pi \times 50$ rad/s
Inductance of inverter inductor L	3.5 mH
Resistance of inverter resistor R	50 mΩ
Inductance of grid inductor L_g	1.75 mH
Resistance of grid resistor r_g	25 mΩ
Capacitance of DC capacitor of inverter C	1,500 μF
Equivalent series resistance of DC capacitor R_{ESR}	60 mΩ
Time delay T_d	1.5×100μs
Proportional gain of current controller k_p	1
Integrator gain of current controller k_i	10
Proportional gain of PLL k_{pllp}	0.5
Integrator gain of PLL k_{plli}	50

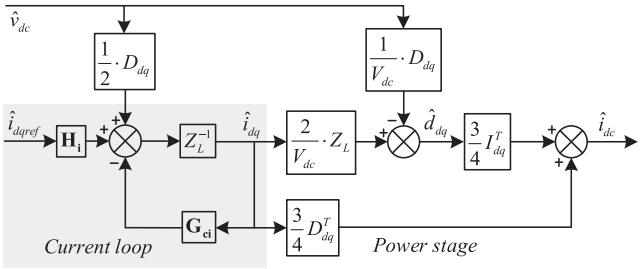

Fig. 6. Small-signal model of VSC with current control.

the effect of PLL would be weakened. PLL will have an obvious effect on the dc impedance of VSC with DC voltage control, unless $k_{\mathrm{pll}p}$ is very small. But the system will become unstable easily when $k_{\mathrm{pll}p}$ is too small. Therefore, the influence of PLL dynamics can be ignored in most cases when there are outer controllers in the system.

The influence of PLL can be ignored in VSCs with outer controllers if the proportional gain of PI regulators is appropriately selected. Thus, to make the impedance model more easily understood, remove the influence of PLL from the model. As mentioned before, when the PCC voltage has a perturbation, the output angle generated by PLL is different from the PCC voltage, and, therefore, the PLL has an effect on the system. The perturbation of the PCC voltage appears when the VSC is connected to a weak grid and grid impedance is considered. Although the grid impedance will influence the PCC voltage, the effect of grid impedance on the dc-side impedance is rather small when it transfers through controller loops. Therefore, the grid impedance is ignored in the following analysis, and assume that VSC is connected to a strong grid.

B. Time Delay and Dead-Time Effect

The small-signal model of VSC under current control without PLL is shown in Fig. 6. It contains two parts; power stage, and current loop. The transfer function from $\hat{v}_{\mathrm{dc}}$ to $\hat{i}_{\mathrm{dc}}$ is the required

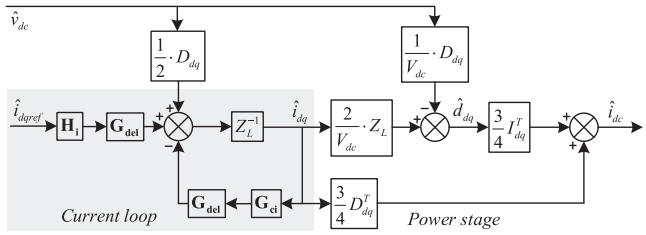

Fig. 7. Small-signal model of VSC under current control with time delay.

dc-side admittance. However, digital control time delay in the control is ignored in the derived impedance model. Thus, a simple discussion of the time delay effect is given before the analysis of controllers. Fig. 7 shows the small-signal model of VSC under current control with time delay, where $\mathbf{G_{del}}$ is the time delay owing to digital control. The expression is given as (33), where T_d is delay time of control system. The DC impedance of different control modes can also be derived in the same way

$$\mathbf{G_{del}} = \begin{bmatrix} G_{\mathrm{del}} & 0 \\ 0 & G_{\mathrm{del}} \end{bmatrix} = \begin{bmatrix} e^{-T_d s} & 0 \\ 0 & e^{-T_d s} \end{bmatrix}. \tag{33}$$

Fig. 8 presents the influence of time delay on the dc-side impedance model of VSC with dc voltage control. $Z_{\mathrm{dc\_}V_{\mathrm{dc}}}$ denotes dc impedance of inverter without dc capacitor, as shown Fig. 8(a). It can be seen that time delay has a significant effect on the phase of the bode diagram in higher frequencies. $Z_{\mathrm{inv\_}V_{\mathrm{dc}}}$ represents dc impedance model when the dc-side capacitor is considered. When the dc capacitor is 10 μF, the two curves are close to each other, as shown in Fig. 8(b). When the dc capacitor is 50 μF, the two bode diagrams are coincident, as shown in Fig. 8(c). It indicates that though time delay has an effect on the high-frequency area of the impedance, the dc-side capacitor plays a leading role in high frequencies, and the time delay effect is relatively minor. Hence, the impedance model without considering time delay is still in accordance with the experimental measurement results of which the dc capacitor is 1500 μF. Besides, the time delay effect is mainly in higher frequencies, whereas the influence of controllers is in low frequency domain. Thus, a simplified model is used to analyze the controller parameters.

A short dead time is implemented to avoid that both switches in a leg conduct simultaneously in VSCs. However, the dead time gives rise to the distorted converter current and even make the system unstable. Dead-time effect has been taken into account in the average model and the small-signal model of VSC in *d–q* frame [28], [29], in which the dead time is regarded as a duty cycle error

$$d_{abc} = d_{abc,\mathrm{ideal}} - \frac{T_{\mathrm{dead}}}{T_s}\mathrm{sign}\left(i_{abc}\right) \tag{34}$$

where d_{abc} is the phase duty cycle, $\mathrm{sign}(i_{abc})$ is the sign function to show the polarity of phase current, T_{dead} is dead-time interval, and T_s is switching time. Transforming it into the *d–q* rotating

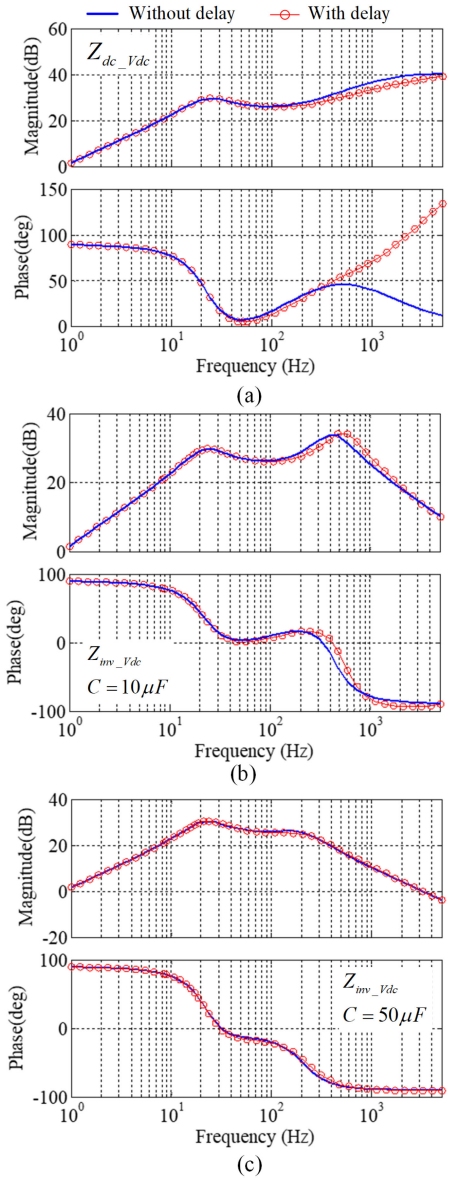

Fig. 8. DC impedance model of VSC under dc voltage control. (a) Without dc capacitor. (b) DC capacitor is 10 μF. (c) DC capacitor is 50 μF.

frame yields the following:

$$d_{dq} = d_{dq,\text{ideal}} - \frac{4T_{\text{dead}}}{\pi T_s}\begin{bmatrix}\frac{i_d}{\sqrt{i_d^2+i_q^2}}\\ \frac{i_q}{\sqrt{i_d^2+i_q^2}}\end{bmatrix}. \tag{35}$$

Substitute it into the standard average model without dead-time effect, the average model including dead-time effect is

$$v_{dq} = -Z_L i_{dq} + d_{dq}\frac{v_{\text{dc}}}{2} - \frac{2T_{\text{dead}}}{\pi T_s}\begin{bmatrix}\frac{i_d}{\sqrt{i_d^2+i_q^2}}\\ \frac{i_q}{\sqrt{i_d^2+i_q^2}}\end{bmatrix} v_{\text{dc}}. \tag{36}$$

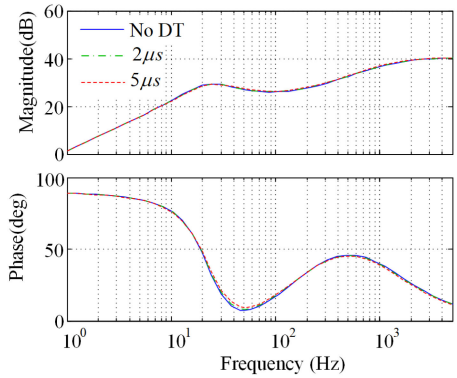

Fig. 9. DC impedance of VSC under dc voltage control without dc capacitor.

By linearizing (36), the small-signal model with dead-time effect is

$$\hat{v}_{dq} = -\left(Z_L + \frac{2T_{\text{dead}}V_{\text{dc}}}{\pi T_s}\frac{1}{\left(I_d^2+I_q^2\right)^{\frac{3}{2}}}\begin{bmatrix}I_q^2 & -I_dI_q\\ -I_dI_q & I_d^2\end{bmatrix}\right)\hat{i}_{dq} + \frac{V_{\text{dc}}}{2}\hat{d}_{dq} + \left(\frac{1}{2}D_{dq} - \frac{2T_{\text{dead}}}{\pi T_s\sqrt{I_d^2+I_q^2}}I_{dq}\right)\hat{v}_{\text{dc}}. \tag{37}$$

It is clear that the dead-time effect introduces not only resistance in d- and q-axis, but also cross-coupling reactance terms [28]. The impedance models of different control modes can also be derived in a same way. Fig. 9 shows dead-time effect on the dc impedance, which is the impedance model of VSC under dc voltage control without dc capacitor. It can be seen that there is little difference in the phase of impedance in medium frequency. Also, the difference will become slightly larger with the increase in dead time. But the difference is still very small and even not beyond the measurement error. Therefore, the dead-time effect on the dc-side impedance can be ignored in the analysis of controller parameters and model verification by experimental measurement.

C. DC Voltage Control

Back to the model shown in Fig. 6, some simplifications have been used to analyze the characteristics of controllers. The transfer function can be derived as

$$\hat{i}_{\text{dc}} = \mathbf{G}_1(\mathbf{s})\,\hat{i}_{dq\text{ref}} + \mathbf{G}_2(\mathbf{s})\,\hat{v}_{\text{dc}} \tag{38}$$

where

$$\mathbf{G}_1(\mathbf{s}) = \left(\frac{3}{2V_{\text{dc}}}I_{dq}^T Z_L + \frac{3}{4}D_{dq}^T\right)(Z_L + \mathbf{G_{ci}})^{-1}\mathbf{H_i},$$

$$\mathbf{G}_2(\mathbf{s}) = \frac{3}{8}D_{dq}^T(Z_L + \mathbf{G_{ci}})^{-1}D_{dq} - \frac{3}{4V_{\text{dc}}}I_{dq}^T\mathbf{G_{ci}}(Z_L + \mathbf{G_{ci}})^{-1}D_{dq}.$$

It can be found that dc-side admittance of VSC with current control is $\mathbf{G}_2(\mathbf{s})$, whereas the first term is removed because $\hat{i}_{dq\text{ref}} = 0$.

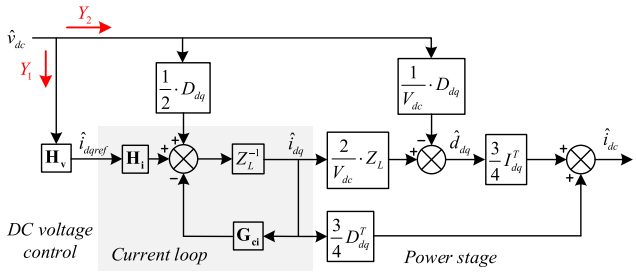

Fig. 10. Diagram of small-signal model of VSC with dc voltage control.

For VSC with dc voltage control, the small-signal model is shown in Fig. 10. Obviously, the transfer function has two paths. One passes the outer controller and the current loop, the other passes through the current loop only to go to $\hat{i}_{\rm dc}$. $Y'_{\rm dc\_}V_{\rm dc}$ is used to present the dc-side admittance of VSC under dc voltage control without PLL

$$Y'_{\rm dc\_}V_{\rm dc} = Y_1 + Y_2 \tag{39}$$

where

$$Y_1 = \mathbf{G}_1(\mathbf{s})\,\mathbf{H_v} = \frac{a\left(s+\omega_{z1}^{Y_1}\right)\left(sk_p+k_i\right)\left(sk_{vp}+k_{vi}\right)}{s\left(s^2L+\left(R+k_p\right)s+k_i\right)} \tag{40}$$

$$Y_2 = \mathbf{G}_2(\mathbf{s}) = \frac{3}{8V_{\rm dc}}\cdot\frac{b\left(s-\omega_{z1}^{Y_2}\right)}{s^2L+\left(R+k_p\right)s+k_i}. \tag{41}$$

According to (40), Y_1 has three poles and three zeros, and the angular frequency of which are easily obtained from (42)–(46). It can be found that z_1 is determined by the operating points of the VSC system and will not change with controllers. z_2 and z_3 depend on the PI parameters of inner and outer PI parameters of current controllers. Moreover, Y_2 has one zero and two poles, as can be seen from (47) and (48), and its poles are the same as those of Y_1. The zero of Y_2 is related only to the PI parameters of current controllers, and thus the admittance Y_2 is irrelevant to the outer control

$$\omega_{z1}^{Y_1} = \frac{2RI_d + 2I_q\omega L + V_{\rm dc}D_d}{2I_dL} \tag{42}$$

$$\omega_{z2}^{Y_1} = \frac{k_i}{k_p} \tag{43}$$

$$\omega_{z3}^{Y_1} = \frac{k_{vi}}{k_{vp}} \tag{44}$$

$$\omega_{p1}^{Y_1} = 0 \tag{45}$$

$$\omega_{p2,p3}^{Y_1} = -\frac{R+k_p}{2L} \pm \frac{\sqrt{\left(R+k_p\right)^2-4k_iL}}{2L} \tag{46}$$

$$\omega_{z1}^{Y_2} = \frac{2(D_dI_d+D_qI_q)k_i}{-2(D_dI_d+D_qI_q)k_p - 2\omega L(D_qI_d-D_dI_q) + V_{\rm dc}(D_d^2+D_q^2)} \tag{47}$$

$$\omega_{p1,p2}^{Y_2} = -\frac{R+k_p}{2L} \pm \frac{\sqrt{\left(R+k_p\right)^2-4k_iL}}{2L}. \tag{48}$$

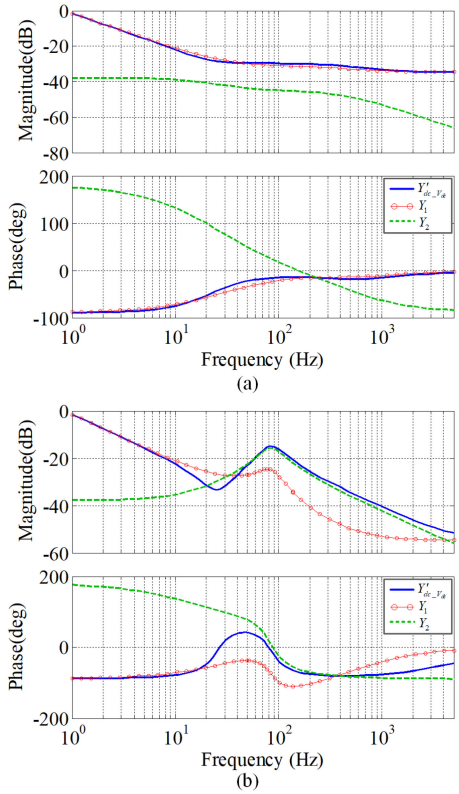

Fig. 11. Bode plot of admittances with different current loop bandwidths. (a) BW = 467 Hz. (b) BW = 138 Hz.

TABLE II
PARAMETERS OF CONTROLLERS OF VSC

Parameter	Value
Proportional gain of current controller k_p	5
Integrator gain of current controller k_i	1,000
Proportional gain of voltage controller k_{vp}	0.05
Integrator gain of voltage controller k_{vi}	10
Proportional gain of power controller k_{pp}	0.001
Integrator gain of power controller k_{pi}	0.1
Proportional gain of voltage controller k_{vp1}	0.1
Integrator gain of voltage controller k_{vi1}	10
Proportional gain of PLL k_{pllp}	0.5
Integrator gain of PLL k_{plli}	50

Fig. 11 compares the bode plot of three admittances. The parameters of power stage are shown in Table I; the parameters of controllers and PLL are shown in Table II. When the proportional gain of current controllers, k_p, is 5, which means that current loop has a wider bandwidth, the bode plot of Y_1 is almost coincident with $Y'_{\rm dc\_}V_{\rm dc}$, as shown in Fig. 11(a). In this case, Y_1 can replace $Y'_{\rm dc\_}V_{\rm dc}$ as the dc-side admittance of VSC with dc voltage control. However, as shown in Fig. 11(b), when current loop has a narrow bandwidth, $Y'_{\rm dc\_}V_{\rm dc}$ approximates Y_1 in lower frequencies and Y_2 in higher frequencies, which shows that the dc-side admittance is affected by outer controller at lower frequencies and is more affected by current controllers at higher frequencies. Therefore, usually current loop bandwidth should be higher than outer control to avoid resonant peak, as shown in Fig. 11(b).

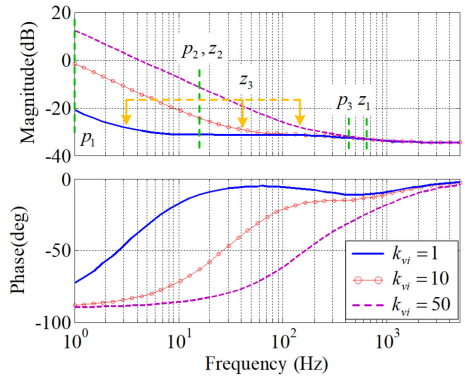

Fig. 12. Zeros and poles on the bode plot of admittance Y_1.

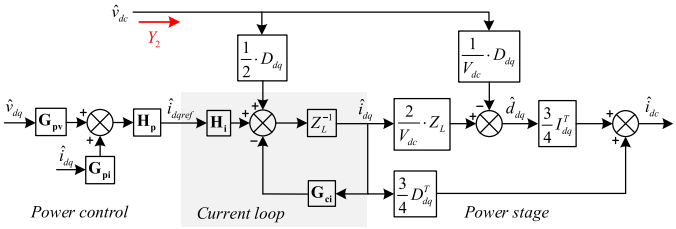

Fig. 13. Diagram of small-signal model of VSC with power control.

When current loop has a wide bandwidth, the characteristics of only Y_1 require analysis. Two zeros and poles caused by the current controllers and the operating points can be canceled out, so that zero z_3 determined by outer controllers is dominant in the admittance. Fig. 12 shows the locations of zeros and poles in the bode plot of impedances of which the parameters are the same as those in Fig. 11(a) except the change of k_{vi}. When k_{vi} increases, the frequency of z_3 also increases. The admittance has a dominant change mainly at lower frequencies. Of course, the change of k_{vp} will also affect the frequency of z_3, according to (44). Therefore, the characteristics of admittance can be designed by the PI parameters of outer controller.

D. Power Control, Droop Control, and AC Voltage Control

The same assumptions also can be used in the model of power control case. Fig. 13 shows the block diagram of small-signal model of VSC with power control. $Y'_{\mathrm{dc\_PQ}}$ is used to present the dc-side admittance of power control case without PLL, as shown in (49). For power control, the dc-side variables $\hat{v}_{\mathrm{dc}}$ or $\hat{i}_{\mathrm{dc}}$ will not be directly controlled by outer controllers. The outer controllers control only ac voltage and ac current, which will have no significant effect on the dc-side admittance. Therefore, outer controllers have little effect on the impedance at lower frequencies when the current loop has a narrow bandwidth. However, when the bandwidth of the current loop becomes wider, the gain of the admittance is like a flat line within the wide bandwidth. In this case, inner current control plays a major role in dc-side impedance, and outer control almost has no effect on the impedance. The perturbation of dc voltage gets through the current loop and power stage to gain the response of dc current.

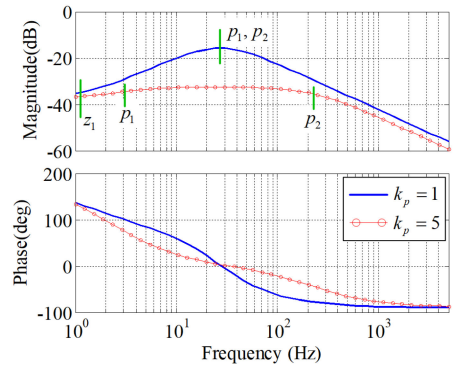

Fig. 14. Zero and poles on the bode plot of admittance Y_2.

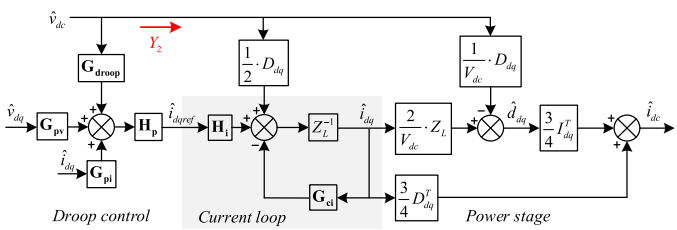

Fig. 15. Diagram of small-signal model of VSC with droop control.

Therefore, Y_2 approximates the admittance $Y'_{\mathrm{dc\_PQ}}$ when the current loop has a wide bandwidth. The zero and poles of Y_2 are shown in Fig. 14. The operating points are shown in Table I, and the parameters of controllers are shown in Table II. The bandwidth of the current loop becomes wide as the proportional gain increases. One pole becomes bigger and the other smaller; therefore, the amplitude–frequency curve of Y_2 is flatter

$$Y'_{\mathrm{dc\_PQ}} = \left(\frac{3}{2V_{\mathrm{dc}}} I_{dq}^T Z_L + \frac{3}{4} D_{dq}^T\right) \times \left(Z_L + \mathbf{G_{ci}} - \mathbf{H_i H_p G_{pi}}\right)^{-1} \frac{D_{dq}}{2} - \frac{3}{4V_{\mathrm{dc}}} I_{dq}^T D_{dq}. \quad (49)$$

For droop control, Fig. 15 shows the simplified model of VSC with droop control, and $Y'_{\mathrm{dc\_droop}}$ is used to present the dc-side admittance of droop control case without PLL in (50). According to the generalized voltage droop strategy [30], when the slope of droop control is very small, the droop control is close to constant dc voltage control, and so the characteristics of the impedance is more similar to that of dc voltage control case. On the contrary, when the slope is bigger, the droop control will approach constant power control. Thus, the characteristics of the impedance is more similar to that of power control case. Undoubtedly, the slope k_{dc} is the main parameter to affect the characteristics of admittance. $Y'_{\mathrm{dc\_droop}}$ has three zeros including a pair of conjugate zeros at low frequency area, which are determined by the slope of droop control k_{dc}. When the slope k_{dc} decreases, the frequency of zeros increases. Practically, the slope is very small, so the impedance changes a lot in low

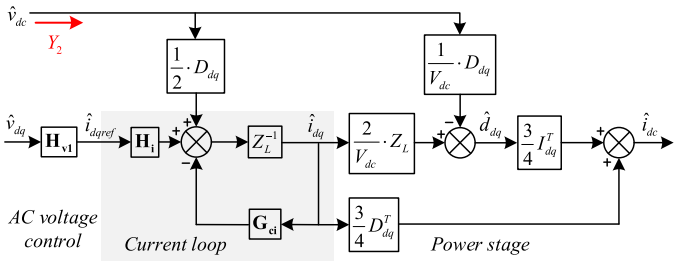

Fig. 16. Diagram of small-signal model of VSC with ac voltage control.

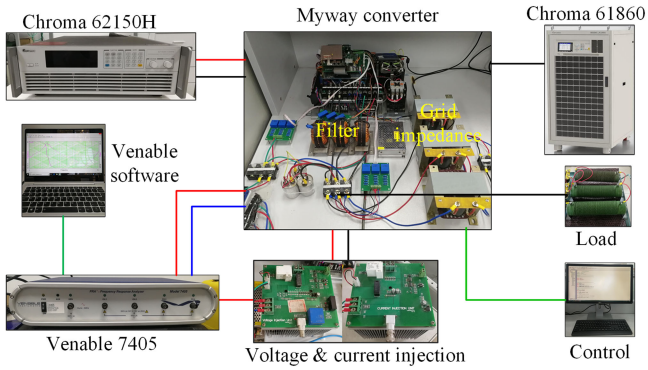

Fig. 17. Experimental system.

frequencies

$$Y'_{\mathrm{dc\_droop}} = \left(\frac{3}{2V_{\mathrm{dc}}} I_{dq}^{T} Z_L + \frac{3}{4} D_{dq}^{T}\right) \left(\begin{array}{c} Z_L + \mathbf{G_{ci}} \\ -\mathbf{H_i H_p G_{pi}} \end{array}\right)^{-1} \cdot \left(\mathbf{H_i H_p G_{droop}} + \frac{D_{dq}}{2}\right) - \frac{3}{4V_{\mathrm{dc}}} I_{dq}^{T} D_{dq}. \tag{50}$$

For ac voltage control, the small-signal model of power stage and current loop are the same as that of the former control modes, and the diagram of small-signal model is shown in Fig. 16. The outer controller controls only the ac variables $\hat{v}_d$ and $\hat{v}_q$ and then generates output to the current loop. Similar to power control, the parameters of ac voltage controllers do not control the dc variables directly. Hence, the parameters of inner control have a main influence on the dc-side admittance of VSC with ac voltage control, and Y_2 is also a good approximation when the current control loop has a wide bandwidth. The characteristic of Y_2 has been analyzed in the power control case, and the same conclusions for an ac voltage case can be arrived at. Therefore, ac voltage control has little effect on the admittance at lower frequencies when the current loop has a narrow bandwidth. Also, inner current control plays a leading role on the dc-side admittance, and outer control has almost no effect when the current loop has a wide bandwidth.

V. Experimental Verification

To verify the dc terminal impedance models and the analysis mentioned above, a voltage-source inverter system has been built, as shown in Fig. 17. A Chroma grid simulator is used to simulate the ac grid. The load is connected to the PCC of the inverter in the case of ac voltage control. A Chroma 62150H is connected to the dc side of the inverter as a dc source. A Venable 7405 frequency response analyzer generates a perturbation signal at the sweep frequency, which is injected into a current injection unit or a voltage injection unit. Then, the injection unit produces a perturbation current or perturbation voltage that could finally be injected into the dc side of the inverter. Next, the dc voltage and dc current are sensed and sent to Venable instrument to calculate the impedance or admittance.

The basic configuration for measuring the dc-side impedance of VSC is shown in Fig. 18. When outer control is dc voltage control and droop control, the dc source works in current source mode. The perturbation current is injected into the dc current

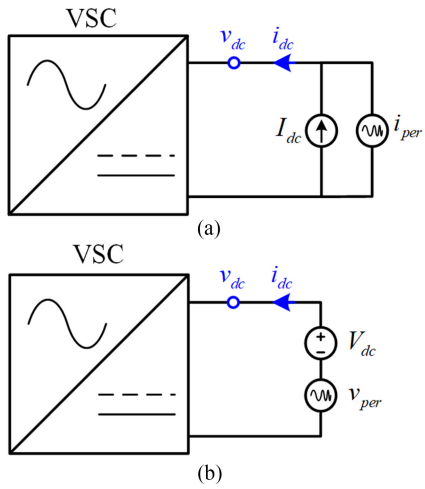

Fig. 18. Measuring system configuration. (a) DC-side impedance, (b) DC-side admittance.

source, as shown in Fig. 18(a). Then, the dc voltage and current are sensed to calculate the dc terminal impedance. For other control modes, the dc source operates in voltage-source mode. The perturbation voltage is injected into the dc voltage source, as shown in Fig. 18(b). Then, the sensed dc voltage and current are sent to the Venable instrument to obtain the dc terminal admittance.

A dc-side capacitor is included in the inverter during the experiments. Therefore, the dc capacitor must be included in the impedance model. For dc voltage control and droop control, the whole dc-side impedance model is

$$Z_{\mathrm{inv}}(s) = \frac{1}{Y_{\mathrm{dc}} + sC}. \tag{51}$$

For other control modes, the dc-side admittances are measured, and the complete model is

$$Y_{\mathrm{inv}}(s) = Y_{\mathrm{dc}} + sC. \tag{52}$$

The range of sweep signal for impedance measurement in the experiment is from 1 to 5 kHz. The parameters of power stage and controllers for the experiment are listed in Table I. Fig. 19 shows the dc-side admittance of grid-connected VSC under current control with different parameters of PLL. It can

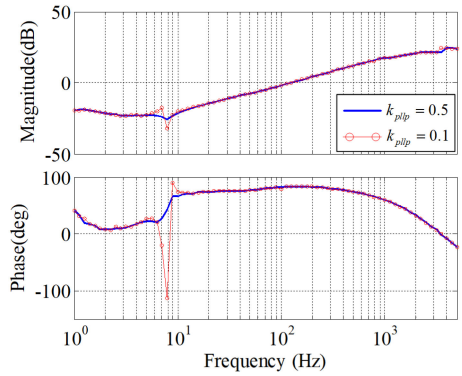

Fig. 19. DC-side admittance of grid-connected VSC with current control and PLL by experiment.

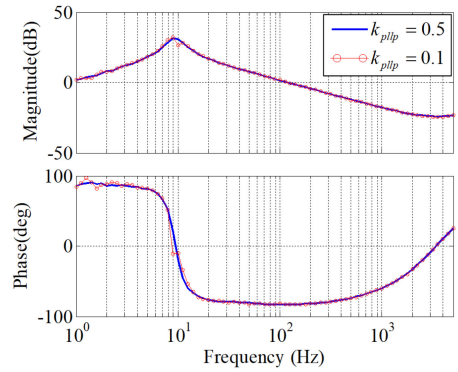

Fig. 20. DC-side impedance of grid-connected VSC with dc voltage control and PLL by experiment.

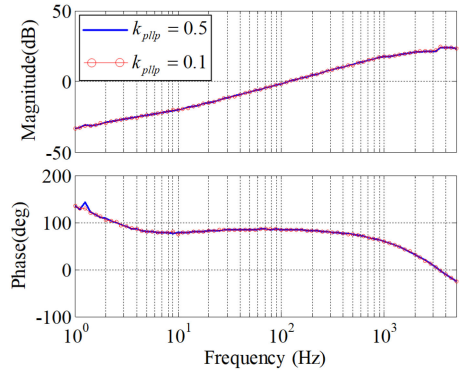

Fig. 21. DC-side impedance of grid-connected VSC with power control and PLL by experiment.

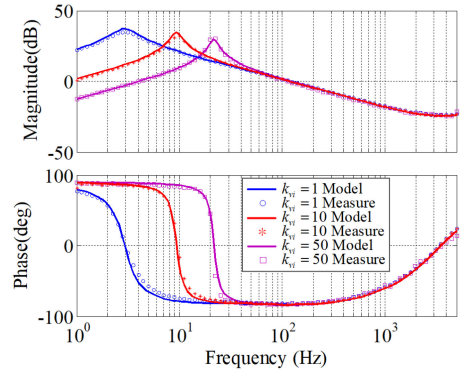

Fig. 22. DC-side impedance of grid-connected VSC with dc voltage control and PLL.

be seen that when the proportional gain of PLL becomes smaller, there is a large jump in the magnitude and phase of admittance, with other conditions being equal.

The dc-side impedance of grid-connected VSC under dc voltage control with different parameters of PLL is shown in Fig. 20. The parameters of the main circuit are listed in Table I, and the parameters of controllers for the experiment are listed in Table II. When the proportional gain of PLL becomes smaller, there is a slight jump in frequency of approximately 10 Hz. However, it can be seen that the jump caused by PLL is much smaller in Fig. 20 compared with that of Fig. 19. It is concluded that PLL also influences the dc-side impedance of VSC with outer controllers, but the effect is not as obvious as the effect on the admittance of VSC under current control with other conditions being the same. Also, if the proportional gain of PLL is greater than 0.5, the influence of PLL does not have to be considered as the red curve in Fig. 20.

Fig. 21 shows the dc-side admittance of grid-connected VSC under power control with different parameters of PLL. The parameters of the main circuit are listed in Table I, and the parameters of controllers for the experiment are listed in Table II. When the proportional gains of PLL are different, the red and blue curves shown in Fig. 21 are almost the same, and there is no jump in the bode plot of the admittances caused by PLL. It is concluded that PLL has very little influence on the dc-side admittance of VSC with power control and can be ignored.

The dc-side impedance of VSC under DC voltage control with different parameters of the dc voltage controller is shown in Fig. 22. The parameters of the main circuit are listed in Table I, and the parameters of PLL and controllers are shown in Table II with the integral gain changes, which are 1, 10, and 50. First, it can be seen that the experimental measurement results are in accordance with the impedance model. Second, the impedance at lower frequencies changes substantially as the integral gain of dc voltage controller increases. The PI parameters of dc voltage controllers have a large effect on the dc-side impedance.

The dc-side admittances of power control case measured by experiment are shown in Figs. 23–25. The parameters of the main circuit are listed in Table I, and the parameters of PLL and controllers are shown in Table II. Fig. 23 indicates that the model of the dc-side admittance is in accordance with the measurement results. Fig. 24 shows admittances measured by experiment with different integral gains of power control when the current loop has a wide bandwidth. It can be seen that the change in the integral gain of power control has almost no effect on the magnitude of the admittance and affects its phase even less. The admittance shows only the characteristics of a resistor and a capacitor. Fig. 25 shows admittances measured by experiment with different proportional gains of inner current

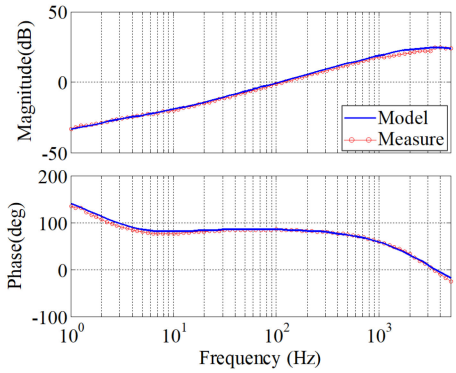

Fig. 23. DC-side admittance of VSC with power control and PLL.

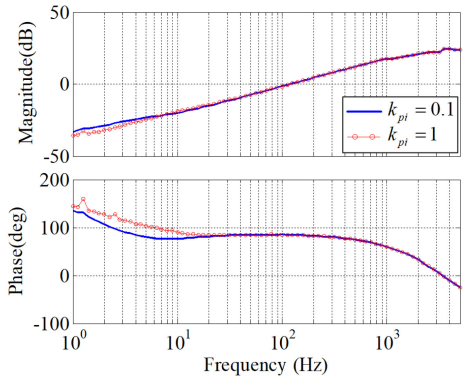

Fig. 24. DC-side admittance of VSC of power control with different parameters of outer controller by experiment.

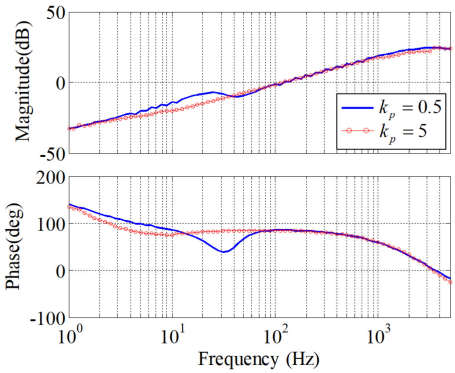

Fig. 25. DC-side admittance of VSC of power control with different parameters of inner controller by experiment.

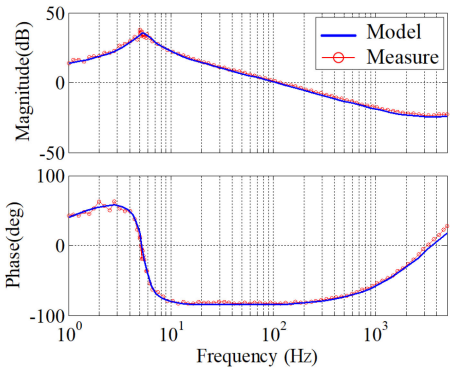

Fig. 26. DC-side impedance of VSC with droop control and PLL.

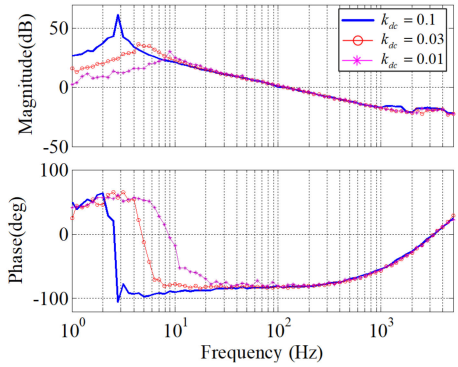

Fig. 27. DC-side impedance of VSC with droop control measured by experiment.

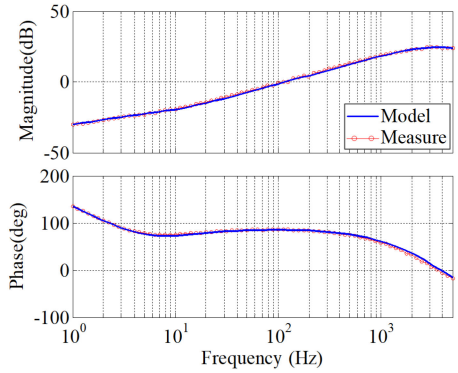

Fig. 28. DC-side admittance of VSC with ac voltage control and PLL.

control. When the proportional gain of inner current control is greater, the bandwidth of current loop is wider. It can be seen that the bandwidth of current loop has a major influence on admittance in the middle frequency area. The current loop bandwidth is better to be wider to keep smooth.

The dc-side impedances of VSC with droop control by experimental measurements are shown in Figs. 26 and 27. The parameters are listed in Tables I and II. Fig. 25 indicates that the model of the dc-side impedance is in accordance with the experimental measurement when the slope $k_{\rm dc}$ is 0.025. Fig. 27 shows the measured impedance results by experiment with different slopes of droop control. It can be seen that the slope of droop control plays a major role in the low frequencies of the impedance.

The dc-side admittances of VSC with ac voltage control measured by experiment are shown in Figs. 28–30. The parameters of the main circuit are listed in Table I, and the parameters of PLL and controllers are shown in Table II. Fig. 28 compares the admittance model and the experiment result. It can be seen that the model of dc-side admittance is in accordance with the experimental measurement, so that the model effectively

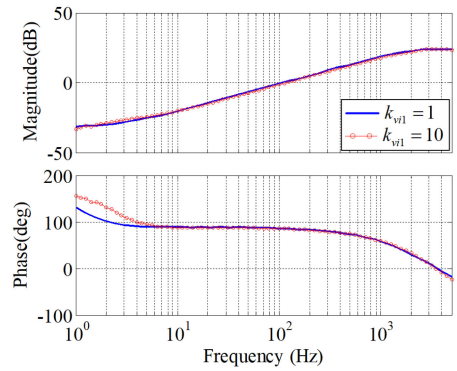

Fig. 29. DC-side admittance of VSC of ac voltage control with different parameters of outer controller by experiment.

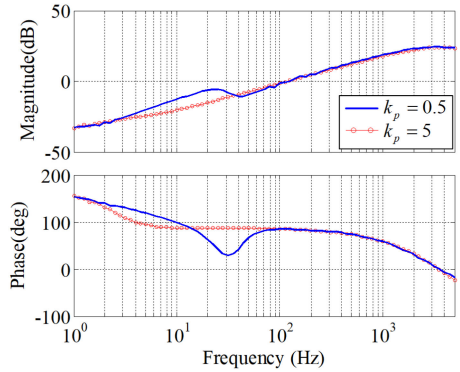

Fig. 30. DC-side admittance of VSC of ac voltage control with different parameters of inner controller by experiment.

represents the terminal characteristics of the dc side of VSC with ac voltage control. Fig. 29 shows the gains of ac voltage control when the current loop has a wide bandwidth. The magnitude curves are the same, but the phase curves have a slight difference in low frequencies. It can be seen that the change in the integral gain of ac voltage control has no effect on the magnitude and has little effect on the phase of the admittance. Fig. 30 shows the admittances measured by experiments with different proportional gains of inner current control. When the bandwidth of current controller is narrow, the change produced by the current controller is obvious in the middle frequency area. Consequently, the bandwidth of current loop should be designed wider to obtain better characteristics of the admittance.

VI. Conclusion

A comprehensive dc terminal impedance of VSCs under different control modes, which are inductor current control, dc voltage control, power control, droop control, and ac voltage control, has been modeled. When the converter is connected to ac grid, the PLL is also taken into account. The models are verified by experimental measurement results.

The parameters of PLL controller influence the dc-side impedance, especially when the proportional gain is very small. However, the effect of PLL is obvious in the impedance of VSC with only current control, but the influence can usually be ignored when VSC is under dc voltage control or power control.

The time delay due to digital control and pulsewidth modulation has a significant effect on the phase of dc impedance in the high-frequencies area. But the time delay effect is relatively minor compared with that of the dc-side capacitor. Dead time has a very small effect on the dc impedance in the medium-frequency range and even can be ignored.

Outer controllers affect impedance at lower frequencies, whereas inner current controllers influence impedance at relatively higher frequencies. For VSC with dc voltage control, parameters of the outer controller undoubtedly have the most influence on the dc terminal impedance. Designing the parameters of dc voltage control has been analyzed in detail. For VSC with droop control, the slope has a main effect on the dc terminal impedance in low-frequency area. For VSC with power control and ac voltage control, parameters of outer controllers have little effect on the admittances. Also, the influence of current controllers is important for the characteristics of dc-side admittances.

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