Model Predictive Current Control of a Seven-Level Inverter With Reduced Computational Burden

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***Abstract*—Multilevel topologies gained considerable attention in medium-voltage high-power applications due to their advantages over classic two-level inverters, such as lower loss, higher power quality, and eliminating interface transformers. Moreover, vast research has been done in order to improve the control of the power converters to achieve more efficient and simple controllers. Model predictive control (MPC) is one of the control techniques that has been widely used in power electronics recently due to its advantages, such as fast dynamic response, no need for PI regulators and pulsewidth modulation blocks, and capability of nonlinearity inclusion. On the other hand, the high number of calculations especially for higher level topologies is the disadvantage of this approach. This article presents a new finite control set MPC (FCS-MPC) approach for a seven-level topology. This approach reduces the number of calculations significantly compared to conventional FCS-MPC. Applying the computational efficient FCS-MPC to control the output current and flying capacitors voltages' of the seven-level topology reduces the number of calculations from 12^3 to 36, whereas the execution time is reduced six times. Moreover, simulation and experimental results have been shown to demonstrate the performance and feasibility of the developed control method applied to a seven-level topology.**

***Index Terms*—Current control, high power converters, model predictive control, multilevel inverters, voltage balancing.**

I. Introduction

DURING recent years, multilevel converters have been one of the most researched topics in power electronics, due to recent requirements such as higher power quality, lower loss, lower electromagnetic interferences, eliminating interface transformers, lower manufacturing cost, and reaching higher power levels, in industrial applications [1], [2]. Moreover, power semiconductors with limited voltage ratings, 6.5-kV voltage rating to the present date, limited the use of classic two-level converters in industrial applications that require megawatt motor drives.

Classic and advanced multilevel topologies are presented to fulfill the aforementioned requirements; however, there are various challenges that still need to be addressed. Flying capacitor (FC), neutral point clamped (NPC), cascaded H-bridges (CHB), which are called as classic multilevel topologies [3], have disadvantages in their higher level topologies. For instance, a significant increase in the number of FCs, and diodes in FC, NPC topology, and bulky phase-shifting transformers in CHB topologies. In addition, control complexity of voltage balancing of FCs and neutral points in FC, and NPC converters increases with respect to an increase in the number of levels, which limits their application in higher voltage and power applications [4].

Advanced topologies that are mostly a combination of classic topologies presented to overcome the challenges of classic topologies. For instance, five-level active NPC [5] is an advanced topology, which is a combination of NPC topology with diodes replaced by clamping switches and 3L-FC topology that does not have the unequal loss distribution among the semiconductors in NPC topology. Nowadays, research is toward reducing the number of active switches and components of multilevel topologies in order to reduce the manufacturing cost and developing control techniques for the proper operation of these converters with less complexity.

A seven-level topology, as shown in Fig. 1, which is an upgrade of the six-level topology in [6], is presented in this article. The presented seven-level topology is a combination of FC and neutral point piloted (NPP) topology [7]. This topology has fewer numbers of active switches and passive components compared to other existing classic and advanced topologies presented in [8]–[14], as shown in Table I, which demonstrates the bill of material cost advantage of the presented seven-level topology. The comparison, as shown in Table I, has been done with respect to the number of components with the voltage rating of $V_{dc}/6$.

Model predictive control (MPC) has gained considerable attention in power electronics during recent years for advantages, such as fast dynamic response, handling nonlinearity of the systems, and no need for proportional-integral (PI) controllers and pulsewidth modulation (PWM) blocks to produce gating for active power semiconductors [15]. MPC methods can be categorized into continuous control set MPC (CCS-MPC) or finite control set MPC finite control set model predictive control (FCS-MPC). In CCS-MPC, a continuous control signal is computed by

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TABLE I
NUMBER OF COMPONENTS IN SEVEN-LEVEL TOPOLOGIES

	7L-CHB [10]	H-7L [11]	7L-ANNPC [12]	7L-MMC [13]	7L-HC [14]	7L-I
IGBT (V_{dc}/6)	36	42	54	72	60	42
FCs (V_{dc}/6)	-	6	15	36	3	18
Neutral points	-	2	-	-	2	-
Isolated dc sources	9	1	1	1	1	1

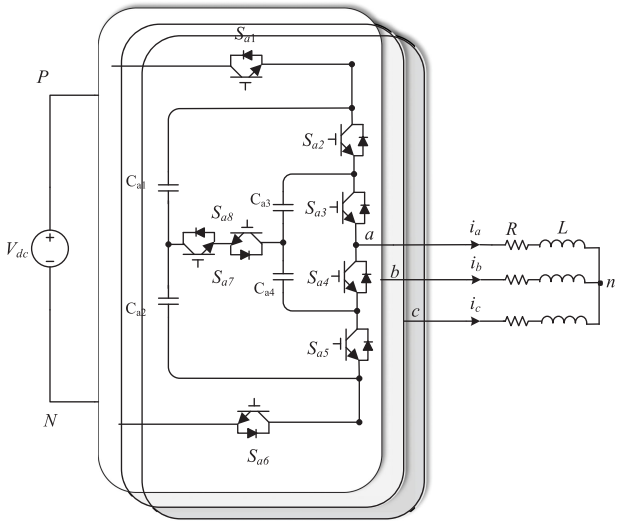


Fig. 1. Circuit diagram of the seven-level topology.

the controller and passed to a modulator to generate the output voltage; however, in FCS-MPC, the converter circuit discrete model is obtained and does not require any modulators [16].

For proper operation, and equal voltage stress on active switches of the presented seven-level topology, the outer and inner FCs of each phase must be balanced at $V_{\rm dc}/3$ and $V_{\rm dc}/6$, respectively. A control technique based on conventional FCS-MPC [15]–[18] can be developed in order to control the FCs voltages. The disadvantage of this approach is the high number of calculation of the developed control method based on FCS-MPC, due to the correlation between the control objectives of each phase with each other. The higher number of calculation results in a slower controller, and longer sampling times, which can affect the performance and output quality of the converter.

In this article, a computational efficient FCS-MPC is developed, which significantly reduces the number of calculations required to control the output current and the FCs voltages of the seven-level topology. The developed control technique reduces the number of computations by an approximation in the power converter's circuit, where the control objectives of each phase can be controlled independently.

The number of calculations to control the output current and FCs voltages of the seven-level topology for the conventional FCS-MPC is 12^3; however, based on the computational efficient FCS-MPC, it is 36, which shows the effectiveness of the new MPC in limiting the number of calculation.

The remainder of this article is organized as follows. In Section II, different strategies of computational efficient model predictive approaches for the high-power multilevel converters are reviewed and compared to the new FCS-MPC developed in this article. The operation of the seven-level topology is explained in Section IV. In Section III, the control method based on the computational efficient FCS-MPC is developed to control the output current and FCs voltages of the seven-level topology. In order to determine the feasibility and effectiveness of the controller for the seven-level topology, simulation and experimental results are shown in Section IV, and Section V, and finally, Section VI concludes this article.

II. ADVANTAGES OF THE NEW FCS-MPC OVER OTHER COMPUTATIONAL EFFICIENT MPC APPROACHES

Recently, MPC has gained significant attention as a tool to control high-power multilevel converters with the development of fast digital control platforms. The fast dynamic response [16] due to no need for PI regulators and PWM blocks, robustness to the variation of system parameters, system's nonlinearity inclusion, and multiple control objectives simultaneous satisfaction are the advantages of control techniques developed based on MPC. Due to the aforementioned advantages, the MPC strategies have been applied to various multilevel topologies [19].

The conventional FCS-MPC [20] requires the discrete mathematical model of the power converter in terms of switching states and parameters of the multilevel power converter to predict the values of the control objectives in each sampling time for the next sampling interval. Then, a cost function is used to determine the best switching state of each phase that minimizes the error between the predicted values of the control objectives and their predefined references. The disadvantage of this approach is the computational burden of the controller based on FCS-MPC due to a large number of switching states in multilevel converters, especially in the higher level topologies, since in each sampling time, the control objectives must be predicted for all of the possible switching states of the three phase. This is due to the correlation between the control objectives of each phase with each other.

In [21], a new MPC algorithm to reduce the number of calculations for multilevel CHB topologies is presented. In this approach, the triangular region that the reference voltage vector resides in is determined, and then only the three nearest voltage vectors are used, which reduces the number of calculations. However, determining the triangle region in higher level topology significantly increases the complexity of the control method.

In [22], the computational burden of MPC is reduced by a priority sorting approach for modular multilevel converters. The control objectives in this approach are the grid-side current and

circulating current, which are satisfied by separate cost functions, and the capacitor voltage balancing objective is satisfied using a priority sorting approach. The computational burden for each control objective is reduced in this approach; however, the complexity of the overall control method is increased. Also, the computational load of the MPC strategy is reduced in [23] for modular multilevel converters where submodule capacitor voltage control is decoupled from the cost function and balanced using a sorting algorithm.

In [24], a computationally efficient FCS-MPC method is proposed for nested neutral point converters. In this approach, undesired switching states are ignored by using Lyapunov principle into the sector distribution method based space vector modulation scheme. In addition, the weighting factor is eliminated by using an optimization strategy based on fuzzy decision-making. The improvement in computational efficiency is achieved in this approach by using complex mathematics, which in a sense removes the simplicity of the FCS-MPC.

The MPC approaches discussed above increase the complexity of the overall control method by introducing complex algorithms into the controller in order to reduce the number of calculations. However, the computational efficient FCS-MPC presented in this article reduces the number of calculations by an approximation in the power converter's circuit equations. In a multilevel converter, with output current control, and FCs voltage balancing as the control objectives, there is a correlation between the control objectives of the three phases due to the common mode voltage (CMV) of the power converter circuit. Applying Kirchhoff's voltage law to the power converter circuit shown in Fig. 1, the phase voltage of the converter with respect to the negative of the dc-link source can be obtained as

$$V_{xN} = Ri_x + L\frac{di_x}{dt} + V_{nN} \tag{1}$$

where $x = a, b, c,$ and i_x is the output current passing through the star-connected load shown as *R* and *L*. The V_{nN} term is the CMV, which can be calculated as

$$V_{nN} = \frac{1}{3}(V_{aN} + V_{bN} + V_{cN}). \tag{2}$$

As can be seen from (1) and (2), the three-phase output currents are related to each other through the CMV, which will force the controller to take into account the three phase simultaneously that increases the number of calculations. Assuming symmetrical sinusoidal output currents, the phase voltages can be rewritten in terms of their spectral components, as the following equations state:

$$V_{xN} = \frac{V_{\rm dc}}{2} + A\sin(\omega t + \varphi + \Phi_x) + {\rm HF}_x \tag{3}$$

where $V_{\rm dc}/2$ is the dc component of the phase voltage, *A* is the fundamental component of the phase voltage (V_{xN}), φ is the phase displacement of the output current and voltage fundamentals, $\Phi_x = \{0, \frac{2\pi}{3}, \frac{-2\pi}{3}\}$ for $x = a, b, c$, respectively, and ${\rm HF}_x$ is the high-frequency component that depends on selected switching pattern. Replacing (3) in (2) will result in

$$V_{nN} = \frac{V_{\rm dc}}{2} + {\rm HF}_a + {\rm HF}_b + {\rm HF}_c. \tag{4}$$

The approximation takes place in (5), where due to the low-pass filtering of most loads, the high-frequency component can be neglected; therefore

$$V_{nN} \approx \frac{V_{\rm dc}}{2}. \tag{5}$$

And by replacing (5) in (1), we obtain

$$V_{xN} \approx Ri_x + L\frac{di_x}{dt} + \frac{V_{\rm dc}}{2}. \tag{6}$$

As demonstrated by (6), the phase voltage and, respectively, the output current of each phase can be controlled independently by the approximation in (5), which will result in the possibility of controlling the output currents separately that reduces the number of calculations of FCS-MPC significantly. In the following section, the controller based on this approach is developed to control the output current and the FCs voltages of the seven-level topology and it is explained how the above approach reduces the number of calculations.

III. Developed FCS-MPC With Reduced Number of Calculation for the Seven-Level Topology

In order to develop the controller for the seven-level topology, the operation of the converter must be understood, since the controller requires the information regarding output voltage and capacitors current based on the switching states of the seven-level topology.

A. Seven-Level Topology Operation

The seven-level topology, as shown in Fig. 1, is a combination of FC and NPP topology, and benefits from the features of these topologies. The seven-level voltage is generated at the output by 12 switching patterns, as shown in Table II. For generating seven-level voltage at the output, and equal voltage stress on the active switches in the top and bottom leg of each phase, the outer and inner FCs must be balanced at their desired values, which are $V_{\rm dc}/3$ and $V_{\rm dc}/6$, respectively. The bidirectional switch creates a controllable path to charge and discharge the capacitors, and in addition, the redundant switching states for levels 2 and 4, which produce the same voltage level with a different effect on the FCs, are used to balance the capacitors voltages. As listed in Table II, each switching pattern based on the direction of the output current has a charging or discharging effect on the FCs. The controller employs these charging and discharging effects to balance the FCs voltages at their desired values.

B. FCS-MPC With Reduced Number of Calculation for the Seven-Level Topology

To apply the FCS-MPC to the seven-level topology, the discrete-time mathematical model of the power converter in terms of the switching states, the load, and system parameters is required. The control objectives are the three-phase output currents and the FCs voltages. In each sampling time, the values of the control objectives and their references should be predicted for the next sampling interval. Then, a cost function is used to

TABLE II
SWITCHING STATES OF THE SEVEN-LEVEL TOPOLOGY

Sx_1	Sx_2	Sx_3	Sx_4	Sx_5	Sx_6	Sx_7	Sx_8	V_{cx1} $i_x>0$	V_{cx2} $i_x<0$	V_{cx3} $i_x>0$	V_{cx4} $i_x<0$	V_{xN}	Output Level
1	1	1	0	0	0	0	0	-	-	-	-	V_{dc}	[6]
1	0	1	0	0	0	1	1	C	-	D	-	$\frac{5V_{dc}}{6}$	[5]
1	1	0	1	0	0	0	0	-	-	C	C	$\frac{2V_{dc}}{3}$	[4c]
1	0	1	0	1	0	0	0	C	C	D	D		[4b]
0	1	1	0	0	1	0	0	D	D	-	-		[4a]
1	0	0	1	0	0	1	1	C	-	-	C	$\frac{V_{dc}}{2}$	[3]
0	0	1	0	0	1	1	1	-	D	D	-		
1	0	0	1	1	0	0	0	C	C	-	-	$\frac{V_{dc}}{3}$	[2c]
0	1	0	1	0	1	0	0	D	D	C	C		[2b]
0	0	1	0	1	1	0	0	-	-	D	D		[2a]
0	0	0	1	0	1	1	1	-	D	-	C	$\frac{V_{dc}}{6}$	[1]
0	0	0	1	1	1	0	0	-	-	-	-	0	[0]

C: Charge FC; D: Discharge FC; - : No impact

select the best switching state that minimizes the error between the predicted and reference values of the control objectives.

In order to obtain the discrete-time model of the output current, the phase voltage (6) and the first-order derivative of the output current are used

$$V_{xN}(k+1) \simeq Ri_x(k+1) + L\frac{di_x}{dt} + \frac{V_{\rm dc}}{2} \tag{7}$$

$$\frac{di_x}{dt} = \frac{i_x(k+1) - i_x(k)}{T_s} \tag{8}$$

where T_s is the sampling time, and $(k+1)$ and (k) refer to the $(k+1)$th, and kth time intervals. From (7) and (8) predicted output current is obtained as

$$i_x(k+1) \simeq \frac{T_s}{L+RT_s}V_{xN}(k+1) + \frac{L}{L+RT_s}i_x(k) - \frac{V_{\rm dc}}{2}\frac{T_s}{L+RT_s}. \tag{9}$$

As can be seen in (9), to calculate the output current for the $(k+1)$th interval, the output current in the kth interval that is obtained by the current sensors and predicted phase voltage for $(k+1)$th is required. To include the switching states in the prediction of the output current, an equation is extracted from Table II to calculate the phase voltage for the next sampling interval as follows:

$$\begin{aligned} V_{xN}(k+1) = {} & V_{\rm dc}(S_{x1}) + V_{Cx4}(k)(S_{x5} - S_{x4}) \\ & + V_{Cx1}(k)(S_{x2} - S_{x3} - S_{x4} + S_{x6}) \\ & + V_{Cx2}(k)(S_{x6} - S_{x5}) + V_{Cx3}(k)(S_{x3} - S_{x2}) \end{aligned} \tag{10}$$

where $V_{Cx}(k)$ is the FCs voltages at the kth instant, which is obtained by the voltage sensors. From (9) and (10) in each sampling time, the output currents for the next sampling interval are calculated.

To predict the FCs voltages for the next sampling interval in terms of switching states, the general equation for the capacitors and the first-order derivative of the FCs voltages are used as follows:

$$\begin{aligned} i_{Cxi}(k) &= C_{xi}\frac{dV_{Cxi}}{dt} \\ \frac{dV_{Cxi}}{dt} &= \frac{V_{Cxi}(k+1) - V_{Cxi}(k)}{T_s} \\ V_{Cxi}(k+1) &= V_{Cxi}(k) + \frac{T_s}{C_{x1}}i_{Cxi}(k) \\ i &= 1, 2, 3, 4. \end{aligned} \tag{11}$$

The FCs voltages and currents are required to calculate the predicted voltage value of the FCs for the next sampling interval. The FCs voltages are obtained from the voltage sensors, and the capacitors currents are calculated in terms of switching states as follows:

$$\begin{aligned} i_{Cx1}(k) &= (S_{x1} - S_{x2})i_x(k) \\ i_{Cx2}(k) &= (S_{x1} - (S_{x2}||S_{x7}))i_x(k) \\ i_{Cx3}(k) &= (S_{x2} - S_{x3})i_x(k) \\ i_{Cx4}(k) &= ((S_{x2}||S_{x7}) - S_{x3})i_x(k) \end{aligned} \tag{12}$$

where $\|$ is the OR binary operation. From (9) to (12), the control objectives are predicted for the next sampling interval. In addition, the references for the control objectives must be predicted. The references for the FCs voltages (V^*_{cxi}) as discussed before are constant and equal to $V_{\rm dc}/3$ and $V_{\rm dc}/6$ for outer and inner capacitors, respectively. Moreover, the output current references, which are three-phase sinusoidal current, are predicted by Lagrange extrapolation [25] as follows:

$$\begin{aligned} i^*_x(k+1) = {} & 4i^*_x(k) - 6i^*_x(k-1) \\ & + 4i^*_x(k-2) - i^*_x(k-3). \end{aligned} \tag{13}$$

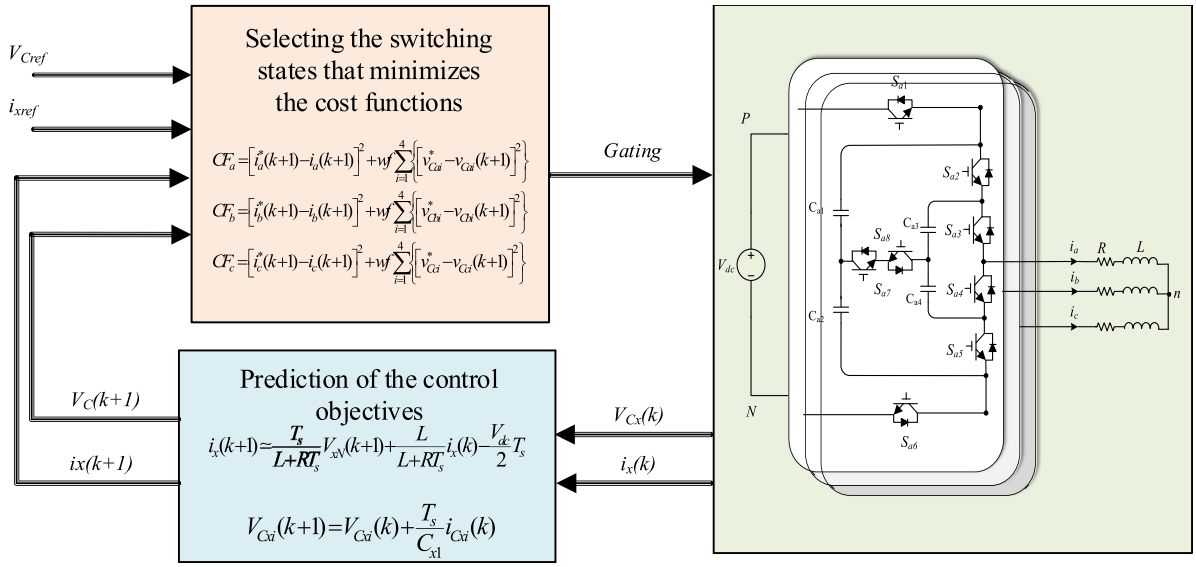


Fig. 2. Block diagram of the developed control method.

In order to minimize the error between the predicted values and their references, a cost function is used to select the best switching state that satisfies the cost function goal. To demonstrate how the number of calculation is reduced by approximation in (5), first, the cost function [16] for the conventional FCS-MPC is shown as follows:

$$\mathrm{CF} = \sum_{x=a,b,c} [i_x^*(k+1) - i_x(k+1)]^2 + \mathrm{wf} \sum_{x=a,b,c} \left\{ \sum_{i=1}^{4} [v_{Cxi}^* - v_{Cxi}(k+1)] \right\}^2. \quad (14)$$

The wf is the weighting factor of the cost function, which determines the importance and priority of the control objectives. Due to the equal importance of the FCs voltages and output current control, the weighting factor is calculated as the ratio of the rated output current, and the voltage reference of the FCs voltages to compensate the difference in nature of the control objectives [26]. For the seven-level topology, since there are two reference voltages for FCs voltages, the wf can be calculated as the ratio of the rated output current and the average of FCs voltage references, which is $V_{\mathrm{dc}}/4$.

As it is shown in (14), in conventional FCS-MPC, due to the correlation between the phase voltage of different phases, the output currents and the FCs voltages are related to each other, respectively. Since the control objectives are related, the switching state of each phase affects the control objectives of other phases. Therefore, the cost function in (14) is implemented by three loops that in each loop cost function is calculated for 12 switching states of the seven-level topology for each phase, to find the best switching pattern among $12^3 = 1728$ switching combination.

By approximation in (5), as discussed before the control objectives of the three-phase system can be controlled separately

TABLE III
PARAMETERS OF THE SIMULATION STUDY SYSTEM

Converter parameters	Values
Converter rating (MVA)	2
Capacitor Value (μF)	1000
Input dc voltage (kV)	10.2
Output frequency (Hz)	60
Output inductance (mH)	22.4
Output load (Ω)	28.4

for each phase by the following cost functions:

$$\begin{aligned}
\mathrm{CF}_a &= [i_a^*(k+1) - i_a(k+1)]^2 + \mathrm{wf} \sum_{i=1}^{4} \left\{ [v_{Cai}^* - v_{Cai}(k+1)]^2 \right\} \\
\mathrm{CF}_b &= [i_b^*(k+1) - i_b(k+1)]^2 + \mathrm{wf} \sum_{i=1}^{4} \left\{ [v_{Cbi}^* - v_{Cbi}(k+1)]^2 \right\} \\
\mathrm{CF}_c &= [i_c^*(k+1) - i_c(k+1)]^2 + \mathrm{wf} \sum_{i=1}^{4} \left\{ [v_{Cci}^* - v_{Cci}(k+1)]^2 \right\}. \quad (15)
\end{aligned}$$

As it is shown in (15), the best switching pattern for each phase is selected separately, which results in the 12×3 number of calculations, which is significantly reduced compared to conventional FCS-MPC. The block diagram of the developed control method is shown in Fig. 2

Fig. 3. Steady-state simulation: $i_{\text{ref}} = 0.9$ p.u. and PF $= 0.9$, $f = 60$ Hz. (a) Output currents. (b) FC voltages.

Fig. 4. Steady-state simulation: $i_{\text{ref}} = 0.9$ p.u. and PF $= 0.5$, $f = 60$ Hz. (a) Output currents. (b) FC voltages.

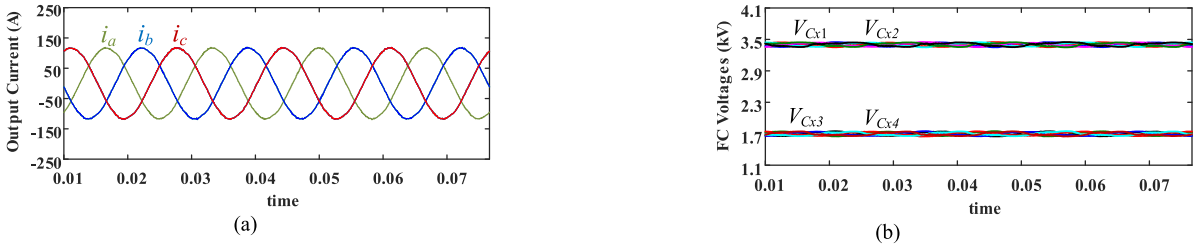


Fig. 5. Steady-state simulation: $i_{\text{ref}} = 0.5$ p.u. and PF $= 0.9$, $f = 60$ Hz. (a) Output currents. (b) FC voltages.

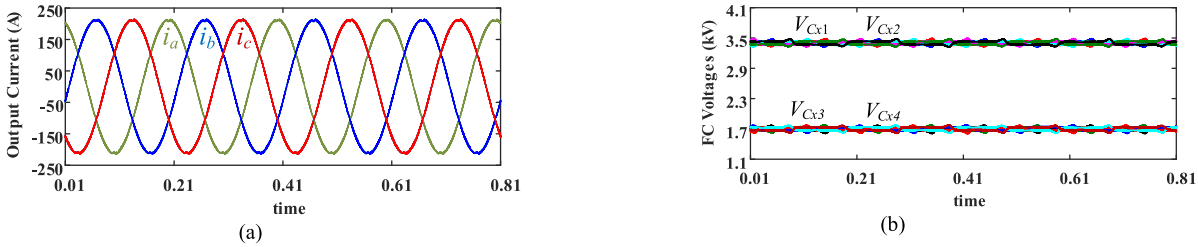


Fig. 6. Steady-state simulation: $i_{\text{ref}} = 0.9$ p.u. and PF $= 0.9$, $f = 5$ Hz. (a) Output currents. (b) FC voltages.

IV. Simulation Results

The simulation results are shown for steady-state and transient conditions, and the output current and FCs voltages are shown in the results. Moreover, a comparison has been done regarding the output power quality, and prediction error between the conventional FCS-MPC and the controller developed for reducing the number of calculations. The system parameters in the simulation results are shown in Table III. The sampling time in simulation results is 50 μs. The developed controller in the results is referred to as Red. MPC.

A. Steady-State Studies With Reduced Number of Calculations

In this section, the steady-state performance of the developed control method is evaluated in different load conditions, power factors (PFs), and output frequencies. In Fig. 3, the output current is set to 0.9 p.u. ($i_{\text{ref}} = 211$ A), whereas the PF and output frequency are set to 0.9 and 60 Hz, respectively. In Fig. 4, the PF is set to 0.5, with the same condition as the results shown in Fig. 3. In Fig. 5, the output current is set to 0.5 p.u. ($i_{\text{ref}} = 117$ A), and in Fig. 6, the output frequency is set to 5 Hz to determine the controller performance in low-frequency operation, whereas the

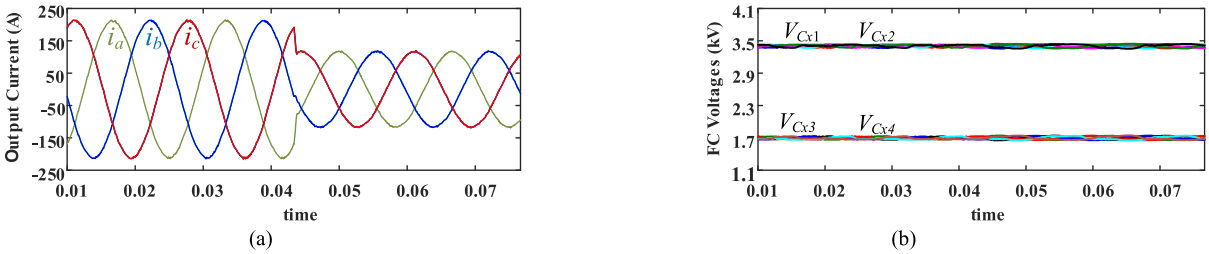


Fig. 7. Transient simulation: i_{ref} changed from 0.9 to 0.5 p.u. (a) Output currents. (b) FC voltages.

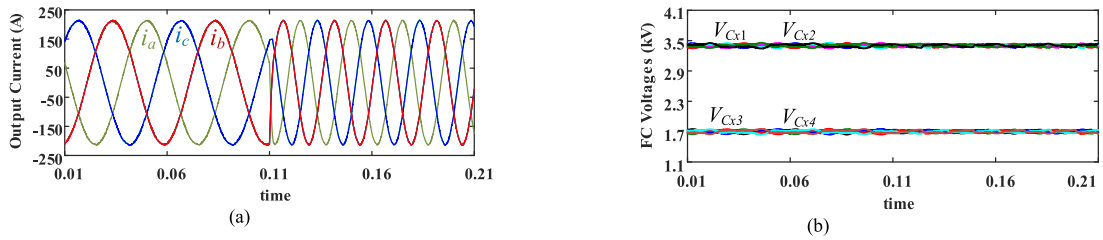


Fig. 8. Transient simulation: i_{ref} changed from $f = 20$ to 40 Hz. (a) Output currents. (b) FC voltages.

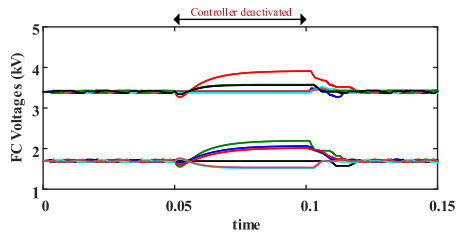


Fig. 9. Transient simulation, controller evaluation.

PF is set to 0.9. As it can be seen in the results, the FCs voltages and output currents tracked their references perfectly.

B. Transients of the Strategy With Reduced Number of Calculations

In this section, transient conditions are simulated by a step-change in current reference and output frequency. The output current is changed from 0.9 to 0.5 p.u. in Fig. 7, and the frequency is changed from 20 to 40 Hz in Fig. 8, whereas the PF is set to 0.9. As it is shown, the FCs voltages are well balanced during the transients, and the output current magnitude and frequency followed the references immediately, which is due to the fast dynamic response feature of the FCS-MPC. In addition, in Fig. 9, the controller is deactivated for 0.05 s, and reactivated to evaluate the controller after a fault that causes an interruption in the controller operation, as it is shown after the controller is reactivated the FCs voltages are converged to their desired value after a few cycles.

C. FCS-MPC Conventional and Reduced Number of Calculation Comparison

In this section, a comparison has been done regarding reference tracking, output power quality, and estimation accuracy between FCS-MPC conventional, and reduced number of calculation approach applied to the seven-level topology. In Fig. 10, the output current of phase *A*, with its reference and phase and line voltages of the seven-level topology, is shown for conventional and computational efficient FCS-MPC. As it is shown in both control methods, the output reference is tracked perfectly, and approximation in the power circuit did not affect the reference tracking capability of the developed control method. In addition, as can be seen in Fig. 10, the phase voltage in the reduced number of calculations has fewer jumps to different levels since the control of each phase has been done separately, which reduces the *dv*/*dt* over the active switches. Moreover, total harmonic distortion (THD) analysis has been done for output voltage and current of the seven-level topology, to compare conventional and computational efficient FCS-MPC. The acceptable THD is dependent on the application. For instance, the acceptable THD for a grid-connected application at the point of common coupling (PCC) is set by IEEE_std519-2014 [27], which is related to the bus voltage level of PCC for voltage THD, and to maximum short-circuit current and maximum load demand current at PCC for current THD. Typically, the current THD should be less than 5%. For motor drive applications, high voltage distortion can cause core losses, which can affect the efficiency of the system and thus requires additional filter before applying the voltage to the motor.

The results are shown in Table IV. As can be seen, the output THD of the conventional approach is better than computational efficient, which is due to the approximation in the mathematical model of the converter to reduce the number of calculation. However, the output THD of the computational efficient approach is still acceptable, and the number of calculations has reduced significantly, as discussed in the experimental result section, which can be assumed as an acceptable tradeoff.

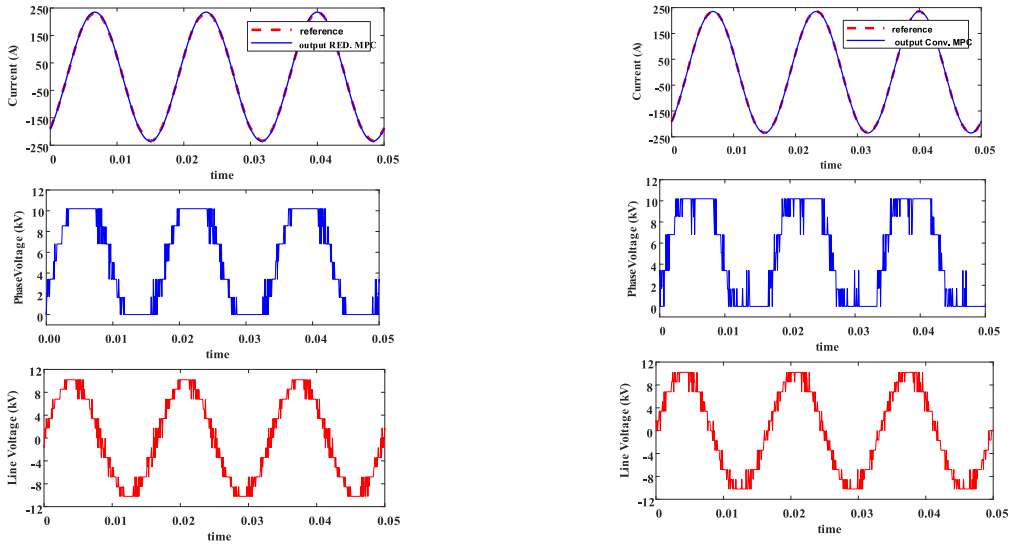


Fig. 10. Reference tracking, phase voltage, and line voltage. (a) Red. MPC. (b) Conv. MPC.

TABLE IV
THD ANALYSIS COMPARISON

Output Current	Line Current THD Red. MPC	Line Current THD Conv. MPC	Line Voltage THD Red. MPC	Line Voltage THD Conv. MPC
1pu	1.05 %	0.66 %	14.84 %	13.94 %
0.8pu	1.20 %	0.82 %	29 %	19.51 %
0.6pu	1.67 %	1.04 %	43.6 %	25 %
0.4pu	1.56 %	1.25 %	39.43 %	29 %
0.2pu	2.97 %	1.98 %	80 %	44 %

The results in Table IV show that the current and voltage THDs decrease when the operating point in Red. MPC changes from 0.6 to 0.4 p.u.; however, this is not the case for conventional MPC. The reason is that this range of the operating point is where there are more flexible and redundant switching states to control the FC; therefore, controlling the capacitors is easier, which results in more focus of the controller on the output current that leads to lower THD for Red. MPC. However, in the conventional method, since there is a single cost function to control all of the FCs voltages, and output currents of the converter, the focus of the controller would be more on the FCs, which lead to increase on the THD of the output current in the aforementioned range.

To investigate the prediction error, the root mean square error (RMSE) of the reference and output current in different load conditions is calculated for both methods, which is shown in Table V. As can be seen, the RMSE for Red. MPC is almost equal to Conv. MPC in rated load, and is slightly higher in lower load conditions. Therefore, the effect of approximation is not significant in the prediction error.

TABLE V
PREDICTION ERROR COMPARISON

Output Current	RMSE Red. MPC	RMSE Conv. MPC
1pu	2.426	2.425
0.8pu	1.657	1.074
0.6pu	1.656	1.021
0.4pu	1.061	0.829
0.2pu	1.008	0.699

TABLE VI
FREQUENCY SPECTRUM OF CMV

Frequency spectrum	CMV
DC component	1.00
3rd order	0.12
9th order	0.02
15th order	0.03
21st order	0.01
27th order	0.02

D. Frequency Spectrum of the CMV

Theoretically, the CMV must contain the switching frequency components and third-order harmonics. The frequency spectrum of the CMV mainly contains the dc value, and the 3rd-, 9th-, 15th-, 21st-, and 27th-order harmonics; however, the dc value is dominant. In order to investigate the frequency spectrum of the CMV, fast Fourier transform analysis has been done in MATLAB\Simulink, results of which are shown in Table VI.

TABLE VII
PARAMETERS OF THE EXPERIMENTAL STUDY SYSTEM

Converter parameters	Values
Converter rating (kVA)	2
Capacitor Value (μF)	1000
Input dc voltage (V)	210
Output frequency (Hz)	60
Output inductance (mH)	10
Output load (Ω)	13

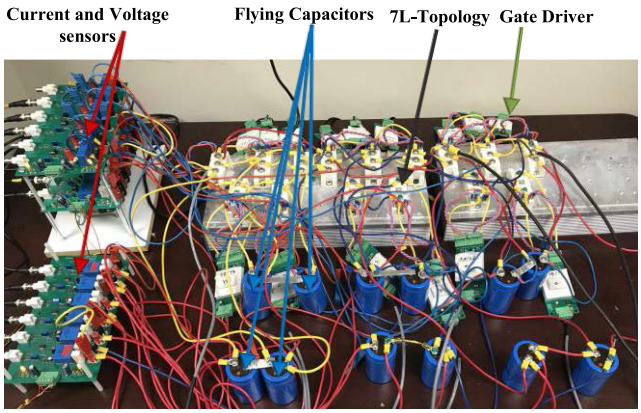


Fig. 11. Scaled-down prototype setup.

As can be seen, the CMV mainly contains the dc component. These results alongside the simulation and experimental studies show that approximation of the CMV as a dc value is valid, and does not have a significant effect on the performance of the controller based on MPC.

V. EXPERIMENTAL RESULTS

Similar to the simulations, experimental results for steady state and transients are shown. The dSPACE has been used as the digital controller platform in the experiments and the sampling time for the studies is set to 50 μs. The parameters used in the experiments are shown in Table VII. The scaled-down prototype is shown in Fig. 11. The insulated-gate bipolar transistor (IGBT) modules are from Semikron model SKM50GB12T4. LEM current sensors (LA55-P) and voltage sensors (LV25-P) are used, and the capacitors are 1000 μF 450 VDC from Cornell Dubilier. Gate drivers, model L501252, from Semikron are used.

A. Steady State

In this section, steady-state studies have been done to evaluate the performance of the seven-level topology controlled by the developed control method. In Fig. 12, the reference and output currents of the seven-level topology and the phase and line voltages are shown, to show the ability of the developed control method in reference tracking experimentally for a frequency of 60 Hz.

In Figs. 13–15, the output currents and FCs voltages are shown where the reference current is set to $i_{\rm ref} = 10$ A and the PF is 0.96, 0.46, and 0, respectively, which demonstrate the perfect operation of the converter and controller in different PFs. In Fig. 14, the resistor is changed to 2 Ω, and in Fig. 15 to 0 Ω in order to change the PF. In Fig. 16, the current is set to 5 A, to show the converter performance in half-load condition, and in Fig. 17, the frequency is set to $f = 5$ Hz, whereas the output current is set to $i_{\rm ref} = 10$ A, and the PF is 0.96. As can be seen in the results, the FCs voltages are well balanced at their desired values, which are 70 and 35 V for outer and inner capacitors, respectively.

B. Transients

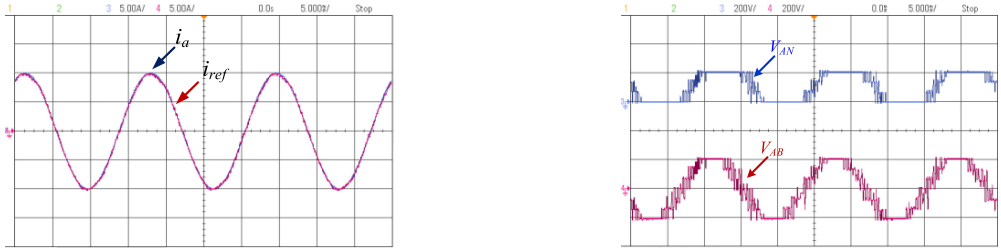
In this section, as in the simulation results, the performance of the developed control method is evaluated while the output current magnitude and frequency change.

In Fig. 18, the output current reference is changed from $i_{\rm ref} = 10$ to 5 A, and in Fig. 19, the frequency is changed from 20 to 40 Hz. As it is shown, the FCs voltages are well balanced during and after the transients, and the output currents followed the change in the current reference perfectly. Moreover, in Fig. 20, the developed control method is evaluated while the controller is deactivated for 50 ms, as it is shown the FCs voltages deviate from their desired value while the controller is deactivated, and after a few cycles that the controller is reactivated the FCs voltages are well balanced at their desired value.

C. Calculation Time Comparison

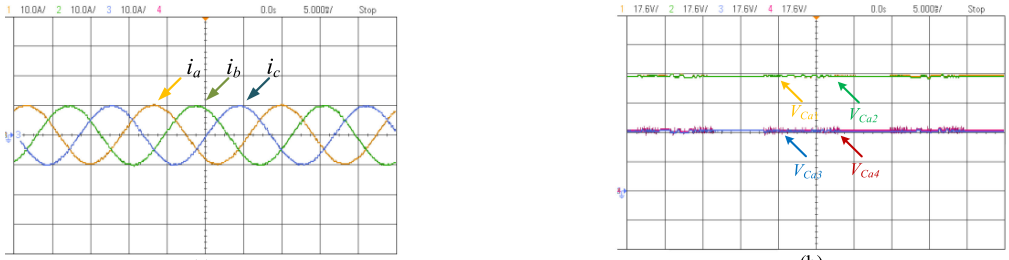
As mentioned, the dSPACE is used to implement the controller to regulate the FCs voltages of the seven-level topology and to control the output current. The step time of the controller can be understood in terms of calculation time of the control method since the dSPACE terminates the controller if it is not able to do the calculation in the specified fixed step time. In this case, the minimum step time to run the controller for conventional MPC is 60 μs, whereas for the reduced number of calculation MPC is 10 μs; therefore, the minimum step time required for implementing the controller based on the reduced number of calculation MPC is reduced to one-sixth times of the time required for the conventional MPC. The execution time is not linear with respect to the reduction of the computations, since other tasks such as feedbacks from the FCs and output currents, gating generators, and initializations require some time that is common for both approaches and affects the overall execution time. Therefore, the execution time is decreased only six times.

This demonstrates the effectiveness of the developed control method in reducing the number of calculations. This is an advantage for applications with more control objectives. The controller can satisfy more objectives in a shorter time since the number of calculations to control the converter is reduced.



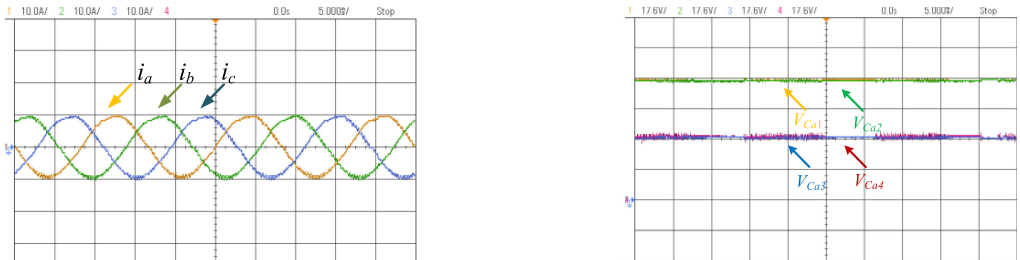
(a) (b)

Fig. 12. Experimental results, reference and actual output currents, phase and line voltages (5 A/div, 200 V/div time: 5 ms/div). (a) Output and ref. currents. (b) Phase and line voltages.



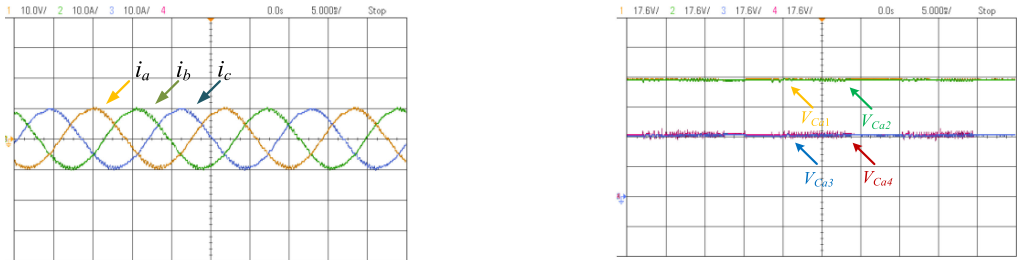
(a) (b)

Fig. 13. Experimental results: $i_{\text{ref}} = 10$ A, $f_o = 60$ Hz, PF $= 0.96$ (10 A/div, 17.6 V/div, 5 ms/div). (a) Inverter output currents. (b) Voltages of FCs.



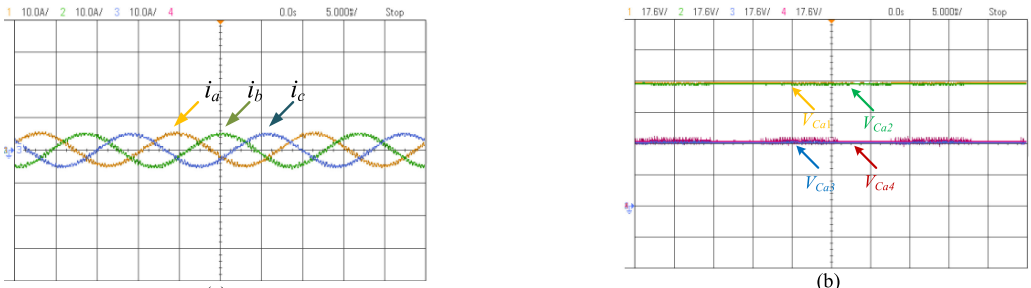
(a) (b)

Fig. 14. Experimental results: $i_{\text{ref}} = 10$ A, $f_o = 60$ Hz, PF $= 0.46$ (10 A/div, 17.6 V/div, 5 ms/div). (a) Inverter output currents. (b) Voltages of FCs.



(a) (b)

Fig. 15. Experimental results: $i_{\text{ref}} = 10$ A, $f_o = 60$ Hz, PF $= 0$ (10 A/div, 17.6 V/div, 5 ms/div). (a) Inverter output currents. (b) Voltages of FCs.



(a) (b)

Fig. 16. Experimental results: $i_{\text{ref}} = 5$ A, $f_o = 60$ Hz, PF $= 0.96$ (10 A/div, 17.6 V/div, 5 ms/div). (a) Inverter output currents. (b) Voltages of FCs.

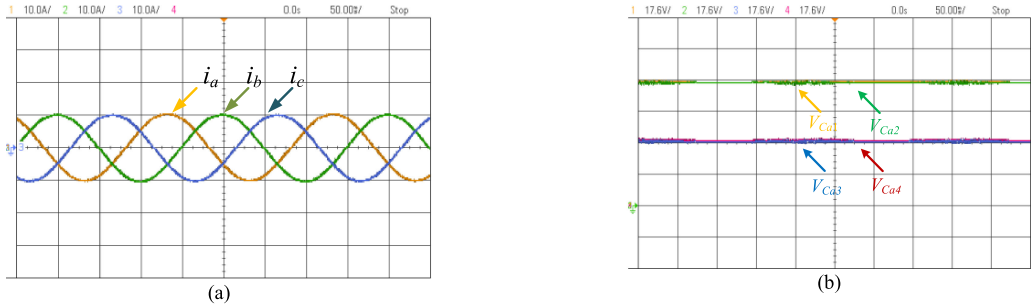


Fig. 17. Experimental results: $i_{\mathrm{ref}} = 10$ A, $f_o = 5$ Hz, PF $= 0.96$ (10 A/div, 17.6 V/div, 50 ms/div). (a) Inverter output currents. (b) Voltages of FCs.

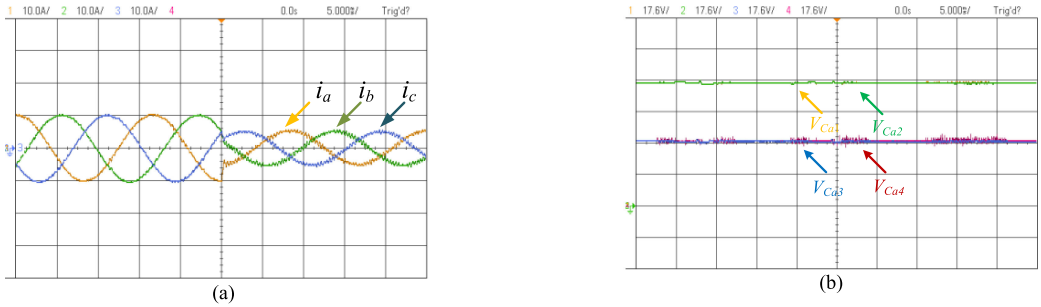


Fig. 18. Experimental results: i_{ref} changes from 10 to 5 A, PF $= 0.96$ (10 A/div, 17.6 V/div, 5 ms/div). (a) Inverter output currents. (b) Voltages of FCs.

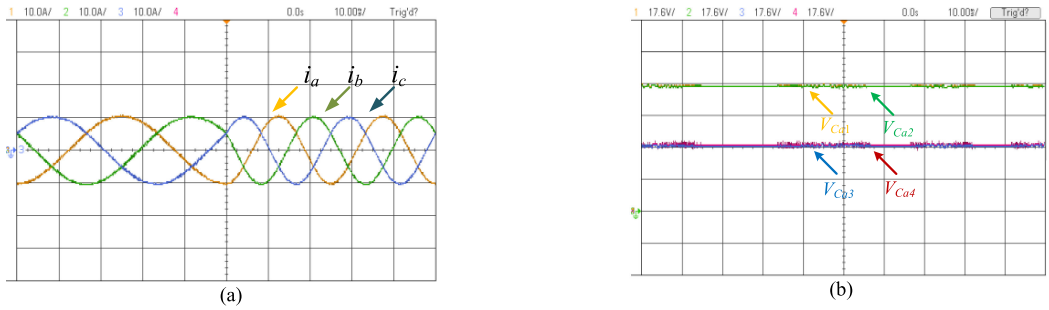


Fig. 19. Experimental results: frequency changes from 20 to 40 Hz, PF $= 0.96$ (10 A/div, 17.6 V/div, 10 ms/div). (a) Inverter output currents. (b) Voltages of FCs.

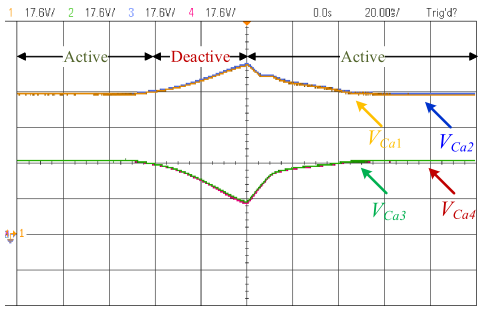


Fig. 20. Voltages of FC when the controller is deactivated and activated.

VI. Conclusion

In this article, a control technique based on a computational efficient FCS-MPC approach is applied to a seven-level topology that has a smaller number of components compared to other existing seven-level topologies. Since the other controller developed based on modulation schemes such as sinusoidal pulse width modulation (SPWM) and space vector modulation (SVM) is not able to satisfy the control objectives of the seven-level topology in all operating conditions, the conventional FCS-MPC was applied to the seven-level topology. As the analysis shows, the number of calculations to control the output current and FCs voltages of the seven-level topology is reduced from 1728 to 36 in this article, whereas the execution time is decreased six times. The simulation and experimental results in steady-state and transient conditions show that the developed control method successfully regulates the FCs voltages and controls the output currents.

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