Methods to Estimate Load-Transient Response of Buck Converter Under Direct-Duty-Ratio and Peak-Current-Mode Control

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***Abstract*—This article provides a simple and effective method to model the closed-loop output impedance of a buck converter under direct-duty-ratio and peak-current-mode (PCM) control as well as under PCM control with output-current-feedforward, which can be used to study, analytically, the time-domain response of the output voltage to a change in the load current. The method is based on the modified small-signal models of the open-loop output impedance and the classical control-engineering method to model the closed-loop dynamics of a system by using the crossover frequency and phase margin of the feedback control loop. The method is validated by using an experimental buck converter as well as simulations. The derived time-domain load-response functions can be effectively used to study in detail the factors determining the transient process of the response. According to the time-domain functions, it can be observed that the initial phase of the transient is determined by the feedback-loop design, and the settling process is determined by the lowest-frequency zeros of the controller together with the zeros of the open-loop output impedance.**

***Index Terms*—Analytic models, DC-DC converter, load response, pulse width modulation.**

I. Introduction

THE MATHEMATICAL treatment of the load-transient response of the direct-duty-ratio (DDR) or voltage-mode (VM)-controlled buck converter has already been introduced in early 1980s [1] based on the small-signal models obtained by applying the state-space-averaging (SSA) technique introduced in [2] and [3]. Similar treatments can be found in many literatures such as in [4]–[6]. It was observed in late 1980s [7], [8] and confirmed later [9]–[11] that the application of load-current feedforward will improve the load response significantly. The load-transient response can also be improved by applying capacitor-current feedforward, because the change in the load current will reflect as a change in the capacitor current as well [12], [13], which will cause the same effects (i.e., a significant reduction in the open-loop output impedance as demonstrated explicitly in [10]) as the output-current-feedforward (OCF) technique [7]–[11]. The fastest load response can be obtained by temporarily shunting the output inductor by means of some external circuitry during the transient phase as introduced, for example, in [14].

There are many design factors in addition to the OCF technique, and the application of the external output-inductor shunting circuitry, which will affect the obtainable transient response [15], [16] such as a proper selection of power-stage components [17]–[19], the control bandwidth [20]–[23], and the phase margin [25], [26] of the feedback loop. It is also known that the existence of the right-half-plane (RHP) zero in the control dynamics will limit the control bandwidth approximately to half the frequency of the zero [16], [27], [28]. The bandwidth limitation leads usually to a rather high closed-loop output impedance, and consequently, to a poor load-transient response [27, pp. 321–329].

The main goal of this article is to introduce an efficient method to obtain an analytical model of the closed-loop output impedance for the DDR, PCM, and PCM-OCF-controlled buck converters, which contains a sufficiently low number of poles for being able to find the analytic time-domain solution for the load-transient response. It is known that the output-voltage-transient behavior, induced by a change in the output current, is governed by the closed-loop output impedance and the applied load-current-step dynamics [15], [16], [28]. The closed-loop output impedance can be given based on the small-signal models of the open-loop output impedance and the feedback loop but the resulting impedance contains a large number of poles, and therefore, the explicit time-domain form of the output-voltage transient is difficult to obtain. The time-domain behavior of the load-transient response can be naturally obtained by simulation but the waveform does not give specific information on the factors affecting the response. The method to solve the problem for obtaining a simplified small-signal model of the closed-loop output impedance is based on the classical control engineering [28, pp. 549–552], [29] to represent the sensitivity function in a simple second-order form, and the open-loop output impedance in a clever way [30]. The open-loop output impedance denotes the output impedance when the output terminal feedback is open. The proposed method is validated by using an experimental buck converter under the named control techniques.

The rest of this article is organized as follows. Section II introduces the theoretical basis for the load-transient-response modeling in terms of classical control engineering, and experimental evidence to validate the control engineering method.

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Section III introduces the theoretical methods to estimate the open-loop output impedance of the converter. Sections IV and V provide the analytical time-domain load-response functions, and the validation of the proposed modeling method. The conclusion is finally presented in Section VI.

II. Control-Engineering Method for Characterizing Closed-Loop System

The aim of this section is to introduce the control-engineering method to characterize a general closed-loop system as a second-order system, and to apply the information for obtaining a useful formulation for the output-voltage load transient, which is applicable for the dc–dc converters as well. It is also shown that a comparable feedback-loop design will yield similar transient responses despite the significant differences in the open-loop behavior of the dc–dc converter in continuous (CCM) and discontinuous (DCM) conduction modes.

A. Sensitivity Function Estimation

According to the classical control engineering [28]–[30], the closed-loop system can be characterized by its estimated complementary sensitivity function $T_e(s)$ as

$$T_e(s) = \frac{\omega_{n-e}^2}{s^2 + s2\zeta_e\omega_{n-e} + \omega_{n-e}^2} \tag{1}$$

where ω_{n-e} and ζ_e denote the estimated undamped natural frequency and damping factor, respectively. ω_{n-e} and ζ_e can be computed according to [29] by

$$\zeta_e = \frac{\tan(\mathrm{PM})}{2(1+\tan^2(\mathrm{PM}))^{\frac{1}{4}}} \quad \omega_{n-e} = \frac{\omega_c}{\sqrt{\sqrt{1+4\zeta_e^4} - 2\zeta_e^2}} \tag{2}$$

where PM denotes the phase margin and ω_c the crossover frequency of the corresponding authentic feedback loop.

Equations (1) and (2) are valid for the second-order converters if the crossover frequency of the feedback loop is designed in such a way that the power-stage resonance does not contribute to the behavior of the closed-loop output impedance. This is obtained by designing the crossover frequency to be higher than at least three times the resonant frequency [27, p. 102] or sufficiently lower than the resonant frequency as discussed in [29]. In the case of higher order converters, the validity of (1) and (2) is explained, for example, in [28, pp. 553–555].

The complementary sensitivity function $T(s)$ can be given based on the corresponding feedback loop gain $L(s)$ according to [28] by

$$T(s) = \frac{L(s)}{1 + L(s)} \tag{3}$$

and therefore, the estimated feedback loop gain $L_e(s)$ can be solved from (1) as

$$L_e(s) = \frac{\omega_{n-e}^2}{s(s + 2\zeta_e\omega_{n-e})}. \tag{4}$$

The behavior of the output-voltage transient (Δv_o), induced by the change in the output current (Δi_o), can be given in frequency domain according to [16], [28], [30], and [31] by

$$\Delta v_o(s) = Z_{o-c}\Delta i_o(s) = S(s)Z_{o-o}\Delta i_o(s) \tag{5}$$

where Z_{o-c} and Z_{o-o} denote the closed-loop and open-loop output impedances of the associated converter, and $S(s)$ the corresponding sensitivity function as $S(s) = (1 + L(s))^{-1}$, respectively. The sensitivity function can be estimated according to (4) to be

$$S_e(s) = \frac{s(s + 2\zeta_e\omega_{n-e})}{s^2 + s2\zeta_e\omega_{n-e} + \omega_{n-e}^2} \tag{6}$$

and the estimate for the output-voltage transient can be finally [cf., (5)] given by

$$\Delta v_o(s) = Z_{o-o}^e \frac{s(s + 2\zeta_e\omega_{n-e})}{s^2 + s2\zeta_e\omega_{n-e} + \omega_{n-e}^2}\Delta i_o(s) \tag{7}$$

where the open-loop output impedance (Z_{o-o}^e) needs to be estimated based on the original open-loop output impedance (Z_{o-o}) for obtaining the simplified load-transient formulation in the frequency domain. Z_{o-o} can be obtained by using proper small-signal modeling methods depending on the internal control mode (i.e., DDR, PCM, etc.) and conduction mode (i.e., CCM or DCM) as introduced, for example, in [27]. It shall be also noted that both of the operating points during the transient shall stay in the same conduction mode (i.e., CCM or DCM) for ensuring the validity of (7).

B. Controller Design Principles

The control or compensation-design methods applied in this article are as follows. The resonant nature of the open-loop DDR-controlled converter in a CCM would require to use a proportional-integral-derivative (PID)-type controller given in (8). The controller zeros are typically placed at the undamped natural frequency (i.e., $1/\sqrt{LC}$ for a buck converter). The first pole is placed at the output capacitor zero (i.e., $\omega_{zC} = 1/r_C C$), and the second pole is placed in such a manner that the phase margin will be as desired. The controller gain (K_{cc}) is selected in such a manner that the desired crossover frequency of the feedback loop is obtained

$$G_{cc-\mathrm{PID}} = K_{cc}\frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s(1 + s/\omega_{p1})(1 + s/\omega_{p2})}. \tag{8}$$

The highly damped nature of the PCM-controlled and DCM-operated DDR-controlled open-loop converters would require to use a proportional-integral (PI)-type controller [cf., (9)], where the zero can be placed at the undamped natural frequency (i.e., $1/\sqrt{LC}$ for a buck converter) or lower than it, and the pole in such a manner that the phase margin will be as desired [27]. The controller gain (K_{cc}) will determine the crossover frequency of the feedback loop, respectively

$$G_{cc-\mathrm{PI}} = K_{cc}\frac{1 + s/\omega_{z1}}{s(1 + s/\omega_{p1})}. \tag{9}$$

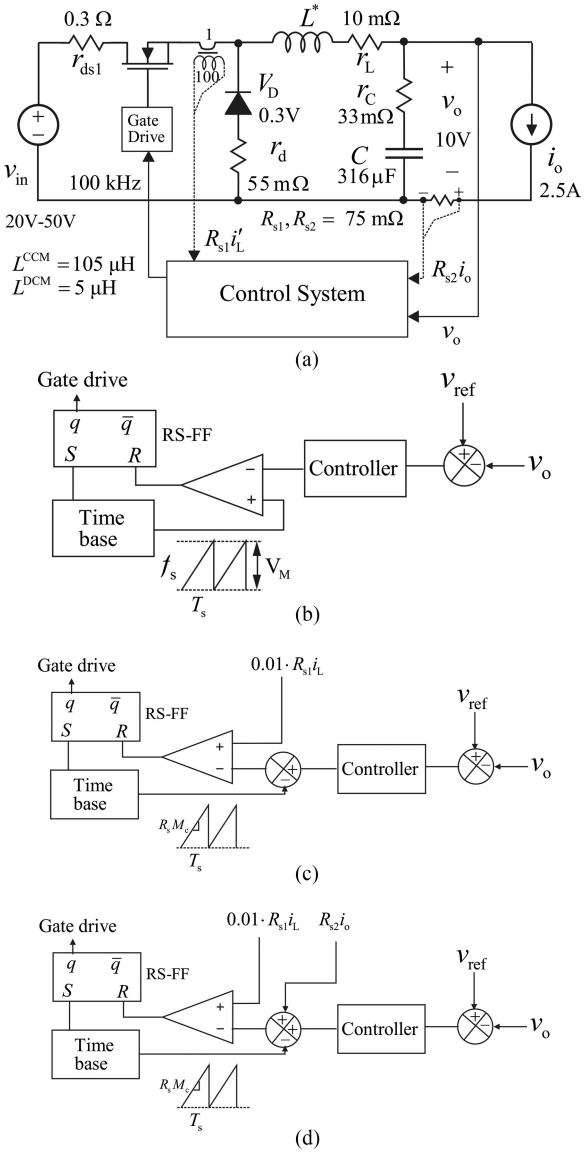

Fig. 1. (a) Power stage of the experimental buck converter with the definition of the component values and the input/output terminal sources. (b) DDR control system. (c) PCM control system. (d) PCM-OCF control system.

C. Experimental Evidence

Fig. 1(a) shows the power stage of the experimental buck converter with the internal and external feedbacks for determining the dynamics of the converter under DDR [see Fig. 1(b)], PCM [see Fig. 1(c)], and PCM-OCF [see Fig. 1(d)] controls. The value of the output inductor equals 105 μH, when the converter is designed to operate in the CCM and 5 μH, when the converter is designed to operate in the DCM, respectively. The experimental output-voltage transient response is obtained by changing the output current from 0.2 to 2.5 A with a slew rate of 250 A/μs by means of an electronic constant-current sink manufactured by CROMA. The frequency responses given in this article are measured by means of Venable Industries frequency response analyzer Model 320 with an impedance measurement kit.

Fig. 2 shows the measured output-voltage-loop gains of the DDR-controlled buck converter operating in the CCM (blue color) and in the DCM (red color) at the input voltage of 50 V, where the crossover frequency of both of the converters is approximately 11.4 kHz, and the corresponding phase margins 46° (CCM) and 50° (DCM), respectively. According to (2), we can compute that $\zeta_e \approx 0.432$ and $\omega_{n-e} \approx 2\pi \cdot 13.7$ krad/s in the CCM as well as $\zeta_e \approx 0.478$ and $\omega_{n-e} \approx 2\pi \cdot 14.2$ krad/s in the DCM.

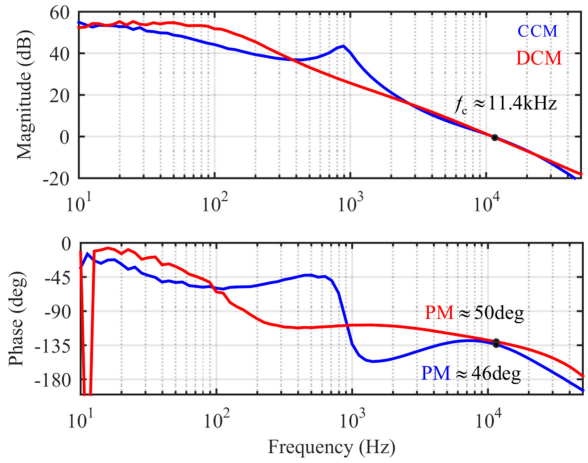

Fig. 2. Measured frequency responses of the DDR-controlled buck converter in CCM (blue) and DCM (red) at the input voltage of 50 V.

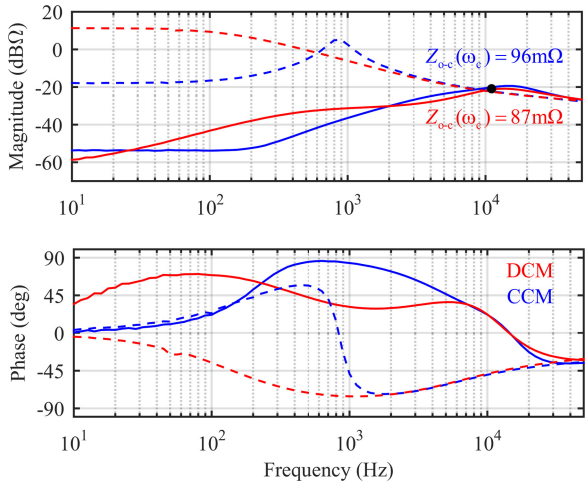

Fig. 3. Measured frequency responses of the open-loop (dashed lines) and closed-loop (solid lines) output impedance (blue, CCM and red, DCM) at the input voltage of 50 V.

Fig. 3 shows the measured open (dashed lines) and closed-loop (solid lines) output impedances of the DRR-controlled buck converter in the CCM (blue color) and in the DCM (red color). The controller designs of the converters are performed as described in Section II-B, and the lowest-frequency zeros are placed at the same frequency, which are known to determine the settling time as well [15], [16], [27]. The comparable control design of the converters (i.e., the location of controller zeros, the crossover frequency of the feedback loop, and the PM) will produce quite similar closed-loop output impedances (cf., the magnitude behavior), which implies that the load transient responses will be similar as well (cf., Fig. 4).

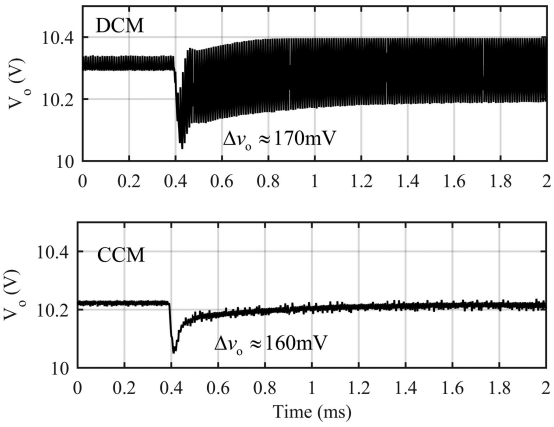

Fig. 4. Measured transient responses of the output voltage to a step change in the output current from 0.2 to 2.5 A in DCM and CCM at the input voltage of 50 V.

Fig. 4 shows the output-voltage load-transient responses when the applied load-current steps are equal. The similarity of the responses is obvious as the behavior of the close-loop output impedances imply (cf., Fig. 3).

It is usually assumed [27] that the dip in the output voltage due to the step change in the output current corresponds to $\Delta v_o \approx Z_{o-c}(\omega_c)\Delta i_o$, where $Z_{o-c}(\omega_c)$ denotes the small-signal output impedance at the feedback-loop crossover frequency (ω_c) (cf., Fig. 2) as given in Fig. 3. Based on the magnitudes of $Z_{o-c}(\omega_c)$, the corresponding predicted voltage dips are 220 mV (CCM) and 200 mV (DCM), which are quite close to the values given in Fig. 4.

The presented experimental evidence shows clearly that the equally designed closed-loop system will provide quite comparable dynamic behavior despite the significant differences in the open-loop dynamics (i.e., highly resonant in the CCM, and highly damped in the DCM) [27].

III. Theoretical Basis for Estimating Open-Loop Output Impedance

The estimate for the open-loop output impedance can be derived based on the small-signal model of the original output impedance, which can be obtained by using proper small-signal modeling methods [30], [32]: The SSA method introduced in [3] will yield accurate models in the CCM for the DDR-controlled converters as demonstrated in [27]. The modified version of the SSA method, introduced in [32] and [33], will yield accurate predictions in the DCM for the DDR-controlled converters as demonstrated in [34]. The models given in [33] are load-resistor affected, which can be applied only when the load-resistor effect is removed as discussed in [35]. Accurate small-signal modeling methods for the PCM-controlled buck converter are introduced and validated in [36] (CCM) and in [37] and [38] (DCM), respectively.

The original open-loop output impedance of a buck converter can be given, in general, according to [27] by

$$Z_{o-o} = \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zL})(s+\omega_{zC})}{s^2 + s2\zeta_o\omega_{n-o} + \omega_{n-o}^2} \tag{10}$$

where r_a denotes the ohmic losses in series with the output inductor, $\omega_{zL} = r_a/L$ denotes the output-inductor-related zero, $\omega_{zC} = 1/r_C C$ denotes the output-capacitor-related zero, ζ_o and ω_{n-o} denote the damping factor and undamped natural frequency of the open-loop power stage, respectively. If the open-loop converter is highly damped as under the PCM control [36], [37] or in the DCM [34], then the poles of the converter are well separated, and they can be estimated according to [27] as

$$\omega_{p-\mathrm{LF}} \approx \frac{\omega_{n-o}}{2\zeta_o} \quad \omega_{p-\mathrm{HF}} \approx 2\zeta_o\omega_{n-o} \tag{11}$$

where $\omega_{p-\mathrm{LF}}$ denotes the low-frequency pole, and $\omega_{p-\mathrm{HF}}$ denotes the high-frequency pole, respectively. Therefore, (10) can be given for a highly damped converter by

$$Z_{o-o} \approx \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zL})(s+\omega_{zC})}{\left(s+\frac{\omega_{n-o}}{2\zeta_o}\right)(s+2\zeta_o\omega_{n-o})}. \tag{12}$$

The estimates for the open-loop output impedance of the buck converter under the named control techniques are given explicitly in the subsequent subsections.

A. DDR-Controlled Buck Converter in CCM

The resonant nature of the open-loop converter causes peaking in the open-loop transfer functions of the converter as well as in the feedback-loop gain (cf., Figs. 2 and 3). The resonant peaking of the feedback-loop gain will remove the resonant peaking from the closed-loop output impedance, when the feedback-loop crossover frequency is sufficiently higher than the resonant frequency (i.e., at least three times) [27].

The estimated feedback-loop gain [$L_e(s)$ in (4)] does not contain similar resonant behavior as the authentic feedback-loop gain (cf., Fig. 2, blue line), which would remove the resonant behavior from the closed-loop output impedance, as shown in Fig. 3 (cf., blue lines). Therefore, the estimated open-loop output impedance shall not contain resonant peaking either but the original order of the system shall be retained. As discussed in [30], the original resonant poles can be replaced by means of the zeros of the feedback controller (ω_{z1} and ω_{z2}) as given in (8). As discussed earlier, the zeros are typically placed at the undamped natural frequency $(\omega_{n-o} = 1/\sqrt{LC})$.

Therefore, the estimate for the open-loop output impedance [cf., (10)] and the output-voltage transient response [cf. (7)] can be given by

$$Z_{o-o}^e \approx \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zL})(s+\omega_{zC})}{(s+\omega_{z1})(s+\omega_{z2})} \tag{13}$$

$$\Delta v_{o-e}(s) = \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zL})(s+\omega_{zC})}{(s+\omega_{z1})(s+\omega_{z2})} \cdot \frac{s(s+2\zeta_e\omega_{n-e})}{s^2 + s2\zeta_e\omega_{n-e} + \omega_{n-e}^2} \cdot \Delta i_o(s). \tag{14}$$

B. Highly Damped Buck Converter

The dynamic behavior of the DCM-operated DDR-controlled buck converter and the PCM-controlled buck converter are highly damped at open loop, because the loss resistor (r_a)

[cf., (10)] is rather large in value [27], [36]–[38] (cf., Fig. 3, dashed red line). Thus, the open-loop poles of the converters can be estimated as given in (11). In addition, the high-frequency zero (ω_{zL}) equals approximately the high-frequency pole $(\omega_{p-\mathrm{HF}})$ as well (cf., [27, pp. 186–172] and [36]). As discussed in Section II, the lowest frequency zero of the controller will determine the settling time of the transient. In this case, the controller is a PI controller having only one zero [cf., (9)]. As a consequence, the low-frequency pole $(\omega_{p-\mathrm{LF}})$ of the original open-loop output impedance will be replaced by the controller zero (ω_z) for obtaining a proper estimate for the open-loop output impedance and the output-voltage transient response according (15) and (16)

$$Z_{o-o}^{e} \approx \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zC})}{(s+\omega_z)} \tag{15}$$

$$\Delta v_{o-e}(s) = \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zC})}{(s+\omega_z)} \cdot \frac{s(s+2\zeta_e\omega_{n-e})}{s^2+s2\zeta_e\omega_{n-e}+\omega_{n-e}^2} \cdot \Delta i_o(s). \tag{16}$$

C. PCM-OCF-Controlled Buck Converter in CCM

The dynamic behavior of the PCM-OCF-controlled buck converter in the CCM is highly damped similarly as the PCM-controlled converter, where the zeros of open-loop output impedance equals the zeros of the CCM-operated DDR-controlled buck converter, and the poles equal the poles of the CCM-operated PCM-controlled converter [10]. In this case, no pole-zero cancellation will take place as in (15), because the loss resistor (r_a) is rather small (cf., [10]). Therefore, the estimates for the open-loop output impedance and the output-voltage transient response can be given according to (17) and (18), respectively. The low-frequency pole $(\omega_{n-o}/2\zeta_o)$ in (17) can be replaced by the controller zero as in (15) but it does not improve the accuracy of the estimate as discussed more in detail in Section V-C.

$$Z_{o-o}^{e} \approx \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zL})(s+\omega_{zC})}{\left(s+\frac{\omega_{n-o}}{2\zeta_o}\right)(s+2\zeta_o\omega_{n-o})} \tag{17}$$

$$\Delta v_{o-e}(s) = \frac{r_a\omega_{n-o}^2}{\omega_{zC}\omega_{zL}} \cdot \frac{(s+\omega_{zL})(s+\omega_{zC})}{(s+\frac{\omega_{n-o}}{2\zeta_o})(s+2\zeta_o\omega_{n-o})} \cdot \frac{s(s+2\zeta_e\omega_{n-e})}{s^2+s2\zeta_e\omega_{n-e}+\omega_{n-e}^2} \cdot \Delta i_o(s). \tag{18}$$

IV. Time-Domain Transients

The time-domain output-voltage-load transient can be given, in general, as

$$\Delta v_{o-e}(t) = \frac{r_a\omega_{n-o}^2}{\omega_{zL}\omega_{zC}} \cdot F(t) \cdot \Delta i_o = r_C \cdot F(t) \cdot \Delta i_o \tag{19}$$

where $F(t)$ denotes the associated time function, which can be obtained by applying the inverse Laplace transform to the given frequency-domain transient-response functions in (14), (16), and (18) as well as by using a proper frequency-domain function for $\Delta i_o(s)$. In this article, $\Delta i_o(t)$ is assumed to be a step function yielding $\Delta i_o(s) = \Delta i_o/s$, where Δi_o denotes the change in the output current. According to (19), we can conclude that the initial voltage drop in the output voltage will be $r_C\Delta i_o$, which is also the absolute minimum voltage drop of the load-transient response.

The time functions $(F(t))$ for the buck converter under the named control techniques are given explicitly in the subsequent subsections assuming that $\zeta_e < 1$.

A. DDR-Controlled Buck Converter in CCM

Equation (14), in Section III-A, defines the frequency-domain output-voltage load transient for a highly resonant CCM-operated buck converter, from which the corresponding time-domain function $(F(t))$ [cf., (19)] can be solved by applying inverse Laplace transformation techniques. The corresponding $F(t)$ can be given in case of $\omega_{z1} = \omega_{z2} = \omega_{n-o}$ by

$$F(t) = (A+Bt)e^{-\omega_{n-o}t} + CEe^{-\zeta_e\omega_{n-e}t}\left(\sin\left(\omega_{n-e}\sqrt{1-\zeta_e^2}\cdot t+\Theta\right)\right)$$
$$E = \sqrt{1+\left(\frac{\frac{D}{C}-\zeta_e\omega_{n-e}}{\omega_{n-e}\sqrt{1-\zeta_e^2}}\right)^2}\ \Theta = \tan^{-1}\left(\frac{\omega_{n-e}\sqrt{1-\zeta_e^2}}{\frac{D}{C}-\zeta_e\omega_{n-e}}\right) \tag{20}$$

where the coefficients *A*, *B*, *C*, and *D* can be solved from the set of simultaneous equations given in Appendix (A.1).

If the controller zeros ω_{z1} and ω_{z2} are placed arbitrarily, then $F(t)$ can be given by

$$F(t) = Ae^{-\omega_{z1}t} + Be^{-\omega_{z2}t} + CEe^{-\zeta_e\omega_{n-e}t}\left(\sin(\omega_{n-e}\sqrt{1-\zeta_e^2}\cdot t+\Theta)\right)$$
$$E = \sqrt{1+\left(\frac{\frac{D}{C}-\zeta_e\omega_{n-e}}{\omega_{n-e}\sqrt{1-\zeta_e^2}}\right)^2}\ \Theta = \tan^{-1}\left(\frac{\omega_{n-e}\sqrt{1-\zeta_e^2}}{\frac{D}{C}-\zeta_e\omega_{n-e}}\right) \tag{21}$$

where the coefficients *A*, *B*, *C*, and *D* can be solved from the set of simultaneous equations given in Appendix (A.2).

The settling time of the transients are determined by the first exponential functions in (20) and (21) when it is assumed that the lowest frequency controller zero equals ω_{z1}.

B. Highly Damped Buck Converter

Equation (16), in Section III-B, defines the frequency-domain output-voltage load transient for a highly damped buck converter (i.e., under PCM control and in DCM operation), from which the corresponding time-domain function $(F(t))$ can be solved by applying inverse Laplace transformation techniques.

The corresponding $F(t)$ can be given by

$$F(t) = Ae^{-\omega_z t} + BDe^{-\zeta_e \omega_{n-e} t}\left(\sin(\omega_{n-e}\sqrt{1-\zeta_e^2}\cdot t + \Theta)\right)$$

$$D = \sqrt{1+\left(\frac{\frac{C}{B}-\zeta_e\omega_{n-e}}{\omega_{n-e}\sqrt{1-\zeta_e^2}}\right)^2}\ \Theta = \tan^{-1}\left(\frac{\omega_{n-e}\sqrt{1-\zeta_e^2}}{\frac{C}{B}-\zeta_e\omega_{n-e}}\right) \quad (22)$$

and the coefficients *A*, *B*, and *C* can be solved from the set of simultaneous equations in Appendix (A.3), respectively.

The settling time of the transient is determined by the first exponential function in (22), having much higher time constant than the time constant of the exponential envelope function of the sinus term (i.e., $1/\omega_z \gg 1/\zeta_e\omega_e$).

C. PCM-OCF-Controlled Buck Converter in CCM

Equation (18), in Section III-C, defines the frequency-domain output-voltage load transient for the highly damped buck converter, where the output-current feedforward has reduced the lossless resistance in series with the output inductor (i.e., PCM-OCF control). The corresponding time-domain function $(F(t))$ can be solved by applying inverse Laplace transformation techniques to (18), yielding

$$F(t) = Ae^{-\frac{\omega_{n-o}}{2\zeta_o}t} + Be^{-2\zeta_o\omega_{n-o}t} + CEe^{-\zeta_e\omega_{n-e}t}\left(\sin(\omega_{n-e}\sqrt{1-\zeta_e^2}\cdot t + \Theta)\right)$$

$$E = \sqrt{1+\left(\frac{\frac{D}{C}-\zeta_e\omega_{n-e}}{\omega_{n-e}\sqrt{1-\zeta_e^2}}\right)^2}\ \Theta = \tan^{-1}\left(\frac{\omega_{n-e}\sqrt{1-\zeta_e^2}}{\frac{D}{C}-\zeta_e\omega_{n-e}}\right) \quad (23)$$

and the coefficients *A*, *B*, *C*, and *D* can be solved from the set of simultaneous equations in Appendix (A.4), respectively.

The first exponential function in (23) does not contribute to the settling process, because the coefficient A is much smaller than the coefficient B although its time constant is highest. The settling time is determined by the second exponential function and the envelope exponential function of the sinus term. Therefore, $F(t)$ can be estimated to be

$$F(t) \approx Be^{-2\zeta_o\omega_{n-o}t} + CEe^{-\zeta_e\omega_{n-e}t}\left(\sin\left(\omega_{n-e}\sqrt{1-\zeta_e^2}\cdot t + \Theta\right)\right). \quad (24)$$

V. Model Validation

We compare the measured and estimated output-voltage load transients in the subsequent subsections, where the estimated transients are obtained by applying MATLAB step function to the corresponding estimated output-voltage-transient equation according to (7) (cf., Section II). The validation can be performed by applying the estimated time-domain functions given in Section IV as well.

Fig. 5 shows the measured output-voltage-feedback-loop gains of the DDR- and PCM-controlled buck converters in the CCM (cf., Fig. 1) at the input voltage of 50 V. The loop gains of the PCM and PCM-OCF-controlled converters are equal when the controllers are the same as discussed in [10]. According to the given crossover frequency and phase margin (cf., Fig. 5), we can compute, based on (2), that $\zeta_{e-\mathrm{DDR}} \approx 0.432$, $\omega_{n-e-\mathrm{DDR}} \approx 2\pi \cdot 13.7$ krad/s, and $\tau_{e-\mathrm{DDR}} \approx 27\ \mu$s as well as $\zeta_{e-\mathrm{PCM}} \approx 0.541$, $\omega_{n-e-\mathrm{PCM}} \approx 2\pi \cdot 16.4$ krad/s, and $\tau_{e-\mathrm{PCM}} \approx 18\ \mu$s, where the time constant (τ_e) equals $1/\zeta_e\omega_{n-e}$.

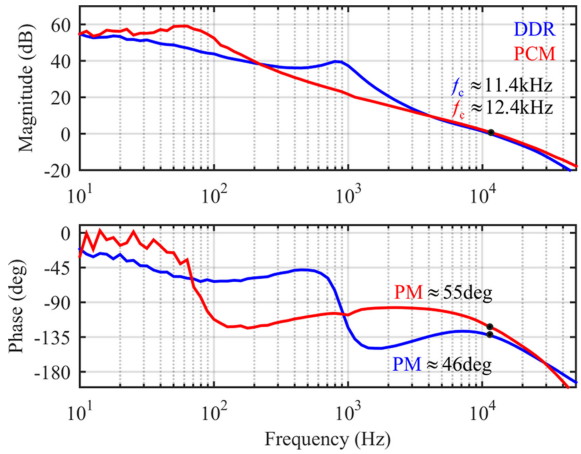

Fig. 5. Measured frequency responses of the DDR (blue) and PCM-controlled (red) buck converter with the definition of the crossover frequency (f_c) and the phase margin (PM) of the feedback loop at the input voltage of 50 V.

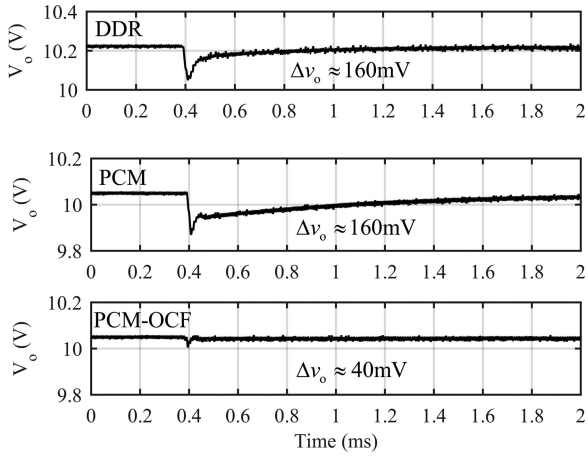

Fig. 6. Experimental output-voltage load-transient responses of the DDR, PCM, and PCM-OCF-controlled buck converters in CCM at the input voltage of 50 V.

Fig. 6 shows the output-voltage load transients of DDR, PCM, and PCM-OCF-controlled buck converters in the CCM (i.e., $\Delta i_o \approx 2.3$ A) at the input voltage of 50 V. The figure indicates clearly that the closed-loop-system time constants do not correlate with settling times at all. As discussed earlier, the settling time of the transient is usually determined by the location of the lowest-frequency controller zero in most of the cases except in the PCM-OCF-controlled buck converter (i.e., the PCM and PCM-OCF-controlled converters have exactly the same controllers in this case).

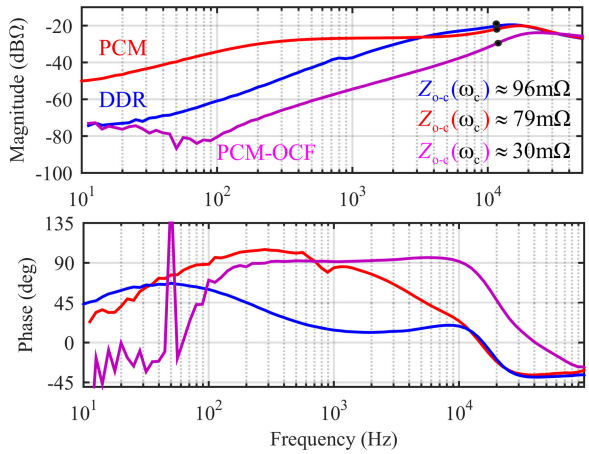

Fig. 7. Measured frequency responses of the close-loop output impedance of the DDR (blue), PCM (red), and PCM-OCF-controlled (magenta) buck converters in CCM at the input voltage of 50 V.

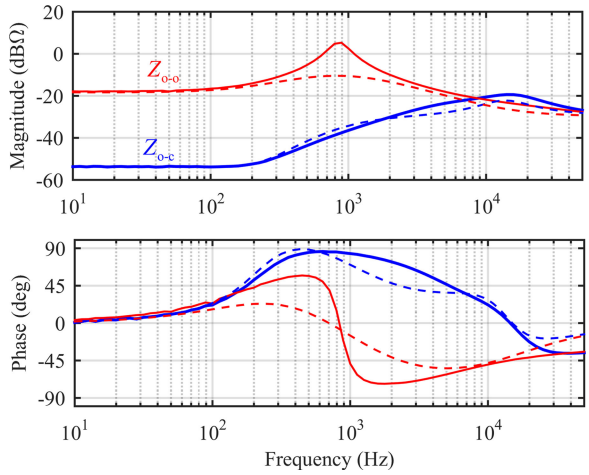

Fig. 8. Measured (solid lines) and estimated (dashed lines) frequency responses of the open-loop (red) and closed-loop (blue) output impedances of the DDR-controlled buck converters at the input voltage of 50 V.

As discussed in [15] and [27], the speed of the settling process is actually visible in the behavior of the low-frequency closed-loop output-impedance magnitude (cf., Fig. 7), where the highest low-frequency impedance magnitude implies the slowest settling speed as well. The information given in Fig. 8 implies that the fastest settling would take place in the PCM-OCF-controlled converter, and the slowest settling would take place in the PCM-controlled converter, as Fig. 7 explicitly confirms as well.

The estimated load-transient responses are produced in the subsequent subsections by applying the step command of MATLAB to $Z^{e}_{o-c}\Delta i_o$, where $\Delta i_o = 2.3$ A. The initial operating point (i.e., 0.2 A) of the experimental converter is in the DCM which means that the given transient estimates will not accurately match with the experimental responses. Therefore, the transient behavior of the DDR and PCM-controlled converter is simulated in such a manner that both of the operating points are in the CCM (i.e., from 1.0 to 2.5 A), and the responses are compared to the corresponding estimates.

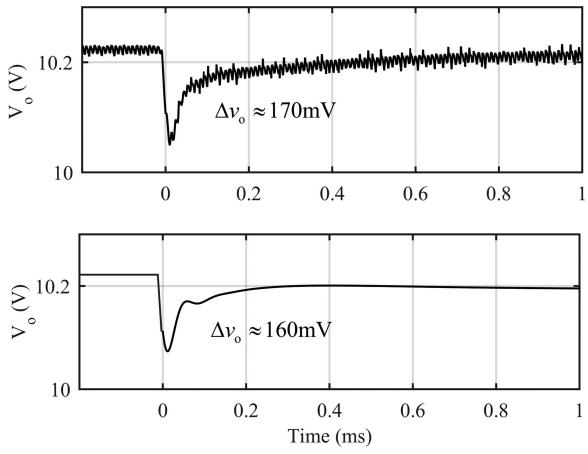

Fig. 9. (Top) Measured and (bottom) estimated output-voltage load transient of the DDR-controlled buck converter at the input voltage of 50 V.

A. DDR-Controlled Buck Converter in CCM

The small-signal open-loop output impedance (Z^{DDR}_{o-o}) of the DDR-controlled buck converter [cf., Fig. 1(a)] can be given according to [27, p. 145] [cf. (10)] by

$$\frac{1}{LC}\cdot\frac{(r_e - r_C)(1 + s\frac{L}{r_e - r_C})(1 + sr_C C)}{s^2 + s\frac{r_e}{L} + \frac{1}{LC}} \tag{25}$$

where $r_e = r_L + Dr_{ds} + D'r_d + r_C$. According to the standard form of the denominator of the second-order system in (1), the damping factor (ζ_o) and the undamped natural frequency (ω_{n-o}) can be given by

$$\varsigma_o = \frac{r_e}{2}\sqrt{\frac{C}{L}} \quad \omega_{n-o} = \frac{1}{\sqrt{LC}}. \tag{26}$$

According to Fig. 1 and the duty ratio at the given final operating point (i.e., $D \approx 0.21$), the values of (26) can be computed to be $\zeta_o \approx 0.12$ and $\omega_{n-o} \approx 2\pi \cdot 874$ rad/s, respectively.

$Z^{e-\text{DDR}}_{o-o}$ can be computed according to (13) and (25) as well as S^{PCM}_{e}can be computed according to (6) based on the feedback-loop crossover frequency and PM given in Fig. 5 (blue color), which determine the estimate for the closed-loop output impedances as $Z^{e-\text{DDR}}_{o-c} = Z^{e-\text{DDR}}_{o-o} \cdot S^{\text{DDR}}_{e}$.

Fig. 8 shows the measured (solid lines) and estimated (dashed lines) open (red) and closed-loop (blue) output impedances. A series impedance of $2{\cdot}3$ mΩ is added into the estimated closed-loop output impedance, which is visible at the measured closed-loop impedance as well (cf., Fig. 8, blue color). The estimates match quite well with the measured impedances.

Fig. 9 shows the measured (top) and estimated (bottom) output-voltage load-transient responses, which have a quite good match in dip value and settling time.

The initial operating point (i.e., 0.2 A) of the experimental converter is in the DCM, and therefore, the developed model does not correctly model the settling behavior of the transient due to the different behavior of the duty ratio (i.e., the initial duty ratio is lower than in the CCM). Therefore, the validity of

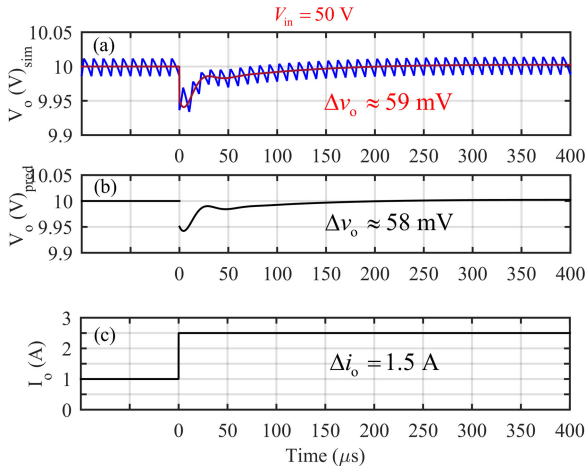

Fig. 10. (a) Simulated and (b) predicted output-voltage load responses to a step change of 1.5 A of load current (c) at the input voltage of 50 V.

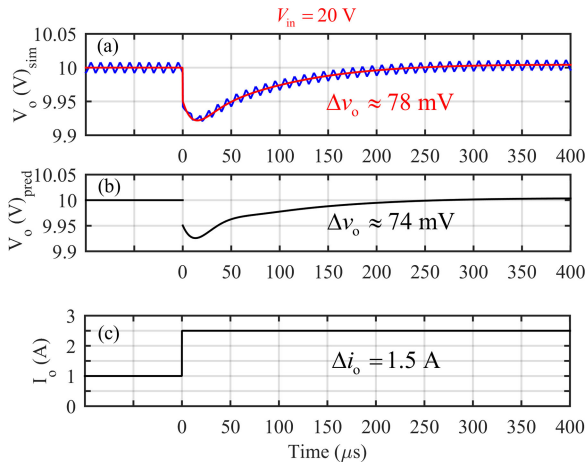

Fig. 11. (a) Simulated and (b) predicted output-voltage load responses to a step change of 1.5 A of load current (c) at the input voltage of 20 V.

the models is evaluated by simulation, where the load-current change is from 1.0 to 2.5 A, respectively. The feedback loop or the compensation is designed in such a way that the feedback-loop crossover frequency and phase margin are 20 kHz and 47°, respectively at the input voltage of 50 V as well as 9.5 kHz and 60° at the input voltage of 20 V, respectively. The simulated responses are measured by using MATLAB Simulink-based switching (blue response in Figs. 10 and 11) and average (red response in Figs. 10 and 11) models [27, pp. 279–291].

The output-voltage load responses in Figs. 10(a) and 11(a), and the corresponding predicted responses in Figs. 10(b) and 11(b) show that the modeling technique yields quite good estimates for the responses, when the input-voltage variation is taken fully into account.

B. PCM-Controlled Buck Converter in CCM

The small-signal open-loop output impedance (Z_{o-o}^{PCM}) of the PCM-controlled buck converter (cf., Fig. 1) can be given according to [27, p. 210] by

$$\frac{1}{LC} \cdot \frac{(r_e - r_C + F_m V_e q_L)\left(1 + s\frac{L}{r_e - r_C + F_m V_e q_L}\right)(1 + sr_C C)}{s^2 + s\frac{r_e + F_m V_e q_L}{L} + \frac{1}{LC}} \tag{27}$$

where

$$\begin{aligned} r_e &= r_L + Dr_{ds} + D'r_d + r_C \\ V_e &= V_{\mathrm{in}} + V_D + (r_d - r_{ds})I_o \\ F_m &= \frac{2L}{T_s(M_c \cdot 2L + (D' - D)V_e)} \\ q_L &= 1 + \frac{DD'T_s}{2L}(r_d - r_{ds}). \end{aligned} \tag{28}$$

According to the standard form of the denominator of the second-order system in (1), the damping factor (ζ_o) and the undamped natural frequency (ω_{n-o}) can be given by

$$\zeta_o = \frac{r_e + F_m V_e q_L}{2} \cdot \sqrt{\frac{C}{L}} \approx \frac{F_m V_e q_L}{2}\sqrt{\frac{C}{L}} \quad \omega_{n-o} = \frac{1}{\sqrt{LC}}. \tag{29}$$

According to Fig. 1 and the duty ratio at the given final operating point (i.e., $D \approx 0.21$), the values of (29) can be computed to be $\zeta_o \approx 11.6$ and $\omega_{n-o} \approx 2\pi \cdot 874$ rad/s, respectively. The high value of damping means that the poles of the converter are well separated as discussed in Section III, and can be estimated by

$$\omega_{p-\mathrm{LF}} \approx \frac{1}{(r_e + F_m V_e q_L)C} \quad \omega_{p-\mathrm{HF}} \approx \frac{r_e + F_m V_e q_L}{L} \tag{30}$$

where LF and HF stands for low frequency and high frequency, respectively. According to (27) and (30), the inductor-related zero (ω_{zL}) and the high-frequency pole $(\omega_{p-\mathrm{HF}})$ approximately cancel each other, and therefore, the open-loop output impedance can be estimated according to (15) (see Section III-B) by

$$Z_{o-o}^{e-\mathrm{PCM}} \approx \frac{1}{C} \cdot \frac{1 + sr_C C}{s + \omega_z}. \tag{31}$$

The corresponding sensitivity function (S_e^{PCM}) can be computed based on (6) by using $\zeta_e = 0.541$ and $\omega_{n-e} = 2\pi \cdot 16.4$ krad/s as given in the beginning of Section IV (Fig. 5, red curves). The closed-loop output-impedance estimate can be given by $Z_{o-o}^{e} = Z_{o-o}^{e-\mathrm{PCM}} S_e^{\mathrm{PCM}}$.

Fig. 12 shows the measured (solid lines) and estimated (dashed lines) open-loop (red) and closed-loop (blue) output impedances of the PCM-controlled CCM-operated converter. The closed-loop estimate matches quite well with the measured closed-loop output impedance. The small difference between the estimated and measured closed-loop impedances at the feedback-loop crossover frequency implies that the output-voltage dip values will differ from each other.

Fig. 13 shows the measured (top) and estimated (bottom) output-voltage load-transient responses to a step change in the

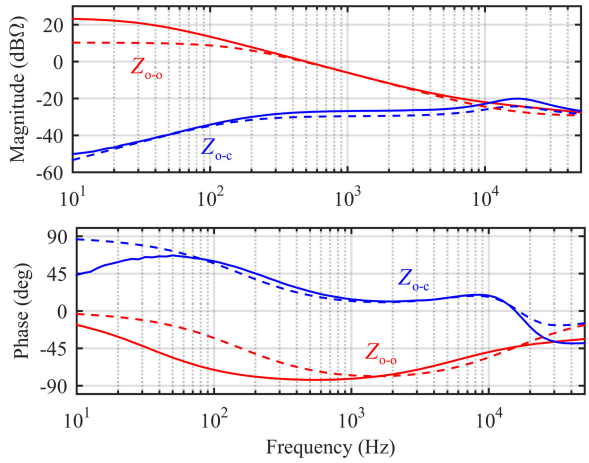

Fig. 12. Measured (solid lines) and estimated (dashed lines) open-loop (red) and closed-loop (blue) output impedances of the PCM-controlled buck converter at the input voltage of 50 V.

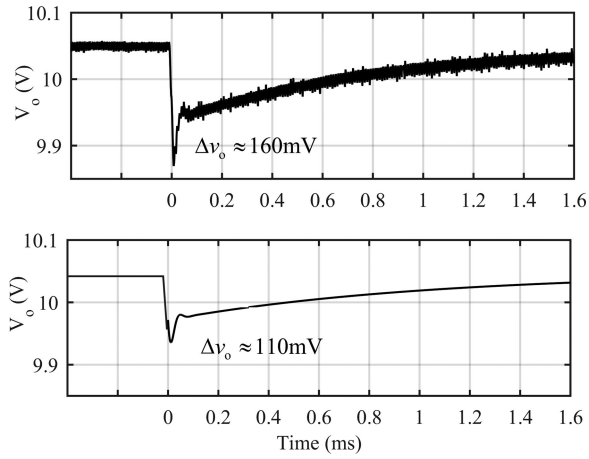

Fig. 13. (Top) Measured and (bottom) estimated output-voltage load transient of the PCM-controlled buck converter at the input voltage of 50 V.

output current. The figure indicates that the measured and estimated responses match each other quite well. The difference in the dip values of the responses may be originated from the differences in the closed-loop output impedance at the loop crossover frequency as discussed above.

The load-transient response of the PCM-controlled converter is reproduced by simulation (see Fig. 14) similarly as in Fig. 10 in the case of DDR-controlled converter. The feedback loop is designed to have a crossover frequency and phase margin of 10 kHz and 50° at the input voltage of 50 V, respectively.

The simulated (a) and predicted (b) responses in Fig. 14 indicate that the estimation method yields good accuracy in the case of the PCM-controlled buck converter as well.

C. PCM-OCF-Controlled Buck Converter in CCM

The small-signal open-loop output impedance $(Z_{o-o}^{\mathrm{PCM-OCF}})$ of the PCM-OCF-controlled buck converter (cf., Fig. 1) can be

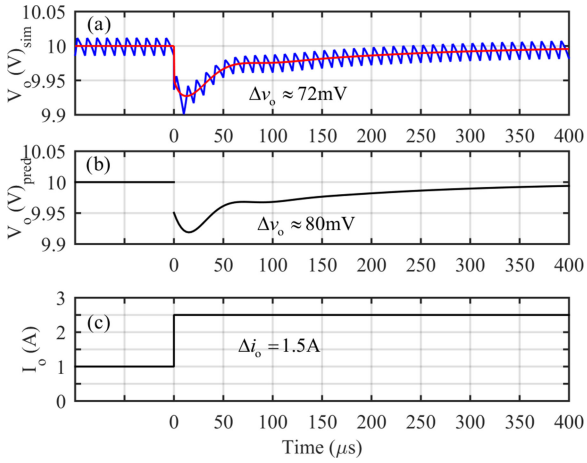

Fig. 14. (a) Simulated and (b) predicted output-voltage load responses to a step change of 1.5 A of load current (c) at the input voltage of 50 V.

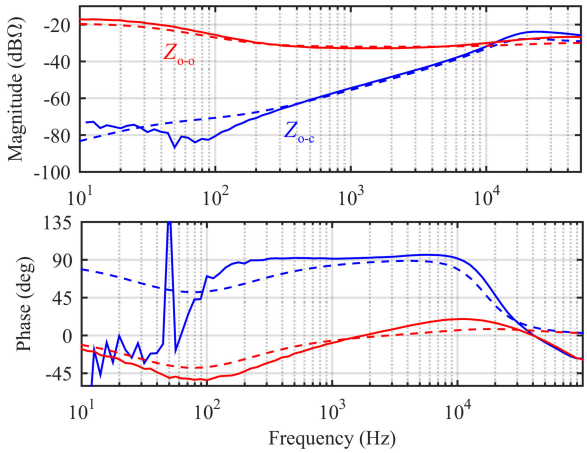

Fig. 15. Measured (solid lines) and estimated (dashed lines) open-loop (red) and closed-loop (blue) output impedances of the PCM-OCF-controlled buck converter at the input voltage of 50 V.

given according to [27, pp. 240–243] by

$$\frac{1}{LC}\cdot\frac{(r_e-r_C)\left(1+s\frac{L}{r_e-r_C}\right)(1+sr_CC)}{s^2+s\frac{r_e+F_mV_eq_L}{L}+\frac{1}{LC}} \tag{32}$$

where r_e, F_m,V_e, and q_L are defined in (28).

The damping factor and the undamped natural frequency are the same as defined for the PCM-controlled converter in Section IV-B. The open-loop output impedance in (32) is used as such as the estimate for the output impedance $(Z_{o-o}^{e-\mathrm{PCM-OCF}})$. $S_e^{\mathrm{PCM-OCF}}$ equals S_e^{PCM} defined in Section IV-B, and therefore, $Z_{o-c}^{e-\mathrm{PCM-OCF}}$ can be given by $Z_{o-o}^{e-\mathrm{PCM-OCF}}\cdot S_e^{\mathrm{PCM}}$.

Fig. 15 shows the measured (solid lines) and estimated (dashed lines) open-loop (red) and closed-loop (blue) output impedances of the PCM-OCF-controlled buck converter. The figure shows that measured and estimated impedances match each other quite well.

Fig. 16 shows the measured (top) and estimated (bottom) output-voltage response to a step change in the output current. The figure shows that the measured and estimated load-transient responses match each other quite well. As discussed

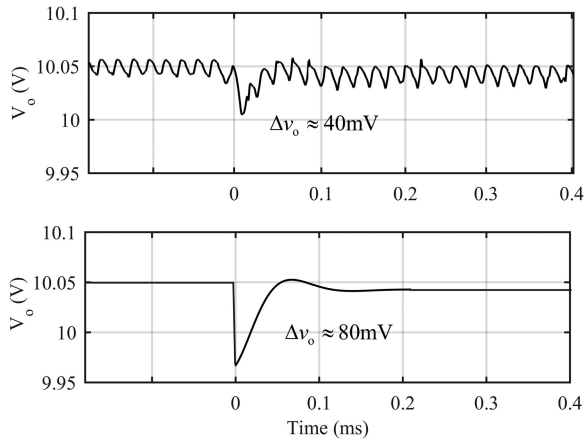

Fig. 16. (Top) Measured and (bottom) estimated output-voltage load transient of the PCM-OCF-controlled buck converter at the input voltage of 50 V.

in Section II-C, the settling process is determined together by the open-loop system high-frequency pole and the closed-loop system time constant [cf., (24)]. As discussed earlier, the dip of the output voltage should be higher than or equal to $r_C\Delta i_o$ (i.e., ≥ 80 mV) as visible at the estimated transient response (bottom figure). The measured transient response shows only half the minimum dip, which is caused by the used filtering of the measured data removing the high-frequency information from the data.

D. Discussions

The small magnitude of the low-frequency closed-loop output impedance implies a short settling time of the transient as well (cf., Figs. 6 and 7), as discussed in [27, pp. 291–304]. The settling time depends actually on the ability of the control system to maintain a high duty-ratio value during the transient. The PCM-OCF-controlled converter has the best ability due to the high-bandwidth output-current feedforward although its controller equals the controller of the PCM-controlled converter. The location of the controller zeros and the feedback-loop crossover frequency affect the behavior of the duty ratio, which is visible as the change in the low-frequency magnitude of the feedback loop (i.e., the higher the low-frequency magnitude, the faster is the transient settling).

The settling process of the PCM-controlled converter can be accelerated by placing the zero of the controller to a higher frequency than used in the experimental converter (i.e., $\omega_z \approx 0.25 \cdot 1/\sqrt{LC}$).

VI. Conclusion

This article provided methods to estimate the closed-loop output impedance of a buck converter under DDR, PCM, and PCM-OCF controls based on the method provided by the classical control engineering as well as on an innovative method to estimate the open-loop output impedance. The methods are equally applicable to any second-order converter. The classical control engineering provides a simple method to estimate the sensitivity function based on the feedback-loop crossover frequency and phase margin. Thus, the closed-loop output impedance can be estimated with a rather low-order estimate (i.e., the number of poles), and therefore, the output-voltage load transient can be easily expressed as an analytic time-domain function. This time-domain function will provide explicit information on the factors, which affects the transient behavior as explicitly demonstrated in this article. All the elements in the given response functions can be expressed in an analytic form based on the set of equations given in Appendix.

Appendix

$$\begin{cases} A + C = 1 \\ A \cdot (\omega_{n-o} + 2\zeta_e\omega_{n-e}) + B + C \cdot 2\omega_{n-o} + D \\ \quad = \omega_{zL} + \omega_{zC} + 2\zeta_e\omega_{n-e} \\ A \cdot (\omega_{n-e}^2 + 2\zeta_e\omega_{n-e}\omega_{n-o}) + B \cdot 2\zeta_e\omega_{n-e} + C \cdot \omega_{n-o}^2 \\ \quad + D \cdot 2\omega_{n-o} = \omega_{zL}\omega_{zC} + (\omega_{zL} + \omega_{zC})2\zeta_e\omega_{n-e} \\ A \cdot \omega_{n-o}\omega_{n-e}^2 + B \cdot \omega_{n-e}^2 + D \cdot \omega_{n-o}^2 = \omega_{zL}\omega_{zC}2\zeta_e\omega_{n-e} \end{cases} \tag{A.1}$$

$$\begin{cases} A + B + C = 1 \\ A \cdot (\omega_{z2} + 2\zeta_e\omega_{n-e}) + B(\omega_{z1} + 2\zeta_e\omega_{n-e}) \\ \quad + C \cdot (\omega_{z1} + \omega_{z2}) + D = \omega_{zL} + \omega_{zC} + 2\zeta_e\omega_{n-e} \\ A \cdot (\omega_{n-e}^2 + 2\zeta_e\omega_{n-e}\omega_{z2}) + B \cdot \left(\omega_{n-e}^2 + 2\zeta_e\omega_{n-e}\omega_{z1}\right) \\ \quad + C \cdot \omega_{z1}\omega_{z2} + D \cdot (\omega_{z1} + \omega_{z2}) = \omega_{zL}\omega_{zC} + (\omega_{zL} \\ \quad + \omega_{zC})2\zeta_e\omega_{n-e} \\ A \cdot \omega_{z2}\omega_{n-e}^2 + B \cdot \omega_{z1}\omega_{n-e}^2 + D \cdot \omega_{z1}\omega_{z2} \\ \quad = \omega_{zL}\omega_{zC}2\zeta_e\omega_{n-e} \end{cases} \tag{A.2}$$

$$\begin{cases} A + B = 1 \\ A \cdot 2\zeta_e\omega_{n-e} + B \cdot \omega_z + C = \omega_{zC} + 2\zeta_e\omega_{n-e} \\ A \cdot \omega_{n-e}^2 + C \cdot \omega_z = \omega_{zC}2\zeta_e\omega_{n-e} \end{cases} \tag{A.3}$$

$$\begin{cases} A + B + C = 1 \\ A \cdot 2(\zeta_o\omega_{n-o} + \zeta_e\omega_{n-e}) + B \cdot \left(2\zeta_e\omega_{n-e} + \frac{\omega_{n-o}}{2\zeta_o}\right) \\ \quad + C \cdot \frac{\omega_{n-o}}{2\zeta_o}(1 + 4\zeta_o^2) + D = \omega_{zL} + \omega_{zC} + 2\zeta_e\omega_{n-e} \\ A \cdot (\omega_{n-e}^2 + 4\zeta_e\omega_{n-e}\zeta_o\omega_{n-o}) + B \cdot \left(\omega_{n-e}^2 + \frac{\zeta_e\omega_{n-e}\omega_{n-o}}{\zeta_o}\right) \\ \quad + C \cdot \omega_{n-o}^2 + D \cdot \frac{\omega_{n-o}}{2\zeta_o}(1 + 4\zeta_o^2) = \omega_{zL}\omega_{zC} + (\omega_{zL} \\ \quad + \omega_{zC})2\zeta_e\omega_{n-e} \\ A \cdot 2\omega_{n-e}^2\zeta_o\omega_{n-o} + B \cdot \frac{\omega_{n-e}^2\omega_{n-o}}{2\zeta_o} + D \cdot \omega_{n-o}^2 \\ \quad = \omega_{zL}\omega_{zC}2\zeta_e\omega_{n-e}. \end{cases} \tag{A.4}$$

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