High-Efficiency Hybrid Dual-Path Step-Up DC–DC Converter With Continuous Output-Current Delivery for Low Output Voltage Ripple

Se-Un Shin, *Member, IEEE*, Sung-Wan Hong, *Member, IEEE*, Hyung-Min Lee, *Member, IEEE*, and Gyu-Hyeong Cho, *Fellow, IEEE*

***Abstract*—This article proposes a new boost converter topology called dual-path step-up dc–dc converter (DPUC). Unlike the conventional boost converter (CBC), the DPUC has a hybrid structure using one inductor and one flying capacitor to make dual current delivery paths. This allows continuous current delivering to the output, reducing both the dc level of the inductor current and the output voltage ripple. Therefore, the DPUC has higher efficiency and smaller output voltage ripple than those of the CBC. In addition, the feedforward characteristic of the flying capacitor can alleviate the effect of right-half-plane zero that degrades the transient response. Even with the inductor dc resistance of 200 mΩ, the DPUC achieves a high efficiency of 95.2% and a small ripple of up to 15 mV.**

***Index Terms*—Boost converter, dc resistance (DCR), dual-path step-up dc–dc converter (DPUC), output delivery current, output voltage ripple, right-half-plane zero (RHP-zero).**

I. Introduction

In RECENT years, as the use of mobile devices with a high functionality increases, a longer battery time is highly desired [1]–[4]. Accordingly, the power management integrated circuit (PMIC) with high efficiency is in the spotlight. As shown in Fig. 1, the PMIC transfers the power from the battery to the loading blocks while converting the battery voltage to the adoptable supply voltages for the loads. Since many high-performance loading blocks are required in the mobile devices, the PMIC should support a large load current ($I_{\rm LOAD}$), so-called, a heavy load condition. In the PMIC, the switched-mode power supplies, such as the buck and boost converters are generally used because these converters have lower power losses than any other PMICs under heavy load condition [5]. However, there are two critical issues in industrial applications when the converters operate under heavy load condition. First, since a number of small inductors, which have a relatively large parasitic dc resistance ($R_{\rm DCR}$), should be used in the mobile devices, the conduction loss ($P_{\rm DCR}$) dissipated at the $R_{\rm DCR}$ significantly degrades the efficiency that leads to the serious heat problem. This $P_{\rm DCR}$ is given by

$$P_{\rm DCR} = {i_{L,\rm rms}}^2 R_{\rm DCR} = \left({I_L}^2 + \frac{{\Delta i_L}^2}{12} \right) R_{\rm DCR} \quad (1)$$

where $i_{L,\rm rms}$, I_L, and Δi_L are the root-mean-square value, the dc component, and the ripple of the i_L, respectively. To reduce the $P_{\rm DCR}$, the easiest solution is using a bulky-size inductor having a small $R_{\rm DCR}$. However, the bulky-size inductor is not preferred due to the strict size limitation of the mobile device. Therefore, reducing the $i_{L,\rm rms}$ can be considered as the alternate solution for high efficiency.

The other issue is the large output ripple voltage Δv_O with switching noise $\Delta v_{\rm SWN}$ that degrades the performance of the loading block [7], [8]. To reduce both Δv_O and $\Delta v_{\rm SWN}$, a large output capacitor with a small effective series resistor $R_{\rm ESR}$ or an additional large buffering capacitor are required on the printed circuit board (PCB) or inside the chip. However, it increases

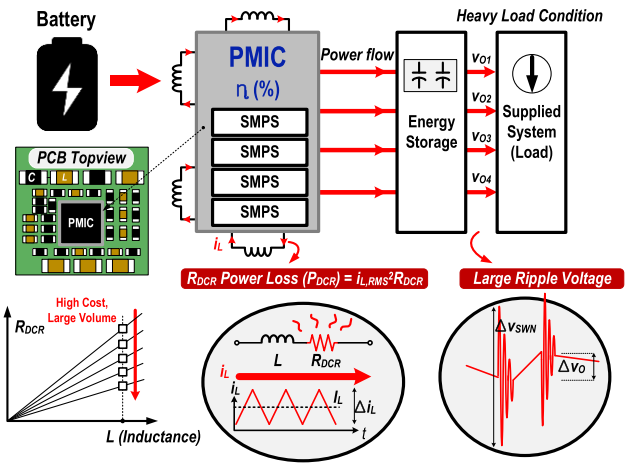

Fig. 1. Conceptual architecture and issues of PMICs in heavy load condition.

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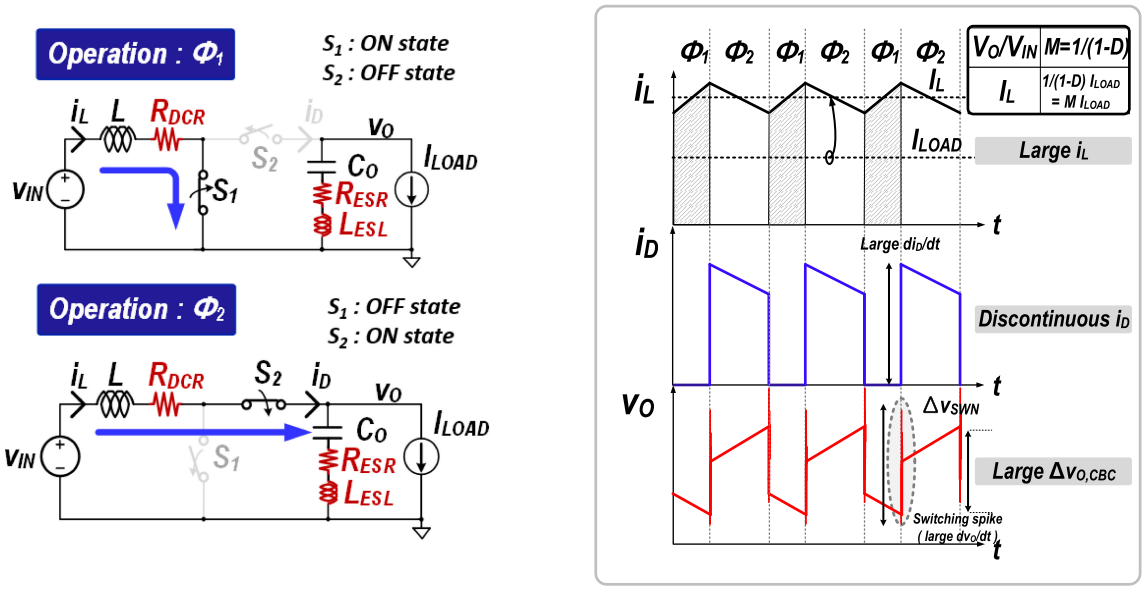


Fig. 2. Operation and timing diagram of the conventional dc–dc boost converter.

the manufacturing cost, which is also not preferred in industry applications.

These issues are considered critical in the conventional boost converter (CBC), as shown in Fig. 2, which is used to increase the supply voltage in a variety of applications, such as light-emitting diode drivers and liquid crystal display bias circuits [9]–[11], [20]–[23]. Unlike the charge pump that has the complex switching network for various configurations [17]–[19], the CBC has a simple topology, which consists of one inductor (L), one output capacitor (C_O), and two power switches (S_1 and S_2). The CBC operates on two phases, Φ_1 and Φ_2. In Φ_1, S_1 turns ON and S_2 turns OFF to build up the i_L. Conversely, in Φ_2, S_1 turns OFF and S_2 turns ON to transfer the i_L to the output. In this operation, the CBC transfers the i_L to the output only during Φ_2; thus, the output delivery current i_D is not continuous. Because of the discontinuous i_D, the aforementioned issues with large $P_{\rm DCR}$, Δv_O, and $\Delta v_{\rm SWN}$ become more severe especially under the heavy load condition. In addition, another issue of the right-half-plane (RHP) zero degrades the performance of the CBC. These issues are explained in detail as follows.

A. Large Inductor Current

Since the average value of i_D must be equal to the $I_{\rm LOAD}$, the I_L becomes larger than the $I_{\rm LOAD}$ as Φ_1 increases. To derive the I_L in CBC $I_{L,\rm CBC}$, the charge balance to the currents flowing through C_O is applied. The $I_{L,\rm CBC}$ is expressed as follows:

$$D\,(-I_{\rm LOAD}) + (1-D)(I_{L,\rm CBC} - I_{\rm LOAD}) = 0 \tag{2}$$

$$I_{L,\rm CBC} = \frac{1}{1-D} I_{\rm LOAD} = M_{\rm CBC} I_{\rm LOAD} (D = \Phi_1/T_S) \tag{3}$$

where D and $M_{\rm CBC}$ are the duty cycle and the voltage conversion ratio of CBC, which is the dc output voltage V_O over the dc input voltage $V_{\rm IN}$, respectively. In the CBC, $M_{\rm CBC}$ is 1/(1-D). Equation (3) shows that $I_{L,\rm CBC}$ becomes $M_{\rm CBC}$ times larger than the $I_{\rm LOAD}$. Accordingly, when this large $I_{L,\rm CBC}$ flows through the small L having a large $R_{\rm DCR}$, it could cause significant conduction loss $P_{\rm DCR}$. This not only lowers the efficiency but also causes the thermal problem in the device.

B. Large Output Voltage Ripple

As shown in Fig. 2, since the i_L is transferred to the output only during Φ_2, the i_D changes abruptly at the beginning and end of the Φ_2. Due to this large discontinuity of the i_D, the CBC has a very large output voltage ripple $\Delta v_{O,\rm CBC}$ compared with the buck converter that continuously transfers the i_L to the output [24]–[26]. Therefore, the bulky size C_O with small $R_{\rm ESR}$, which are not preferred in the industry, is required to minimize $\Delta v_{O,\rm CBC}$.

C. Large Switching Noise

In addition, the large discontinuity of i_D causes a large voltage spike ($\Delta v_{\rm SWN}$) due to the parasitic inductance ($L_{\rm ESL}$) component that is connected to the output capacitor in series. This $\Delta v_{\rm SWN}$ is given by

$$\Delta v_{\rm SWN} = L_{\rm ESL} \frac{di_D(t)}{dt}. \tag{4}$$

Since the $di_D(t)/dt$ is significantly large due to the discontinuity of the i_D, the $\Delta v_{\rm SWN}$ becomes also large, which degrades the performance of the loading block.

D. RHP-Zero

On the other hand, it is well known that the CBC has an RHP-zero effect that worsens the transient response [15]. This is because a temporarily opposite reaction occurs at the i_D when an $I_{\rm LOAD}$ changes. The RHP-zero of CBC ($w_{zp,\rm CBC}$) is expressed as

$$w_{zp,\rm CBC} = \frac{(1-D)^2 R}{L} = \frac{R}{{M_{\rm CBC}}^2 L} \tag{5}$$

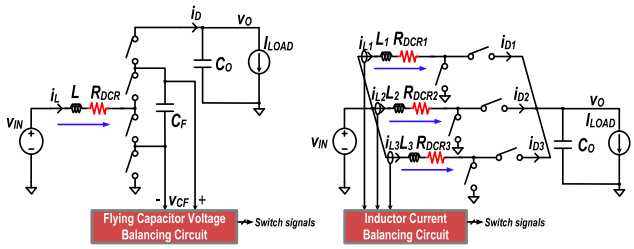


Fig. 3. Alternative boost topologies for reducing the conduction loss in R_{DCR}. (a) Multilevel boost converter. (b) Interleaved boost converter.

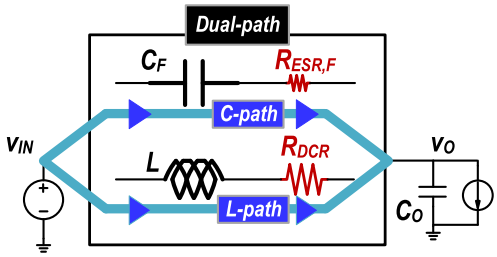


Fig. 4. Conceptual structure of the dual-path dc–dc converter.

where R is the output load resistance. From (5), since this RHP-zero is located at the low frequency under the heavy load condition with a large conversion ratio, we cannot ignore the effect of RHP-zero and have to consider it in the controller design.

There have been various attempts using the additional passive components to solve the issues noted above. In Fig. 3(a), a multilevel converter using the additional flying capacitor can reduce both Δi_L and Δv_O due to the reduced amplitude of the switching node voltage with an effectively increased switching frequency [12], [13]. However, even though Δi_L decreases, the effect of reducing $i_{L,\mathrm{rms}}$ is negligible under the heavy load condition because the I_L is dominant in the $i_{L,\mathrm{rms}}$. Moreover, since the current is still delivered to the output discontinuously, the Δv_O is not much decreased. Also, the complex controller for regulating the voltage across the flying capacitor should be additionally used [12]. On the other hand, an interleaved converter with additional inductors can reduce the I_L flowing through each inductor, which eventually reduces the P_{DCR}, as shown in Fig. 3(b). However, it requires additional inductors that are larger in size and higher in cost than the other passive components [14], [15]. Moreover, the current delivered to the output would be discontinuous, and an additional current balancing technique is required for each inductor.

To solve these issues in the heavy load condition with the small-size inductor, this article, an expanded version of the article presented in [16], proposes a new topology named a dual-path step-up dc–dc converter (DPUC). This article additionally includes the conduction loss analysis, the small-signal analysis for transfer function in different modes, and the detailed circuit description for the controller and gate drivers to fully analyze and characterize the proposed DPUC. As shown in Fig. 4, without adopting the interleaved structure that requires a complex balancing controller and additional inductors, the dual-path topology has two paths for the current with a hybrid structure using an inductor (L-path) and a flying capacitor (C-path), which makes the i_L low. Since the series parasitic resistance of the flying capacitor $R_{\mathrm{ESR},F}$ is generally much smaller than R_{DCR}, the conduction loss dissipated at C-path is also much smaller than that of the L-path. Owing to the lowered i_L by C-path, the P_{DCR} could decrease even when a larger R_{DCR} is adopted than that used in the CBC. In addition, Δv_O can be reduced owing to the continuous output delivery current i_D. Thus, the proposed DPUC can achieve better performance in heavy load conditions with the small-size inductor.

The rest of the article is organized as follows. In Section II, the concept of the proposed boost converter with the dual path is explained and analyzed. The controller implementation for the proposed boost converter is described in Section III. Measurement results and performance comparisons are presented in Section IV. Finally, a brief conclusion is provided in Section V.

II. Proposed Dual-Path Step-Up Converter

A. Proposed Topology

The DPUC consists of one inductor (L), an output capacitor (C_O), a flying capacitor (C_F), and five power switches (S_1–S_5), as shown in Fig. 5. In Φ_1, S_1 is turned ON to build up i_L. Simultaneously, S_3 and S_5 are turned ON and C_F is connected in series with C_O to form the C-path. Then, the energy is transferred to the output through C_F even though i_L is not delivered to the output during this period. In Φ_2, S_2 and S_4 are turned ON. Accordingly, L and C_F are connected in series to form an L-path. Thus, i_L can be delivered to the output through C_F. By repeating Φ_1 and Φ_2, the i_D of the DPUC can deliver the current to the output all the time.

The conversion ratio of the DPUC (M_{DPUC}) is expressed by the voltage-second balance on the inductor as follows:

$$DV_{\mathrm{IN}} + (1-D)\,(2V_{\mathrm{IN}} - 2V_O) = 0 \tag{6}$$

$$M_{\mathrm{DPUC}} = \frac{2-D}{2(1-D)}, \quad (0 < D < 1). \tag{7}$$

In (7), since the duty cycle D varies from 0 to 1, M_{DPUC} can vary ideally from 1 to infinity. The range of the conversion ratio of the DPUC is the same as that of the CBC. Therefore, unlike the switched capacitor converter, which has the limitation of conversion ratio, the DPUC has a step-up characteristic without the limitation of the conversion ratio.

B. Reduced Inductor Current

The noted point of the operation in the DPUC is the current of C-path ($i_{C,\phi 1}$), which is a part of the flying capacitor current i_C in Φ_1, it is defined as

$$i_{C,\Phi 1} = I_0 e^{-\frac{t}{\tau}} \tag{8}$$

where τ is the time constant composed of both resistance and capacitance including C_F in the C-path. The charge balance of the C_F defines the coefficient I_0 of (8). In other words, both the average values of $i_{C,\phi 1}$ in C-path and $i_{C,\phi 2}$, which is the L-path current in Φ_2, should be the same in steady state, which

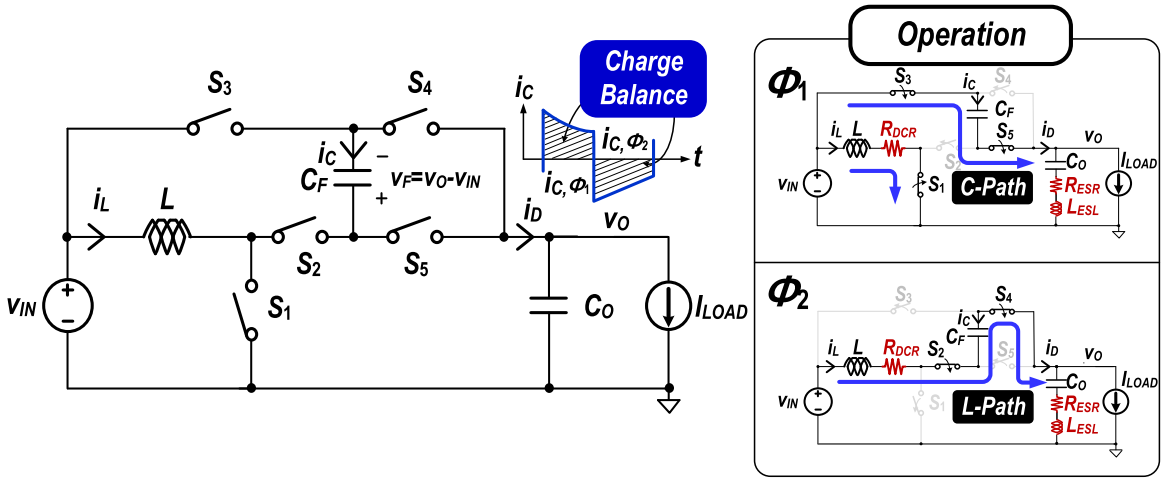


Fig. 5. Operation of the proposed dual-path dc–dc step-up converter.

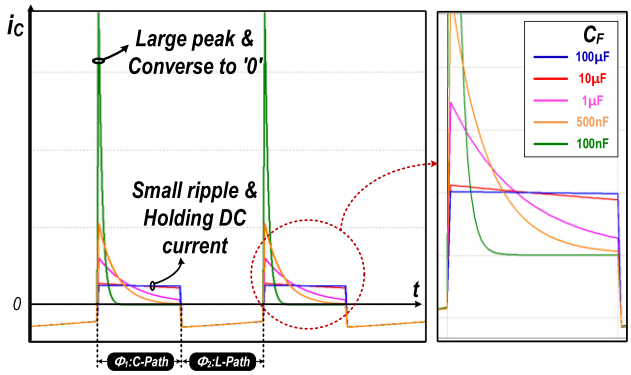


Fig. 6. Capacitor current simulation waveforms with different C_F values.

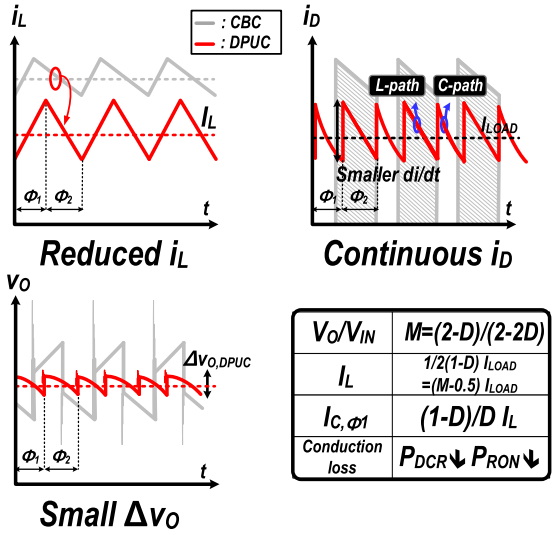


Fig. 7. Waveforms of the proposed dual-path dc–dc step-up converter.

is expressed as follows:

$$\int_0^{DT_S} i_{C,\Phi 1}(t)dt = \int_{DT_S}^{T_S} i_{C,\Phi 2}(t)dt$$

$$\int_0^{DT_S} I_0 e^{-\frac{t}{\tau}} dt = (1-D)I_L T_S$$

$$I_0 = \frac{(1-D)I_L T_S}{\tau(1-e^{-DT_S/\tau})}. \tag{9}$$

Substituting (9) into (8), $i_{C,\phi 1}$ is given by

$$i_{C,\Phi 1} = \frac{(1-D)I_L T_S}{\tau(1-e^{-DT_S/\tau})} e^{-\frac{t}{\tau}}. \tag{10}$$

As shown in (10), it can be noted that $i_{C,\phi 1}$ depends on the time constant τ. If τ is very small, the *C*-path of DPUC operates similar to the charge pump, which has a large peak current due to charge sharing [19]. However, since the goal of the *C*-path is making continuous i_D, it is preferred to adopt a large τ for holding the dc current. Therefore, the large C_F is required for the large τ.

However, since the capacitance is related to the volume, it is important to choose an optimum capacitance of C_F. Fig. 6 shows the effect of τ in $i_{C,\phi 1}$ as simulation results. As mentioned above, since $i_{C,\phi 1}$ depends on C_F, when the value of C_F is low, $i_{C,\phi 1}$ has the large peak at the start and converses to zero current at the end. However, the larger C_F is selected, the smaller the ripple of $i_{C,\phi 1}$ and it holds dc current even at the end of the phase. On the other hand, when the large C_F over an optimum value is used, the effect of reducing the ripple of $i_{C,\phi 1}$ is getting low. Therefore, in this article, we chose 10 μF as the optimum value of C_F.

Fig. 7 shows the waveforms of the DPUC to explain its advantages visually. In terms of i_L, the *C*-path of the DPUC reduces the i_L because this path makes the i_D continuous.

From the charge balance of the C_F, the relationship between the average value of the $i_{C,\phi 1}$ ($I_{C,\phi 1}$) and the dc value of the i_L in the DPUC ($I_{L,\mathrm{DPUC}}$) is expressed as

$$I_{C,\Phi 1} = \frac{1-D}{D} I_{L,\mathrm{DPUC}}. \tag{11}$$

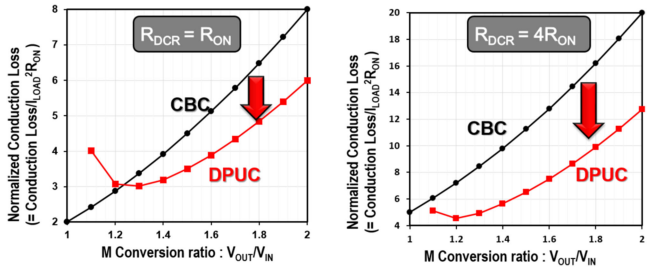


Fig. 8. Comparison of the conduction loss in the case of (a) $R_{\mathrm{DCR}} = R_{\mathrm{ON}}$ and (b) $R_{\mathrm{DCR}} = 4R_{\mathrm{ON}}$.

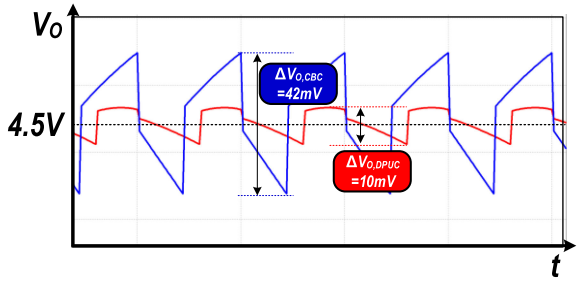


Fig. 9. Simulation results of $\Delta v_{O,\mathrm{CBC}}$ and $\Delta v_{O,\mathrm{DPUC}}$ on the same operating condition.

Using (11), the charge balance of C_O is considered as follows:

$$D\left(I_{C,\Phi 1} - I_{\mathrm{LOAD}}\right) - (1-D)\left(I_{L,\mathrm{DPUC}} - I_{\mathrm{LOAD}}\right) = 0 \tag{12}$$

$$I_{L,\mathrm{DPUC}} = \frac{1}{2-2D} I_{\mathrm{LOAD}} = \left(M_{\mathrm{DPUC}} - \frac{1}{2}\right) I_{\mathrm{LOAD}}. \tag{13}$$

As shown in (13), $I_{L,\mathrm{DPUC}}$ is reduced to (M_{DPUC}-1/2) I_{LOAD} lower than $I_{L,\mathrm{CBC}}$, which is M_{CBC} I_{LOAD} at the same operating condition. Using these results, the conduction loss of the CBC ($P_{\mathrm{cond,CBC}}$) and the conduction loss of the DPUC ($P_{\mathrm{cond,DPUC}}$) with the same conversion ratio (M) are compared as follows:

$$P_{\mathrm{cond,CBC}} = M^2 {I_{\mathrm{LOAD}}}^2 (R_{\mathrm{ON}} + R_{\mathrm{DCR}}) \tag{14}$$

$$\begin{aligned} P_{\mathrm{cond,DPUC}} &= (M-0.5)^2 {I_{\mathrm{LOAD}}}^2 \left(DR_{\mathrm{ON}} + 2(1-D)R_{\mathrm{ON}} \right. \\ &\quad \left. + 2\frac{(1-D)^2}{D} R_{\mathrm{ON}} + R_{\mathrm{DCR}} \right) \\ &= (M-0.5)^2 {I_{\mathrm{LOAD}}}^2 \left(2R_{\mathrm{ON}} - \frac{2M-2}{2M-1} R_{\mathrm{ON}} \right. \\ &\quad \left. + \frac{1}{(2M-1)(M-1)} R_{\mathrm{ON}} + R_{\mathrm{DCR}} \right). \end{aligned} \tag{15}$$

In this analysis, the ripple of the current is ignored because the dc component of the current is dominant to the conduction loss under the heavy load condition. In addition, the ON-resistance of switches is equal to R_{ON} for the simple analysis.

In Fig. 8, the conduction loss is compared with a normalized conduction loss divided by ${I_{\mathrm{LOAD}}}^2 R_{\mathrm{ON}}$. In the case that R_{DCR} is equal to R_{ON}, Fig. 8(a) shows that the conduction loss of the DPUC is lower than that of the CBC from when the conversion ratio M is higher than 1.2. Also, as the larger the R_{DCR} is used, such as four times R_{ON}, the greater the difference in conduction losses between the DPUC and CBC is caused, as shown in Fig. 8(b).

Intuitively, the conduction loss is proportional to the resistance and the square of the current. Therefore, the conduction loss is more sensitive to the current level than the resistance of the switch. Since the DPUC has two current paths to reduce the current level flowing through each path, which is the key point of the DPUC, its conduction loss can be less than that of the CBC even though DPUC has more power switches, leading to higher efficiency than the CBC in heavy load conditions.

C. Reducing Output Voltage Ripple and Switching Noise

The continuous i_D reduces the output voltage ripple of the DPUC $\Delta v_{O,\mathrm{DPUC}}$. In Fig. 9, the simulation result shows the comparison of Δv_O without Δv_{SWN} at $V_{\mathrm{IN}} = 2.5$ V, $V_O = 4.5$ V, $I_{\mathrm{LOAD}} = 500$ mA, $C_O = 10\,\mu$F, $T_S = 1\,\mu$s, and $R_{\mathrm{ESR}} = 30$ mΩ. Under this operating condition, $\Delta v_{O,\mathrm{CBC}}$ is 42 mV, while $\Delta v_{O,\mathrm{DPUC}}$ is 10 mV. Also, since the di_D/dt of the DPUC is significantly smaller than the di_D/dt of the CBC owing to the continuous i_D, we can expect that the Δv_{SWN} generated by L_{ESL} is greatly reduced.

D. Derivation of Transfer Function

The state-space averaging method is used to obtain the steady-state value and the small-signal models of the DPUC. Based on the two-phase operation of the DPUC in Fig. 5, three equations can be obtained according to the current and voltage relationships of the energy storing elements. In Φ_1

$$\frac{dv_O(t)}{dt} = \frac{v_{\mathrm{IN}}(t) - v_F(t) - v_O(t)}{r_F C_O} - \frac{v_O(t)}{RC_O} \tag{16}$$

$$\frac{dv_F(t)}{dt} = \frac{v_{\mathrm{IN}}(t) - v_F(t) - v_O(t)}{r_F C_O} \tag{17}$$

$$\frac{di_L(t)}{dt} = \frac{1}{L} v_{\mathrm{IN}}(t) \tag{18}$$

where v_{IN}, v_F, and r_F are the input voltage, the voltage across the C_F, and the parasitic resistance of the C-path including both R_{ESR} of the C_F and ON-resistance of the power switches, respectively.

To represent in matrix form, two vectors are identified as

State vector: $x = \begin{bmatrix} v_o(t) \\ v_F(t) \\ i_L(t) \end{bmatrix}$ and input vector: $u = [v_{\mathrm{IN}}(t)]$.

Equations (16)–(18) can be written as

$$\Phi_1 : \dot{x} = \boldsymbol{A_1} x + \boldsymbol{B_1} u \tag{19}$$

TABLE I
MATRICES FOR STATE-SPACE EQUATIONS

Matrices for State Equation	$\boldsymbol{A_1}=\begin{bmatrix}-(1/RC_O+1/r_FC_O) & -1/r_FC_O & 0\\ -1/r_FC_F & -1/r_FC_F & 0\\ 0 & 0 & 0\end{bmatrix}, \boldsymbol{A_2}=\begin{bmatrix}-1/RC_O & 0 & 1/C_O\\ 0 & 0 & -1/C_F\\ 1/L & 0 & -r_F/L\end{bmatrix}, \boldsymbol{B_1}=\begin{bmatrix}1/r_FC_O\\ 1/r_FC_F\\ 1/L\end{bmatrix}, \boldsymbol{B_2}=\begin{bmatrix}0\\ 0\\ 1/L\end{bmatrix}$
Steady-State Value	$x_0=\begin{bmatrix}V_O\\ V_F\\ I_L\end{bmatrix}=\begin{bmatrix}\frac{2(-2+D)DR}{-r_F-4(1-D)DR}V_{IN}\\ \frac{((-1+D)r_F-2D^2R)}{r_F+4(1-D)DR}V_{IN}\\ \frac{(-2+D)D}{(1-D)(-r_F-4(1-D)DR)}V_{IN}\end{bmatrix}\underset{(r_F=0)}{\simeq}\begin{bmatrix}\frac{(2-D)}{2(1-D)}V_{IN}\\ \frac{-D}{2(1-D)}V_{IN}\\ \frac{(2-D)}{4(1-D)^2R}V_{IN}\end{bmatrix}=\begin{bmatrix}MV_{IN}\\ (1-M)V_{IN}\\ (M-0.5)I_{LOAD}\end{bmatrix}, u_0=[V_{IN}]$
Matrices Calculated in Derivation	$\boldsymbol{A}=D\boldsymbol{A_1}+(1-D)\boldsymbol{A_2}=\begin{bmatrix}-(1/RC_O+D/r_FC_O) & -D/r_FC_O & (1-D)/C_O\\ -D/r_FC_F & -D/r_FC_F & -(1-D)/C_F\\ -(1-D)/L & (1-D)/L & -(1-D)r_F/L\end{bmatrix}, \boldsymbol{B}=D\boldsymbol{B_1}+(1-D)\boldsymbol{B_2}=\begin{bmatrix}D/r_FC_O\\ D/r_FC_F\\ 1/L\end{bmatrix}$ $\boldsymbol{E}=(\boldsymbol{A_1}-\boldsymbol{A_2})x_0+(\boldsymbol{B_1}-\boldsymbol{B_2})u_0=\begin{bmatrix}\frac{(-2+D)(-1+2D)}{C_O(-1+D)(r_F+4(1-D)DR)}V_{IN}\\ \frac{(-2+D)}{C_F(-1+D)(r_F+4(1-D)DR)}V_{IN}\\ \frac{1}{(1-D)L}V_{IN}\end{bmatrix}$

where

$$\boldsymbol{A}_1=\begin{bmatrix}-(1/RC_O+1/r_FC_O) & -1/r_FC_O & 0\\ -1/r_FC_O & -1/r_FC_O & 0\\ 0 & 0 & 0\end{bmatrix}$$

$$\boldsymbol{B}_1=\begin{bmatrix}1/r_FC_O\\ 1/r_FC_F\\ 1/L\end{bmatrix}$$

and $\dot{x}$ are the derivative matrices of x. According to the above method, the state equation in Φ_2 can also be derived as follows (all the matrices including both $\boldsymbol{A_2}$ and $\boldsymbol{B_2}$ are listed in Table I):

$$\Phi_2 : \dot{x}=\boldsymbol{A_2}x+\boldsymbol{B}_2u. \tag{20}$$

Using (19) and (20), the averaged state-space equation can be derived as

$$\begin{aligned}\dot{x}&=(D\boldsymbol{A_1}+(1-D)\boldsymbol{A_2})x+(D\boldsymbol{B_1}+(1-D)\boldsymbol{B_2})\\&=\boldsymbol{A}x+\boldsymbol{B}u.\end{aligned} \tag{21}$$

By applying the perturbation analysis [6], the state equation of the small-signal ac model is obtained

$$\dot{\hat{x}}=\boldsymbol{A}\hat{x}+\boldsymbol{B}\hat{u}+\boldsymbol{E}\hat{d} \tag{22}$$

where $\boldsymbol{E}=(\boldsymbol{A}_1-\boldsymbol{A}_2)\boldsymbol{x}_0+(\boldsymbol{B}_1-\boldsymbol{B}_2)u_0$ and perturbed quantities are the hatted letters, e.g., $\hat{d}$ is the perturbed quantity of D, and x_0 and u_0 are the steady-state values of two vectors x, u in Table I.

To easily derive a transfer function $G_{vd,\mathrm{DPUC}}(s)$ from duty D to the output voltage of the DPUC, the above state-space equation can be approximated as the second-order transfer function form while assuming r_F is negligible. The $G_{vd,\mathrm{DPUC}}(s)$ is given by

$$\begin{aligned}G_{vd,\mathrm{DPUC}}(s)&=\left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{u}=0,r_F=0}\\&=\frac{(4(1-D)^2R-(2-D)Ls)V_{\mathrm{IN}}}{2(1-D)^2(4(1-D)^2R+Ls+(C_O+C_F)LRs^2)}.\end{aligned} \tag{23}$$

The important parameters of $G_{vd,\mathrm{DPUC}}(s)$, such as low frequency gain $G_{d0,\mathrm{DPUC}}$, the double pole frequency $w_{0,\mathrm{DPUC}}$, quality factor Q_{DPUC}, and RHP-zero frequency $w_{zp,\mathrm{DPUC}}$, can be obtained from (23)

$$G_{d0,\mathrm{DPUC}}=\frac{V_{\mathrm{IN}}}{2(1-D)^2}=\frac{(2M-1)^2V_{\mathrm{IN}}}{2} \tag{24}$$

$$\begin{aligned}w_{0,\mathrm{DPUC}}&=\frac{2(1-D)}{\sqrt{L(C_F+C_O)}}\\&=\frac{2}{(2M-1)\sqrt{L(C_F+C_O)}}\end{aligned} \tag{25}$$

$$\begin{aligned}Q_{\mathrm{DPUC}}&=2(1-D)\sqrt{\frac{(C_F+C_O)R}{L}}\\&=\frac{2}{2M-1}\sqrt{\frac{(C_F+C_O)R}{L}}\end{aligned} \tag{26}$$

$$w_{zp,\mathrm{DPUC}}=\frac{4(1-D)^2R}{(-2+D)L}=\frac{2R}{M(2M-1)L}. \tag{27}$$

It is noticeable that both double pole and RHP-zero are higher than those of the CBC [6]. To compare the simplified model $G_{vd,\mathrm{DPUC}}(s)$ with the transfer function $G_{vd,\mathrm{CBC}}(s)$ from duty D to the output voltage in the CBC, the frequency responses are simulated at the given operating point ($V_{\mathrm{IN}}=2.8\,\mathrm{V}, V_O=4.2\,\mathrm{V}$, $R=7\,\Omega, L=4.7\,\mu\mathrm{H}, C_F=C_O=10\,\mu\mathrm{F}, r_F=0.1\,\Omega$, and R_{ON}

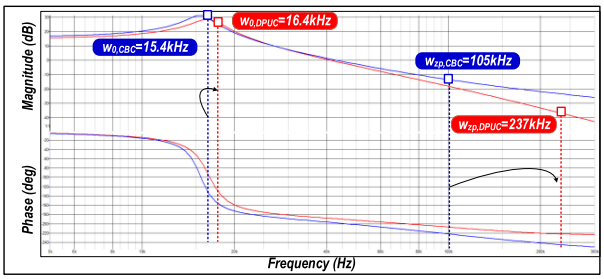


Fig. 10. Simulated $G_{vd}(s)$ bode plot of the DPUC and CBC.

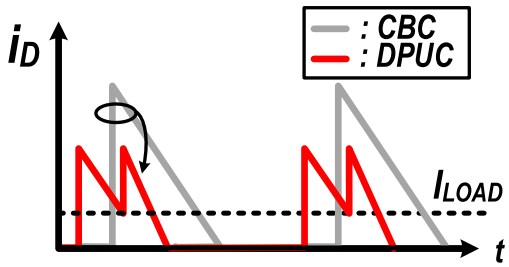


Fig. 11. Output delivery current of the DPUC and CBC in DCM.

is ignored), as shown in Fig. 10. From this figure, we can verify the simplified model $G_{vd,\mathrm{DPUC}}(s)$ and identify that the DPUC has two times higher RHP-zero than that of the CBC. Therefore, the DPUC could have a better transient response and an easier compensation than the CBC.

E. Discontinuous Conduction Mode (DCM)

Moreover, even in the DCM, since the two current paths with *C*-path and *L*-path exist the same as the continuous conduction mode (CCM), the DPUC can maintain the advantage that the current can be delivered to the output during the build-up time of the i_L. Therefore, as shown in Fig. 11, the DPUC in DCM also reduces the peak of the i_D and increases the efficiency.

III. Controller Implementation

Fig. 12 shows the top structure of the DPUC. The DPUC adopts the conventional peak current mode controller [6] by sensing the i_L that flows through S_1. Among the implemented blocks, we will discuss several important blocks in this section.

A. Three-Phase Mode Operation

1) Reduced Peak of Capacitor Current: The DPUC basically operates on the two-phase mode in the time domain with Φ_1 and Φ_2, as explained in Fig. 5. In the two-phase mode operation, the $I_{C,\Phi1}$ is determined by the duration of Φ_1 due to the charge balance of C_F. When Φ_1 is shorter, $I_{C,\Phi1}$ becomes higher, which increases the rms current reducing overall efficiency and increasing Δv_O. To maintain $I_{C,\Phi1}$ low even though the Φ_1 is very short, we insert the intermediate phase, Φ_3, between Φ_1 and Φ_2, as shown in Fig. 13. This is just an insertion of the operation phase in the time domain. There is no requirement

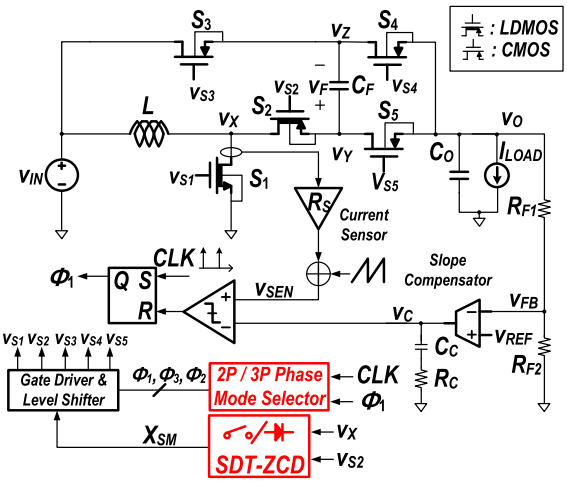


Fig. 12. Top structure of the DPUC.

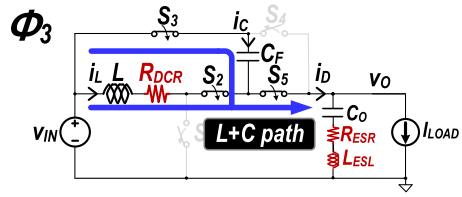


Fig. 13. Intermediate phase (Φ_3) for three-phase mode ($L + C$ path).

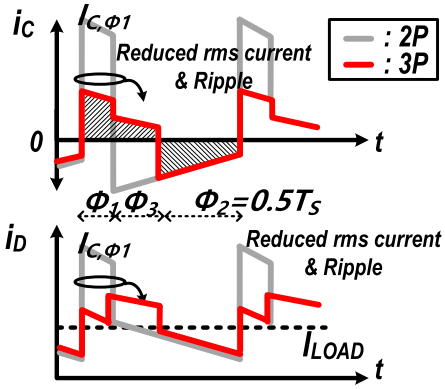


Fig. 14. Reduced peak of i_C and i_D in three-phase mode.

of the additional switches or passive components for this three-phase mode. Moreover, since all switches are turned ON and OFF once in a single period, the three-phase mode does not have additional switching losses compared with the two-phase mode. In Φ_3, switches S_2, S_3, and S_5 are turned ON at the same time to combine the *L*-path and the *C*-path so that the current can be delivered to the output ($L + C$ path). As shown in Fig. 14, if the charging time of the capacitor is the same as the discharging time of the capacitor when Φ_1 is short, $I_{C,\phi1}$ can be maintained as I_L based on (11). In other words, if $\Phi_1 + \Phi_3 = 0.5\,T_S$, both the forward current and the reverse current flow through C_F during $0.5\,T_S$. This means that the $I_{C,\Phi1}$ does not become high even though Φ_1 is very short in the three-phase mode. Therefore, this three-phase mode reduces the rms current. The conduction

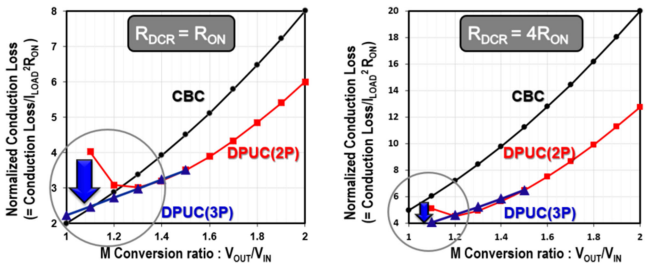


Fig. 15. Comparison of the conduction loss in the case of (a) $R_{\mathrm{DCR}} = R_{\mathrm{ON}}$ and (b) $R_{\mathrm{DCR}} = 4R_{\mathrm{ON}}$ for three-phase mode.

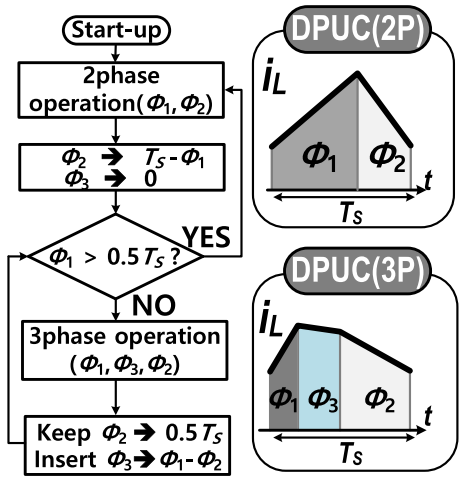


Fig. 16. Algorithm of phase-mode selector for three-phase mode operation.

loss of the DPUC in the three-phase mode ($P_{\mathrm{cond,DPUC\_3P}}$) is expressed as follows:

$$\begin{aligned} P_{\mathrm{cond,DPUC\_3P}} &= \left(\frac{M}{1.5}\right)^2 {I_{\mathrm{LOAD}}}^2(4 - 3D + R_{\mathrm{DCR}}) \\ &= \left(\frac{M}{1.5}\right)^2 {I_{\mathrm{LOAD}}}^2 \\ &\quad \times \left[\left(\frac{4.5}{M_{\mathrm{DPUC}}} - 0.5\right) R_{\mathrm{ON}} + R_{\mathrm{DCR}}\right]. \end{aligned} \tag{28}$$

From (28), $P_{\mathrm{cond,DPUC\_3P}}$ is compared with $P_{\mathrm{cond,CBC}}$ and $P_{\mathrm{cond,DPUC}}$ of the two-phase mode DPUC for two cases of $R_{\mathrm{DCR}} = R_{\mathrm{ON}}$ and $R_{\mathrm{DCR}} = 4R_{\mathrm{ON}}$, as shown in Fig. 15(a) and (b), respectively. Owing to the three-phase mode operation, the $P_{\mathrm{cond,DPUC\_3P}}$ can be reduced even when the conversion ratio M is low.

The phase mode selector, which operates with a simple algorithm, as shown in Fig. 16, automatically adjust the operation mode by comparing Φ_1 and 0.5 Ts.

2) Reduced Output Voltage Ripple: Owing to the three-phase mode operation, the reduced $I_{C,\Phi 1}$ maintains Δv_O smaller than $\Delta v_{O\_\mathrm{CBC}}$ even in low M condition. In Fig. 17, the simulation result shows the comparison of Δv_O without Δv_{SWN} at $V_{\mathrm{IN}} =$ 4 V, $V_O = 4.5$ V, $I_{I\mathrm{LOAD}} = 500$ mA, $C_O = 10\,\mu$F, $T_S = 1\,\mu$s,

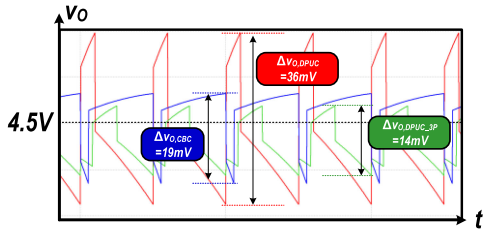


Fig. 17. Simulation results of $\Delta v_{O,\mathrm{CBC}}$, $\Delta v_{O,\mathrm{DPUC}}$, and $\Delta v_{O,\mathrm{DPUC\_3P}}$ on the same operating condition.

and $R_{\mathrm{ESR}} = 30\,\mathrm{m}\Omega$. Under this operating condition, $\Delta v_{O,\mathrm{DPUC}}$, which is the Δv_O of the two-phase mode, is larger than $\Delta v_{O,\mathrm{CBC}}$ because of short Φ_1, while Δv_O of three-phase mode DPUC $\Delta v_{O,\mathrm{DPUC\_3P}}$ is smaller than those of any other cases. Likewise, since the di_D/dt of the three-phase mode DPUC is smaller than those of both two-phase DPUC and CBC in low M condition, the Δv_{SWN} of the three-phase DPUC generated by L_{ESL} is also smaller than others.

The three-phase mode DPUC can also achieve better performance in low conversion ratio conditions than the two-phase DPUC, which has low performance, such as large output voltage ripple and conduction loss.

3) Derivation of Transfer Function in Three-Phase Mode: In the three-phase mode, the small-signal model is different from the two-phase mode. The state-space averaging method is used to obtain the steady-state value and small-signal models of the three-phase mode DPUC. The three-phase state equation of the DPUC can be derived by inserting Φ_3 to the two-phase state equation of the DPUC as follows (all the matrices for the three-phase mode DPUC are listed in Table II):

$$\Phi_3 : \dot{x} = \boldsymbol{A_3}x + \boldsymbol{B}_3 u. \tag{29}$$

Since the number of the state is three and the duty of Φ_2 (D_2) is $0.5T_S$ (0.5), the averaged state-space equation can be derived as

$$\begin{aligned} \dot{x} &= (D\boldsymbol{A_1} + (0.5 - D)\boldsymbol{A_3} + 0.5\boldsymbol{A_2})x \\ &\quad + (D\boldsymbol{B_1} + (0.5 - D)\boldsymbol{B}_3 + 0.5\boldsymbol{B_2})u \\ &= \boldsymbol{A}x + \boldsymbol{B}u. \end{aligned} \tag{30}$$

Applying the perturbation analysis

$$\dot{\hat{x}} = \boldsymbol{A}\hat{x} + \boldsymbol{B}\hat{u} + \boldsymbol{E}\hat{d} \tag{31}$$

where $\boldsymbol{E} = (\boldsymbol{A_1} - \boldsymbol{A_3})x_0 + (\boldsymbol{B_1} - \boldsymbol{B}_3)u_0$.

To easily derive a transfer function $G_{vd,\mathrm{DPUC\_3P}}(s)$ from duty D to the output voltage of the three-phase mode DPUC, the above equation can be approximated as the second order transfer function form as follows:

$$\begin{aligned} &G_{vd,\mathrm{DPUC\_3P}}(s) \\ &= \left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{u}=0, r_F=0} \\ &= \frac{24V_{\mathrm{IN}}(R - \frac{L}{(1.5-D)^2}s)}{((1.5 - D)^2 R + Ls + (C_O + C_F)LRs^2)}. \end{aligned} \tag{32}$$

TABLE II
MATRICES FOR THE STATE-SPACE EQUATIONS OF THE THREE-PHASE MODE DPUC

Matrices for State Equation	$\boldsymbol{A}_1=\begin{bmatrix}-(1/RC_O+1/r_FC_O) & -1/r_FC_O & 0\\ -1/r_FC_F & -1/r_FC_F & 0\\ 0 & 0 & 0\end{bmatrix}, \boldsymbol{A}_2=\begin{bmatrix}-1/RC_O & 0 & 1/C_O\\ 0 & 0 & -1/C_F\\ 1/L & 0 & -r_F/L\end{bmatrix}, \boldsymbol{A}_3=\begin{bmatrix}-1(1/RC_O+1/r_FC_O) & -1/r_FC_O & 1/C_O\\ -1/r_FC_F & -1/r_FC_F & 0\\ -1/L & 0 & 0\end{bmatrix}, \boldsymbol{B}_1=\begin{bmatrix}1/r_FC_O\\ 1/r_FC_F\\ 1/L\end{bmatrix}, \boldsymbol{B}_2=\begin{bmatrix}0\\ 0\\ 1/L\end{bmatrix}, \boldsymbol{B}_3=\begin{bmatrix}1/r_FC_O\\ 1/r_FC_F\\ 1/L\end{bmatrix}$
Steady-State Value	$x_0=\begin{bmatrix}V_O\\ V_F\\ I_L\end{bmatrix}=\begin{bmatrix}\frac{3(3-2D)RV_{IN}}{4r_F+(3-2D)^2R}\\ -\frac{2V_{IN}(r_F+(3-2D)DR)}{4r_F+(3-2D)^2R}\\ \frac{6V_{IN}}{4r_F+(3-2D)^2R)}\end{bmatrix}\underset{(r_F=0)}{\simeq}\begin{bmatrix}\frac{3}{3-2D}V_{IN}\\ -\frac{2D}{3-2D}V_{IN}\\ \frac{6}{(3-2D)^2R}V_{IN}\end{bmatrix}=\begin{bmatrix}MV_{IN}\\ (1-M)V_{IN}\\ \frac{2M}{3}I_{LOAD}\end{bmatrix}, u_0=V_{IN}$
Matrices Calculated in Derivation	$\boldsymbol{A}=D\boldsymbol{A}_1+(0.5-D)\boldsymbol{A}_3+0.5\boldsymbol{A}_2=\begin{bmatrix}-(1/2r_FC_O+1/RC_O) & -1/2r_FC_O & (1-D)/C_O\\ -1/2r_FC_F & -1/2r_FC_F & -1/2C_F\\ -(1-D)/L & 1/2L & -r_F/2L\end{bmatrix}, \boldsymbol{B}=D\boldsymbol{B}_1+(0.5-D)\boldsymbol{B}_3+\boldsymbol{B}_2=\begin{bmatrix}1/2r_FC_O\\ 1/2r_FC_F\\ 1/L\end{bmatrix}$ $\boldsymbol{E}=(\boldsymbol{A}_1-\boldsymbol{A}_3)x_0+(\boldsymbol{B}_1-\boldsymbol{B}_3)u_0=\begin{bmatrix}-\frac{6V_{IN}}{C_O(4r+(3-2D)^2R)}\\ 0\\ \frac{3(3-2D)RV_{IN}}{4r_FL+(3-2D)^2LR}\end{bmatrix}$

Important parameters of $G_{vd,\mathrm{DPUC\_3P}}(s)$, such as low frequency gain $G_{d0,\mathrm{DPUC\_3P}}$, the double pole frequency $w_{0,\mathrm{DPUC\_3P}}$, quality factor $Q_{\mathrm{DPUC\_3P}}$, and RHP-zero frequency $w_{zp,\mathrm{DPUC\_3P}}$, are obtained as follows:

$$G_{d0,\mathrm{DPUC\_3P}}=\frac{24V_{\mathrm{IN}}}{(1.5-D)^2}=\frac{32}{3}M^2V_{\mathrm{IN}} \tag{33}$$

$$w_{0,\mathrm{DPUC\_3P}}=\frac{(1.5-D)}{\sqrt{L(C_F+C_O)}}=\frac{3}{2M\sqrt{L(C_F+C_O)}} \tag{34}$$

$$Q_{\mathrm{DPUC\_3P}}=(1.5-D)\sqrt{\frac{(C_F+C_O)R}{L}}=\frac{3}{2M}\sqrt{\frac{(C_F+C_O)R}{L}} \tag{35}$$

$$w_{zp,\mathrm{DPUC\_3P}}=\frac{(1.5-D)^2R}{L}=\frac{9}{4}\frac{R}{M^2L}. \tag{36}$$

From (5), (27), and (36), we can identify that the RHP-zero of the three-phase DPUC $w_{zp,\mathrm{DPUC\_3P}}$ is higher than those of both CBC and two-phase mode DPUC. To verify this simplified model $G_{vd,\mathrm{DPUC\_3P}}(s)$ of the DPUC and comparing with both $G_{vd,\mathrm{DPUC}}(s)$ and $G_{vd,\mathrm{CBC}}(s)$, the frequency responses are simulated at a given operating point ($V_{\mathrm{IN}}=4$ V, $V_O=4.5$ V, $R=7\,\Omega$, $L=4.7\,\mu$H, $C_F=C_O=10\,\mu$F, $r_F=0.1\,\Omega$, and R_{ON} is ignored), as shown in Fig. 18.

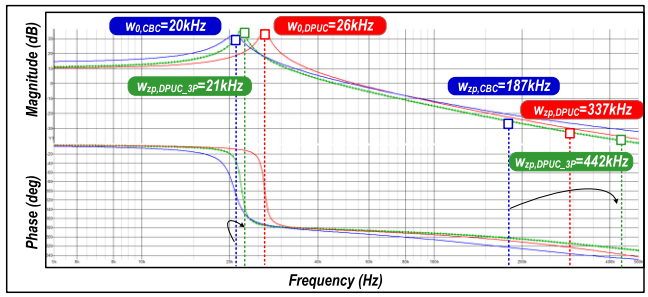


Fig. 18. Simulated $G_{vd}(s)$ bode plot of the CBC and DPUC with different modes.

B. Gate Driving Technique

The gate drivers of S_1, S_3, and S_4 switches can be implemented with a conventional gate driver (CGD). S_2 and S_5 require a special gate driver due to the higher voltage $2V_O-V_{\mathrm{IN}}$ than the output voltage V_O. First, the gate driver for S_2 is shown in Fig. 19(a). A bias current I_{CLAMP} generates appropriate V_{CLAMP} that protects the S_2 from the breakdown. Clamping transistor M_{CLAMP} limits the lower voltage of the S_2 gate driver in discharging the gate voltage of S_2.

Fig. 19(b) shows the gate driver for S_5 which is modified from a dynamic gate controller (DGC) of [3]. In this driver, we used a simple logic gate and eliminated a bootstrap technique that requires a large bootstrap capacitor. S_5 is turned ON with 0 V by the CGD through the transmission gate (TX) in Φ_1 and Φ_3. In contrast, when v_Y becomes $2V_O-V_{\mathrm{IN}}$ in Φ_2, CGD cannot turn S_5 OFF. To fully turn the S_5 OFF, M_H is added in this gate driver for S_5. This M_H enables to turn the S_5 OFF by connecting v_Y the gate of S_5. At this time, TX is turned OFF in Φ_2 to eliminate the current path of CGD. Thus, since this DGC uses internal voltage v_Y, it can be implemented without the external voltage or bootstrap technique.

C. Zero-Current Detection (ZCD) for DCM Control

The DPUC in DCM has the same operation phases Φ_1 and Φ_2 as in the CCM. It also has the same advantages that $i_{C,\Phi1}$ can flow to the output even during the build-up time of the i_L,

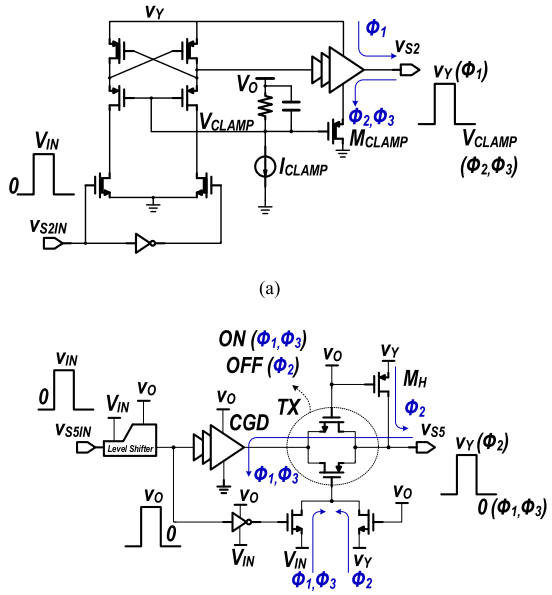


Fig. 19. Gate drivers for (a) S_2 and (b) S_5.

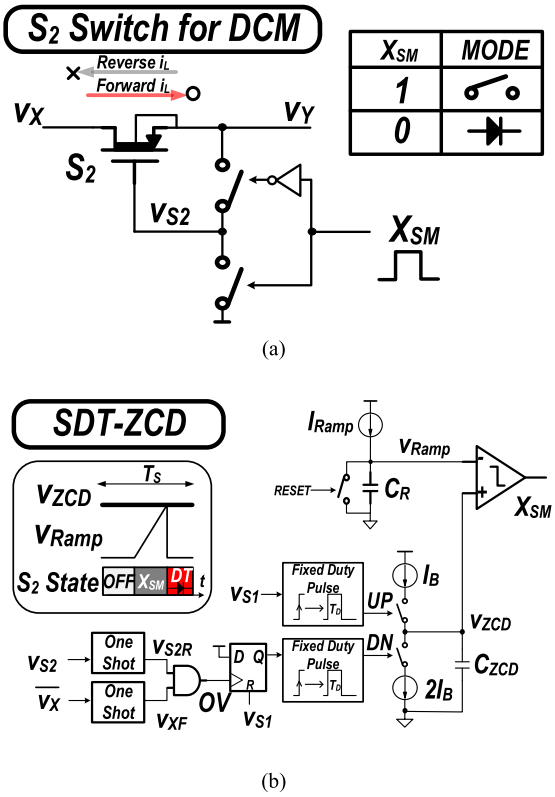


Fig. 20. (a) Mode of switch S_2 for (a) ZCD and (b) SDT-ZCD circuit.

reducing the peak of i_D. The difference between CCM and DCM is only that the converter has the OFF-state, in which all the power switches are turned OFF, when the i_L becomes zero. For this DCM operation, there is a technique to compare the voltage across the switch to perform the ZCD of the i_L [20]–[22]. However, this approach results in an inaccurate

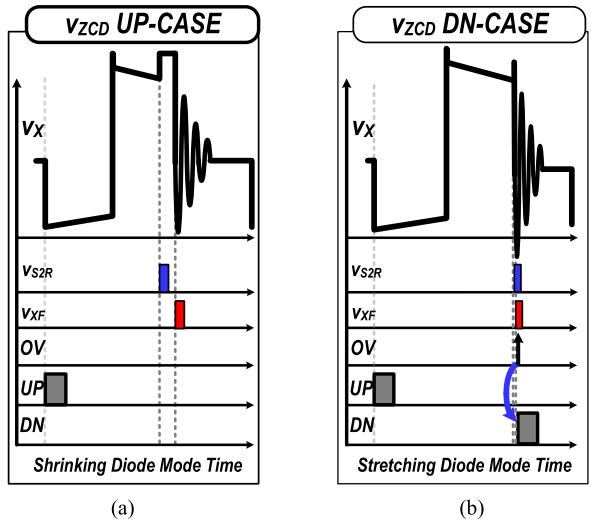


Fig. 21. Waveform of (a) up case and (b) down case for STD-ZCD.

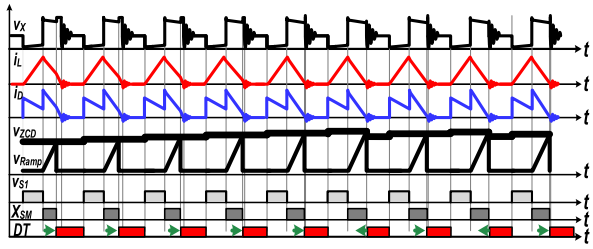
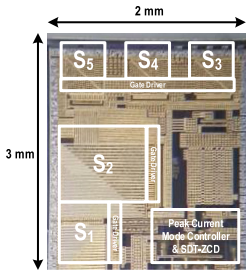


Fig. 22. Timing diagram of SDT-ZCD.

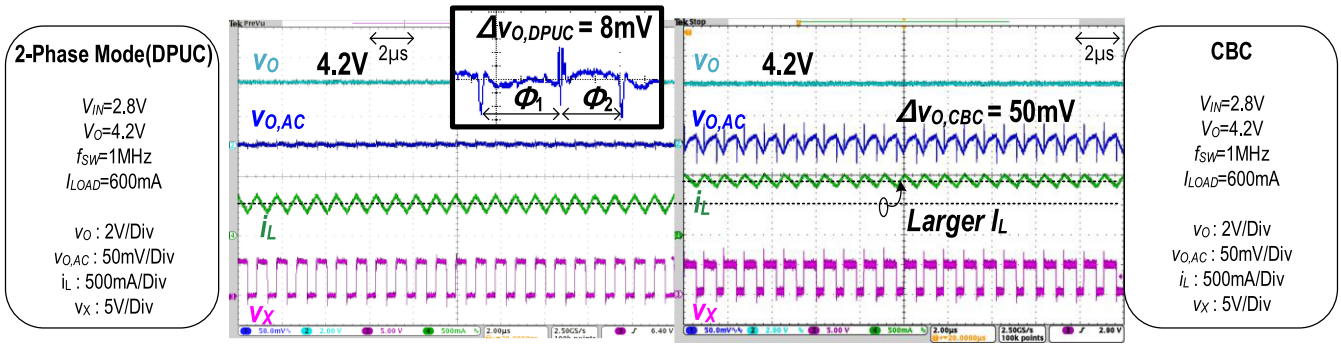


Switch	Type	Width / Length
S_1	8V N-LDMOS	90mm / 800nm
S_2	8V P-LDMOS	240mm / 300nm
S_3	5V P-CMOS	140mm / 500nm
S_4	5V P-CMOS	140mm / 500nm
S_5	5V P-CMOS	140mm / 500nm

Fig. 23. Chip micrograph.

ZCD due to the offset and delay of the comparator, which reduces efficiency under the light I_{LOAD} condition. To solve this problem, ZCD using the switching node (v_X) information can be used [27]. In this article, the ZCD using v_X information is adopted as a shrinking diode time zero-current detector (SDT-ZCD).

As shown in Fig. 20(a), S_2 allows the ZCD for DCM in the DPUC topology. In the case of X_{SM} signal driving S_2, the switch is turned ON when X_{SM} is high as the switch mode, and S_2 is reconfigured to the diode connection when X_{SM} is low as the diode mode. When the current flows in the forward direction through S_2, the conduction loss is reduced in the switch mode. After a certain delay, it operates in the diode mode to passively prevent the reverse current without the special circuit. At this time, it is effective to reduce the time of the diode mode as much as possible. Fig. 20(b) shows the SDT-ZCD controller that



(a) (b)

Fig. 24. Measured waveforms of (a) two-phase mode DPUC and (b) CBC.

automatically tracks the optimum delay. The SDT-ZCD uses the falling edge v_{XF} of the v_X node and the rising edge v_{SR} of v_{S2} to reduce the diode mode time *DT*. Initially, at the start, *UP* signal with fixed duty T_D is generated. Then, the I_B charges $C_{\rm ZCD}$ to increase the $v_{\rm ZCD}$. This $v_{\rm ZCD}$ increases the turn-ON time of S_2 by increasing the X_{SM} width compared with the ramp signal generated at the rising edge of X_{SM}.

As shown in Fig. 21, when the diode mode time is held more than the optimum, v_{S2R} and v_{XF} are not overlapped, and the increased $v_{\rm ZCD}$ is maintained (*UP* case). Conversely, if the diode mode time is held less than the optimum, v_{S2R} and v_{XF} are overlapped when S_2 is turned OFF. This results in a *DN* signal with a fixed duty T_D to decrease $v_{\rm ZCD}$ through $2I_B$ (*DN* case). This reduces the width of the X_{SM} in the next cycle and increases the diode mode time again. Since T_D is related to the resolution for accurate ZCD time, if T_D is large, the resolution of the control voltage $v_{\rm ZCD}$ in the SDT-ZCD is low, which makes the controller hard to find accurate ZCD time. In contrast, if T_D is small, the resolution becomes high, which helps the controller to find accurate ZCD time. Even if the small T_D requires a long settling time for the STD-ZCD, the fast settling time for ZCD is not required for DCM in the steady state. Constructing this digital feedback using *UP* and *DN* signals, it is possible to realize the accurate ZCD. Fig. 22 shows the timing diagram in which the optimum diode time is determined. The SDT-ZCD can operate accurately compared with the conventional ZCD which is inaccurate due to the offset and delay of the comparator. To design the accurate ZCD, increasing $C_{\rm ZCD}$ or reducing I_B can be helpful to implement high resolution in the SDT-ZCD.

IV. Measurement Results

The proposed DPUC was designed with 1P4M 0.18 μm BCD process. As shown in Fig. 23, the chip area is 2 mm $\times$ 3 mm. In this work, a CMOS device which has a breakdown voltage of 5 V is used. Since the voltage at the switching node v_X becomes $2V_O - V_{\rm IN}$ in Φ_2, laterally diffused metal-oxide-semiconductor (LDMOS) that has a higher breakdown voltage than that of the CMOS device is used for S_1. Also, in Φ_1, the voltage stress of S_2 is the same with V_O. Since the maximum V_O of this work is 5 V, we designed the S_2 with the LDMOS for the robust operation. These are the reasons that both S_1 and S_2 are larger than the other switches.

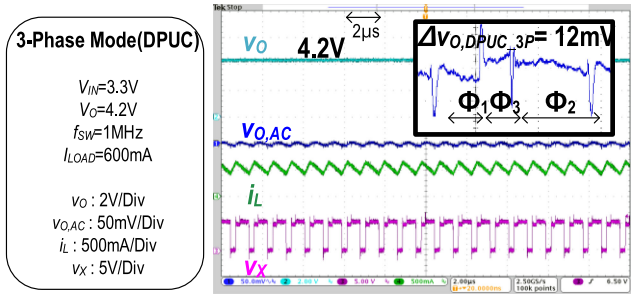


Fig. 25. Measured waveforms of the three-phase mode DPUC.

Fig. 24 shows the measured waveforms at $V_{\rm IN} = 2.8$ V, $V_O = 4.2$ V, and $I_{\rm LOAD} = 600$ mA. Since Φ_1 is greater than $0.5Ts$ in operating conditions, the DPUC operates in the two-phase mode, as shown in Fig. 24(a). For the comparison, Fig. 24(b) shows the operating waveform of the CBC under the same condition. It shows that the i_L of the CBC is much larger than that of the DPUC. Also, the $\Delta v_{O\_\rm CBC}$ is 50 mV, while $\Delta v_{O\_\rm DPUC}$ is only 8 mV owing to the continuous i_D.

Fig. 25 shows the measured waveforms at $V_{\rm IN} = 3.3$ V, $V_O = 4.2$ V, and $I_{\rm LOAD} = 600$ mA. Since Φ_1 is smaller than $0.5\,T_S$, the DPUC operates in the three-phase mode. $\Delta v_{O,\rm DPUC\_3P}$ is also so small as 12 mV.

Fig. 26 shows the $\Delta v_{O\_\rm DPUC}$ as $V_{\rm IN}$ varies from 2.4 to 4.2 V under the condition of $V_O = 4.5$ V and $I_{\rm LOAD} = 500$ mA. Compared with the $\Delta v_{O\cdot\rm CBC}$, while the DPUC does not adopt the interleaved structure that requires additional inductors, it has maximally three times smaller Δv_O in the two-phase operation owing to the continuous i_D. In addition, the DPUC can keep Δv_O small owing to the three-phase operation, as $V_{\rm IN}$ increases.

Fig. 27 shows the measured waveforms at $V_{\rm IN} = 2.8$ V, $V_O = 4.2$ V, $I_{\rm LOAD} = 40$ mA, and switching frequency $f_{SW} = 700$ kHz, when the DPUC operates in DCM. It shows that the $\Delta v_{O,\rm DPUC}$ is also small as 5 mV. In addition, the operation of the SDT-ZCD is verified by the enlarged v_X waveform.

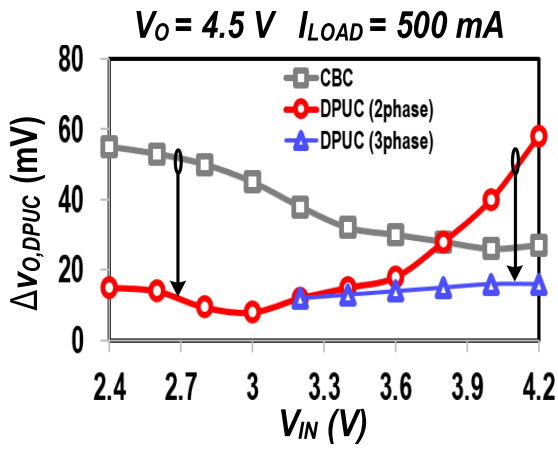


Fig. 26. Measured output ripple of the DPUC.

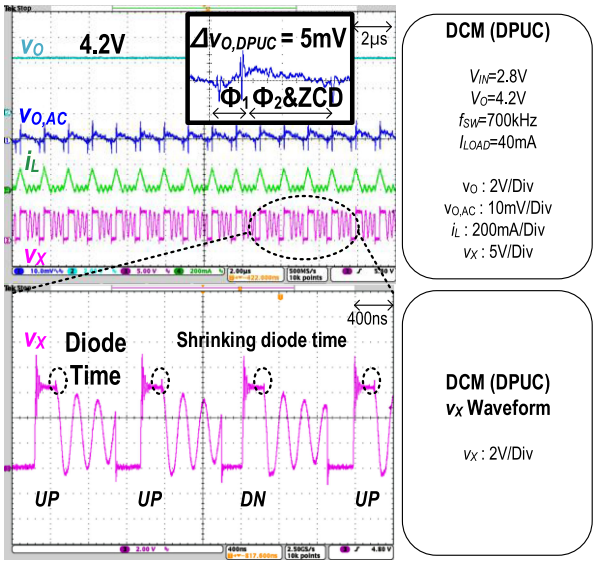


Fig. 27. Measured waveforms of the DPUC in DCM with SDT-ZCD.

The load transient response is measured under the same condition, as shown in Fig. 28. When I_{LOAD} changes from 200 to 600 mA, the undershoot of the v_O in the DPUC is 190 mV with alleviated RHP-zero effect. Meanwhile, the large undershoot of v_O in CBC was 280 mV in Fig. 28(a). Likewise, the overshoot of v_O in the DPUC, when I_{LOAD} changes from 600 to 200 mA, is reduced from 250 to 130 mV compared with that in the CBC, as shown in Fig. 28(b).

Fig. 29 shows the simulated waveforms of i_D and i_L under the load transient conditions. It can be seen that the rapid reaction of C-path current alleviates the RHP-zero effect as Φ_1 changes in the DPUC. Therefore, the DPUC can achieve faster transient response than the CBC while using the same PWM controller. This effect makes it easy to ensure the stability of the DPUC using any conventional controller.

Fig. 30 shows the measured efficiency at $V_{\mathrm{IN}} = 3$ V and $V_O = 4.2$ V. Although a small size inductor having R_{DCR} of 200 mΩ is used, the maximum efficiency reaches 95.2% higher than the CBC. This prototype was designed to drive the target

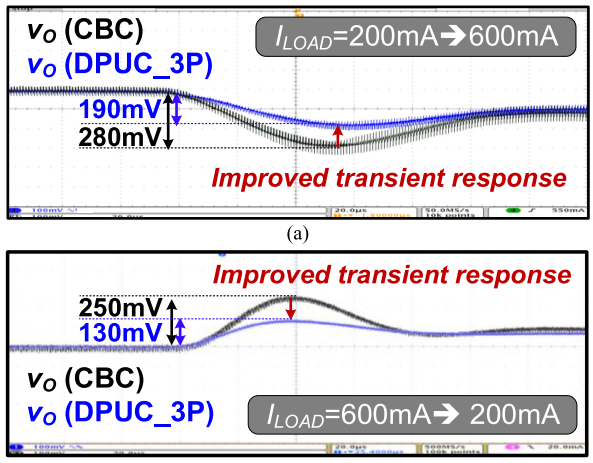


Fig. 28. Measured output voltage waveforms when I_{LOAD} changes (a) from 200 to 600 mA and (b) from 600 to 200 mA.

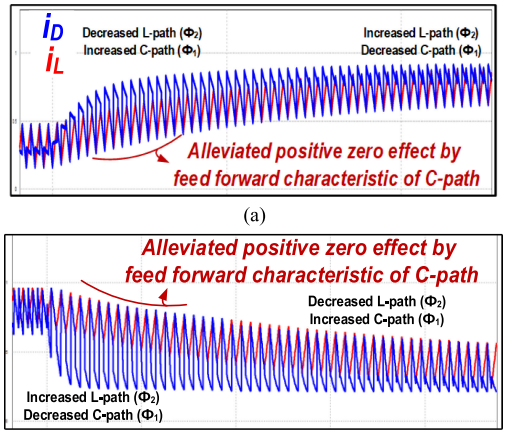


Fig. 29. Simulated output delivery current and inductor current waveforms in (a) load step-up case and (b) load step-down case.

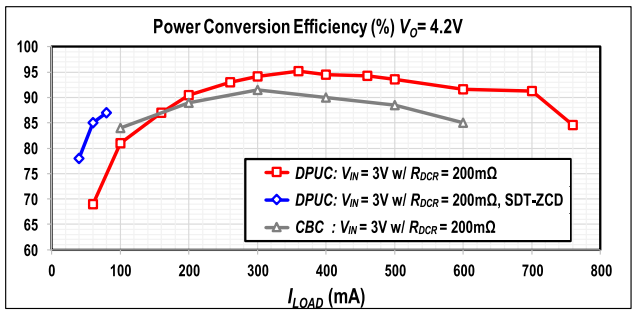


Fig. 30. Measured efficiency of the DPUC.

load current range of 300–500 mA. The target load current range can be changed in the design stage for the heavier load condition. Outside of the target load current range, the power efficiency can be degraded due to the unoptimized conduction or switching losses. Especially, when I_{LOAD} is larger than 200 mA, DPUC shows a higher efficiency than CBC. However, because of the additional power switches, DPUC has a lower efficiency in the light load condition than CBC. Therefore, the SDT-ZCD

TABLE III
COMPARISON TABLE

	This Work	2014JSSC [20]	2012 TPE [15]	TPS6107 [21]	2013JSSC [22]
Process	0.18 μm BCD	0.35 μm BCD	0.3 μm CMOS	N/A	0.35 μm CMOS
Input voltage	2-4.2 V	2.7~4.5 V	3.1~3.3 V	0.9-5.5 V	1.8~3.2 V
Output voltage	3-5 V	8 V	4.5 V	1.8-5.5 V	3-4.2 V
Inductor (L)	4.7 μH	10 μH	470nH/470 nH	1.5-2.5 μH	1 μH
Capacitor	10 μF/10 μF*	10 μF	20 μF	10 μF	10 μF
Switching frequency	1 MHz : CCM (<1 MHz : DCM)	1 MHz	5 MHz	1.2 MHz	1 MHz/N (N=2^i and i=0-5)
Load current	10-800 mA	20-300 mA	400 mA	5-600 mA	5-800 mA
Active area	3.2 mm^2	**1.863 mm^2	0.911 mm^2	N/A	1.75 mm^2
Topology	DPUC	CBC	2-Phase CBC	CBC	CBC
Output delivery current	Continuous	Discontinuous	Discontinuous	Discontinuous	Discontinuous
Reduced inductor current	YES	NO	YES	NO	NO
Ripple Voltage	< 15 mV	90 mV	20 mV	N/A	80 mV
Peak Efficiency (R_{DCR} of L)	95.2% (200 mΩ)	90% (11 mΩ)	N/A	92%	94.8% (9 mΩ)

*Flying capacitor.
**Off-chip diode is not included.

is adopted to improve the efficiency of the DPUC under the light I_{LOAD} condition.

Table III presents the performances of the DPUC compared with the related papers adopting the CBC topology. Since the output delivery current is continuous in the DPUC, Δv_O is significantly reduced to less than 15 mV compared with the CBC. Even with R_{DCR} of 200 mΩ, the DPUC has a higher efficiency than the other CBC works. This means that the DPUC can use a smaller and a cheaper inductor than the CBC topology.

V. CONCLUSION

This article proposes a new boost converter topology called DPUC. Unlike CBC, which has a single path, the proposed DPUC has a hybrid structure using one inductor and one flying capacitor without the complex voltage balancing circuits. It allows that the DPUC has two current paths, which are *C*-path and *L*-path, respectively. Owing to these two paths, the i_L is lower than that of the CBC, and the i_D is delivered to the output continuously. The reduced i_L improves the efficiency of the converter lowering the conduction loss, especially when the small-size inductor with large R_{DCR} is adopted or *M* is high in the heavy load condition. Moreover, the continuous i_D makes much smaller output ripple voltage, Δv_O, than that of the CBC. In addition, the feedforward characteristic of the flying capacitor reduces the RHP-zero effect that degrades the transient response of the CBC. This article also includes a detailed analysis of the conduction loss and transfer function of the DPUC topology. Finally, the measured results show that the DPUC has a high efficiency of 95.2% and a small ripple of up to 15 mV, even though the inductor having R_{DCR} of 200 mΩ is used.

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