# Development of High-Power High Switching Frequency Cryogenically Cooled Inverter for Aircraft Applications

Handong Gui, *Student Member, IEEE*, Zheyu Zhang, *Senior Member, IEEE*, Ruirui Chen, *Student Member, IEEE*, Ren Ren, *Student Member, IEEE*, Jiahao Niu, *Student Member, IEEE*, Haiguo Li, Zhou Dong, *Student Member, IEEE*, Craig Timms, Fei Wang, *Fellow, IEEE*, Leon M. Tolbert, *Fellow, IEEE*, Benjamin J. Blalock, *Senior Member, IEEE*, Daniel Costinett, *Senior Member, IEEE*, and Benjamin B. Choi

***Abstract*—To better support the superconducting propulsion system in the future aircraft applications, the technologies of high-power high switching frequency power electronics systems at cryogenic temperatures should be investigated. This article presents the development of a 40-kW cryogenically cooled three-level active neutral point clamped inverter with 3 kHz output line frequency and 140 kHz switching frequency. Si MOSFETs are characterized at cryogenic temperatures, and the results show that they have promising performance such as lower ON-resistance and switching loss. The design of the inverter is presented in detail with the special consideration of the cryogenic temperature operation. Moreover, a packaging and integration architecture is designed and fabricated to demonstrate the feasibility and performance of the inverter in the lab. It is able to achieve no leakage with good thermal and air insulation. With the inverter and packaging, the experimental results show that the inverter operates properly at cryogenic temperatures. The loss is measured at different load conditions, and the loss analysis is given, which shows that the cryogenically cooled inverter has 30% less loss than operating at room temperature.**

***Index Terms*—Active neutral point clamped converter, aircraft, cryogenic, efficiency, Si MOSFET.**

Manuscript received February 21, 2019; revised July 11, 2019; accepted October 10, 2019. Date of publication October 24, 2019; date of current version February 20, 2020. This work was supported by the Boeing Company and NASA. This work made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation (NSF) and U.S. Department of Energy under NSF Award Number EEC-1041877, and the CURENT Industry Partnership Program. Recommended for publication by Associate Editor D. Dujic. *(Corresponding author: Handong Gui.)*

H. Gui, R. Chen, R. Ren, J. Niu, H. Li, Z. Dong, C. Timms, F. Wang, L. M. Tolbert, B. J. Blalock, and D. Costinett are with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA (e-mail: hgui@vols.utk.edu; rchen14@vols.utk.edu; rren3@vols.utk.edu; jniu3@vols.utk.edu; hli96@vols.utk.edu; zdong9@vols.utk.edu; ctimms@vols.utk.edu; fred.wang@utk.edu; tolbert@utk.edu; bblalock@tennessee.edu; daniel.costinett@utk.edu).

Z. Zhang is with the Zucker Family Graduate Education Center, Clemson University Restoration Institute, North Charleston, SC 29405 USA (e-mail: zheyu.zhang@ieee.org).

B. B. Choi is with the NASA Glenn Research Center, Cleveland, OH 44135 USA (e-mail: benjamin.b.choi@nasa.gov).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2949711

## I. Introduction

POWER generation using superconducting systems that operate at cryogenic temperatures in aircraft applications can provide lower power losses, which offers intriguing propulsion system benefits [1]–[3]. Conventionally, power electronics systems in such systems are placed inside the thermal insulation environment with the room temperature maintained [1], [4], [5]. Thus, the extra thermal insulation and temperature regulation increase the complexity, weight, volume, and cost of the power conversion system. Therefore, it would be beneficial if the power electronics systems can directly operate at cryogenic temperature.

On the other hand, reducing size, weight, and loss is always a critical target for electrical systems in aircraft applications. Generally, increasing the switching frequency of the power converter can help decrease the size and weight of the electromagnetic interference (EMI) filter. In addition, the line frequency of the motor of the propulsion system can be increased with higher switching frequency, which also contributes to smaller and lighter motors running at higher speed. Based on earlier research, cryogenic temperatures can provide the potential to adopt higher switching frequency and achieve lower conduction and switching loss for the power conversion system [1], [2], [4], [5].

However, it is challenging to develop power converters that operate properly at cryogenic temperatures (typically lower than 123 K) due to the following unknown domains.

1) Components, which include power semiconductor devices, passive components, and integrated circuits. Their characteristics can change significantly with the temperature and are worth investigating.
2) Power stage, which includes the topology selection and circuit design. The design needs to include the special consideration of the difference caused by the cryogenic temperatures compared to the design at room temperature.
3) Inverter packaging and cooling system integration, which is required to provide the cryogenic temperature with a coolant and guarantee the proper thermal/air insulation for safe testing in the lab.

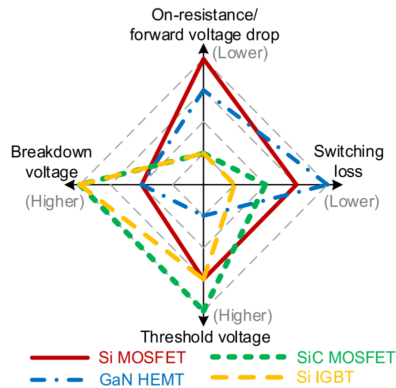



Fig. 1. Comparison among devices' performance at cryogenic temperature.

For high-power and medium-voltage applications, the main candidates of active power devices at room temperature are Si MOSFETs, Si IGBTs, SiC MOSFETs, and GaN HEMTs. Several articles on the characterization of these devices at cryogenic temperatures have been reported. SiC MOSFETs have much higher ON-resistance at low temperatures, which makes them not suitable for cryogenic applications [6]–[10].

GaN HEMTs show improved static ON-resistance and constant breakdown voltage at cryogenic temperatures compared to that at room temperature [11]–[13]. Unfortunately, the dynamic ON-resistance can increase when the temperature drops because of the current collapse phenomenon, which significantly deteriorates the efficiency improvement brought by the reduction of static ON-resistance especially in high switching frequency applications [14]–[16].

Si IGBTs show better switching performance at cryogenic temperatures and also lower forward voltage drop at cryogenic temperatures compared to room temperature [17]–[19]. However, the switching speed and ON-state loss still cannot rival that of Si MOSFETs, and it is hard to use them for applications with switching frequency higher than 100 kHz. Si MOSFETs show decreased ON-resistance and faster switching speed at cryogenic temperatures [20]–[24].

Fig. 1 summarizes the comparison among different devices at cryogenic temperatures. In all, it can be observed that Si MOSFETs are good candidates to achieve high efficiency in high-power high switching frequency applications, and more information about their performance at cryogenic temperatures is needed.

Meanwhile, there are not many reports about converter designs at cryogenic temperatures [4], [5], [25]–[30]. Table I lists the topologies, power, and switching frequency used by other researchers. The maximum reported power level of the cryogenically cooled converter prototypes was 2.5 kW, and most of the switching frequencies were lower than 100 kHz. In addition, there was no specific detailed cooling system design provided that would be suitable for high-power electronics testing.

In this article, a cryogenically cooled inverter with 40 kW output power, 3 kHz output line frequency, and 140 kHz switching frequency is presented. The key technologies in developing the converter are addressed comprehensively as follows.

TABLE I
CRYOGENICALLY COOLED TOPOLOGIES IN EXISTING LITERATURE

| Reference | Topology | Power level | Switching frequency |
|---|---|---|---|
| [4] | Full Bridge | 24 W | Unknown |
| [5] | Full Bridge | 20 W | 20 kHz |
| [25] | Full Bridge | 8 W | 100 kHz |
| [26] | Switched Capacitor | 1 kW | 120 kHz |
| [27] | Full Bridge | 2.5 kW | 20 kHz |
| [28] | Half Bridge | 320 W | 10 kHz |
| [29] | Buck | 175 W | 50 kHz |
| [30] | Multi Resonant Buck | 55 W | 200 kHz |

1) High-speed Si power MOSFETs at cryogenic temperatures are characterized, which includes both static and dynamic performances.
2) Power stage design with the special consideration of cryogenic temperature operation is provided.
3) Inverter packaging, cooling system integration, and testing procedure that can guarantee the proper operation of the converter at cryogenic temperatures in the lab are introduced.
4) The capability to run high-power high switching frequency converter at cryogenic temperatures is verified with testing results.
5) Loss of the cryogenically cooled inverter is compared with the room temperature one, which validates the benefit of running the inverter at cryogenic temperatures.

This article is organized as follows. Section II presents the characterization of the Si power MOSFETs and the selection of other parts for the cryogenically cooled inverter. Section III shows the design of the inverter for cryogenic temperature operation. Section IV demonstrates the design of the inverter packaging, cooling system integration, and control architecture considering testing the inverter in the lab. Section V gives the experimental results and Section VI provides a brief conclusion.

## II. DEVICE CHARACTERIZATION AND SELECTION AT CRYOGENIC TEMPERATURES

### A. Power Semiconductor Devices

A cryogenic chamber is used to serve as the container for the device under test (DUT) and provide the required cryogenic temperature. For the static characterization, the curve tracer B1505A from Keysight is connected with the DUT, and the Kelvin connection is used to guarantee the accuracy of the measurement, as shown in Fig. 2. The picture of the testing platform is shown in Fig. 3. The temperature inside the chamber can be regulated, and the liquid nitrogen is injected from a dewar. A high accuracy diode-based temperature sensor from Lakeshore is attached to the device to provide the temperature information.

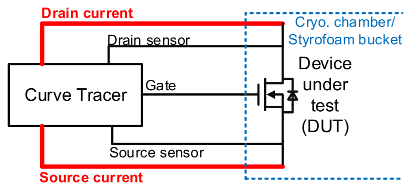



Fig. 2. Configuration for static characterization.

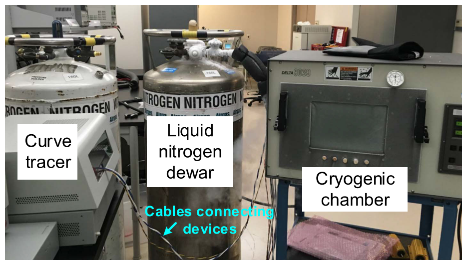



Fig. 3. Testing platform for static characterization.

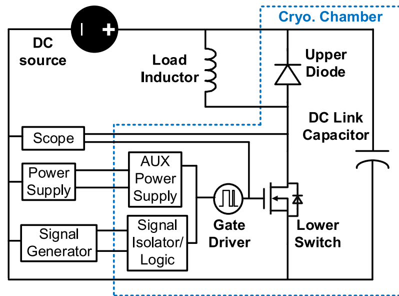



Fig. 4. Configuration for dynamic characterization.

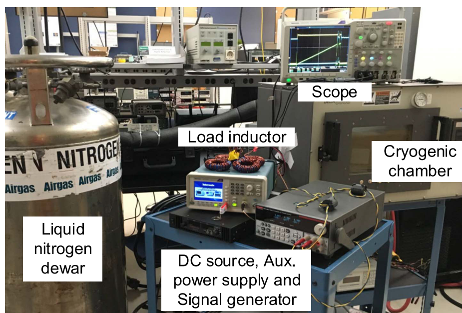



Fig. 5. Testing platform for dynamic characterization.

For the dynamic characterization, a double pulse test (DPT) is adopted to get the switching performance. Figs. 4 and 5 illustrate the configuration and testing platform of the DPT, respectively. Not only the DUT, but also the gate drive, dc-link capacitors, signal isolator, and other auxiliary circuits are located inside the chamber at cryogenic temperature. This is due to the concern for high ringing and noise during fast switching transients caused by parasitics. Literature shows that Si MOSFETs can switch even faster at cryogenic temperatures [20]–[24], so noise can be an issue. Thus, putting the gate drive circuits close to the DUT can minimize the parasitics in the loop. Moreover, it can help mimic the real operating condition in a converter.

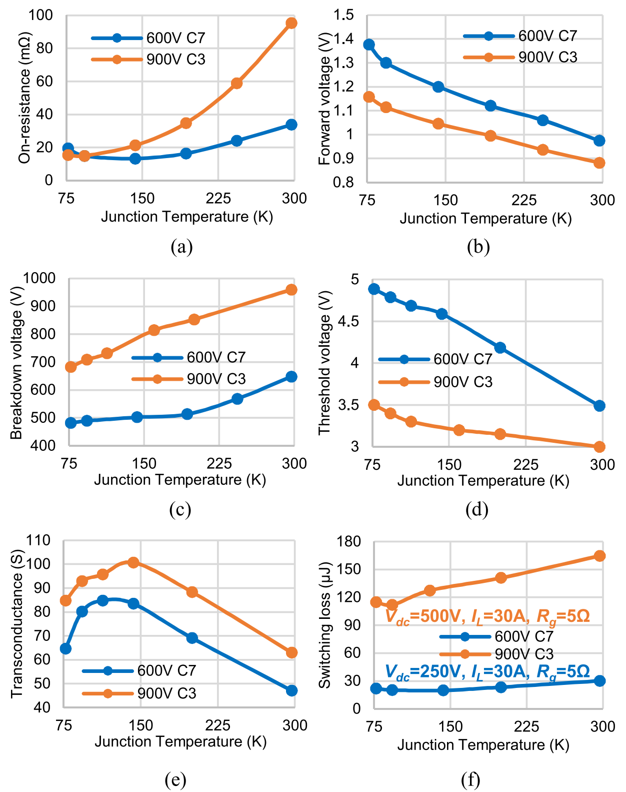



Fig. 6. Characteristics of two Si MOSFETS at different temperatures. (a) On-resistance. (b) Body diode forward voltage. (c) Breakdown voltage. (d) Threshold voltage. (e) Transconductance. (f) Switching loss.

With the setup, Si MOSFETs from different manufacturers are tested in the range of room and cryogenic temperatures. Two MOSFETs from Infineon are compared here because they have the best overall performance and are candidates for the converter: IPZ60R040C7 (600 V, 50 A CoolMOS) and IPW90R120C3 (900 V, 35 A CoolMOS). The ON-resistance, breakdown voltage, body diode forward voltage drop, transconductance, threshold voltage, as well as the turn-ON and turn-OFF loss are tested and demonstrated in Fig. 6.

Fig. 6(a) illustrates the ON-resistance of the two Si MOSFETs. From room temperature to around 100 K, the ON-resistance drops, and this is due to the increased carrier mobility at low temperatures. However, the ON-resistance increases as the cryogenic temperature is approached, and it can be explained by the reduced number of carriers being available, which is referred to as carrier freeze-out [31]. Note that although the C3 CoolMOS exhibits much higher ON-resistance than that of C7 CoolMOS at room temperature, it decreases faster as temperature drops and is lower than the C7 CoolMOS at 77 K.

Fig. 6(b) plots the body diode forward voltage drop when the drain current is 50 A for both of the MOSFETs. It can be seen that both devices show an increased forward voltage drop as the temperature decreases, and the trend is similar. This is because of an increased potential barrier height at the pn-junction due to a reduction in the intrinsic carrier concentration at low

TABLE II
SELECTION OF ICS AND PASSIVE COMPONENTS FOR CRYOGENIC OPERATION

| Parts | Selection |
|---|---|
| Integrated ICs | CMOS based |
| DC-link capacitors | Metallized polypropylene film |
| Decoupling capacitors | NP0/C0G |
| Resistors | Metal film/Thin film |

TABLE III
REQUIREMENTS OF 40 kW INVERTER

| | |
|---|---|
| Input voltage | 1 kV DC |
| Output voltage | 600 V RMS line-to-line AC |
| Output power | 40 kW |
| Fundamental frequency | 3 kHz |
| Switching frequency | 140 kHz |

temperatures. The C3 CoolMOS has lower body diode forward voltage drop than the C7 CoolMOS does.

The measured breakdown voltage of the two devices is shown in Fig. 6(c). The breakdown voltage declines because the mean free path of the carrier increases at low temperature, which contributes to higher impact ionization efficiency. So, more electron–hole pairs with high energy are created to launch the impact ionization, and the avalanche is enhanced. From the testing result, the breakdown voltage of the tested Si MOSFETs at 77 K is only 80% of that at room temperature.

Fig. 6(d) shows the threshold voltage of the two MOSFETs increases at cryogenic temperature because of the reduction of intrinsic carrier concentration. Fig. 6(e) demonstrates the transconductance, which first increases from room temperature to about 100 K, and then decreases when the temperature is close to 77 K. The reason is similar to that of ON-resistance, which is caused by carrier freeze-out.

In terms of switching performance, Fig. 6(f) plots the switching loss of the two DUTs with the same gate resistance (5 Ω). Note that due to the variety of rated voltage, the dc bus voltage of the DPT is different for the two MOSFETs. The dc bus voltage is 250 V for the 600 V C7 MOSFET, while it is 500 V for the 900 V C3 MOSFET. From Fig. 6(f), switching loss decreases as temperature drops but the loss decreases slower or even increases below 125 K. This is influenced by both the inversion layer mobility and the transconductance.

### *B. Integrated Circuits and Passive Components*

In addition to power semiconductor devices, other parts in the circuits, such as integrated circuits (ICs) and passive components, are also critical for the performance of the converter. Table II lists the selection of the ICs and passive components for this application. Note that magnetic components are also important but are not included in the power stage and, thus, are out of the scope of this article.

For ICs, two main techniques are widely used in room temperature applications: bipolar junction transistor (BJT) based and Complementary metal–oxide–semiconductor (CMOS) based. According to the survey, BJT-based ICs show poor performance at cryogenic temperature due to the significant decrease of current gain caused by the reduction of emitter injection efficiency and carrier lifetime [32]–[34]. On the other hand, CMOS-based ICs have improved performance at lower temperatures, and the main improvement is the switching speed [35]–[38]. Due to the increase in carrier mobility and saturation velocity at low temperatures, the transconductance of both n-channel and p-channel MOSFETs increases. Therefore, CMOS-based ICs are good candidates for cryogenic operation.

The most widely used capacitors in power electronics applications are electrolytic capacitors, film capacitors, and ceramic capacitors. Many articles have pointed out that both aluminum and tantalum electrolytic capacitors perform poorly at low temperatures [39]–[42]. In film capacitors, the polypropylene and polyphenylene sulfide show stable characteristics throughout the room and cryogenic temperatures. Ceramic capacitors are categorized into two classes according to the features of different dielectric materials. The ceramic capacitors in Class 1, like NP0/C0G, can provide high-tolerance capacitance and low loss with stable voltage and temperature coefficients. On the other hand, capacitors in Class 2 exhibit the variation in capacitance with temperature and voltage, which makes them not suitable for cryogenic operation.

For resistors, researchers have found that thin film, metal film, and wirewound are good candidates, while carbon and ceramic composition are poor at cryogenic temperature [4], [5].

It is worth highlighting that based on the testing observation, surface mount components should be soldered on PCBs. If the surface-mount resistors/capacitors (like in snubber circuits) are directly soldered to the pins of the discrete power devices, the mismatch in coefficient of thermal expansion can cause cracks in resistors/capacitors. In such cases, through-hole resistors/capacitors can be used as their pins are more resilient.

## III. INVERTER DESIGN FOR CRYOGENIC OPERATION

The specification of the inverter is listed in Table III based on the NASA requirement for future more electric aircraft applications [43]. The objective is to design, build, and test a technology demonstrator of high efficiency and specific power MW-class inverter intended for eventual use in aircraft electric high-speed superconducting motors. To attenuate the risks and verify the technologies, a 40 kW-small-scaled inverter is first targeted. With the tested results of the Si MOSFETs in Section II, the inverter power stage is designed as follows.

### *A. Topology and Device Selection*

Fig. 7 shows the employed three-level active neutral point clamped (ANPC) inverter. Compared with the traditional two-level voltage source inverter (VSI), a three-level ANPC inverter allows lower voltage stress of power semiconductors. For the inverter with 1 kV input dc bus, each power device only needs

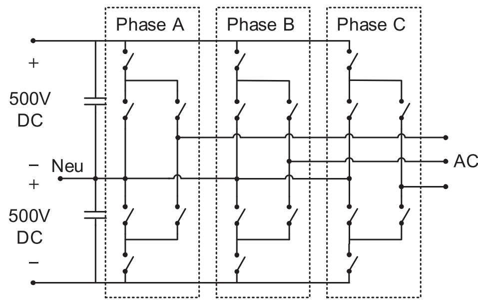



Fig. 7. Three-level ANPC inverter topology.

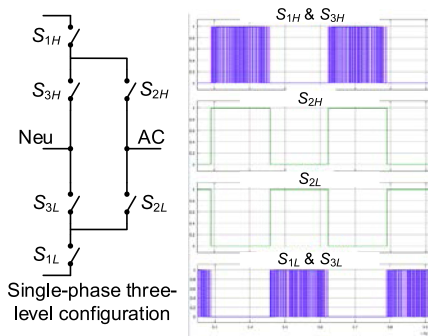



Fig. 8. Switch functions of a single-phase three-level ANPC inverter.

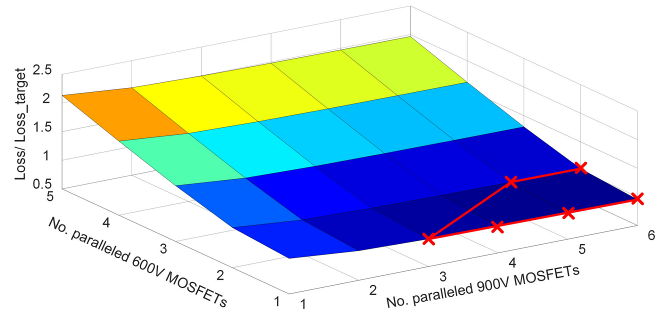



Fig. 9. Loss with different number of devices in parallel.

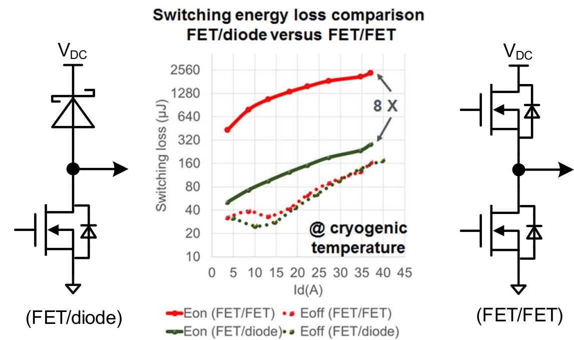



Fig. 10. Impact of reverse recovery on switching energy loss at cryogenic temperature.

to handle 500 V operation voltage. As shown in Section II, Si MOSFETs have a lower breakdown voltage at cryogenic temperatures. Therefore, reducing the voltage stress of the MOSFETs can provide more flexibility for selecting devices. Furthermore, the three-level ANPC inverter has less EMI and reduced *dv/dt* compared with two-level VSI, which is beneficial for the lightweight EMI filter design. Compared with traditional three-level NPC inverter consisting of four active switches and two diodes per single phase, all the power semiconductor devices employed in the three-level ANPC inverter are active switches [44]–[48], which enables more flexibility for modulation, vector selection and lower loss at cryogenic temperature.

Fig. 8 depicts the switch pattern of the three-level ANPC inverter. The high-frequency switching events occur between outer switch/clamping switch ($S_{1H}/S_{3H}$ and $S_{1L}/S_{3L}$). Only one switching event occurs between two inner switches ($S_{2H}/S_{2L}$) during one fundamental cycle. Since almost all the hard switching commutations occur between the outer switch and neighboring clamping switch, the layout optimization for parasitic minimization and fast switching only needs to be focused on the switching loop of outer switch and neighboring clamping switch.

To meet the loss requirement, it can be concluded from Fig. 8 that the MOSFETs with promising switching performance should be utilized for outer switches and clamping switches because of the high switching frequency, while Si MOSFETs with excellent conduction performance should be employed for inner switches since they only operate at fundamental frequency. From Fig. 6(f), it is apparent that the switching loss of two series-connected 600 V C7 MOSFETs at cryogenic temperature is much lower than that of one 900 V C3 MOSFET. Considering that the voltage stress across each switch in Fig. 7 is 500 V, two 600 V C7 Si MOSFETs need to be series connected to form one switch since the breakdown voltage is 480 V at 77 K. On the other hand, the conduction loss of one 900 V C3 MOSFET is lower than two series-connected 600 V C7 MOSFETs at cryogenic temperature, as shown in Fig. 6(a). Therefore, two series-connected 600 V C7 MOSFETs are selected to be the outer and clamping switches ($S_{1H}/S_{1L}$ and $S_{3H}/S_{3L}$) at cryogenic temperature. Hence, 900 V C3 MOSFET is used for the inner switch ($S_{2H}/S_{2L}$) without series connection.

Paralleling devices is worth considering to optimize the loss. The loss calculation is done based on a simulation model developed in Simulink and is shown in Fig. 9. The paralleled number is determined based on the following principles: first, the total loss should be lower than the target, which is less than 1 kW at full-load condition; and second, the total number of MOSFETs should be as small as possible to optimize the power density and reduce parasitics. The red outlined region in Fig. 14 indicates the cases that can meet the loss requirement. Among them, it is observed that using one 600 V C7 MOSFETs set (including two MOSFETs in series) and three 900 V C3 MOSFETs in parallel can achieve the smallest number of devices.

### *B. Reverse Recovery Elimination*

Reverse recovery due to the MOSFET's body diode becomes less severe as the temperature decreases, but still dominates the turn-ON switching energy loss and the total switching loss at cryogenic temperature in hard switching applications. As shown in Fig. 10, switching performance of Si MOSFETs under

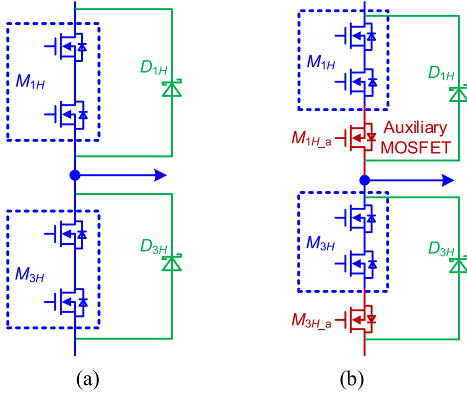



Fig. 11. Solutions to eliminate reverse recovery. (a) With only SiC SBD. (b) With both antiseries-connected MOSFET and SiC SBD

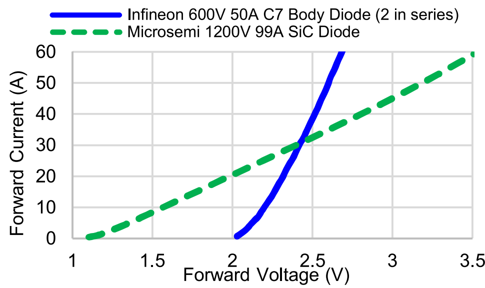



Fig. 12. Comparison of forward voltage of two series-connected Si MOSFETS' body diode and one SiC SBD at 77 K.

two configurations at cryogenic temperature are tested. One is FET/diode configuration that consists of one Si MOSFET and one SiC Schottky barrier diode (SBD). In this case, there is no reverse recovery-related turn-ON loss due to the excellent reverse recovery characteristics of the SiC SBD. The other is FET/FET configuration with two Si MOSFETs in the phase-leg configuration. In this case, the body diode of a Si MOSFET is used as the freewheeling diode for switching commutation. Therefore, the reverse recovery shows up. The test results show that the turn-OFF losses for these two cases are similar and the difference can be explained by the different junction capacitances of SiC SBD and Si MOSFET. However, for turn-ON losses, the difference is significant (by a factor of 8), which will definitely worsen the total switching loss of the power conversion subsystem, and then the efficiency of the overall inverter system.

The conventional way to mitigate the reverse recovery is to parallel an SiC SBD with the MOSFET, as shown in Fig. 11(a). The promise is that all the current flows through the SiC SBD, and the body diode of the MOSFET does not conduct. Thus, the forward voltage drop of the SiC SBD with the load current should be lower than the knee voltage of the body diode. Unfortunately, based on the testing result, the ON-resistance of the SiC SBD increases greatly when the temperature drops. Fig. 12 plots the comparison between the forward voltage drop of two series-connected 600 V/50 A C7 CoolMOS body diode and one 1200 V/99 A SiC SBD from Microsemi at 77 K. Based on the calculation, the peak phase current is about 52 A. From Fig. 12,

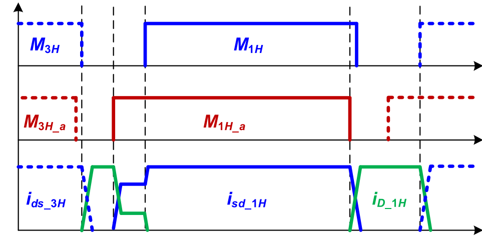



Fig. 13. Operating principle of reverse recovery elimination control.

it is apparent that the forward voltage of one SiC SBD is even higher than that of two Si MOSFETs' body diodes at 52 A. To avoid the conduction of body diodes, at least three SiC SBDs are required to be paralleled with the MOSFETs. Since the SiC SBD only conducts during the dead time, using many SiC SBDs not only increases the size, weight, and cost of the system but also results in more junction capacitance that increases the switching loss. So, an alternative solution is required to eliminate the reverse recovery issue.

To solve the abovementioned issue, an auxiliary MOSFET is introduced to connect in antiseries with the two 600 V MOSFETs as depicted in Fig. 11 (b) [49]. A SiC SBD is paralleled with three MOSFETs like the conventional way. Fig. 13 plots the operating principle of the reverse recovery elimination control with the auxiliary MOSFET. Assuming the load current flows into the node of the phase leg, the high-side auxiliary MOSFET $M_{1H_a}$ turns ON before the 600 V MOSFETs $M_{1H}$ are ON. Once $S_H$ conducts, both the body diode of $M_{1H}$ and the SiC SBD $D_{1H}$ conducts, and the load current distributes between them. Then $M_{1H}$ turns ON with zero voltage, and all the current flows through the channel of $M_{1H}$ because of the low ON-resistance compared with the forward voltage drop of $D_{1H}$. $M_{1H_a}$ turns OFF slightly earlier than $M_{1H}$, so the current is blocked by $M_{1H_a}$ and has to flow into $D_{1H}$. Therefore, $M_{1H}$ are turned OFF with zero current, and there is no way that the current can flow through the body diode of $M_{1H}$, which eliminates the reverse recovery current. When $M_{1H}$ is OFF, the charging current of the output capacitance discharges $M_{1H_a}$ and flows through the body diode of $M_{1H_a}$, since $M_{1H}$ and $M_{1H_a}$ are antiseries connected. Thus, there is no voltage stress on $M_{1H_a}$ and it can turn ON with zero voltage. It means that very low voltage rating with the high-current capability MOSFET can be used here, which reduces any additional conduction loss. The Si MOSFET IPT004N03L (30 V/300 A) from Infineon was selected, and the tested ON-resistance at 77 K is 0.31 mΩ.

Fig. 14 depicts the detailed structure of a single phase in the three-level ANPC inverter with an optimized number of devices and the control of reverse recovery current elimination.

### C. Short-Circuit Protection

The ON-resistance of Si MOSFETs can drop by half or more at cryogenic temperature. Therefore, the short-circuit current of a Si MOSFET at cryogenic temperature is much higher than that at room temperature. As shown in Fig. 15, the saturation current of the MOSFET increases from 500 to 930 A at 77 K. If the turn-OFF

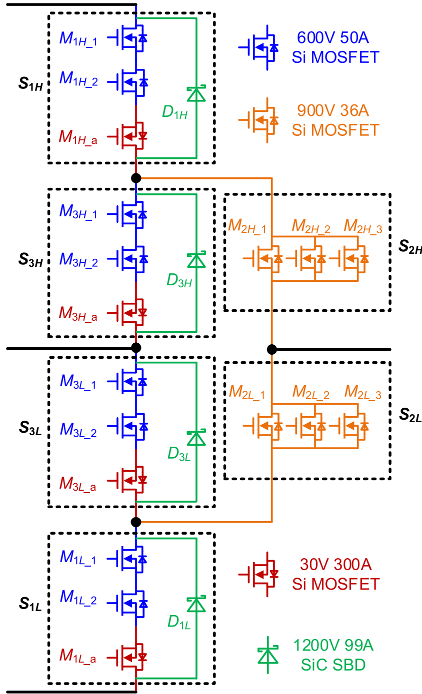
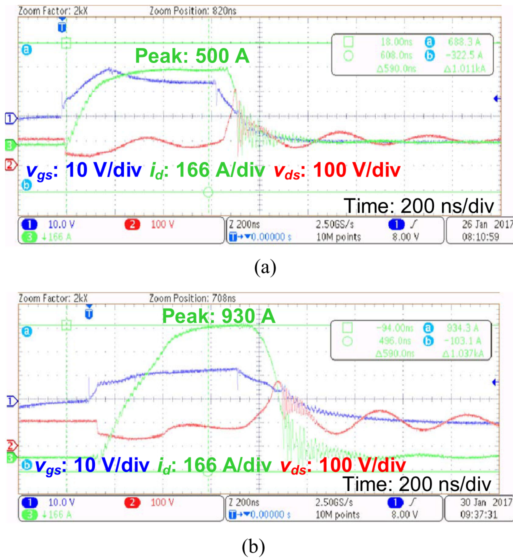



Fig. 14. Detailed structure of single phase in a three-level ANPC inverter.




(a)

(b)

Fig. 15. Short-circuit testing of Si MOSFET with 100 V bus voltage. (a) At room temperature. (b) At 77 K.

resistance still follows the design at room temperature, the high *di/dt* during turn-OFF can cause severe voltage spike and damage the MOSFET. So, the larger soft turn-OFF resistance needs to be selected based on the testing results at cryogenic temperature.

## IV. Inverter Packaging and Cooling System Integration for Cryogenic Testing

To test the inverter at cryogenic temperatures in the lab, the following parts need to be designed: a coldplate for liquid nitrogen flowing to cool the inverter; a package with inverter integrated to provide thermal and air insulation; and a control and protection architecture for proper operation and safety.

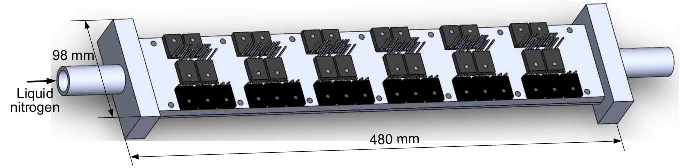



Fig. 16. Coldplate with devices attached.

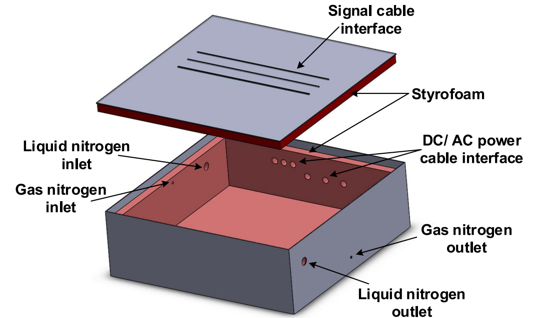



Fig. 17. Design of enclosure.

### A. Coldplate

Fig. 16 illustrates the three-dimensional drawing of the designed coldplate with power MOSFETs attached. It is made of aluminum because of its light weight and has a channel for liquid nitrogen to flow. A thermal simulation is conducted, and the temperature of the devices at full-load condition is around 100 K while that of coldplate ranges from 80 to 95 K.

### B. Inverter Packaging and Integration

The package of the inverter is a key part and requires special design for proper and safe cryogenic testing in the lab. The basic requirements for the packaging mainly include the following.

1) No leakage: The density of liquid nitrogen is over 6000 times higher than gaseous nitrogen; it is highly possible to introduce high pressure in the enclosure if there is leakage. In addition, the temperature of liquid nitrogen is extremely low, and leakage can cause cold injury.
2) Good thermal insulation: Operators should be protected from the cryogenic temperature of the converter system.
3) Good air insulation: Because the temperature is far lower than 0 °C, the vapor in the air can freeze and cause a short circuit in the converter.

To meet the above requirements, an enclosure is designed, as shown in Fig. 17. It is processed based on a stainless steel box. Several holes with different sizes are drilled in the enclosure for liquid/gas nitrogen flow and power input/output. In addition, slots are cut on the lid of the enclosure for the connection between the circuits inside and outside of the enclosure. Note that such packaging is developed for lab testing and may not be required or can be simplified in a real aircraft.

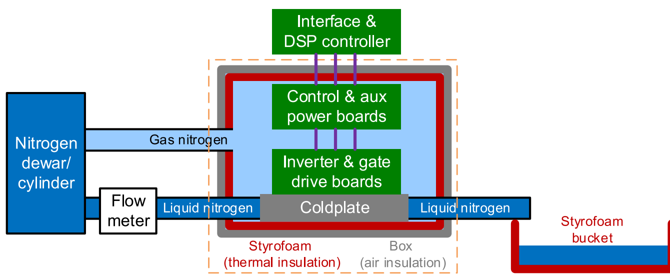



Fig. 18. Structure of cryogenic testing platform.

Fig. 18 shows the conceptual diagram of the packaging and the testing platform. It should be noted that both liquid and gaseous nitrogen is utilized. The liquid nitrogen flows through coldplates and cools down the temperature inside the enclosure. The gaseous nitrogen serves as an air insulator to avoid icing issues. Thus, the gas nitrogen runs first to push all the air out of the enclosure before the liquid nitrogen starts to run. Although there are slots on the lid, they are very thin and the gaseous nitrogen keeps running during the testing process, so it does not influence the air insulation capability. Inside the enclosure, pieces of Styrofoam with 2.5 cm thickness are attached to the six walls to form the thermal insulation. For all the pipes used in the system, the Yor Lok tube fittings are adopted to guarantee proper sealing. Moreover, cryogenic epoxy fills gaps between tubes and the walls of the enclosure. With these attempts, all the aforementioned requirements can be well met. The power stage, gate drives, and isolated power supplies inside the enclosure are connected by ribbon cables with the control and interface board outside. The interface also includes the voltage and current measurements.

### C. Control and Protection Architecture

Fig. 19 shows the basic control and protection architecture. In addition to the regular control and protection, such as space vector modulation (SVM) modulator, CAN bus communication, over-current/voltage sensing, and the cryogenic cooling related protections are also included. The PC communicates with a temperature monitor, flow meter, and oxygen ratio meter and controls the dc source and hardware protection. When the underflow rate, abnormal temperature, or oxygen deficiency is detected, not only the converter would be shut down, but also the E-stop signal would be triggered and liquid/gas nitrogen input should be shut down, and the operators should leave the lab.

## V. Experimental Results and Discussion

### A. Testing Setup and Procedure

Figs. 20 and 21 show the testing platform and inverter prototype based on the design discussed in Section IV.

The testing procedure is as follows.

1) Start control power for controller and gate drive, so that the system protection can be activated.
2) Inject gaseous nitrogen to push all the air inside the enclosure out and avoid icing.
3) Open liquid nitrogen.
4) Wait for the temperature of coldplate to be lower than 100 K.
5) Run power test.
6) Shut down the main power.
7) Shut down liquid nitrogen.
8) When the temperature of coldplate is higher than 0 °C, shut down gas nitrogen.
9) Shut down control power.

### B. Function Validation

Fig. 22 plots the gate–source voltage of the 600 V MOSFET as well as the antiseries-connected auxiliary MOSFET. Note that the auxiliary MOSFET turns ON and OFF earlier than the 600 V MOSFET, which matches well with the operating principle in Fig. 13. With this control sequence, the reverse recovery of the CoolMOS can be fully eliminated.

Fig. 23 depicts the comparison of the voltage balance of the two series-connected 600 V MOSFETs at room temperature and cryogenic temperature with full voltage and load. Due to the thermal constraint at room temperature, the test was done with multiple pulses per second instead of continuously running. The zoomed-in waveforms during turn-ON and turn-OFF are plotted as well. At cryogenic temperature, the voltage balance is not as good as that at room temperature, especially for the turn-ON voltage overshoot caused by the gate drive characteristic mismatch in control and gate drive circuits. However, the maximum drain–source voltage at cryogenic temperature is 386 V, which is lower than the breakdown voltage. Therefore, the unbalance is still within acceptable range and does not impact the operation of the inverter. Also, it is worth highlighting that the drain–source voltage during switching transient is clean, which indicates that there is no reverse recovery.

The output line-to-line voltage and phase current waveforms with full voltage and load at cryogenic temperature are shown in Fig. 24. The three phases are well balanced, and the rms current is 38 A.

### C. Loss Testing and Analysis

The energy loss of the inverter at cryogenic temperature is tested at different load conditions, and the result is plotted in Fig. 25(a). At full-load condition, the loss is 871 W.

Fig. 25(b) shows the loss trend from the start to steady state at half load. It is observed that the loss decreases a little after running. This can match with the ON-resistance trend of the devices as it decreases when the temperature increases from 77 K. However, the loss difference between the steady state and the start point is small (32 W), and the required time for the inverter to achieve thermal equilibrium is short (5 min), which indicates that the temperature rise of the devices is small and the cooling system is effective.

With the tested loss at cryogenic temperature, it is important to analyze the loss breakdown and compare it with the room temperature case at the same switching frequency. Fig. 26(a) illustrates the comparison of the estimated loss breakdown at cryogenic temperature and the estimated loss with the same inverter architecture at room temperature under full voltage and

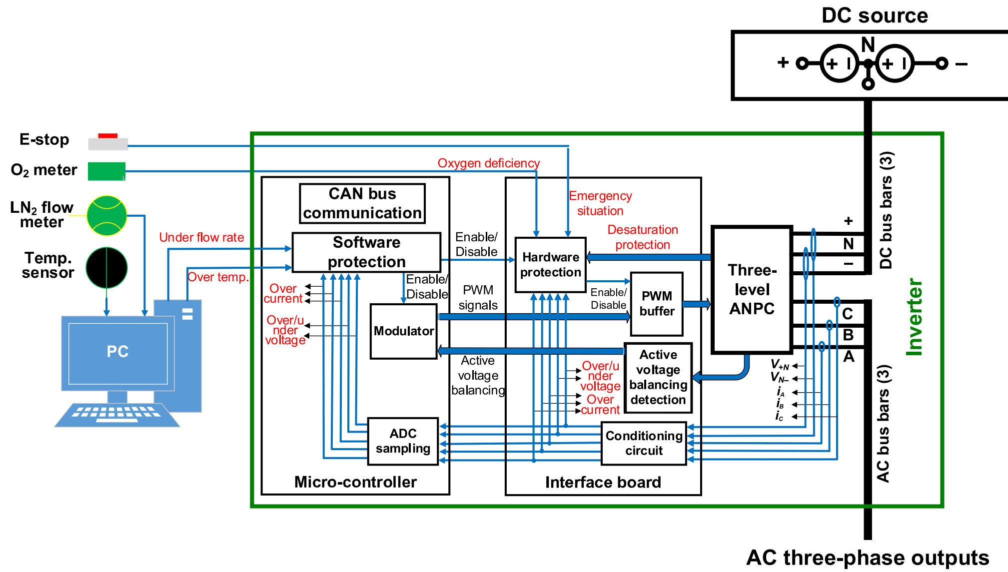



Fig. 19. Control and protection architecture.

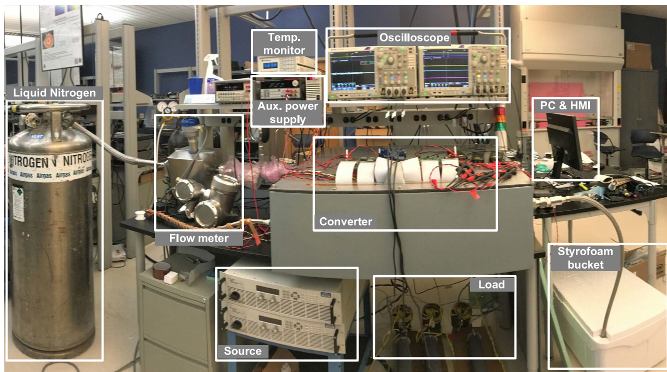



Fig. 20. Cryogenically cooled converter testing platform.

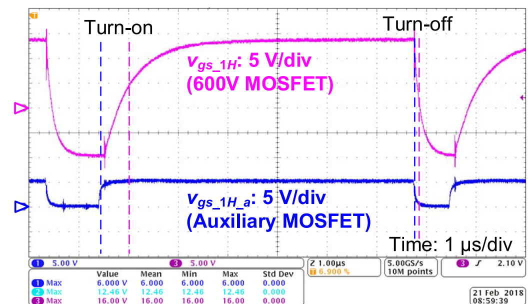



Fig. 22. Gate drive sequence of 600 V MOSFET and auxiliary MOSFET for reverse recovery elimination.

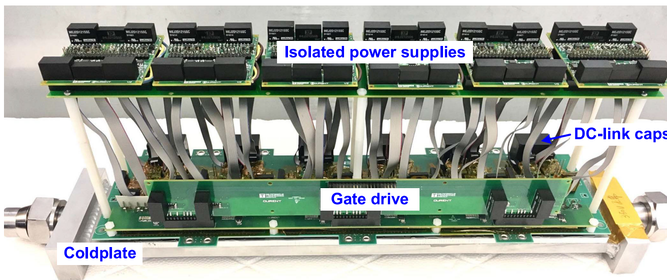



Fig. 21. Inverter prototype.

load condition. The total loss in Fig. 26(a) can match well with the experimental results. Due to the reduction of ON-resistance, the conduction loss at cryogenic temperature is 2.7 times lower than that at room temperature.

At low temperatures, the breakdown voltage of the Si MOSFET decreases. Thus, the switching speed has to be reduced, and RCD snubbers are introduced to suppress the voltage overshoot caused by the parasitics in the switching loop of the series and paralleled devices, which increases the switching loss. At room temperature, there is more margin for voltage overshoot, so the snubbers have different values, and the absorbed energy can be reduced. However, the inherent switching loss of the 600 V MOSFET at room temperature is 1.5 times higher than that at cryogenic temperature. This net effect results in similar total switching loss at cryogenic and room temperature. For the busbar loss and PCB loss that is included in "other" of Fig. 26(a), the lower ambient temperature inside the enclosure can lead to lower loss since the resistance of copper and aluminum decreases as temperature drops. If the busbar can be firmly attached to and cooled by the coldplate, the loss reduction can be larger. In total, the loss at cryogenic temperature is 30% lower than that at room temperature.

With the comparison, it can be concluded that the inverter operating at cryogenic temperature can achieve significantly lower loss than operating at room temperature. To achieve the same

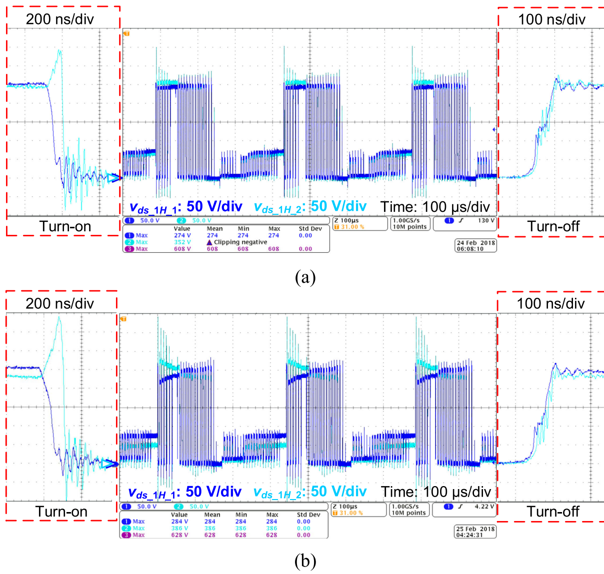



Fig. 23. Drain–source voltage of series-connected 600 V MOSFETS at full voltage and full-load condition. (a) At room temperature. (b) At cryogenic temperature.

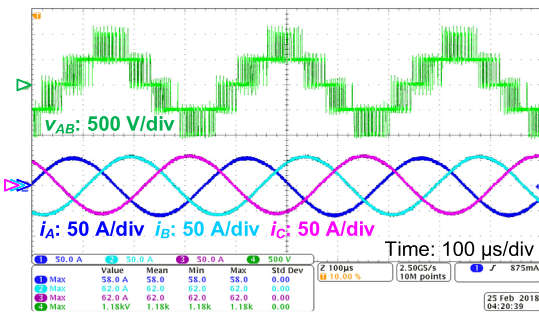



Fig. 24. Line-to-line voltage and phase current at cryogenic temperature, full voltage, and full-load condition.

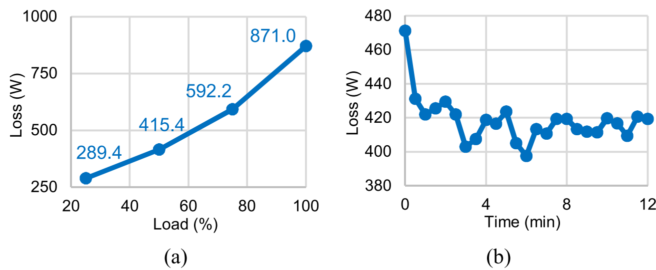



Fig. 25. Loss of inverter at cryogenic temperature. (a) At different load conditions. (b) Change with time at half load.

switching frequency at room temperature, a larger coldplate would have to be adopted for better heat dissipation capability. The weight of the adopted cryogenic coldplate is 0.6 kg. Based on the loss at room temperature, in Fig. 26(a), a water-cooled coldplate with 1.3 kg weight and 0.04 K/W thermal resistance from Wakefield-Vette (Part No. 180-11-12C, 500 × 127 × 18 mm) can be used to maintain a 45 K temperature increase. Hence, the weight of the converter system would increase, which is critical in aircraft applications. Fig. 26(b) plots the weight breakdown of the converter. The total weight is 1.7 kg, and the mass density is 23.3 kW/kg.

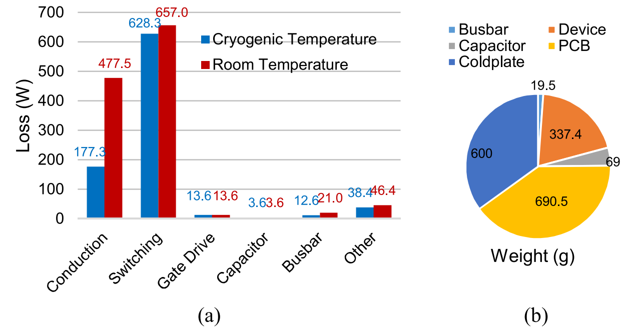



Fig. 26. Loss and weight breakdown. (a) Loss at full-load condition. (b) Weight distribution.

## VI. Conclusion

A 40 kW inverter with 3 kHz output line frequency and 140 kHz switching frequency operating at cryogenic temperature is presented in this article. Si power MOSFETs are selected and characterized at the cryogenic temperature. The results show that both the ON-resistance and switching loss decrease at low temperatures compared to room temperature, which is beneficial for reducing the overall loss of the inverter. The three-level ANPC converter is chosen as the topology, and the number of devices is selected based on the loss requirement and the device characteristics at cryogenic temperature. In addition, functions like reverse recovery elimination and short-circuit protection are specially designed for the cryogenic temperature operation. The packaging and integration of the inverter as well as the cooling system are also designed, which consists of liquid and gas nitrogen, a coldplate, and an insulated enclosure. The inverter was tested in the lab with good thermal and air insulation. The testing results show that the inverter can operate properly at cryogenic temperature with all functions working effectively. The loss at full load is 871 W. The inverter can achieve 30% lower total loss at full load compared to operating at room temperature.

## References

[1] K. Rajashekara and B. Akin, "A review of cryogenic power electronics-status and applications," in *Proc. IEEE Int. Elect. Mach. Drives Conf.*, 2013, pp. 899–904.

[2] P. Haldar *et al.*, "Improving performance of cryogenic power electronics," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 2370–2375, Jun. 2005.

[3] H. Gui *et al.*, "Review of power electronics components at cryogenic temperatures," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2019.2944781.

[4] J. Bourne, R. Schupbach, B. Hollosi, J. Di, A. Lostetter, and H. A. Mantooth, "Ultra-wide temperature (−230°C to 130°C) DC-motor drive with SiGe asynchronous controller," in *Proc. IEEE Aerosp. Conf.*, 2008, pp. 1–15.

[5] J. Garrett, R. Schupbach, H. A. Mantooth, and A. B. Lostetter, "Development of an extreme environment DC motor drive full bridge power stage using commercial-off-the-shelf components," in *Proc. Int. Planet. Probe Workshop*, 2006.

[6] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, “Cryogenic and high temperature performance of 4H-SiC power MOSFETs,” in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 207–210.

[7] T. Chailloux, C. Calvez, N. Thierry-Jebali, D. Planson, and D. Tournier, “SiC power devices operation from cryogenic to high temperature: investigation of various 1.2 kV SiC power devices,” *Mater. Sci. Forum*, vol. 778–780, pp. 1122–1125, 2014.

[8] H. Chen *et al.*, “Cryogenic characterization of commercial SiC Power MOSFETs,” *Mater. Sci. Forum*, vol. 821–823, pp. 777–780, 2015.

[9] H. Gui *et al.*, “Characterization of 1.2 kV SiC power MOSFETs at cryogenic temperatures,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 7010–7015.

[10] J. Qi *et al.*, “Temperature dependence of dynamic performance characterization of 1.2 kV SiC power MOSFETs compared with Si IGBTs for wide temperature applications,” *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9105–9117, Sep. 2019.

[11] J. Colmenares, T. Foulkes, C. Barth, T. Modeert, and R. C. N. Pilawa-Podgurski, “Experimental characterization of enhancement mode gallium-nitride power field-effect transistors at cryogenic temperatures,” in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, 2016, pp. 129–134.

[12] Z. Xue-Fang, W. Li, L. Jie, W. Lai, and X. Jian, “Electrical characteristics of AlInN/GaN HEMTs under cryogenic operation,” *Chin. Phys. B*, vol. 22, no. 1, 2013, Art. no. 017202.

[13] R. Ren *et al.*, “Characterization of 650 V enhancement GaN HEMT at cryogenic temperatures,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 891–897.

[14] S. Nuttinck, S. Pinel, E. Gebara, J. Laskar, and M. Harris, “Cryogenic investigation of current collapse in AlGaN/GaN HFETS,” in *Proc. Gallium Arsenide Appl. Symp.*, 2003, pp. 213–215.

[15] C.-H. Lin, W.-K. Wang, P.-C. Lin, C.-K. Lin, Y.-J. Chang, and Y.-J. Chan, “Transient pulsed analysis on GaN HEMTs at cryogenic temperatures,” *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 710–712, Oct. 2005.

[16] R. Cuerdo *et al.*, “The kink effect at cryogenic temperatures in deep submicron AlGaN/GaN HEMTs,” *IEEE Electron Device Lett*., vol. 30, no. 3, pp. 209–212, Mar. 2009.

[17] A. Caiafa, A. Snezhko, J. Hudgins, E. Santi, and R. Prozorov, “IGBT operation at cryogenic temperatures: Non-punch-through and punch-through comparison,” in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, vol. 4, pp. 2960–2966.

[18] S. Yang, “Cryogenic characteristics of IGBTs,” Doctoral dissertation, Dept. Electron., Elect., Syst. Eng., Univ. Birmingham, Birmingham, U.K., 2005.

[19] A. Caiafa, X. Wang, J. Hudgins, E. Santi, and P. R. Palmer, “Cryogenic study and modeling of IGBTs,” in *Proc. IEEE 34th Annu. Conf. Power Electron. Spec.*, 2003, vol. 4, pp. 1897–1903.

[20] R. Singh and B. J. Baliga, *Cryogenic Operation of Silicon Power Devices*. New York, NY, USA: Springer, 2012.

[21] Z. Zhang *et al.*, “Characterization of high-voltage high-speed switching power semiconductors for high frequency cryogenically-cooled application,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1964–1969.

[22] K. K. Leong, B. T. Donnellan, A. T. Bryant, and P. A. Mawby, “An investigation into the utilisation of power MOSFETs at cryogenic temperatures to achieve ultra-low power losses,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 2214–2221.

[23] O. Mueller, “Properties of high-power Cryo-MOSFETs,” in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 31st IAS Annu. Meet.*, 1996, vol. 3, pp. 1443–1448.

[24] Y. Chen *et al.*, “Experimental investigations of state-of-the-art 650-V class power MOSFETs for cryogenic power conversion at 77K,” *IEEE J. Electron Devices Soc.*, vol. 6, no. 1, pp. 8–18, Oct. 2018.

[25] A. J. Forsyth *et al.*, “Cryogenic converter for superconducting coil control,” *IET Power Electron.*, vol. 5, no. 6, pp. 739–746, Jul. 2012.

[26] C. Barth *et al.*, “Experimental evaluation of a 1 kW, single-phase, 3-level gallium nitride inverter in extreme cold environment,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 717–723.

[27] O. M. Mueller and K. G. Herd, “Ultra-high efficiency power conversion using cryogenic MOSFETs and HT-superconductors,” in *Proc. IEEE Power Electron. Spec. Conf.*, 1993, pp. 772–778.

[28] C. Gold and O. M. Mueller, “Cryogenically-cooled switching circuit,” U.S. Patent US 617 255 0B1, Jan. 9, 2001.

[29] B. Ray, S. S. Gerber, R. L. Patterson, and I. T. Myers, “Liquid nitrogen temperature operation of a switching power converter,” NASA-TM-106867, 1995 [Online].

[30] B. Ray, S. S. Gerber, R. L. Patterson, and I. T. Myers, “77 K operation of a multi-resonant power converter,” in *Proc. Power Electron. Spec. Conf.*, 1995, vol. 1, pp. 55–60.

[31] N. Ahmad, “Carrier freeze-out effects in semiconductor devices,” *J. Appl. Phys.*, vol. 61, no. 5, pp. 1905–1909, 1987.

[32] W. P. Dumke, “The effect of base doping on the performance of Si bipolar transistors at low temperatures,” *IEEE Trans. Electron Devices*, vol. 28, no. 5, pp. 494–500, May 1981.

[33] R. Singh and B. J. Baliga, “Cryogenic operation of power bipolar transistors,” *Solid-State Electron.*, vol. 39, no. 1, pp. 101–108, 1996.

[34] J. M. C. Stork, D. L. Harame, B. Mayerson, and T. N. Nguyen, “Base profile design for high-performance operation of bipolar transistors at liquid-nitrogen temperature,” *IEEE Trans. Electron Devices*, vol. 36, no. 8, pp. 1503–1509, Aug. 1989.

[35] W. F. Clark, B. El-Kareh, R. Pires, S. L. Titcomb, and R. L. Anderson, “Low temperature CMOS—A brief review,” *IEEE Trans. Compon. Hybrid Manuf. Technol.*, vol. 15, no. 3, pp. 397–404, Jun. 1992.

[36] G. Ghibaudo and F. Balestra, “Low temperature characterization of silicon CMOS devices,” in *Proc. Int. Conf. Microelectron.*, 1995, vol. 2, pp. 613–622.

[37] T. K. Makiniemi and P. Kosonen, “A low temperature pipelined analog-to-digital converter,” in *Proc. 8th IEEE Int. Conf. Electron. Circuits Syst.*, 2001, vol. 2, pp. 849–852.

[38] B. Okcan, P. Merken, G. Gielen, and C. Van Hoof, “A cryogenic analog to digital converter operating from 300 K down to 4.4 K,” *Rev. Sci. Instrum.*, vol. 81, no. 2, 2010, Art. no. 024702.

[39] F. Teyssandier and D. Prêle, “Commercially available capacitors at cryogenic temperatures,” in *Proc. Int. Workshop Low Temp. Electron.*, 2010.

[40] M.-J. Pan, “Performance of capacitors under DC bias at liquid nitrogen temperature,” *Cryogenic*, vol. 45, no. 6, pp. 463–467, 2005.

[41] R. L. Patterson, A. Hammond, and S. S. Gerber, “Evaluation of capacitors at cryogenic temperatures for space applications,” in *Proc. Conf. Rec. IEEE Int. Symp. Elect. Insul.*, 1998, vol. 2, pp. 468–471.

[42] L. Faria, A. Passaro, L. Nohra, and R. d’Amore, “Influence of the cryogenic temperature and the BIAS voltage on the spontaneous polarization effect of X5R dielectric capacitors,” *Proc. Int. Refereed J. Eng. Sci.*, vol. 1, no. 1, pp. 14–21, 2012.

[43] NASA Research Announcement, “Research opportunities in aeronautics–2015 (ROA-2015),” Amendment no. 3 NNH14ZEA001N, 2015.

[44] Y. Jiao, S. Lu, and F. C. Lee, “Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg,” *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3255–3266, Jul. 2014.

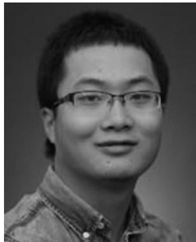
[45] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, “Improved modulation scheme for loss balancing of three-level active NPC converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, Apr. 2017.

[46] Q.-X. Guan *et al.*, “An extreme high efficient three-level active neutral-point-clamped converter comprising SiC & Si hybrid power stage,” *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8341–8352, Oct. 2018.

[47] C.-Q. Xiang, S. Cheng, H. Ding, B.-K. Mao, X. Wu, and T.-J. Yu, “Improved virtual space vector modulation for three-level neutral-point-clamped converter with feedback of neutral-point voltage,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5452–5464, Jun. 2018.

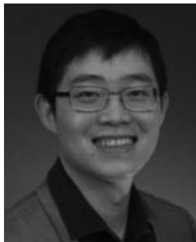
[48] C. Xia, G. Zhang, Y. Yan, X. Gu, T. Shi, and X. He, “Discontinuous space vector PWM strategy of neutral-point-clamped three-level inverters for output current ripple reduction,” *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5109–5121, Jul. 2017.

[49] D. DeWitt, C. Brown, and S. Robertson, “The pinch-off circuit: Reducing noise and component stresses by eliminating body diode conduction in synchronous rectifiers,” in *Proc. 22nd Annu.IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 1531–1536.



**Handong Gui** (S'14) received the B.S. and M.S. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2013 and 2016, respectively. He is currently working toward the Ph.D. degree in electrical engineering with The University of Tennessee, Knoxville, TN, USA.

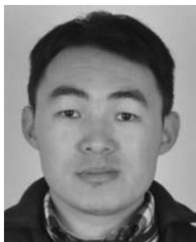
His research interests include wide-bandgap devices and applications, multilevel converters, and electrified transportations.



**Zheyu Zhang** (S'12–M'15–SM'19) received the B.S. and M.S. degrees from the Huazhong University of Science and Technology, Wuhan, China, and the Ph.D. degree from The University of Tennessee, Knoxville, TN, USA, in 2008, 2011, and 2015, respectively, all in electrical engineering.

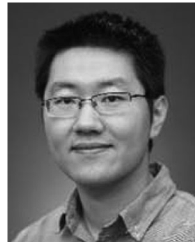
He is the Warren H. Owen-Duke Energy Assistant Professor of Engineering with Clemson University, Clemson, SC, USA. From 2015 to 2018, he was a Research Assistant Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville. Later, he joined General Electric Research as the Lead Power Electronics Engineer at Niskayuna, NY, USA, from 2018 to 2019. He has authored or coauthored more than 80 papers in the most prestigious journals and conference proceedings, filed more than 10 patent applications with one licensed, authored one book and one book chapter, and presented four IEEE tutorial seminars. His research interests include wide-bandgap-based power electronics, modularity and scalability technology, medium-voltage power electronics, advanced manufacturing and cooling technology (e.g., cryogenic cooling) applied in power electronics, and highly efficient, ultradense, cost-effective power conversion systems for electric propulsion, electrified transportation, renewables, energy storage, and grid applications.

Dr. Zhang is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He was the recipient of two prize paper awards from the IEEE Industry Applications Society and IEEE Power Electronics Society.



**Ruirui Chen** (S'15) received the B.S. degree from the Huazhong University of Science and Technology, Wuhan, China, and the M.S. degree from Zhejiang University, Hangzhou, China, in 2010 and 2013, respectively. He is currently working toward the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

From 2013 to 2015, he was an Electrical Engineer with FSP-Powerland Technology, Inc., Nanjing, China. His research interests include high power density converters for aircraft applications, multilevel converters, pulsewidth modulation techniques, converter paralleling control, and conducted EMI.



**Ren Ren** (S'14) received the B.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2012. Since 2012, he has been working toward the Ph.D. degree in electrical engineering with the Jiangsu Key Laboratory of New Energy Generation and Power Conversion, Nanjing University of Aeronautics and Astronautics, Nanjing, China. Since 2017, he has also been working toward the Ph.D. degree in electrical engineering with the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks, The University of Tennessee, Knoxville, TN, USA.

His research interests include high-frequency converters design using wide-bandgap devices, design optimization and automation in power electronics, soft-switching resonant converter, and high-frequency digital control in power electronics.

**Jiahao Niu** (S'16) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2016. He is currently working toward the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

His current research interests include design and control of high-power ac drives, modular multilevel converters, and widebandgap semiconductors and their applications.

**Haiguo Li** received the B.S. and M.S. degrees in electrical engineering from Shanghai Jiaotong University, Shanghai, China, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree with The University of Tennessee, Knoxville, TN, USA.

His research interests include grid requirements impact on converter, grid-connected converter design, and SiC device applications.

**Zhou Dong** (S'19) received the B.S. and M.S. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree in electrical engineering with The University of Tennessee, Knoxville, TN, USA.

His research interests include widebandgap semiconductor device applications, magnetic components modeling, and electrical power system protections.

**Craig Timms** received the B.S. degree in electrical engineering from the University of Dayton, Dayton, OH, USA, in 2016, and the M.S. degree from The University of Tennessee, Knoxville, TN, USA, in 2018.

He is currently a Power Electronics Engineer working on electric powertrains with Seres, Santa Clara, CA, USA.

**Fei Wang** (S'85–M'91–SM'99–F'10) received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, and the M.S. and Ph.D. degrees from the University of Southern California, Los Angeles, CA, USA in 1982, 1985, and 1990, respectively, all in electrical engineering.

From 1990 to 1992, he was a Research Scientist with the Electric Power Lab, University of Southern California. In 1992, he joined as an Application Engineer with the Department of GE Power Systems Engineering, Schenectady, NY, USA. From 1994 to 2000, he was a Senior Product Development Engineer with the GE Industrial Systems, Salem, VA, USA. From 2000 to 2001, he was the Manager of Electronic and Photonic Systems Technology Lab, GE Global Research Center, Schenectady, NY, USA and Shanghai, China. In 2001, he joined as a Research Associate Professor with the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, and became an Associate Professor in 2004. From 2003 to 2009, he was the CPES Technical Director. Since 2009, he has been a Professor and the Condra Chair of Excellence in Power Electronics with The University of Tennessee and Oak Ridge National Lab, Knoxville, TN, USA. He is a Founding Member and the Technical Director of the multiuniversity NSF/DOE Engineering Research Center for Ultra-wide-area Resilient Electric Energy Transmission Networks, The University of Tennessee. His research interests include power electronics and power systems.

Dr. Wang is a Fellow of the U.S. National Academy of Inventors.

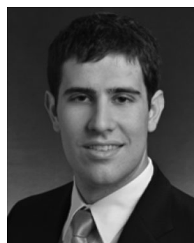
**Leon M. Tolbert** (S'88–M'91–SM'98–F'13) received the bachelor's, M.S., and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, GA, USA, in 1989, 1991, and 1999, respectively, all in electrical engineering.

From 1991 to 1999, he was with Oak Ridge National Laboratory, Oak Ridge, TN, USA. He was appointed as an Assistant Professor with the Department of Electrical and Computer Engineering, The University of Tennessee, Knoxville (UTK), in 1999. He is currently the Min H. Kao Professor with the Min H. Kao Department of Electrical Engineering and Computer Science, The University of Tennessee. He is also a Founding Member of the NSF/DOE Engineering Research Center, Center for Ultra-wide-area Resilient Electric Energy Transmission Networks, UTK. He is also a part-time Senior Research Engineer with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory.

Dr. Tolbert is a Registered Professional Engineer in the state of Tennessee. He was a recipient of the 2001 IEEE Industry Applications Society Outstanding Young Member Award, and six prize paper awards from the IEEE Industry Applications Society and IEEE Power Electronics Society. From 2007 to 2013, he was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS. From 2010 to 2012, he was elected to serve as a Member-at-Large for the IEEE Power Electronics Society Advisory Committee; from 2011 to 2012, as the Chair of the PELS Membership Committee; and from 2012 to 2014, a member of the PELS Nominations Committee. From 2014 to 2017, he was the Paper Review Chair for the Industry Power Converter Committee of the IEEE Industry Applications Society.

**Benjamin J. Blalock** (S'86–M'97–SM'06) received the B.S. degree from The University of Tennessee (UT), Knoxville, TN, USA, and the M.S. and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, GA, USA, in 1991, 1993, and 1996, respectively, all in electrical engineering.

He is the Blalock-Kennedy-Pierce Professor of analog electronics with the Department of Electrical Engineering and Computer Science, UT, where he directs the Laboratory of Integrated Circuits and Systems. His research interests include analog/mixed-signal integrated circuit design for extreme environments (both wide temperature and radiation) across multiple semiconductor technologies, ultralow power analog signal processing, multichannel monolithic instrumentation systems, mixed-signal/mixed-voltage circuit design for systems-on-a-chip, and gate drive integrated circuits for wide-bandgap (SiC and GaN) power electronics. He has coauthored more than 200 refereed papers.



**Daniel Costinett** (S'10–M'13–SM'18) received the Ph.D. degree in electrical engineering from the University of Colorado Boulder, Boulder, CO, USA, in 2013.

He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville (UTK), TN, USA. Prior to joining UTK, he was an instructor with Utah State University, in 2012. He is currently a Codirector of Education and Diversity with the National Science Foundation/Department of Energy Research Center for Ultra-wide-area Resilient Electric Energy Transmission Networks. He is also a Joint Faculty with the Power Electronics and Electric Machinery Research Group, Oak Ridge National Laboratory. His research interests include resonant and soft switching power converter design, high-efficiency wired and wireless power supplies, on-chip power conversion, medical devices, and electric vehicles.

Dr. Costinett was a recipient of the National Science Foundation CAREER Award in 2017. He currently serves as an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS.

**Benjamin B. Choi** received the B.S., M.S., and Ph.D. degrees from the Department of Mechanical Engineering, University of Illinois at Urbana Champaign, Champaign, IL, USA, in 1984, 1986, and 1990, respectively.

Since joining NASA GRC in 1990, he has been working on structural dynamics system modeling, analysis, and control, especially in vibration control using magnetic bearing system and artificial intelligence technology for nearly 12 years. Since then, he started looking at the development of a bearingless motor technology for the electric propulsion system for future aircraft and NASA missions. He has also extended his research into suppressing blade resonance using piezoelectric materials or shape memory alloy. During the last ten years, he has been involved in the propulsion electric grid simulator for future turboelectric distributed propulsion aircraft.