Letters

Current Balancing of Paralleled SiC MOSFETs for a Resonant Pulsed Power Converter

Qunfang Wu, *Member, IEEE*, Mengqi Wang, *Member, IEEE*, Weiyang Zhou, *Member, IEEE*, and Xiaoming Wang

***Abstract*—Paralleling silicon carbide (SiC) MOSFETS is a cost-effective solution for increasing pulse current rating. However, the device SiC MOSFETS mismatch and asymmetrical circuit layout would lead to imbalance current of the paralleled SiC MOSFETS. In this letter, we propose a passive approach, that is, a coupled inductor instead of the conventional resonant inductor, which is used for a resonant pulsed power converter. The coupled inductor enables even current sharing of the parallel SiC MOSFETs, and also helps with pulsewidth adjustment, which leads to a simplified system without complex control circuit compared with the active solution. The configuration of the proposed topology, operating principle, imbalance current limitation mechanism, and design guidelines are fully discussed and presented. Additionally, experiments are carried out to verify the analysis and effectiveness of the proposed solution. The proposed method can be extended to the scenario with more than two parallel.**

***Index Terms*—Current sharing, paralleling, pulsed power converter, SiC MOSFET.**

I. Introduction

OZONE is widely used in industrial applications such as food storage, water purification, odor alleviation, and color removal. The most cost-effective and popular method of ozone generation is to break down oxygen molecules in a dielectric barrier discharge (DBD) chamber [1]. Usually, the DBD chamber is fed by a high-frequency power supply to increase the ozone production. As of today, high-frequency resonant converters of various topologies are used for ozone power supplies, such as full bridge, half bridge, and push–pull topologies [2], [3]. For these topologies, the number of power switches is more than one, and each power switch requires its own gate driver circuit, which increases the cost and complexity. To reduce the component count and increase the converters' efficiency, the single-switch resonant converters in [4] and [5] have been proposed, and they are the preferred choice due to their simplicity.

In each of the aforementioned pulse power supplies, the performance mainly depends on the behaviors of the switch devices. The SiC MOSFET has become a favorable alternative due to its faster switching speed, lower switching loss, higher thermal conductivity, and high voltage blocking voltages compared with its Si counterpart, making it the ideal device for pulsed generation applications [5]. However, to date, commercial SiC MOSFETs have had a limited current-rating, and they often require paralleled connection to increase their current-rating for higher power applications. For the parallel operation of SiC MOSFETs, current imbalance has always been an issue, which may result from device mismatch and an asymmetrical circuit layout. Recently, some effective approaches, including both active [6] and passive [7], [8] solutions, have been reported to address this problem. The active method in [6] needs to design the sensor circuit and feedback control, which increases the complexity of the system. In contrast, the passive solution has the advantages of low cost, fast dynamics, and easy design, which make it a preferable approach; however, external gate resistors and extra source inductance were required in [7], and a differential mode choke was added in the drain terminal in [8]. In this letter, we propose an SiC MOSFET single-switch resonant pulsed power converter with the capability of automatic current sharing. A coupled inductor, instead of a conventional resonant inductor, is implemented to realize current balancing and simultaneously assist with accurate pulsewidth adjustment. The operating principle, theoretical analysis of the imbalance mechanism, and design guidelines are discussed in the following sections. We also present experimental results to verify the effectiveness of the proposed converter.

Manuscript received September 5, 2019; revised October 10, 2019; accepted November 1, 2019. Date of publication November 7, 2019; date of current version February 20, 2020. *(Corresponding authors: Mengqi Wang; Weiyang Zhou.)*

The authors are with the Department of Electrical and Computer Engineering, University of Michigan, Dearborn, MI 48128 USA (e-mail: qunfangw@umich.edu; mengqiw@umich.edu; zweiyang@umich.edu; mingmike@umich.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2952326

II. Proposed Pulsed Power Converter and Its Operating Principle

Fig. 1 shows the configuration of the proposed resonant pulsed power converter, which is comprised of an input inductor $L_{\rm in}$, two diodes D_1 and D_2, two SiC MOSFETs S_1 and S_2, a coupled inductor L_c, a resonant capacitor C_r, and a high-frequency transformer *Tr* with a turns ratio of 1:n. The output of *Tr* is connected to the ozone chamber. The ozone chamber is usually modeled as

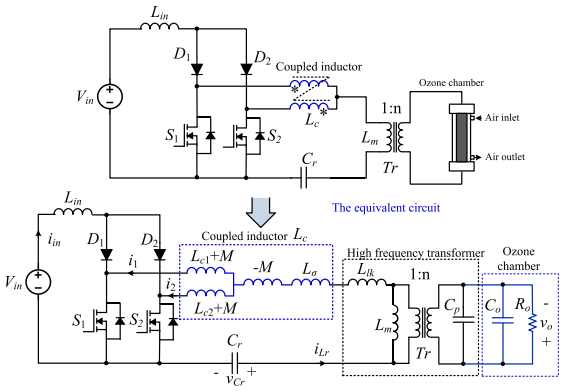

Fig. 1. Configuration of the proposed pulsed power converter and its equivalent circuit.

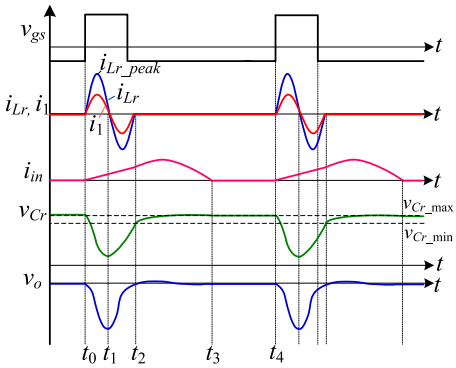

Fig. 2 Key operational waveforms of the proposed converter.

a capacitive load [5], [9], which is represented by a parallel connection of capacitor C_o and resistor R_o. Moreover, based on the widely used high-frequency transformer and coupled inductor model [10], the equivalent circuit of the proposed converter can be obtained, as shown in Fig. 1, where L_{c1}, L_{c2} ($L_{c1} = L_{c2} = L_{cs}$) and M are the self-inductance of each winding and the mutual inductance between them, respectively. L_δ is the leakage inductance of the coupled inductor. L_{lk}, L_m, and C_p are the equivalent leakage inductance, magnetizing inductance, and the equivalent stray capacitance of the high-frequency transformer, respectively.

To simplify the description of the operating principle, all the secondary parameters of the high-frequency transformer are referred to, like the primary ones: $C_{\rm eq} = n^2(C_p + C_o)$ and $R_{\rm eq} = R_o/n^2$. The operation of the proposed power converter is composed of four modes. Fig. 2 shows the key waveforms of the resonant inductor current i_{Lr}, switch S_1 current i_1, input current $i_{\rm in}$, resonant capacitor voltage v_{Cr} and output pulsed voltage v_o. Fig. 3 illustrates the equivalent circuit of Mode 1–Mode 4.

Mode 1 (t_0–t_1): S_1 and S_2 are ON, and prior to t_0, the capacitor C_r has already been charged to $V_{Cr\_\max}$. After t_0, the input voltage applies to the input inductor, and the input current $i_{\rm in}$ increases linearly. Meanwhile, a resonant loop is formed, which consists of L_c, L_{lk}, $C_{\rm eq}$, and C_r, as shown in Fig. 3(a). Note that the transformer magnetizing inductance L_m and the reflected

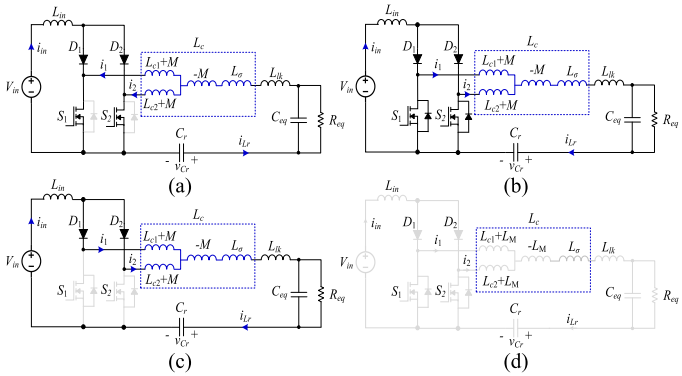

Fig. 3. Equivalent circuit of each model for the proposed converter.

road $R_{\rm eq}$ are large enough to be excluded from the resonance during this fast process. The key expressions of $i_{\rm in}$, i_{Lr}, v_o, V_{cr}, and $V_{Cr\max}$ can be approximately derived as follows:

$$i_{\rm in}(t) = V_{\rm in} \cdot t / L_{\rm in} \tag{1}$$

$$i_{Lr}(t) = V_{Cr\max}\sin(\omega t)/(L_{\rm eq}\omega) \tag{2}$$

$$v_o(t) = nV_{Cr\max}[1 - \cos(\omega t)]/(L_{\rm eq}C_{\rm eq}\omega) \tag{3}$$

$$V_{Cr}(t) = V_{Cr\max}[1 - 1/(L_{\rm eq}C_r\omega^2)] + V_{Cr\max}\cos(\omega t)/(L_{\rm eq}C_{\rm eq}\omega^2) \tag{4}$$

$$V_{Cr\max} = V_{\rm in} + \sqrt{(1 + L_{\rm eq}/L_{\rm in})(V_{\rm in}C_{\rm eq}T_{\rm pulse}/(C_r^2 + C_{\rm eq}^2))} \tag{5}$$

where $T_{\rm pulse}$ represents the pulse voltage width. ω ($\omega = 2\pi f_r$ and f_r is the resonant frequency) and $L_{\rm eq}$ are the resonant angular frequency and equivalent resonant inductance, respectively, which are expressed as follows:

$$\begin{cases} \omega = \sqrt{(C_{\rm eq} + C_r)/(L_{\rm eq}C_{\rm eq}C_r)} \\ L_{\rm eq} = L_{lk} + L_\delta + (L_{cs} - M)/2 \end{cases}. \tag{6}$$

This mode ends at t_1 and the last time is a half resonant period.

Mode 2 (t_1–t_2): At t_1, i_{Lr} is reversed and continues flowing through the channels and the body diodes of S_1 and S_2 simultaneously, since the SiC MOSFET has a relatively large voltage drop on its body diode. The resonant capacitor C_r finishes discharging at the end of Mode 2, and all expressions in this interval are the same as in Mode 1.

Mode 3 (t_2–t_3): At t_2, S_1 and S_2 are OFF, and the input inductor $L_{\rm in}$ takes part in the resonant loop, as shown in Fig. 3(c). The resonant process is similar to that of Mode 1, while the equivalent resonant inductance should be equal to $L_{\rm in}$+$L_{\rm eq}$.

During this interval, switches S_1 and S_2 are turned OFF when currents i_1 and i_2 flowing through of S_1 and S_2 fall to zero. At t_3, the voltage across S_1 and S_2 is charged to $V_{Cr\max}$ and this stage ends.

Mode 4 (t_3–t_4): After t_3, there is no current flowing in the circuit, and the v_{Cr} remains at $V_{Cr\max}$. The equivalent circuit is shown in Fig. 3(d).

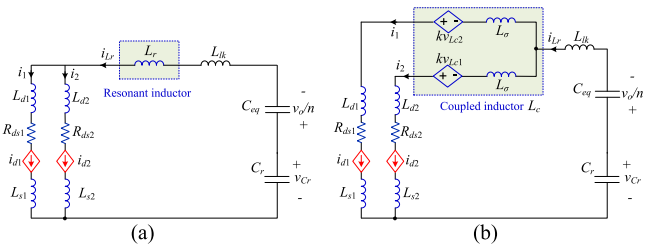

Fig. 4. Equivalent circuit model. (a) Without the coupled inductor. (b) With the coupled inductor.

III. Current Sharing Principle and Design Guidelines

A. Imbalance Current Between Paralleled SiC mosfets

Current imbalance between paralleled SiC MOSFETs is mainly caused by some inevitable factors, such as device mismatch, asymmetrical circuit layout, and unequal junction temperatures, which have been studied and analyzed comprehensively in [7]–[9]. For this converter, similarly, currents through S_1 and S_2 during the critical process of t_0–t_2 are inconsistent due to the mismatched resistance R_{ds1} and R_{ds2} (R_{ds1} and R_{ds2} includes ON-state resistance of the switch and the stray resistance in each power loop), mismatched drain inductance L_{d1} and L_{d2}, and mismatched common source inductance L_{s1} and L_{s2} in the power loop. Fig. 4(a) indicates the equivalent circuit model without the current-sharing solution. In this figure, assume that imbalanced resistance $\Delta R_{ds} = R_{ds1}$–R_{ds2}; imbalanced drain inductance $\Delta L_d = L_{d1}$–L_{d2}; and imbalanced common source inductance $\Delta L_s = L_{s1}$–L_{s2}, such that, the imbalance Δi, caused by mismatched ΔR_{ds} and $\Delta L_d + \Delta L_s$, can be derived as the following equations:

$$\Delta i(R_{ds}) = -K_1(R_{ds2}\sin\omega t - a\omega\cos\omega t) - a\omega K_1 e^{-\frac{R_{ds2}}{a}t} \tag{7}$$

$$\Delta i(\Delta L_{\rm d} + \Delta L_{\rm s}) = -K_2(R_{ds2}\cos\omega t + a\omega\sin\omega t) + R_{ds2}K_2 e^{-\frac{R_{ds2}}{a}t} \tag{8}$$

where

$$\begin{cases} K_1 = \frac{\Delta R_{ds} V_{cr\max}}{2\omega L_{\rm eq}(R_{ds2}^2 + a\omega^2)}, \quad K_2 = \frac{(\Delta L_{\rm d} + \Delta L_{\rm s}) V_{cr\max}}{2L_{\rm eq}(R_{ds2}^2 + a\omega^2)} \\ a = L_{d2} + L_{s2}. \end{cases} \tag{9}$$

Taking the specifications shown in Table I as an example, by (6)–(8), the numerical results of Δi caused by $\Delta L_d + \Delta L_s$ and influenced by ΔR_{ds} are illustrated in Fig. 5(a) and (b) at the input voltage $V_{\rm in} = 300$ V. It can be found that imbalance current Δi is very sensitive to $\Delta L_d + \Delta L_s$ and ΔR_{ds}, and the magnitude of Δi dramatically rises with the increase of ΔR_{ds} and $\Delta L_d + \Delta L_s$. Herein, the pulsed width $T_{\rm pulse}$ is 1.4 μs and Δi reaches its maximum value at the resonant peak current point ($T_{\rm pulse}$/4).

B. Current-Sharing Principle With Coupled Inductor

For ease of derivation and understanding the current sharing principle, the symmetrical coupled inductor model presented in [10] is used for our analysis. Fig. 4(b) demonstrates the equivalent circuit mode with the coupled inductor. According to Kirchhoff's voltage and current laws, the imbalance current Δi can be derived as follows:

$$\Delta i = -\frac{(\Delta L_d + \Delta L_s)\frac{V_{Cr\max}}{2L_{\rm eq}}\cos(\omega t) + \Delta R_{ds}\frac{V_{Cr\max}}{2L_{eq}\omega}\sin(\omega t)}{[L_\delta + L_{d2} + L_{s2} + (k+k^2)L_{cs}]s + R_{ds2}} \tag{10}$$

where $s = j\omega$. k and L_{cs} are the coupling coefficient and self-inductance of the coupled inductor, respectively.

From (10), since $(k+k^2)L_{cs} \gg L_\delta + L_{d2} + L_{s2}$, the imbalance current Δi is mainly limited by the term $(k+k^2)L_{cs}$. Similarly, taking the parameters shown in Table I, for example, the suppression value of Δi can be mapped as shown in Fig. 5(c). We can find that either the larger the self-inductance L_{cs} or the higher the coupling coefficient k, the smaller the imbalance current Δi. However, a large L_{cs} implies a big volume, heavy weight, and greater cost, therefore, this is a tradeoff when designing L_{cs} in practice. Herein, if we set the ratio of imbalanced current γ ($\gamma = \Delta i/i_{Lr}$) to less than 5%, the selection range of L_{cs} and k should be designed to be below the dotted red line, as shown in Fig. 5(c).

TABLE I
Parameters and Parasitic Values

Parameter	Value
Input inductance, L_{in}	2.2 mH
Equivalent capacitance, C_p+C_o	470 pF
Resonant capacitance, C_r	200 nF
Individual resonant inductance, L_r	560 nH
Transformer turn ratio, n	18
Leakage inductance of transformer, L_{lk}	27.5 nH
Source inductance, L_{s2}	12 nH
Mismatched source inductance, ΔL_s	3 nH
Drain inductance, L_{d2}	17 nH
Mismatched drain inductance, ΔL_d	2 nH
Imbalance resistance, ΔR_{ds}	2 mΩ
Self-inductance of coupled inductor, L_s	1.4 μH
Coupling coefficient, k	0.2
Leakage inductance of coupled inductor, L_δ	25 nH

C. Design Guidelines of the Coupled Inductor

When designing the coupled inductor, two factors should be fulfilled. The first one is the pulsewidth of the output voltage $T_{\rm pulse}$, which is determined by the requirement of the ozone chamber. For this converter, $T_{\rm pulse}$ can be calculated by

$$T_{\rm pulse} = 2\pi / \left(\sqrt{\left(\frac{C_{\rm eq} + C_r}{L_{\rm eq}C_{\rm eq}C_r}\right)}\right). \tag{11}$$

Once $T_{\rm pulse}$ is determined, by combining it with parameters $C_{\rm eq}$ and C_r, the equivalent resonant inductance $L_{\rm eq}$ will be determined mandatorily. According to the above analysis, $L_{\rm eq}$ is equal to $L_{lk} + L_\delta + (L_{cs}$–$M)/2$. For example, based on the extracted $C_{\rm eq} = 152.3$ nF and $C_r = 200$ nF for the following prototype, the relationship curve between $T_{\rm pulse}$ and $L_{\rm eq}$ can be plotted as Fig. 6. It can be observed that when the pulse width is set to 1.4 μs, the desired $L_{\rm eq}$ should be designed as 0.58 μH.

The other factor is the imbalance current limitation, which can be calculated by (10). Fig. 7 illustrates the procedure and

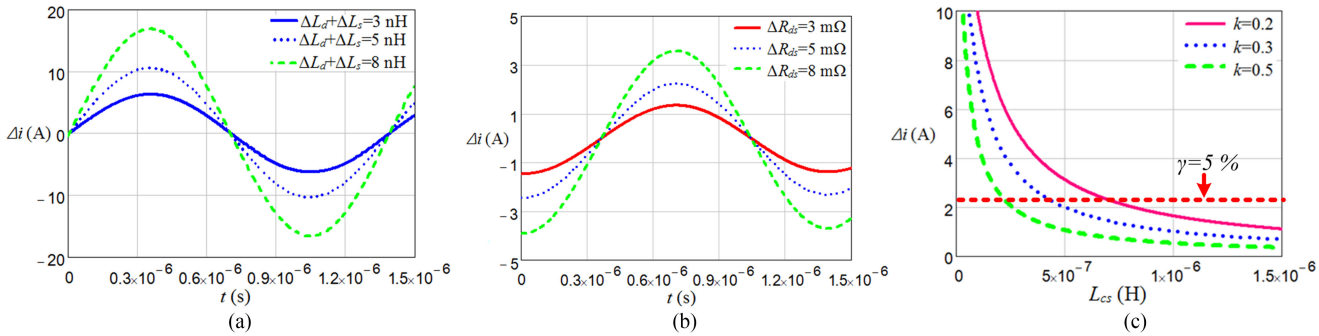

Fig. 5. (a) Imbalance current caused by different mismatched $\Delta L_d + \Delta L_s$ at $V_{\rm in} = 300$ V. (b) Imbalanced current affected by different mismatched ΔR_{ds} at $V_{\rm in} = 300$ V. (c) Imbalanced current limited by self-inductance L_{cs} with different coefficients k.

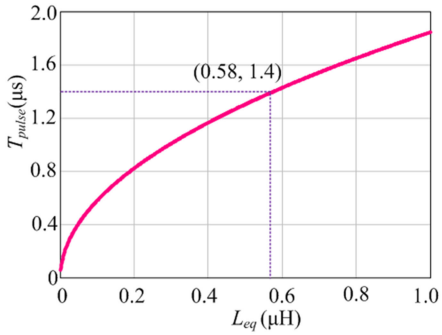

Fig. 6. Relationship curve between the $T_{\rm pulse}$ and $L_{\rm eq}$ with $C_{\rm eq} = 152.3$ nF and $C_r = 200$ nF.

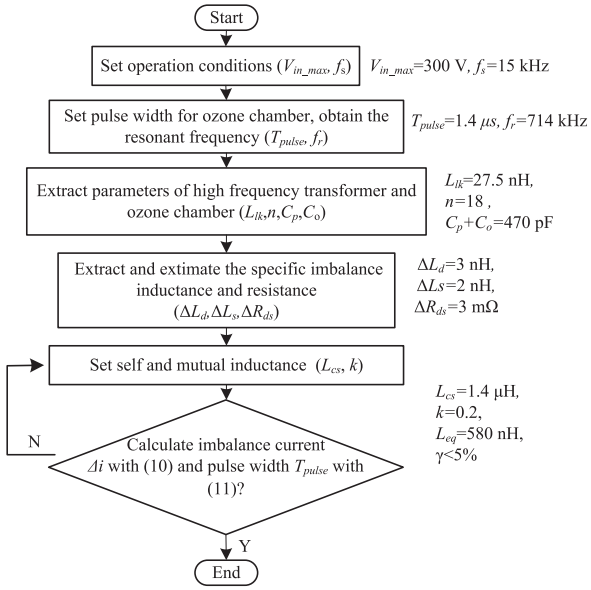

Fig. 7. Design flowchart for the coupled inductor.

design flowchart of the coupled inductor. The parameters in the following experiment are listed beside the corresponding steps. Based on the specifications of the following prototype, the coupled inductor with self-inductance $L_s = 1.4$ μH and coupling coefficient $k = 0.2$ is finally designed to achieve a desired pulse width $T_{\rm pulse} = 1.4$ μs and a ratio of imbalanced current $\gamma < 5\%$.

TABLE II
EXPERIMENT COMPARISON BETWEEN WITH AND WITHOUT COUPLED INDUCTOR FOR CURRENT BALANCING

	Without coupled inductor			With coupled inductor		
V_{in} (V)	200	250	300	200	250	300
i_{Lr_peak}(A)	57	72	90	57	72	90
Δi(A)	4.5	6	10	0.5	1.5	2.1
γ	15.8%	16.7%	22.2%	1.8%	4.2%	4.6%

IV. EXPERIMENTAL VERIFICATION AND EXTENSION

A. Experimental Verification

A converter prototype has been built to verify the effectiveness of the proposed solution. The converter has a 200–300 VDC input, –8 kV maximum output, 1.4 μs pulsewidth, and 15 kHz pulse generation frequency. Two SiC MOSFETs C2M0080120D from Cree are implemented and the magnetic core OR43622UG with three winding turns and some additional gap is designed as the coupled inductor. A TI TMS320F28335 DSP control board is used to generate the gate signal for S_1 and S_2. The PCB parameters are extracted by the software ANSYS Q3D, and combined with the spice mode and datasheet of C2M0080120D, the key parameters are obtained and listed in Table I. In addition, a conventional resonant inductor (L_r) is employed to realize the same pulsewidth output, and to investigate the performance of imbalance current without the coupled inductor under the same condition.

Fig. 8 demonstrates the key experimental waveforms of the gate driver voltage v_{gs}, output pulse voltage v_o, and currents through two switches, i_1 and i_2, at different input voltages i.e., 200, 250, 300 V, respectively. Fig. 8(a)–(c) are the results of a no current-balancing solution (with a conventional resonant inductor) and Fig. 8(e) and (f) are the waveforms of the proposed solution. The key characteristics are quantified in Table II. From Fig. 8 and Table II, it can be seen that the output pulsewidth is around 1.4 μs under all conditions, and the maximum output pulse voltage reaches –8 kV, which coincides well with the designed specification. The sum of the currents through two switches has approximately the same value with or without the coupled inductor, however, compared with the scenario without the coupled inductor, the imbalance current of the peak value of the resonant current is reduced from 10 to 2.1 A, which means

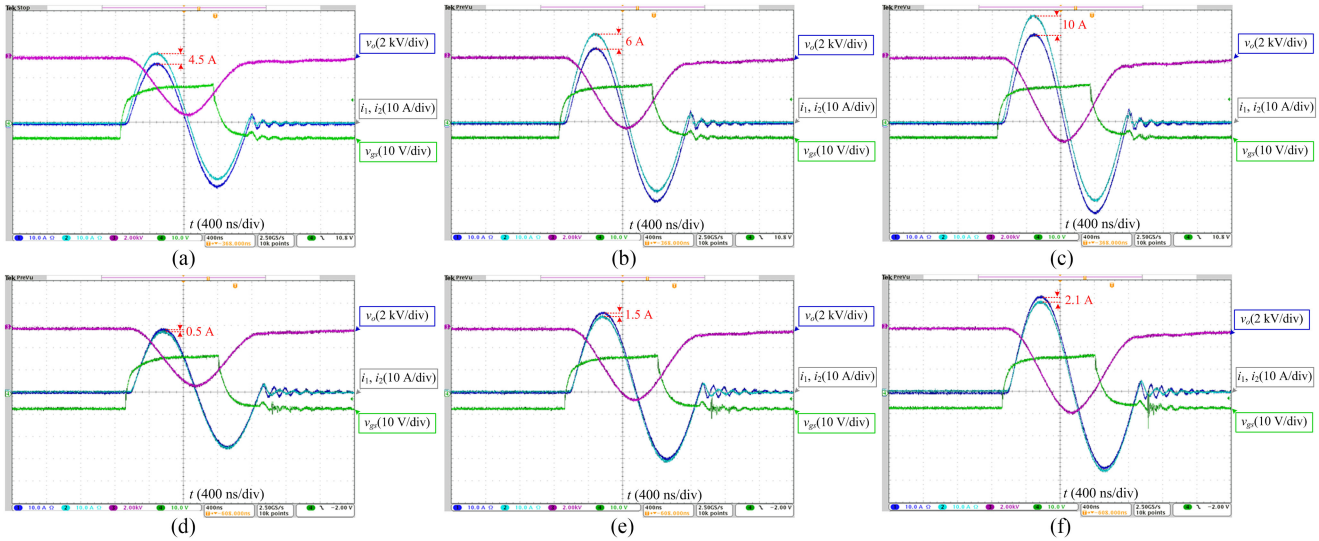

Fig. 8. Experimental results at different currents through switch S_1 and S_2 under different input voltages $V_{\text{in}} = 200$, 250, and 300 V, respectively. (a)–(c) With an individual inductor. (d)–(f) With the coupled inductor.

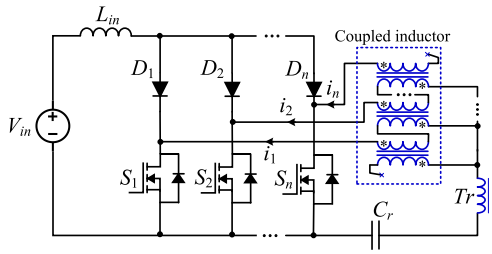

Fig. 9. Extension of the proposed current balancing method.

the ratio of imbalanced current can be reduced from 22.2% to 4.6%, which is less than the above set value of 5%. That is to say, the proposed solution has an obvious effect.

B. Extension of the Proposed Current Balancing Solution

The proposed method can be extended to the scenario with more than two parallel SiC MOSFETs, and theoretically, the maximum number of parallel devices can be infinite. Fig. 9 shows the extension circuit with n parallel SiC MOSFETs, where each SiC MOSFET branch involves two windings in series connection. Two neighbor devices couple with each other to balance the current through each SiC MOSFET. More importantly, the equivalent inductance of the coupled inductors helps with pulsewidth adjustment for the pulsed generator.

V. Conclusion

In this letter, a passive current balancing approach with a coupled inductor is proposed to limit the imbalance current of parallelled SiC MOSFETs in a resonant pulsed converter. The employed coupled inductor not only enables the current-sharing effect, but also helps with the pulsewidth adjustment. The imbalance current and its suppression mechanism, design guidelines, are discussed in depth, and the experimental results show that, at the maximum current condition, the ratio of the imbalanced current given the proposed solution can be reduced from 22.2% to 4.6% compared with that of the solution without the coupled inductor. The proposed solution can be extended to the application with more than two parallel SiC MOSFETS.

References

[1] B. L. Loeb, C. M. Thompson, J. Dragob, H. Takahara, and S. Baig, "Worldwide ozone capacity for treatment of drinking water and wastewater: A review," *Ozone, Sci. Eng.*, vol. 34, no. 1, pp. 64–77, Jan. 2012.

[2] V. Kinnares and P. Hothongkham, "Circuit analysis and modeling of a phase-shifted pulse width modulation full-bridge-inverter-fed ozone generator with constant applied electrode voltage," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1739–1752, Jul. 2010.

[3] J. M. Alonso, J. Garcia, A. J. Calleja, J. Ribas, and J. Cardesin, "Analysis, design, and experimentation of a high-voltage power supply for ozone generation based on current-fed parallel-resonant push-pull inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1364–1372, Sep./Oct. 2005.

[4] B. Kang, K. S. Low, J. J. Soon, and Q. V. Tran, "Single-switch quasi-resonant DC-DC converter for a pulsed plasma thruster of satellites," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4503–4513, 2017.

[5] Q. Wu, M. Wang, W. Zhou, X. Wang, G. Liu, and C. You, "Analytical switching model of a 1200V SiC MOSFET in a high-frequency series resonant pulsed power converter for plasma generation," *IEEE Access*, vol. 7, pp. 99622–99632, Jul. 2019.

[6] Z. Zhang, J. Dix, F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[7] Y. Mao, Z. Miao, C. M. Wang, and K. D. T. Ngo, "Passive balancing of peak currents between paralleled MOSFETs with unequal threshold voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3273–3277, May 2017.

[8] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke" *IEEE Trans. Ind. Electron.*, vol. 99, no. 2, pp. 1508–1519, Feb. 2020.

[9] Z. Salam, M. Facta, and M. Amjad, "Dielectric barrier discharge ozonizer using the transformerless single-switch resonant converter for portable applications," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 2197–2206, May/Jun. 2014.

[10] G. Zhu, B. McDonald, and K. Wang, "Modeling and analysis of coupled inductors in power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Washington, DC, USA, Feb. 2009, pp. 83–89.