An *LLC*-Based Highly Efficient S2M and C2C Hybrid Hierarchical Battery Equalizer

Faxiang Peng, *Student Member, IEEE*, Haoyu Wang, *Senior Member, IEEE*, and Zhengqi Wei

***Abstract*—In battery equalization systems, string-to-cell (S2C) and cell-to-cell (C2C) structures each has its unique advantages and disadvantages regarding efficiency, components count, energy-flow-path length, and circuit extendibility. In this article, a novel hybrid battery equalizer combining the advantages of both S2C and C2C structures is proposed. The proposed hierarchical equalizer is based on half-bridge *LLC* resonant converter in the string-to-module layer and buck–boost converter in the two-level C2C layer. The characteristics of *LLC* converter are analyzed to fit the voltage equalization applications. The design considerations of *LLC* converter and buck–boost converter are addressed to ensure zero-voltage-switching among all MOSFETs and the optimal operation of each layer. Therefore, high conversion efficiency can be achieved in both layers. Comparing with other equalization techniques, the proposed hybrid structure achieves a good compromise among efficiency, components count, energy-flow-path length, and circuit extendibility. To validate the concept, a high switching frequency experimental platform is designed and tested to balance eight series-connected batteries. The experimental results well validate the theoretical analysis and the proposed design methodology.**

***Index Terms*—Battery equalizer, buck–boost converter, *LLC* converter, zero-voltage-switching (ZVS).**

I. Introduction

LOW-VOLTAGE lithium-ion battery cells are typically series-connected to meet the voltage and power requirements of specific applications, such as electric vehicles and energy storage systems [1]. In the battery string, cell variance might incur mismatch issues during charging and discharging processes: certain cells may be overcharged or depleted [2]. Therefore, battery equalizers are required to mitigate this mismatch issue. Generally, efficiency, components count, energy-flow-path length, and circuit extendibility are the figure of merits to evaluate the performance of battery equalizers.

Conventional dissipative equalizers suffer from zero efficiency and heat management issues [2]. To improve, non-dissipative equalizers have been developed. Fig. 1(a) showcases a mainstream cell-to-cell (C2C) equalization structure. The equalizer unit (EU) transfers energy between two adjacent cells.

Manuscript received May 14, 2019; revised September 8, 2019; accepted October 11, 2019. Date of publication October 16, 2019; date of current version February 20, 2020. This work was supported by the National Natural Science Foundation of China under Grant 51607113. Recommended for publication by Associate Editor F. H. Khan. *(Corresponding author: Haoyu Wang.)*

The authors are with the Power Electronics and Renewable Energies Laboratory, School of Information Science & Technology, ShanghaiTech University, Shanghai 201210, China (e-mail: pengfx@shanghaitech.edu.cn; wanghy.shanghaitech@gmail.com; weizhq1@shanghaitech.edu.cn).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2948040

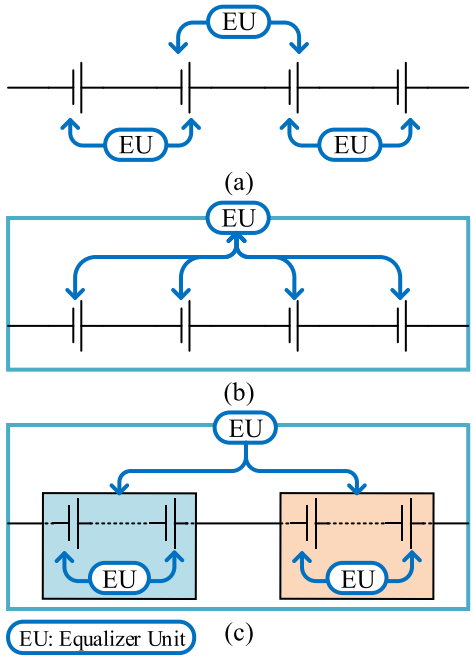


Fig. 1. Energy flow of non-dissipative equalization techniques. (a) Bidirectional cell-to-cell (C2C). (b) Bidirectional string-to-cell (S2C). (c) Modularized equalization structure.

To realize this EU, buck–boost converter [3], [4] and switched capacitor [5], [6] have been employed. The energy flow path of the C2C structure is determined by the distance between two cells. Therefore, both equalization speed and conversion efficiency degrade with the increase of energy-flow-path length. To reduce the average energy-flow-path length between cells, multiwinding transformer [7], double-tied switched capacitor [8], and star-structured switched capacitor [9] are introduced. However, the equalization speed of switched capacitor-based equalizers is extremely slow when the cell voltage difference is trivial. Generally, those C2C structures own the benefit of good circuit extensibility. However, it typically comes with long energy-flow length, especially for the long string scenarios.

Fig. 1(b) showcases a bidirectional string-to-cell (S2C) equalization structure. The energy can be transferred from the entire string to a single cell. In [10]–[13], a multiplex network is implemented to select a specific energy transfer path. However, the switch count in this multiplex network is typically high. In [14] and [15], a multiwinding transformer is introduced to reduce the switch count. However, the design complexity of the transformer scales up rapidly with the increase of string

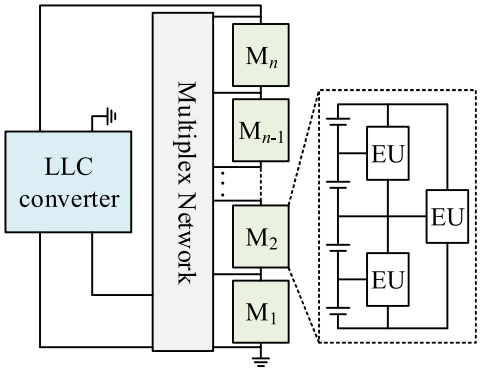


Fig. 2. Proposed hybrid equalization structure with n cell modules.

length. Moreover, the transformer leakage inductance incurs transients issue, which deteriorates the equalizing performance. Similarly, in [16]–[18], voltage multipliers (VMs) composed of diodes and capacitors are introduced to reduce the switch count. However, the diode forward voltage drop counts a considerable portion of the cell voltage. Thus, the conversion efficiency is low. Generally, those S2C structures own the benefits of direct energy transfer path and shared EU. However, a multiplex network with high switch count is typically required. Moreover, in the worst scenario with only one cell overcharged, the equalization speed becomes extremely slow.

To further improve the overall performance, various modularized equalization techniques with a combination of module-equalizer and cell-equalizer have recently been reported. Fig. 1(c) shows the schematic of a two-layer-based structure [19]–[23]. As shown, module-equalizer and cell-equalizer are configured as the outer and inner layers, respectively. Module-equalizer and cell-equalizer can operate simultaneously, which facilitate an accelerated equalization. In [24] and [25], a multilayer structure is proposed. This structure can effectively shorten the average energy-flow-path and improve the equalization speed. In [26]–[28], a multiwinding transformer is introduced into the modularized equalizer, which improves the circuit extensibility and equalization speed.

Inspired by the modularized structures, a hybrid hierarchical equalization structure is proposed in this article. The proposed hybrid structure is featured with enhanced efficiency and circuit extensibility. As shown in Fig. 2, this hybrid structure combines the *LLC* resonant converter-based string-to-module (S2M) equalizer and buck–boost converter-based C2C equalizer. In S2M equalizer, a multiplex network with moderate switch count is introduced to select the specific energy-flow path. The *LLC*-based equalizer is shared among all the modules.

The main contributions of this article are summarized as follows. First, a novel *LLC*-based S2M and C2C hybrid hierarchical battery equalizer is proposed. The proposed hybrid structure achieves a good compromise among efficiency, components count, energy-flow-path length, and circuit extendibility. Second, a comprehensive design methodology is proposed to guide the design of *LLC*-based constant-current module equalizer. Third, an advanced recovery-effect immune equalization strategy is proposed to improve the balancing accuracy.

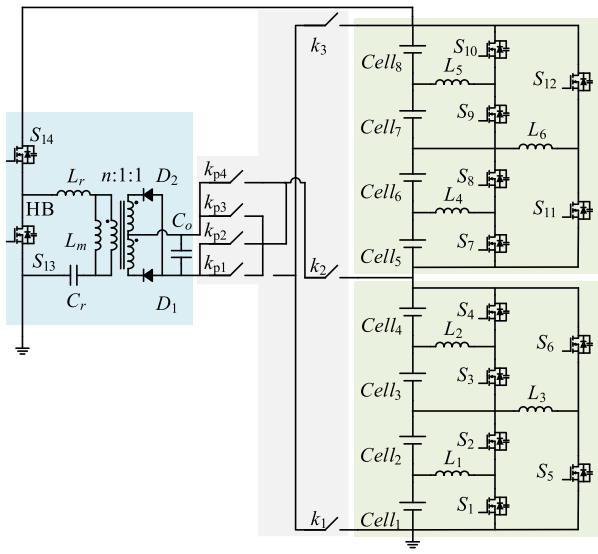


Fig. 3. Detailed schematic of the proposed battery equalizer with eight cells.

II. Operation Principles

A. S2M and C2C Hybrid Architecture

Fig. 3 shows the schematic of the proposed hybrid equalizer with two modules and eight cells. As shown, the input of the *LLC*-based module equalizer is connected to the terminal of the string, while the output is connected to the multiplex network. The multiplex network consists of four polarity-selecting switches (k_{p1}–k_{p4}) and three module-selecting switches (k_1–k_3). Different equalization paths from the string to module can be directly established by properly configuring the multiplex network. Thus, the *LLC*-based module equalizer can be shared by different modules via the multiplexer. This reduces the required semiconductor devices count. Within each module, the buck–boost-based cell equalizer unit serves to equalize each single cell. By combining the module equalizer and the cell equalizer, a hybrid hierarchical equalization architecture can be configured. This architecture inherits the advantages of both equalization techniques while avoids corresponding disadvantages.

B. LLC-*Based Module Equalizer*

When Module 1 is undercharged, the string to module equalization is activated. Meanwhile, k_{p1}, k_{p4} and k_1, k_2 turn ON and k_{p2}, k_{p3} and k_3 turn OFF. Fig. 4 shows the key waveforms of *LLC*-based module equalizer when it operates at resonant frequency. The primary switches (S_{13} and S_{14}) turn ON and OFF complementarily with certain dead time t_d. The generated square-wave is fed to the resonant tank (L_r, C_r, and L_m). Meanwhile, the discharging current of string i_{string} flows into the resonant tank via S_{14}. Thus

$$I_{\text{string}} = \frac{1}{T_s}\int_0^{\frac{T_0}{2}} i_{Lr}(t)dt \tag{1}$$

where I_{string} is the dc value of i_{string}, T_s is the switching period, T_0 is the resonant period. As shown in Fig. 4, the resonant

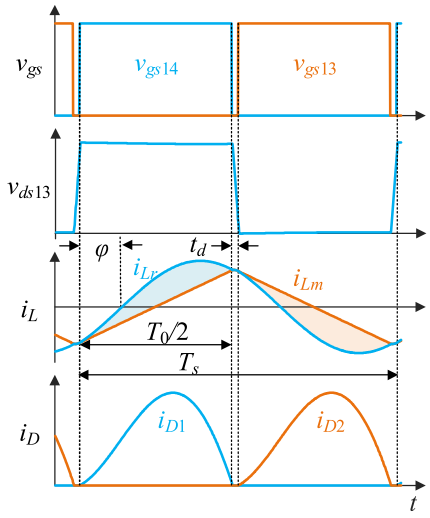


Fig. 4. Key waveforms of *LLC*-based module equalizer.

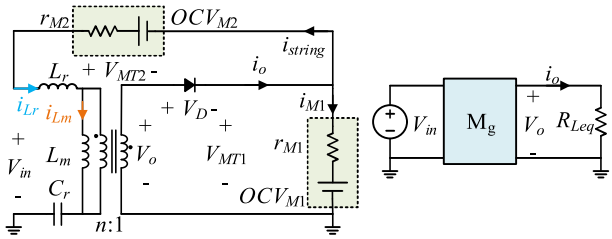


Fig. 5. Equivalent circuit when Module 1 is undercharged.

inductor current i_{Lr} is sinusoidal and the magnetizing current i_{Lm} is triangular. On the secondary side, the rectifier diodes (D_1 and D_2) conduct alternatively to establish an energy-flow path. The difference between i_{Lr} and i_{Lm} flows into the rectifier and charges Module 1. This means

$$\frac{1}{Ts/2}\int_0^{\frac{T_0}{2}}[i_{Lr}(t)-i_{Lm}(t)]dt=\frac{I_o}{n} \tag{2}$$

where I_o is the dc output current, n is the turns ratio of the transformer. Thus, the string can charge the undercharged Module 1 via the *LLC*-based module equalizer. Correspondingly, during one switching period, the dc charging current of Module 1 I_{M1} can be derived as follows:

$$I_{M1}=I_o-I_{\text{string}}=\frac{2\sqrt{2}I_{\text{rms},Lr}(2n-1)\cos(\varphi)}{\omega_0 T_s} \tag{3}$$

where $I_{\text{rms},Lr}$ is the rms value of i_{Lr}, ω_0 is the angular resonant frequency, φ is the initial phase of i_{Lr}.

Fig. 5 shows the equivalent circuit when Module 1 is undercharged. The modules are modeled by an ideal voltage source (OCV_{Mi}) with certain internal resistance (r_{Mi}). Here, OCV_{Mi} represents the open-circuit voltage of Module i. In Fig. 5, the string terminal voltage is applied to the input port of module equalizer ($V_{\text{in}}=V_{MT1}+V_{MT2}$). Meanwhile, V_o charges Module 1 via the multiplex network. Thus, V_o equals $V_{MT1}+V_D$ by considering the forward voltage drop of rectifier diodes.

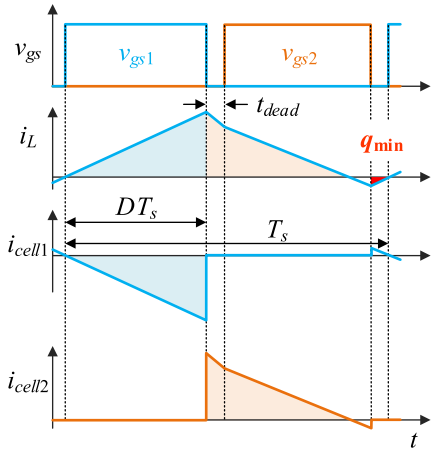


Fig. 6. Key waveforms of buck–boost-based cell equalizer unit.

The output current can be expressed as follows:

$$I_o=\frac{V_o}{R_{Leq}}=\frac{V_{MT1}+V_D}{R_{Leq}} \tag{4}$$

where R_{Leq} is the equivalent load resistance of the module equalizer. Combining (1)–(4), the dc charging current of Module 1 I_{M1} can be derived as follows:

$$I_{M1}=\left(1-\frac{1}{2n}\right)\frac{V_{MT1}+V_D}{R_{Leq}}. \tag{5}$$

C. Buck–Boost-Based Cell Equalizer

As shown in Fig. 3, in each module, every two adjacent cells or sub-strings are parallel to a buck–boost-based cell equalizer unit. This provides a bidirectional and flexible energy flow path. Here, we focus on basic equalization unit to interpret the operation principles. Fig. 6 shows the corresponding key waveforms in one switching period. When the voltage mismatch occurs, the two MOSFETs (S_1 and S_2) turn ON and OFF complementarily following the buck–boost switching pattern. The excessive charge of the source cell (indicated by the blue region in Fig. 6) is transferred to the inductor L_1 and the stored energy in L_1 is further transferred to the target cell (indicated by the orange region in Fig. 6). During the commutation, the body diode of target side MOSFET S_2 provides the freewheeling path for the inductor current i_L. Therefore, the body diode conducts before the conduction of the MOSFET channel, which establishes the ZVS turn-ON condition for S_2.

On the other hand, to achieve ZVS turn-ON of the source side MOSFET S_1, i_L must be slightly negative before S_2 turns OFF. This means the cell equalizer must be controlled to operate in bipolar continuous conduction mode (CCM). The negative i_L discharges and charges the output capacitance C_{oss} of S_1 and S_2, respectively. The charge Q transferred from L to those two C_{oss} is expressed as follows:

$$Q=\Delta VC_{oss}=2(V_{CSource}+V_{CTarget}+V_d)C_{oss} \tag{6}$$

where V_d is the forward voltage drop of the MOSFET body diode, $V_{CTarget}$ and $V_{CSource}$ are the terminal voltage of source

cell (with higher voltage) and target cell (with lower voltage). Moreover, the dead time t_{dead} must be properly designed to ensure both ZVS turn-ON of S_1 and a minimized circulating current. The required minimum charge $q_{\min}$ (indicated by the red region in Fig. 6) stored in L is expressed as follows:

$$q_{\min} = \frac{1}{2} t_{\text{dead}} i_{L,\min} = \frac{1}{2} t_{\text{dead}}^2 \frac{V_{Csource}}{L}. \tag{7}$$

Thus, the dead band should be designed as follows:

$$t_{\text{dead}} \geq \sqrt{\frac{4\left(V_{CSource} + V_{CTarget} + V_d\right)}{V_{CSource}} L C_{oss}}. \tag{8}$$

Since i_L decreases to negative before S_2 turn OFF, the constrains of duty cycle D can be derived as follows:

$$D \leq \frac{V_{CTarget}}{V_{CSource} + V_{CTarget}} - \frac{V_{CTarget} - V_d}{\left(V_{CSource} + V_{CTarget}\right) T_s} t_{\text{dead,min}}. \tag{9}$$

Thus, both the conversion efficiency and a suitable equalization speed can be realized by optimizing D and t_{dead}. In each module, the cells can be balanced without considering the operation condition of module equalizer. This simplifies the control algorithm of the entire system. The detailed analysis and design considerations for the bipolar buck–boost-based cell equalizer have been presented in [25]. Thus, the following section mainly focuses on the analysis and design of the module equalizer.

III. Key Design Considerations

A. Design Consideration of the Proposed Hybrid Equalizer

This article proposes a hybrid equalizer that combining the *LLC* resonant converter-based string-to-module (S2M) equalizer and buck–boost converter-based C2C equalizer shown in Fig. 2. To design such a hybrid and overall optimized equalization structure, the following considerations should be included.

1) To obtain more energy-flow path, the two-layer buck–boost C2C equalizer and the *LLC*-based S2M equalizer are combined to build the hierarchical structure, which provide a more available energy-flow path.
2) To achieve a high conversion efficiency, the significant switching loss in high switching frequency is reduced by addressing the optimal design considerations of *LLC* and buck–boost, which ensure ZVS turn-ON of all MOSFETs.
3) To reduce the components count of this hybrid method, the modularized design concept with shared module equalizer is introduced and a multiplex network with moderate switch number is utilized to build the direct energy-flow path of module balancing.
4) To improve the circuit extendibility, the cell equalizer inherits the merit of traditional C2C structure that easily increases the equalizer unit when the cell number scales up.

In long cell string scenarios, following the design considerations, the proposed hybrid hierarchical equalization structure can flexibly configure the number of single cells and cell modules to fit such applications.

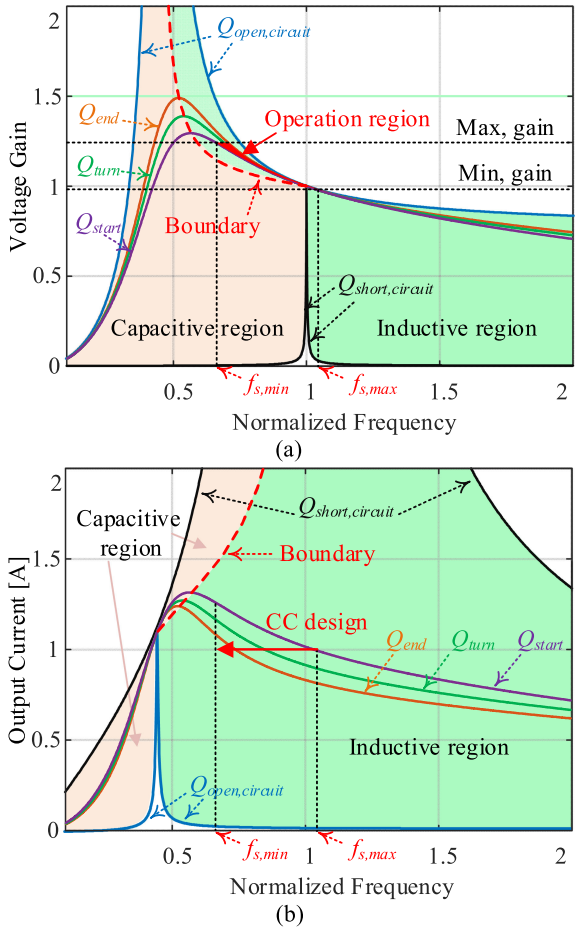


Fig. 7. Electrical profiles of *LLC* converter based on FHA. (a) Voltage gain. (b) Output current.

B. Constant Current Balancing of Module Equalizer

According to the *LLC* operation analysis in [29], based on the first harmonic approximation (FHA) technique, the dc voltage gain of *LLC* converter is expressed as follows:

$$\mathrm{M}_g = \frac{n(V_{MT1} + V_D)}{\left(V_{MT1} + V_{MT2}\right)/2} = \frac{1}{\sqrt{\left(1 + \frac{1}{L_n} - \frac{1}{f_n^2 L_n}\right)^2 + Q_e^2 \left(f_n - \frac{1}{f_n}\right)^2}} \tag{10}$$

where L_n is the inductance ratio ($L_n = L_m/L_r$), f_n is the normalized frequency ($f_n = f_s/f_0$), f_0 is the resonant frequency, and Q_e is the quality factor of the resonant tank ($Q_e = \pi^2\sqrt{L_r/C_r}/8n^2R_{Leq}$).

Correspondingly, the curves of voltage gain versus normalized frequency under different load conditions are depicted in Fig. 7(a). According to the operation characteristics of the *LLC* converter, to enhance the conversion efficiency and achieve the purpose of module voltage equalization, the *LLC*-based module

equalizer should be designed to operate in the vicinity of resonant frequency, as highlighted in Fig. 7(a). Since the output voltage and conversion efficiency vary during the equalization process, the voltage gain of the designed module equalizer should fully cover the potential voltage range.

For the string with two modules, each module voltage is balanced to half of the string voltage. According to (10), the transformer turns ratio *n* can set as unity due to the half-bridge structure. Meanwhile, when the voltage of every single cell varies, the potential module voltage can be derived as follows:

$$\begin{cases} V_{MT1,\min} = mV_{C,\min} + I_{M1}r_{M1} \\ V_{MT1,\max} = mV_{C,\max} + I_{M1}r_{M1} \end{cases} \tag{11}$$

where *m* is the cell number in each module, $V_{C,\max}$ and $V_{C,\min}$ are the maximum and minimum cell voltages, respectively. Thus, the required voltage gain can be expressed as follows:

$$\begin{cases} \mathrm{M}_{g,\min} = \frac{nV_{o,\min}}{V_{\text{in}}/2} = \frac{n(mV_{C,\min}+I_{M1}r_{M1}+V_D)}{(V_{MT1}+V_{MT2})/2} \\ \mathrm{M}_{g,\max} = \frac{nV_{o,\max}}{V_{\text{in}}/2} = \frac{n(mV_{C,\max}+I_{M1}r_{M1}+V_D)}{(V_{MT1}+V_{MT2})/2}. \end{cases} \tag{12}$$

As shown in Fig. 7(a), in the beginning phase of the equalization (as the purple curve indicates), if the peak voltage gain is higher than the required maximum value, the *LLC* converter would always operate in the inductive region. This facilitates a highly efficient equalization process.

According to (4) and (11), when Module 1 is being charged, the equivalent load resistance R_{Leq} may vary. This means the operation state of the module equalizer changes accordingly. This increases the complexity of the parameter design process. However, if I_o is controlled as constant, the charging process is controllable. By integrating (4) and (10), I_o can be derived as follows:

$$I_o = \frac{2n\left(V_{MT1}+V_{MT2}\right)/\pi^2}{\sqrt{\frac{L_r}{C_r}\left(\frac{1}{Q_e^2}\left(1+\frac{1}{L_n}-\frac{1}{f_n^2 L_n}\right)^2+\left(f_n-\frac{1}{f_n}\right)^2\right)}}. \tag{13}$$

Based on (13), Fig. 7(b) shows the output current curves versus normalized frequency under different load conditions. As shown, for a specific resonant circuit, I_o can be regulated by modulating f_s correspondingly during the entire charging process. This means a controllable module equalization is achievable. In this article, a closed-loop PI controller is introduced to regulate the output current. This ensures both a controllable module equalization and a simplified parameters design of the *LLC* converter. With constant I_o, the possible load variation range is as follows:

$$\frac{V_{o,\min}}{I_o} = R_{Leq,\min} \le R_{Leq} \le R_{Leq,\max} = \frac{V_{o,\max}}{I_o}. \tag{14}$$

Therefore, the possible variation range of Q_e is as follows:

$$\frac{\pi^2 I_o\sqrt{L_r/C_r}}{8n^2V_{o,\max}} = Q_{e,\text{end}} \le Q_e \le Q_{e,\text{start}} = \frac{\pi^2 I_o\sqrt{L_r/C_r}}{8n^2V_{o,\min}}. \tag{15}$$

As concluded in [30], the attainable peak voltage gain is affected by the combination of L_n and Q_e. Thus, by choosing a suitable L_n to meet the Q_e range, the required voltage gain can be achieved, as shown in Fig. 7(a).

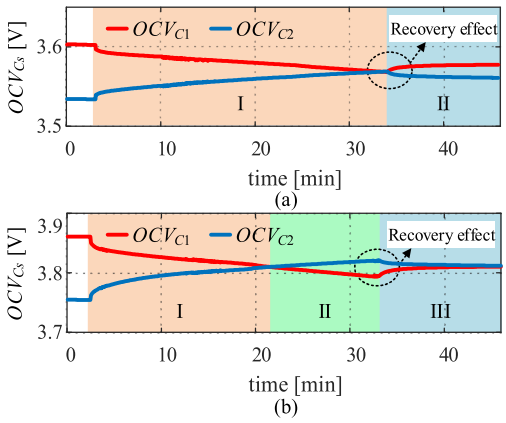


Fig. 8. Open circuit voltages with different equalization stages. (a) Without recovery-eliminating stage. (b) With recovery-eliminating stage.

C. ZVS Conditions for Module Equalizer

As analyzed in [30], to achieve a high conversion efficiency by considering both conduction loss and switching loss for module equalizer, L_m should be optimized to both ensure ZVS and to minimize the circulating current. Thus

$$L_m = \frac{T_0 t_d}{16C_{oss}}. \tag{16}$$

Meanwhile, L_m can be derived as follows:

$$L_m = \frac{4n^2 L_n Q_e R_{Leq}}{\pi^3 f_0}. \tag{17}$$

This equation indicates that for a designed L_m, the product of L_n and Q_e is fixed. This means once Q_e is chosen, L_n can be calculated correspondingly. Therefore, by integrating (15)–(17), L_n, Q_e, and L_m can be designed to meet the module equalization requirement. Moreover, with the predesigned f_0, the resonant parameters (L_m, L_r, and C_r) can be designed based on the calculated L_n and Q_e.

D. Recovery Effect Immune Equalization Strategy

Lithium-ion batteries are featured with the recovery effect [31]. When the battery is charged/discharged and then stays idle for a while, the battery state-of-charge resumes to a certain saturation value. This recovery effect can be clearly observed in the measured results as shown in Fig. 8(a). The open-circuit voltages of two cells converge at the end of equalization stage (I) and then diverges in idle stage (II). It incurs error to the judgment of equalization ending point.

In order to improve the equalization accuracy and to resist the battery recovery effect, in this article, a recovery-effect immune equalization strategy is proposed. The main idea is to utilize the recovery effect to reduce the voltage mismatch in the idle stage. As shown in Fig. 8(b), a recovery-eliminating stage [stage II in Fig. 8(b)] is enforced between equalizing stage (I) and idle stage (III). After certain redundancy, the equalizer switches

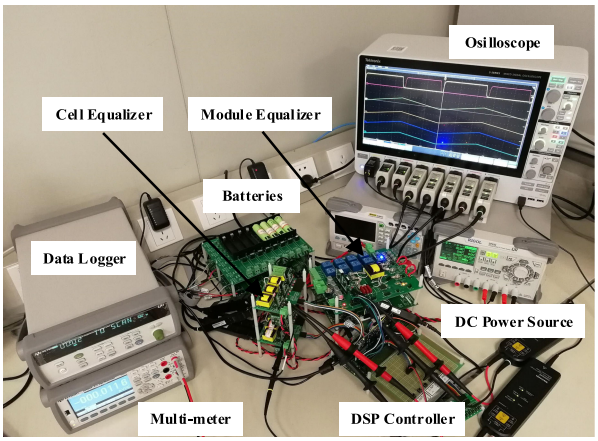
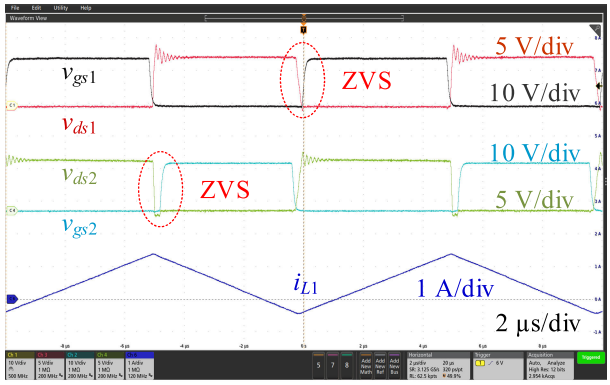


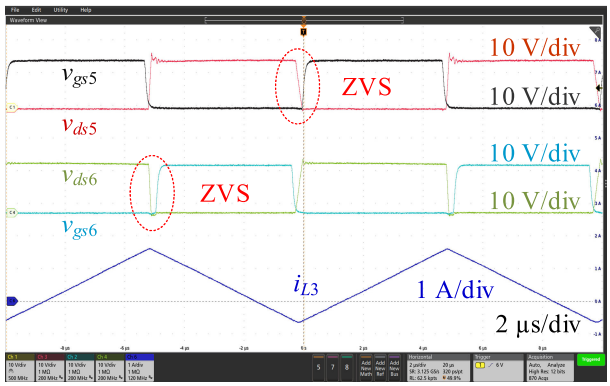
Fig. 9. Photo of the experiment setup.

TABLE I
DESIGN PARAMETERS

Module Equalizer (LLC)	MOSFETs		BSC016N06NS
	Magnetizing Inductor		L_m: 9.09 μH
	Resonant Inductor		L_r: 2.14 μH
	Resonant Capacitors		C_r: 296 nF
	Resonant Frequency		200 kHz
	Turns ratio		1:1:1
	Relays		SRD-05VDC
	Diodes		STPS5L60S
Cell equalizer (Buck-Boost)	MOSFETs		BSC010N04LS
	Inductors	Level_1	L_1: 10.02 μH; L_2: 10.15 μH
			L_4: 10.03 μH; L_5: 10.12 μH
		Level_2	L_3: 16.30 μH; L_6: 16.23μH
	Switching Frequency		100 kHz
	Monitor IC		BQ76PL536
	Controller		TMS320F28379
	Battery		NCR18650PF



(a)



(b)

Fig. 10. Key waveforms of the two-level buck–boost-based cell equalizer. (a) First level: v_{gs1}, v_{ds1} of S_1, v_{gs2}, v_{ds2} of S_2, and i_{L1}. (b) Second level: v_{gs5}, v_{ds5} of S_5, v_{gs6}, v_{ds6} of S_6, and i_{L3}.

to the idle mode, OCV_s converge automatically. Comparing to Fig. 8(a), the proposed recovery-effect immune equalization strategy facilitates an improved equalization accuracy.

IV. EXPERIMENT EVALUATION

A. Experiment Setup

To verify the theoretical analysis, a laboratory prototype is built and tested to balance eight series-connected cells. Fig. 9 shows the test bench. The detailed schematic has been depicted in Fig. 3. The design parameters are listed in Table I. NCR18650PF lithium-ion cells are employed. Meanwhile, the module multiplex network is implemented by relays (SRD-05VDC). As discussed in Section III, the proposed closed-loop PI control for *LLC* converter and optimal design methodology for buck–boost converter is realized in a DSP (TMS320F28379). Moreover, to improve the conversion efficiency of *LLC*-based module equalizer, the power Schottky diodes (STPS5L60S) with low forward voltage are utilized. In order to reduce the complexity of the voltage sensing circuit, a monitor IC (BQ76PL536) is utilized to detect every cell voltage.

B. Experiment Results

1) Key Waveforms: Figs 10(a) and (b) shows the critical switching waveforms of the first level and the second level for cell equalizer, respectively. It can be seen that all the MOSFETs v_{ds} drop to zero before the corresponding gate signal v_{gs} is applied in terms of the waveforms of S_1, S_2, S_5, and S_6. This indicates a clear ZVS turn-ON of all the MOSFETs. Meanwhile, the current waveforms of L_1 and L_3 decrease to a negative value slightly, validating the proposed bipolar CCM operation of the cell equalizer. When both switches turn ON and OFF alternatively, the charge of cell$_1$ transfers to the inductor (L_1) and the stored energy in L_1 further transfers to cell$_2$ when i_{L2} decreases. This establishes the energy flow path between those two cells.

Fig. 11 presents the key waveforms of module equalizer when the equalization starts and ends. Both primary switches (S_{13} and S_{14}) realize and maintain ZVS turn-ON during the entire equalization process, according to the waveforms of v_{ds} and v_{gs} in Fig. 11. Typically, the output current I_o of the module equalizer keeps a constant value (1 A) when the switching frequency f_s decreases. This validates the proposed design of *LLC*-based constant-current module equalizer in Section III.

2) Measured Efficiency: To evaluate the conversion efficiency of the proposed equalizer, the measured efficiency curves of cell equalizer and module equalizer are plotted in Figs. 12–14. When the output voltage of one basic buck–boost unit in the first level varies from 3.0 to 4.2 V and that in the second level varies from 6.0 and 8.4 V, the corresponding average efficiency is 92.48% and 95.59%. Due to ZVS turn-ON of all MOSFETs and minimized circulating current, a general high overall efficiency

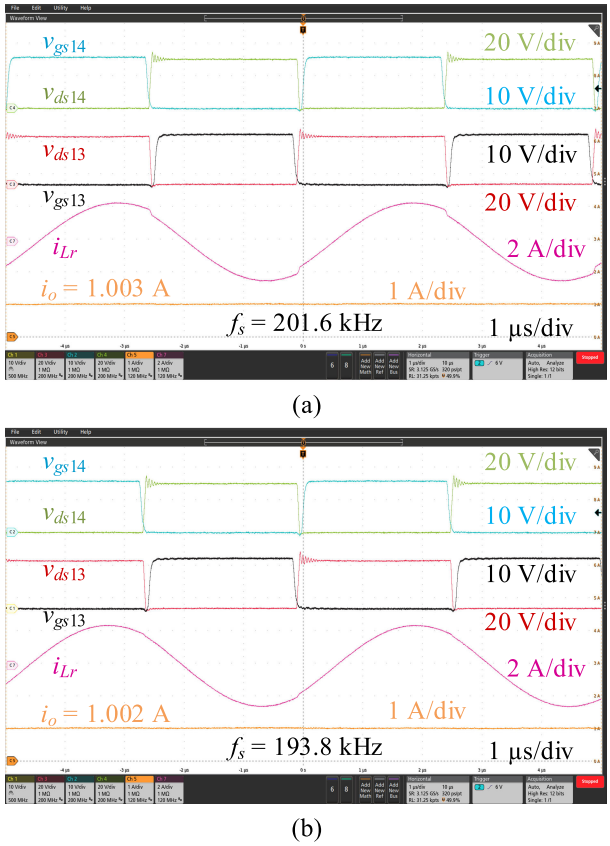


Fig. 11. Key waveforms of the *LLC*-based module equalizer. v_{gs13}, v_{ds13} of S_{13}, v_{gs14}, v_{ds14} of S_{14}, i_{Lr} and i_o when the equalization starts (a) and ends (b).

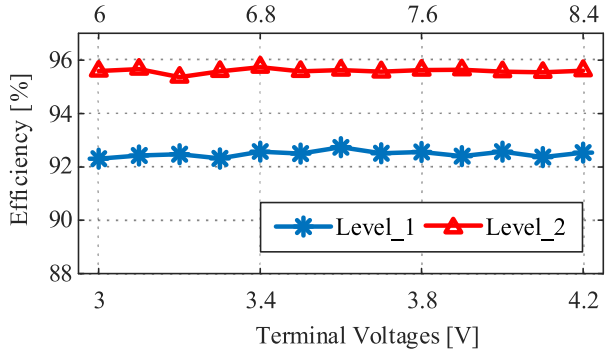


Fig. 12. Measured efficiency of the two-level buck–boost-based cell equalizer during balancing process.

is achieved on both two levels. In low power application, the wire induced conduction loss is more substantial in low voltage scenarios. Therefore, the first level with lower voltage exhibits a relatively lower efficiency, as shown in Fig. 12.

Fig. 13 presents the conversion efficiency of *LLC*-based module equalizer for the different load when f_s varies around f_0. As shown, for every equivalent load when the input voltage equals 30 V, the module equalizer always exhibits a peak efficiency when f_s is matched to f_0. Meanwhile, the average efficiency at each load condition falls into the range of 93.5% to 93.8%. When the output current is regulated to 1 A, the corresponding conversion efficiency and switching frequency f_s are presented

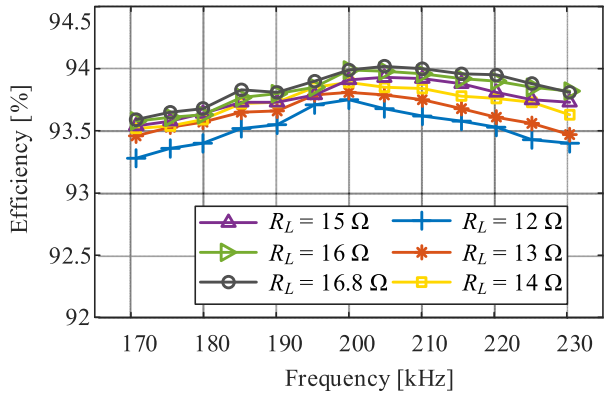


Fig. 13. Measured efficiency of the *LLC*-based module equalizer versus f_s in different load conditions.

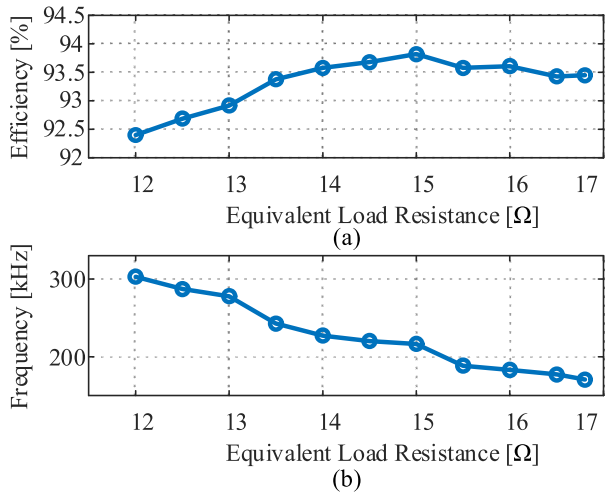


Fig. 14. Measured efficiency of the *LLC*-based module equalizer with I_o = 1 A during balancing process.

in Fig. 14. When load resistance increases, the output voltage increases with constant output current. Thus, f_s decreases correspondingly. This validates the theoretical analysis in Fig. 7(b). During the entire load variation range (assuming cell voltage varies from 3.0 to 4.2 V), the module equalizer exhibits 93.8% peak efficiency and overall good efficiency performance.

3) Voltage of Cells and Modules: For the eight series-connected lithium-ion cell string with different initial cell voltages, Figs. 15 and 16 show the experimental terminal voltages (V_{Ts}) and open-circuit voltage (OCV_s) of every single cell and module, respectively. The voltage data are recorded by Keysight 34972 A. As shown in Fig. 15, the initial voltages are 3.654, 3.585, 3.578, 3.504, 3.80, 3.737, 3.737, and 3.686 V. In each module, every two cells or strings with two series-connected cells are equalized by the hierarchical cell equalizer, and their voltages converge to the average value correspondingly. As highlighted in Fig. 15(a), the proposed recovery-effect immune equalization strategy is applied to eliminate the voltage mismatch by utilizing the battery recovery effect. This helps to improve the equalization accuracy effectively. Meanwhile, each

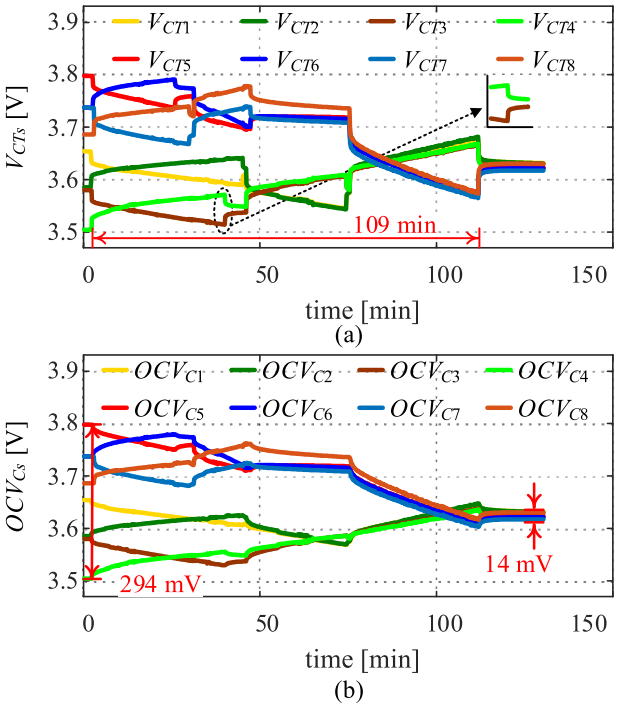


Fig. 15. Cell voltages during the equalization process when the initial voltages are 3.654, 3.585, 3.578, 3.504, 3.80, 3.737, 3.737, and 3.686 V. (a) Terminal voltage (V_{CT}). (b) Open-circuit voltage (*OCV*).

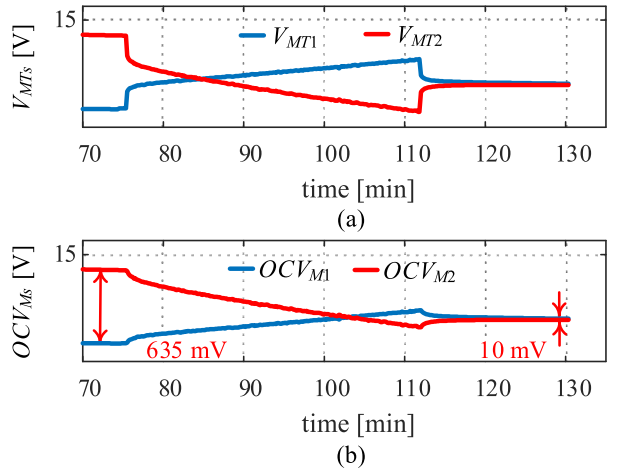


Fig. 16. Module voltages during the equalization process. (a) Terminal voltage (V_{CT}). (b) Open-circuit voltage (*OCV*).

module voltage converges (in Fig. 16) when the module equalizer is activated. After the total equalization process of 109 min, the differences of OCV_{Cs} and OCV_{Ms} converges from 294 to 14 mV and from 635 to 10 mV, respectively. This validates the theoretical analysis and battery equalizer design.

C. Performance Comparison

A comprehensive comparative analysis is conducted between the proposed equalizer and other equalizers. The performances are evaluated in ten perspectives, which are main components count, voltage stress of MOSFETs, modularization, energy flow, control complexity, efficiency, size, balancing speed, implementation, and cost. It should be noted that "Modularization" is based on the modularization capability. For instance, the modular structures excel at modularization. "Energy flow" is evaluated by the number of available equalization path. "Control complexity" is decided by the number and sort of control signals, monitoring networks, and the complexity of control algorithms. "Efficiency" is measured by the conversion efficiency of equalization circuit and the required number of balancing cycles. "Size" is determined by the required components count. The bulky magnetic components (multiwinding transformer) with large volume cause poor "size" performance. "Balancing speed" is determined by the provided balancing current (balancing power) and the average energy-flow-path length. "Implementation" is evaluated by the practical application possibility of the equalizer for a long battery string. "Cost" is the sum of prices of all the components. Table II details the comparison results of different equalization techniques.

As shown, in [1], the shunt resistor-based passive equalizer exhibits excellent modularization, control complexity, size, implementation and low cost, which are widely used in the industrial applications. However, it suffers from zero efficiency because the cell charge is dissipated by shunt resistor. In [3], the buck–boost converter-based C2C technique outperforms in circuit extensibility because the equalizer unit simply scales up with the increase of cell number. However, it presents low balancing speed and poor energy flow due to its long energy-flow-path length. To improve, a chain-structured [6] and a star-structured [9] switched-capacitor are utilized to reduce the energy-flow-path length compared to the series-coupled structure [3]. Both equalizers demonstrate very good energy flow and excellent implementation. However, the equalization speed of switched-capacitor-based equalizers is extremely slow when the cell voltage difference is trivial. In [11], a quasi-resonant converter-based bidirectional C2S equalizer is proposed, which shares a two-winding transformer via a multiplex network. This design shows very good modularization, energy flow, and good balancing speed. By utilizing the quasi-resonant operation mode to realize the ZVS turn-ON of MOSFETs, leading to improved efficiency. However, this requires additional components and complex control signals, leading to poor control complexity. Similarly, in [12], a bidirectional C2S/S2C equalization structure based on a shared dual full-bridge converter is designed, which shows very good energy flow and modularization. However, the required switch count in the multiples network is large because every single cell needs to be selected when voltage mismatch occurs. In [13], a time-shared flyback converter-based equalizer with low balancing current is introduced, which reduces the size. Nevertheless, only one balancing loop with 70% efficiency can operate at one moment, this leads to low balancing speed and low efficiency. In [14], a multiwingding transformer-based flyback converter is utilized to realized bidirectional C2S/S2C equalization, which presents good energy flow. However, this method requires one transformer winding per cell to build the energy-flow path. This causes a bulky size and is difficult to implement for long battery string scenarios. In [16], VMs-based S2C equalizer is proposed to reduce the

TABLE II
COMPARISON OF DIFFERENT EQUALIZERS

References		[1]	[3]	[6]	[9]	[11]	[13]	[12]	[14]	[16]	[19]	[23]	[27]	This work
Equalization methods		Passive method	C2C			C2S		S2C			Modular structure			
		Shunt resistor	Buck-Boost	Chain-structured switched-capacitor	Star-structured switched-capacitor	Quasi-resonant converter	Flyback (Two-winding)	Full-bridge converter	Flyback (Multi-winding)	Voltage multipliers	Multiport converter &Buck-Boost	Inductor carrier	Forward conversion	*LLC* & Buck-Boost
No.	MOSFETs &Drivers	N	$2N$	2N+4	$2N$	2(N+1)+8	$2(N$-1)	8	N+1	2	$2(N+m$-1)	$2N+6m$	N	$6m$+2
	SW stress	V_c	$2V_c$	(N-1)V_c	V_c/2	NV_c	NV_c	$(N/2)V_c$	$(N+k)V_c$	NV_c	$(N/m)V_c$	$(N/m)V_c$	V_c	NV_c
	Diodes	0	0	0	0	2	$2N$-1	0	0	$2N$	0	0	1	2
	Capacitors	0	0	N	N-1	5	0	0	0	$2N$+1	$3m$	0	0	2
	Inductors	0	*0*	0	0	2	0	0	0	0	N-1	m+1	0	$3m$
	Transformers (No. of windings)	0	N/2 (2)	N+2(3)	0	1(2)	1(2)	1(2)	1(N+1)	1(2)	1(m)	0	1(N+2)	1(3)
	Relays	0	0	0	0	0	0	N+4	0	0	m	0	0	m+5
Modularization		E	P	S	G	VG	VG	VG	VG	VG	E	VG	G	E
Energy flow		P	P	S	VG	VG	G	VG	VG	P	G	VG	VG	VG
Control complexity		E	VG	G	G	P	VG	S	G	E	G	E	VG	G
Efficiency		P	S	G	VG	VG	P	VG	P	S	G	P	VG	VG
Size		E	S	VG	VG	G	G	S	P	VG	P	S	P	S
Balancing speed		P	P	S	S	G	P	VG	S	S	E	G	G	VG
Implementation		E	E	G	E	G	VG	S	P	G	G	G	P	G
Cost		Low	Medium	High	Medium	Medium	Medium	Low	Low	Low	High	High	Low	Medium
		N	2.25N+0.4	2.7N+5.6	2.2N-0.2	2N+13.4	2.3N-1.25	0.6N+11.3	1.2N+1.7	0.7N+3.1	2.6N+3.4m-2.1	2N+6.6m+0.6	1.2N+1.05	8.4m+6.8

Component cost per unit ($): MOSFET (0.2), MOSFET Driver IC (0.8), Diode (0.15), winding (0.2), Transformer Core (0.9), Relay (0.6) [32].
The cell voltage is assumed equal to V_c. m and N is the number of cell modules and single cells, respectively. k is the turns ratio of the transformer in [14].
E: Excellent, VG: Very Good, G: Good, S: Satisfactory, P: Poor.

required number of active switches. It presents outstanding control, good implementation performance, small size, and low cost. However, the voltage drop of rectifier diodes causes a low conversion efficiency. The two-layer-based modular structure in [19] performs good energy flow, balancing speed and modularization, while the required multiwinding transformer limits its implementation. This two-layer structure requires high components count, causing high cost for implementation. In [23], the inductor carrier-based modular structure shows very good energy flow from any cells/modules to any cells/ modules. However, it presents low efficiency due to the hard-switching of power switches. In [27], multiwinding transformer is introduced into the modularized equalizer based on forward conversion, which improves the circuit extensibility and equalization speed to some extent. However, this method also suffers from bulky size and is difficult to implement for long battery strings. In the proposed hybrid structure, by introducing basic C2C to facilitate the circuit extensibility and utilizing hierarchical structure to improve energy-flow performance. Meanwhile, combining the *LLC*-based S2M equalizer with the optimal design of buck–boost-based cell equalizer, both high conversion efficiency and a shorten energy-flow path can be achieved. To build the energy-flow path of certain undercharged cell module, it requires a multiplex network implemented by relays with a moderate number as presented in Table II. This may increase the equalizer size to a certain extent. However, considering the other perspectives, the proposed S2M and C2C hybrid hierarchical equalization structure achieves a good compromise among efficiency, energy flow, balancing speed, size, modularization, and cost.

V. CONCLUSION

In this article, a hybrid battery equalizer which combines the advantages of both S2C and C2C structures is proposed. The proposed hierarchical equalizer is based on half-bridge *LLC* resonant converter in the S2M layer, and buck–boost converter in the two-level C2C layer. The design considerations of the *LLC* converter and buck–boost converter are addressed and analyzed to ensure ZVS among all MOSFETs. Moreover, a recovery effect immune equalization strategy is proposed to improve the equalization accuracy.

As a proof of concept, an experimental platform is designed and tested to balance eight series-connected batteries. The switching frequency of the *LLC*-based module equalizer is constrained between 170 and 230 kHz. A 93.8% peak efficiency and overall good efficiency performance are achieved. The switching frequency of the two-level buck–boost-based cell equalizer is set as 100 kHz. The top and bottom levels exhibit 95.59% and 92.48% average efficiency, correspondingly. The experimental results well validate the theoretical analysis and the proposed design methodology.

REFERENCES

[1] M. M. Hoque, M. A. Hannan, A. Mohamed, and A. Ayob, "Battery charge equalization controller in electric vehicle applications: A review," *Renewable Sustain. Energy Rev.*, vol. 75, pp. 1363–1385, Aug. 2017.
[2] J. Gallardo-Lozano, E. Romero-Cadaval, M. I. Milanes-Montero, and M. A. Guerrero-Martinez, "Battery equalization active methods," *J. Power Sources*, vol. 246, pp. 934–949, Jan. 2014.
[3] T. H. Phung, A. Collet, and J. C. Crebier, "An optimized topology for next-to-next balancing of series-connected lithium-ion cells," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4603–4613, Sep. 2014.

[4] Y. S. Lee and G. T. Cheng, "Quasi-resonant zero-current-switching bidirectional converter for battery equalization applications," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1213–1224, Sep. 2006.
[5] Y. Yuanmao, K. W. E. Cheng, and Y. P. B. Yeung, "Zero-current switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3234–3242, Jul. 2012.
[6] M. Y. Kim, C. H. Kim, J. H. Kim, and G. W. Moon, "A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3989–3999, Aug. 2014.
[7] Y. Shang, N. Cui, and C. Zhang, "An optimized any-cell-to-any-cell equalizer based on coupled half-bridge converters for series-connected battery strings," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8831–8841, Sep. 2019.
[8] A. C. Baughman and M. Ferdowsi, "Double-tiered switched-capacitor battery charge equalization technique," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2277–2285, Jun. 2008.
[9] Y. Shang, N. Cui, B. Duan, and C. Zhang, "Analysis and optimization of star-structured switched-capacitor equalizers for series-connected battery strings," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9631–9646, Nov. 2018.
[10] M. A. Hannan, M. M. Hoque, S. E. Peng, and M. N. Uddin, "Lithium-ion battery charge equalization algorithm for electric vehicle applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2541–2549, May/Jun. 2017.
[11] J. Lu, Y. Wang, and X. Li, "Isolated bidirectional DC–DC converter with quasi-resonant zero-voltage switching for battery charge equalization," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4388–4406, May 2019.
[12] J. Sun, C. Zhu, R. Lu, K. Song, and G. Wei, "Development of an optimized algorithm for bidirectional equalization in lithium-ion batteries," *J. Power Electron.*, vol. 15, no. 3, pp. 775–785, 2015.
[13] A. M. Imtiaz and F. H. Khan, "'Time shared flyback converter' based regenerative cell balancing technique for series connected li-ion battery strings," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5960–5975, Dec. 2013.
[14] M. Einhorn, W. Roessler, and J. Fleig, "Improved performance of serially connected Li-ion batteries with active cell balancing in electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 60, no. 6, pp. 2448–2457, Jul. 2011.
[15] J. Du, R. Xu, X. Chen, Y. Li, and J. Wu, "A novel solar panel optimizer with self-compensation for partial shadow condition," in *Proc. 28th Annu. - IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 92–96.
[16] M. Uno and A. Kukita, "Two-switch voltage equalizer using an LLC resonant inverter and voltage multiplier for partially shaded series-connected photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1587–1601, Mar. 2015.
[17] M. Uno and K. Tanaka, "Double-switch single-transformer cell voltage equalizer using a half-bridge inverter and a voltage multiplier for series-connected supercapacitors," *IEEE Trans. Veh. Technol.*, vol. 61, no. 9, pp. 3920–3930, Nov. 2012.
[18] M. Fu, C. Zhao, J. Song, and C. Ma, "A low-cost voltage equalizer based on wireless power transfer and a voltage multiplier," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5487–5496, Jul. 2018.
[19] Z. Zhang, H. Gui, D. J. Gu, Y. Yang, and X. Ren, "A hierarchical active balancing architecture for lithium-ion batteries," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2757–2768, Apr. 2017.
[20] C. H. Kim, M. Y. Kim, H. S. Park, and G. W. Moon, "A modularized two-stage charge equalizer with cell selection switches for series-connected lithium-ion battery string in an HEV," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3764–3774, Aug. 2012.
[21] C. H. Kim, M. Y. Kim, and G. W. Moon, "A modularized charge equalizer using a battery monitoring IC for series-connected Li-ion battery strings in electric vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3779–3787, Aug. 2013.
[22] M. Uno, K. Yashiro, and K. Hasegawa, "Modularized equalization architecture with voltage multiplier-based cell equalizer and switchless switched capacitor converter-based module equalizer for series-connected electric double-layer capacitors," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6356–6368, Jul. 2019.
[23] S. W. Lee, K. M. Lee, Y. G. Choi, and B. Kang, "Modularized design of active charge equalizer for Li-ion battery pack," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8697–8706, Nov. 2018.
[24] F. Mestrallet, L. Kerachev, J. C. Crebier, and A. Collet, "Multiphase interleaved converter for lithium battery active balancing," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2874–2881, Jun. 2014.
[25] F. Peng, H. Wang, and L. Yu, "Analysis and design considerations of efficiency enhanced hierarchical battery equalizer based on bipolar CCM buck–boost units," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4053–4063, Jul. 2019.
[26] Y. Shang, B. Xia, C. Zhang, N. Cui, J. Yang, and C. Mi, "A modularization method for battery equalizers using multiwinding transformers," *IEEE Trans. Veh. Technol.*, vol. 66, no. 10, pp. 8710–8722, Oct. 2017.
[27] Y. Shang, N. Cui, B. Duan, and C. Zhang, "A global modular equalizer based on forward conversion for series-connected battery strings," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1456–1469, Sep. 2018.
[28] C. S. Lim, K. J. Lee, N. J. Ku, D. S. Hyun, and R. Y. Kim, "A modularized equalization method based on magnetizing energy for a series-connected lithium-ion battery string," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1791–1799, Apr. 2014.
[29] H. Chen, X. Wu, and S. Shao, "A current sharing method for interleaved high frequency LLC converter with partial energy processing," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1498–1507, Feb. 2020.
[30] F. C. Lee, J. D. Van Wyk, W. Liu, Y. Liang, and B. Lu, "Optimal design methodlogy for LLC resonant converter," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2006, pp. 533–538.
[31] C. K. Chau, F. Qin, S. Sayed, M. H. Wahab, and Y. Yang, "Harnessing battery recovery effect in wireless sensor networks: Experiments and analysis," *IEEE J. Sel. Areas Commun.*, vol. 28, no. 7, pp. 1222–1232, Sep. 2010.
[32] "DigiKey Electronics - Electronic Components Distributor." [Online]. Available: https://www.digikey.com/. Accessed on: Sep. 5, 2019.

Faxiang Peng (S'18) received the B.S. degree in electrical engineering and automation from the Xi'an University of Technology, Xi'an, China, in 2017. He is currently working toward the M.S. degree with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China, since 2017.

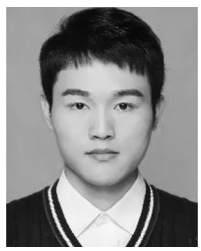
His research interests include battery management systems, battery equalization, and resonant converter design.

Mr. Peng's first-authored paper has been nominated into the finalist of IEEE IAS TSC Prize Paper Award-2019.

Haoyu Wang (S'12–M'14–SM'18) received the bachelor's (Hons.) degree in electrical engineering from Zhejiang University, Hangzhou, China, and the master's and Ph.D. degrees from the University of Maryland, College Park, MD, USA, both in electrical engineering.

He is currently a Tenure Track Assistant Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China. His research interests include power electronics, plug-in electric and hybrid electric vehicles, the applications of wide bandgap semiconductors, renewable energy harvesting, and power management integrated circuits.

Dr. Wang is an Associate Editor of IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION, and an Associate Editor of *CPSS Transactions on Power Electronics and Applications*.



Zhengqi Wei received the B.S. degree in electronic information science and technology from Shaanxi Normal University, Xi'an, China, in 2019. He is currently working toward the M.S. degree in the School of Information Science and Technology, ShanghaiTech University, Shanghai, China, since 2019.

His research interests include battery management systems and battery equalization.