A Physics-Based Transient Electrothermal Model of High-Voltage Press-Pack IGBTs Under HVdc Interruption

Yifei Luo, Fei Xiao, Binli Liu, and Yongle Huang

***Abstract*—The wide use of press-pack insulated-gate bipolar transistors (IGBTs) in high-voltage dc (HVdc) applications makes the accurate modeling of high-voltage press-pack IGBTs more urgent. Based on the mechanism of the switching transient, a physics-based electrothermal transient model of the high-voltage press-pack IGBT is proposed. Considering the wider base width of high-voltage IGBTs (HVIGBTs), a transient model of the HVIGBT with buffer layer is presented taking into account the carrier recombination in the base region and the injection level in the buffer layer. Besides, a modified thermal network of press-pack IGBTs is implemented considering the double-sided heat transfer structure. An electrothermal coupling model of high-voltage press-pack IGBTs is then obtained combining the proposed electro and thermal models. Finally, simulations of key dynamic performances of the proposed HVIGBT model match well with the testing results. Furthermore, the HVdc interruption process of a solid breaker with different number of series-connected IGBTs is simulated using the proposed IGBT model and tested. The testing results show good consistency between the simulated and measured voltage and current of the series-connected press-pack IGBTs, which brings strong support to the accurate design of solid breakers in the HVdc transmissions.**

***Index Terms*—Carrier recombination, double-sided heat transfer, HVdc interruption, press-pack insulated-gate bipolar transistor (IGBT), transient electrothermal coupling.**

NOMENCLATURE

A	Chip area.
b	Mobility ratio in base.
b_H	Mobility ratio in N+ SPT layer.
C_{DSJ}	Drain–source depletion layer capacitance.
C_{GD}	Gate–drain capacitance.
C_{GS}	Gate–source capacitance.
D	Ambipolar diffusion coefficient in base.
D_{PH}	Hole diffusion coefficient in buffer layer.
E_g	Band gap energy of Si.
I_{PH}	Hole current in buffer layer.
I_T	Total current of IGBT.
I_{CE}	IGBT collector–emitter current.
I_G	Gate current.
I_{sne}	Emitter electron saturation current.
J_{PH}	Hole current density in buffer layer.
J_T	Total current density.
L	Base diffusion length.
n_i	Intrinsic carrier concentration.
N_L	N- base doping concentration.
N_H	Doping concentration in buffer layer.
P_{H0}	Hole concentration at $x_H = 0$.
P_{HW}	Hole concentration at $x_H = W_H$.
P_{L0}	Hole concentration at $x = 0$.
q	Electron charge.
Q_L	Base charge.
Q_H	Buffer layer charge.
Q_T	Total charge.
R_g	Gate resistance.
T_j	Junction temperature.
T_0	Room temperature.
μ_n	Electron mobility.
μ_p	Hole mobility.
μ_{n0}	Electron mobility under room temperature.
μ_{p0}	Hole mobility under room temperature.
V_{bi}	Built-in electric potential.
V_{GS}	Gate–source voltage.
W_H	Buffer layer width.
W	Quasi-neutral base width.
W_L	Metallurgic base width.
W_d	Depletion region width.
δ_p	Excess hole concentration injected into base.
τ_L	Excess carrier lifetime in base.
τ_H	Excess carrier lifetime in buffer layer.
$\varepsilon_{\mathrm{si}}$	Dielectric coefficient of silicon.

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I. INTRODUCTION

WITH the fast development of economy and energy resources, more and more critical demands on the power electronics system design are requested. Being the core components in the power converter system, power semiconductor devices are attracting growing attentions to their structure design and reliability evaluation. Recently, to make better use of the

renewable energy and optimize the power energy distribution, the world has strengthened the construction of dc power grids. By the end of 2015, China's installed wind power and solar power has reached 129 and 43.18 GW, respectively [1]. There are already more than 20 HVdc projects in operation in China which include UHVdc lines and voltage-source converter-HVdc lines such as Nanao 200 MW three-terminal HVdc project in 2013, Zhoushan five-terminal HVdc project in 2014, Xiamen 1000 MW HVdc project in 2015, and so on [1]. All those will achieve the multipoint interconnection from the central China to all other regions in China. Besides, the idea of dc power grids has also been proposed in some European and American countries such as the "Super Smart Grid 2050" in Europe and the "Grid 2030" in USA. All those will implement the HVdc transmission network to achieve the balance between demands and supplies in a very wide region.

The solid breaker is a key component in HVdc systems for their reliability and The HVdc interruption is a critical process of the breaker. Therefore, the power semiconductor devices are the core components to complete this process. With the series–parallel connection of large amounts of devices, interruption under high voltage and large current can be achieved. Therefore, the device safety under this aperiodic impact will request precise modeling of the power electronic devices to accurate describe the interruption process.

The insulated-gate bipolar transistor (IGBT) is a type of widely used full-control power electronic devices which has the advantages of simple driver, high power and low consumption [2], [3]. It goes through several generations and is now widely used in HVdc transmission, aeronautics and astronautics, vessel fabrication and rail traffic. Currently, there are mainly two types of packages for IGBTs: insulated module and press pack. The press-pack module is mainly implemented in series connection applications especially in HVdc transmission because of its short-circuit characteristic under failure, which still maintains the normal system operation even if one device fails [4]–[6]. Therefore, an accurate model of press-pack IGBTs is an important precondition to achieve the accurate design of both the HVdc system and the reliability evaluation of power electronic instruments.

The IGBT switching transient is always accompanied by the carrier doping distribution variation and charge/discharge of inner junction capacitors, which is a very complicated process. Besides, the transient characteristics of IGBTs are also affected by device parameters, the freewheeling diodes, driver circuits, stray inductance, temperature, etc. [7]–[9]. Therefore, it is very difficult to implement a transient model both presenting high-voltage transient characteristics and being utilized in the practical solid breaker circuit simulations. Fossum, Baliga and Hefner all presented different IGBT transient models [10]–[12] and probably the most typical one is the Hefner model in which some carrier distribution assumptions are still in use in today's new IGBTs [13]. For plane gate IGBTs, many transient models have been implemented in the past years. However, those models are mainly used in middle/low-voltage applications and may introduce errors in high-voltage applications [14]. In [15] and [16], the high-voltage transient model is implemented from the perspective of carrier lifetime but lacking of considerations of thermal coupling. Although the electrothermal coupling is investigated in both modular and press-pack IGBTs in some publications [17]–[20], those still focus on either one-way coupling or behavior-based models, which may not be accurate enough to describe the complicated applications.

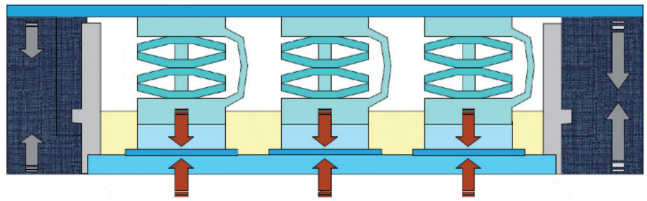

Fig. 1. Structure of ABB's HiPak press-pack IGBTs.

In this article, a physics-based transient modeling method of high-voltage press-pack IGBTs is investigated based on the press-pack structure. The transient physical model and thermal model of the high-voltage press-pack IGBTs are proposed based on the chip semiconductor structure and the package structure separately. Furthermore, a transient electrothermal simulation model is established combining the proposed electro and thermal models. Finally, the proposed model is verified first in single device double pulse testing and then in a solid breaker circuit with series-connected press-pack IGBTs under the HVdc interruption.

II. Structure of Press-Pack IGBTs

The current package types of IGBTs can be divided into module and press-pack. Being different from the module, press-pack eliminates the bonding wires and the heat dissipates from both sides of the IGBT as shown in Fig. 1 [21]. More importantly, press-pack IGBTs short circuit after failure. Therefore, press-pack IGBTs have lower thermal resistance, higher operation temperature, and higher reliability, which are very suitable for HVdc transmissions.

The following sections will focus on the physics-based high-voltage electrical modeling and the double-sided thermal transmission modeling as shown in Fig. 2. The electrothermal model of press-pack IGBTs is then achieved by coupling the electro and thermal models.

III. Electrothermal Transient Modeling of Press-Pack HV-IGBTs

A. Physics-Based Transient Model of HVIGBT

Fig. 3 shows a typical structure of IGBT chips, in which the N+ buffer layer can be replaced by field stop (FS), soft punch through (SPT), and other new structures. The modeling coordinate is shown in Fig. 4, where the boundary between P+ emitter and N+ buffer is set as the zero of coordinate x_H to analyze the buffer layer, and the boundary between N+ buffer and N– base is set as the zero of coordinate x to analyze the base region.

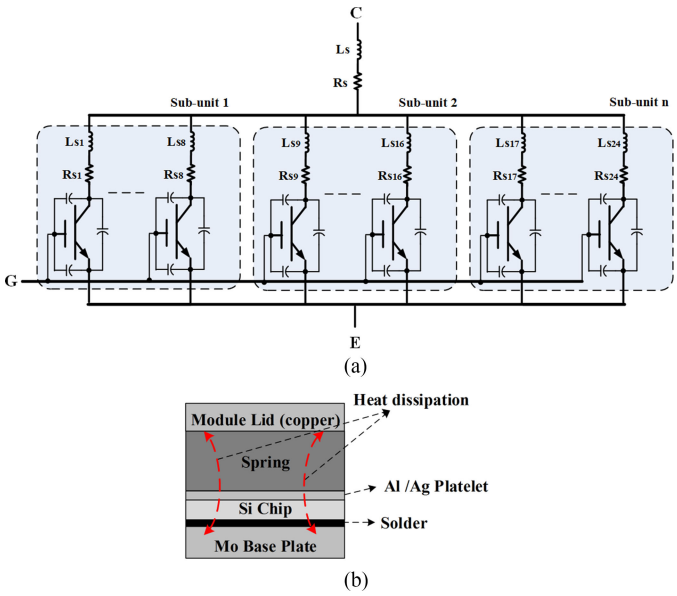

Fig. 2. Schematic diagram of the press-pack IGBT. (a) Module structure based on chips. (b) Heat dissipation of press-pack package.

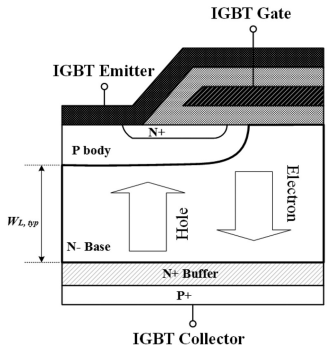

Fig. 3. Profile of a typical IGBT and the carrier movement during switching.

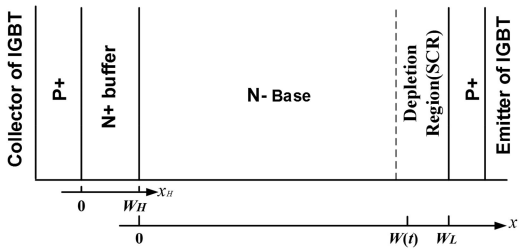

Fig. 4. Modeling coordinate of typical IGBTs.

Since the N– base is in the high-level injection under conduction, the transmission formulas of electron and hole current in N– base can be written as [22]

$$J_n = nq\mu_n E + qD_n \frac{dn}{dx} \tag{1}$$

$$J_p = pq\mu_p E - qD_p \frac{dp}{dx}. \tag{2}$$

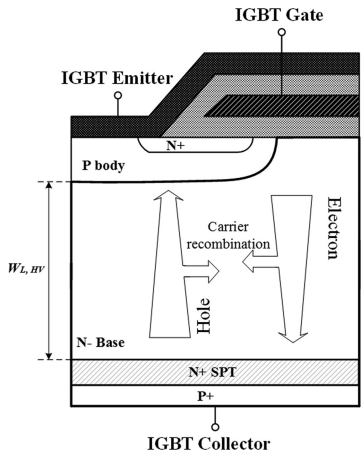

Fig. 5. Carrier movement during switching in the high-voltage IGBT ($W_{L,\mathrm{HV}} > W_{L,\mathrm{typ}}$).

Based on the high-level injection, $n \approx \delta n$, $p \approx \delta p$; thus, $\delta n \approx \delta p$. The ambipolar transmission formulas of hole current in N– base can be derived as

$$J_p = \frac{1}{1+b} J_T - qD \frac{d\delta p}{dx} \tag{3}$$

where $J_T = J_n + J_p$ is the total current density, $b = \mu_n/\mu_p$ is the mobility ratio in base, and $D = \frac{2D_pD_n}{D_p+D_n}$ is the ambipolar diffusion coefficient in base.

During the switching transient, N– base still satisfies the high-level injection and low-gain condition. The continuous formula of excess carriers under ambipolar diffusion is

$$\frac{d^2(\delta p)}{dx^2} = \frac{\delta p}{L^2} + \frac{1}{D}\frac{d(\delta p)}{dt}. \tag{4}$$

For the high-voltage press-pack IGBT in this article, the base width is bigger than that in middle-to-low voltage IGBTs. This leads to different results during the HVdc transient modeling. For middle-to-low voltage IGBTs, all the excess carriers flowing through N– base can be assumed to be swept out of base during the switching transient because of the narrow base width. However, for high-voltage IGBTs, the base width W_L is much bigger and the ambipolar diffusion length L is no longer larger than W_L. Therefore, the recombination of excess carriers in the base region must be considered during the switching transient. This difference can be shown as Figs. 3 and 5.

According to the derivation of typical IGBTs [23], the distribution of excess carriers in N– base at steady state is

$$\delta p\,(x) = P_{L0} \frac{\sin h\left(\frac{W-x}{L}\right)}{\sin h\left(\frac{W}{L}\right)}. \tag{5}$$

Assuming the redistribution of base charge is a small perturbation adding to the charge control term during the switching transient, the charge accumulation during the base charge redistribution can be considered doing approximately linear variation (first-order approximation), as shown in Fig. 6. This case is especially fitted in HVdc interruption applications which have very large switching current.

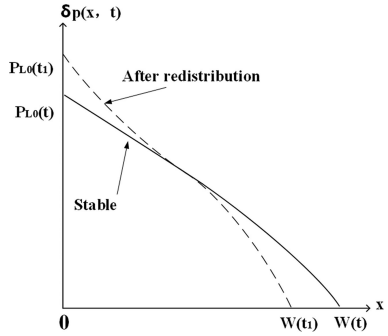

Fig. 6. First-order approximation of the hole concentration in the quasi-neutral base of IGBTs.

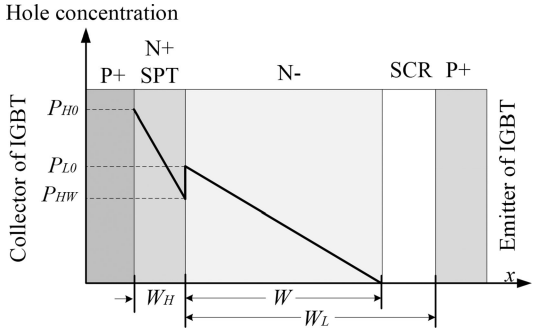

Fig. 7. Schematic diagram of carrier distribution in N+ SPT layer and N– base.

Making the first-order approximation to (5) and inserting it into (4), the hole concentration in N– base can be written as

$$\delta p\,(x,t) = P_{L0}(t)\left[1-\frac{x}{W(t)}\right] - \frac{P_{L0}(t)}{D\cdot W(t)}\frac{dW(t)}{dt} \times \left[\frac{x^2}{2} - \frac{xW\,(t)}{6} - \frac{x^3}{3W\,(t)}\right] + P_{L0}\,(t)\left[\frac{x^2}{2L^2} - \frac{x^3}{6W\,(t)\,L^2} - \frac{xW\,(t)}{3L^2}\right]. \quad (6)$$

Equation (6) shows that the third term in the right side needs to be considered in HVIGBTs, which is related to the carrier recombination in base during the switching transient because of the wide base width. This is different from that in typical IGBTs [12], [13].

The hole current in base can then be obtained as (7) by inserting (6) into (1)

$$I_{p,\mathrm{HV}}(x) = \frac{1}{1+b}I_T - qAD\left\{-\frac{P_{L0}(t)}{W(t)} - \frac{P_{L0}(t)}{D\cdot W(t)}\frac{dW(t)}{dt} \times \left[x - \frac{W(t)}{6} - \frac{x^2}{W(t)}\right] + P_{L0}(t)\left[\frac{x}{L^2} - \frac{x^2}{2W(t)L^2} - \frac{W(t)}{3L^2}\right]\right\} \quad (7)$$

where $I_T = I_{p,\mathrm{HV}} + I_{n,\mathrm{HV}}$.

Besides, during the large current switching, the carrier extraction of the depletion region is significant. Therefore, the calculations of both junction capacitors and quasi-neutral base width need to consider the influence of base current on the charge distribution in the depletion region [23]. *W*(*t*) and C_{BCJ} (*t*) are thus written as follows:

$$W_d = \sqrt{\frac{2\varepsilon_{si}\left(V_{\mathrm{CE}}\,(t)+V_{bi}\right)}{q\left(N_L + \frac{I_p}{qAv_{\mathrm{sat},p}} - \frac{I_n}{qAv_{\mathrm{sat},n}}\right)}} \quad (8)$$

$$W(t) = W_L - \sqrt{\frac{2\varepsilon_{si}\left(V_{\mathrm{CE}}\,(t)+V_{bi}\right)}{q\left(N_L + \frac{I_p}{qAv_{\mathrm{sat},p}} - \frac{I_n}{qAv_{\mathrm{sat},n}}\right)}} \quad (9)$$

$$C_{\mathrm{BCJ}}\,(t) = \frac{A\varepsilon_{si}}{W_d}. \quad (10)$$

$Q_L(t)$ is defined as

$$Q_L(t) = \int_0^{W(t)} qA\cdot\delta p(x,t)dx = \frac{qAWP_{L0}}{2}. \quad (11)$$

From (7) to (11), the hole current in the N– base region of the HVIGBT is calculated as

$$I_{p,\mathrm{HV}}(x=0) = \frac{I_T}{1+b} + \left(\frac{2D}{W^2} + \frac{C_{\mathrm{BCJ}}}{3Q_B}\frac{dV_{\mathrm{AC}}}{dt} + \frac{2}{3\tau_L}\right)Q_L \quad (12)$$

$$I_{p,\mathrm{HV}}(x=W) = \frac{I_T}{1+b} + \left(\frac{2D}{W^2} + \frac{C_{\mathrm{BCJ}}}{3Q_B}\frac{dV_{\mathrm{AC}}}{dt} - \frac{1}{3\tau_L}\right)Q_L \quad (13)$$

where $Q_B = q\mathrm{AWN}_L$.

The total charge of the base and N+ SPT layer is defined as

$$Q_T = Q_L + Q_H. \quad (14)$$

The hole current in the base region is also related with the N+ SPT layer. Since the doping concentration in the N+ SPT layer is lower than that in PT structure, it is at high-level injection with low gain during conduction. Therefore, hole current density in the N+ SPT layer is calculated as

$$J_{\mathrm{pH}} = \frac{1}{1+b_H}J_T - qD_H\frac{d(\delta p_H)}{dx_H}. \quad (15)$$

To solve the carrier continues equation, the boundary conditions: $P_H(x_H=0,t) = P_{H0}(t)$ and $\delta P_H(x_H = W_H, t) = P_{\mathrm{HW}}(t)$ are used, and at the boundary between N+ SPT layer and N– base, the following relation should be satisfied:

$$P_{\mathrm{HW}}\cdot(P_{\mathrm{HW}} + N_H) = P_{L0}\cdot(P_{L0}+N_B). \quad (16)$$

Based on the high-level injection in both N+ SPT layer and base, the above equation can be simplified as $P_{\mathrm{HW}} = P_{L0}$, as shown in Fig. 7.

Therefore, $I_{\mathrm{pH}}\,(x_H)$ can be obtained as

$$I_{\mathrm{pH}} = \frac{1}{(1+b_H)}I_T + \frac{qAD_H}{W_H}(P_{H0} - P_{\mathrm{HW}}) = \frac{1}{(1+b_H)}I_T + \frac{Q_H}{\tau_{Hb}} - \frac{2}{\tau_{Hb}}\frac{W_H}{W}Q_L \quad (17)$$

where $Q_H = \frac{qAW_H}{2}(P_{H0}+P_{\mathrm{HW}})$, $\tau_{Hb} = \frac{W_H^2}{2D_{\mathrm{pH}}}$.

Since the hole current flowing in and out of the boundary between N+ SPT layer and base are equal, the Q_L can be derived from (12), (14) and (17)

$$Q_L = \frac{Q_T - \left(\frac{1}{1+b} - \frac{1}{1+b_H}\right) I_T \tau_{Hb}}{1 + \frac{2D\tau_{Hb}}{W^2} + \frac{\tau_{Hb} C_{\mathrm{BCJ}}}{3Q_B} \frac{dV_{\mathrm{AC}}}{dt} + \frac{2\tau_{Hb}}{3\tau_L} + \frac{2W_H}{W}}$$
$$= \frac{W^2}{W_{\mathrm{eff}}^2} \left[Q_T - \left(\frac{1}{1+b} - \frac{1}{1+b_H} \right) I_T \tau_{Hb} \right] \quad (18)$$

where

$$\frac{W_{\mathrm{eff}}^2}{W^2} = 1 + \frac{2D\tau_{Hb}}{W^2} + \frac{\tau_{Hb} C_{\mathrm{BCJ}}}{3Q_B} \frac{dV_{\mathrm{AC}}}{dt} + \frac{2\tau_{Hb}}{3\tau_L} + \frac{2W_H}{W}. \quad (19)$$

Considering the displacement current in the junction capacitors during the transient process, the electron current at the edge of the quasi-neutral region in N– base can be solved as [23]

$$I_{n,\mathrm{HV}}(x = W) = I_{\mathrm{mos}} + (C_{\mathrm{DSJ}} + C_{\mathrm{GD}}) \frac{dV_{\mathrm{ds}}}{dt} - C_{\mathrm{GD}} \frac{dV_{\mathrm{GS}}}{dt} \quad (20)$$

where

$$\frac{dV_{\mathrm{GS}}}{dt} = \frac{I_G}{C_{\mathrm{GS}} + C_{\mathrm{GD}}} + \frac{C_{\mathrm{GD}}}{C_{\mathrm{GS}} + C_{\mathrm{GD}}} \frac{dV_{bc}}{dt}. \quad (21)$$

Carrier recombination and the reverse injection of the P+ emitter satisfy the charge control equation, as shown in (22). The last term in the right side of (22) represents the minority charge in N+ SPT layer under thermal equilibrium condition

$$\frac{dQ_T(t)}{dt} = I_{n,\mathrm{HV}}(x = W) - \frac{Q_L}{\tau_L} - \frac{Q_H}{\tau_H} + \frac{qAW_H n_i^2}{\tau_H N_H}. \quad (22)$$

Finally, the voltage and current characteristics of HVIGBT at switching transient can be obtained through (12)–(22) and the external circuit constraint. To solve the numerical convergence problem when the N– base of IGBT is in the punch through mode, *W* is set to a very small value instead of zero which cannot affect the result.

As described above, the proposed electro model takes account into the carrier recombination during switching transient because of the wider base region of HVIGBT. In addition, different injection-level condition in buffer layer is applied since the doping concentration of buffer layer in the SPT structure is much lower than typical PT IGBTs. Furthermore, a treatment of the quasi-neutral region width in the N– base is helpful to present the punch-through mode of N– base under high-voltage during the model calculation.

Fig. 8 shows the external circuitry including the load and freewheeling diodes. The proposed HVIGBT model is for single chip and multiplied by the number of chips in package (32 IGBT chips in the tested module) to represent one press-pack device. In addition, the inner gate resistance and stray inductance are set for the whole module. This could make the device simulation more efficient while still maintain good accuracy. The model is successfully implemented in Saber using Mast programming to achieve the flexible simulation.

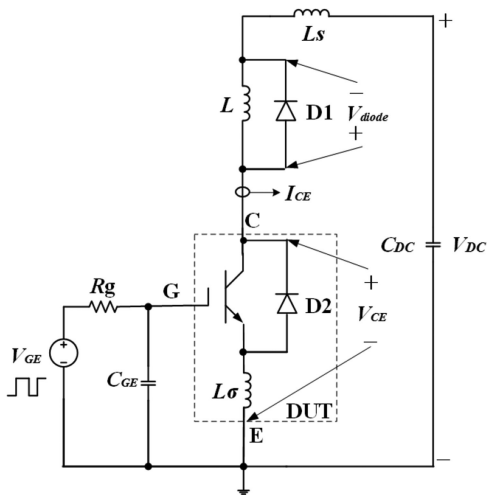

Fig. 8. Double-pulse simulation schematic diagram of the proposed IGBT model.

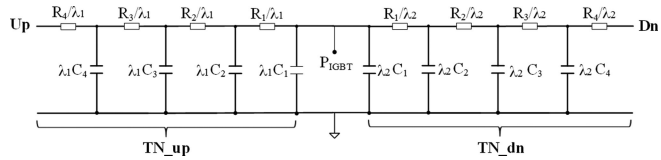

Fig. 9. Equivalent Cauer TN of the press-pack IGBT.

B. Thermal Model of Press-Pack Package

As shown in Fig. 2(b), press-pack IGBTs have double-sided heat dissipation structure. Therefore, the thermal network (TN) of press-pack is different from that of the modular package as shown in Fig. 9. Because the press-pack structure investigated in this article is asymmetric as shown in Fig. 1, the heat dissipation ratio of two sides are different.

To build the TN of the investigated press-pack IGBT, the thermal resistance in the up and down sides are first assumed as $R_{\mathrm{th,up}}$ and $R_{\mathrm{th,dn}}$. Then, the equivalent thermal resistance $R_{\mathrm{th}(jc)}$ in the datasheet can be written as

$$R_{\mathrm{th}(jc)} = R_{\mathrm{th,up}} || R_{\mathrm{th,dn}}. \quad (23)$$

Assuming the ratio of heat dissipation to up and down directions is λ_1 and λ_2 separately, and the total power consumption is P_{out}, then the heat dissipated to up and down directions as P_{up} and P_{dn} is written as follows:

$$P_{\mathrm{up}} = \lambda_1 P_{\mathrm{out}} \quad (24)$$

$$P_{\mathrm{dn}} = \lambda_2 P_{\mathrm{out}} \quad (25)$$

$$\lambda_1 + \lambda_2 = 1. \quad (26)$$

Assuming the temperature difference between the junction and case is ΔT, then

$$R_{\mathrm{th,up}} = \frac{\Delta T}{P_{\mathrm{up}}} = \frac{\Delta T}{\lambda_1 P_{\mathrm{out}}} = \frac{1}{\lambda_1} R_{\mathrm{th}(c-j)} \quad (27)$$

$$R_{\mathrm{th,dn}} = \frac{\Delta T}{P_{\mathrm{dn}}} = \frac{\Delta T}{\lambda_2 P_{\mathrm{out}}} = \frac{1}{\lambda_2} R_{\mathrm{th}(c-j)}. \quad (28)$$

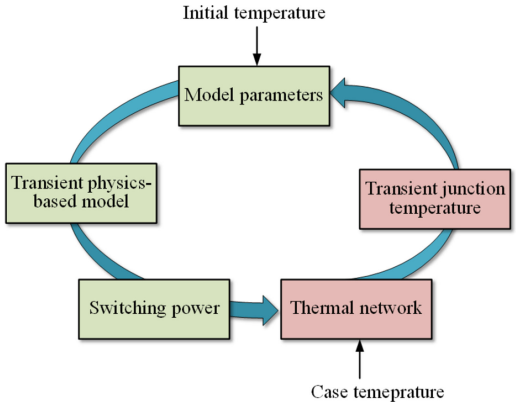

Fig. 10. Principle of electrothermal coupling of IGBTs.

TABLE I
TEMPERATURE DEPENDENCES OF THE MODEL PARAMETERS

Parameter	Temperature dependency [12], [13]
$\mu_n(T)$	$\mu_n(T)=\mu_{n0}\cdot\left(\frac{T_j}{T_0}\right)^{-\gamma}$
$\mu_p(T)$	$\mu_p(T)=\mu_{p0}\cdot\left(\frac{T_j}{T_0}\right)^{-\gamma}$
K_p	$K_p \propto K_{p0}\cdot(\frac{T_0}{T_j})^{\lambda}$
τ	$\tau=\tau_0\cdot\left(\frac{T_j}{T_0}\right)^{\alpha}$
n_i	$n_i=3.87\times10^{16}T^{1.5}\exp(-\frac{E_g}{2kT})$

Besides, since the two-sided heat dissipation equal to the equivalent thermal dissipation, the time constant of TN should be the same. Thus, (29) and (30) are satisfied

$$C_{\rm up}=\lambda_1 C_{\rm eq} \tag{29}$$

$$C_{\rm dn}=\lambda_2 C_{\rm eq}. \tag{30}$$

Based on the testing results of thermal resistance from the device supplier and datasheet, λ_1 and λ_2 can be obtained.

Therefore, the total TN of the press-pack IGBT is established as Fig. 9, where $P_{\rm IGBT}$ is the power consumption of the IGBT.

C. Proposed Electrothermal Coupling Model

Based on the proposed physics-based electromodel and double-sided TN of the press-pack IGBT, the electrothermal coupling model can be obtained by the connection between the power consumption and the junction temperature, as shown in Fig. 10. The power consumption is calculated through the electromodel under the initial temperature. The junction temperature is then calculated with this power consumption through the TN and feeds back to the electromodel to update the power consumption at a new temperature. The temperature dependences of electromodel parameters are shown in Table I.

The power consumption of the IGBT is calculated as

$$P_{\rm IGBT}=i_{\rm CE}\cdot v_{\rm CE}. \tag{31}$$

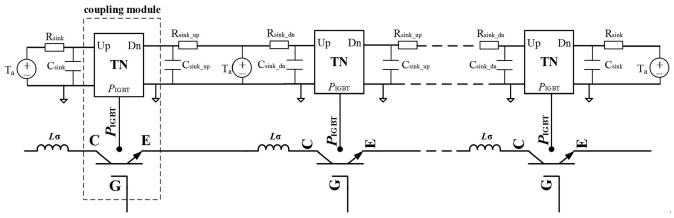

Fig. 11. Electrothermal coupling structure of single and series-connected press-pack IGBTs.

Considering the HVdc applications, the electrothermal model of the single IGBT and the structure of series-connected IGBTs is shown in Fig. 11. Because of the series connection of press-pack IGBTs, the device TN is also in cascade connection.

For the heatsink in the series-connected IGBTs, it needs to be set as two *RC* network connecting with the two IGBTs of its two sides. As shown in Fig. 11, $R_{\rm sink\_up}$ $(C_{\rm sink\_up})$ and $R_{\rm sink\_dn}$ $(C_{\rm sink\_dn})$ are the equivalent *RC* TN of one heatsink splitting into two for the IGBTs at each side of the heatsink, $R_{\rm sink}$ $(C_{\rm sink})$ are the total RC value for one heatsink, and T_a is the ambient temperature. To simplify, thermal resistance of case to heatsink has been included into the thermal resistance of the heatsink.

Normally, the equivalent *RC* TN of each side of the heatsink can be set half of the total *RC* of the heatsink if the heat of its two sides is the same. Otherwise, the equivalent *RC* of each side needs to be adjusted according to the ratio of the heat of the two sides of the heatsink.

For liquid cooling system, the *RC* TN could also be considered the same way as heatsink. The ambient temperature is set as the average temperature of the in and out water. The *RC* value can be calculated according to the size and structure of the water cooling heatsink. Normally, the water temperature in one heatsink can be considered even although there is small difference between in out water. Therefore, $R_{\rm sink\_up}$ $(C_{\rm sink\_up})$ and $R_{\rm sink\_dn}$ $(C_{\rm sink\_dn})$ of liquid cooling system could be half of the total *RC* of the liquid cooling heatsink without considering the ratio of heat generation at its two sides.

Therefore, the presented TN gives a clear view of how to build the whole electrothermal coupling circuit for IGBTs in serial.

IV. MODEL PARAMETER EXTRACTION

Model parameter extraction is important to utilize the model. In this article, different ways are used to extract the model parameters such as datasheet, empirical values, and testing waveforms [23]. During the extraction, parameters are also calibrated according to the sensitivity of characteristics of the parameters. The tested device in this article is ABB 2000K451300 4500 V/2000 A press-pack IGBT and the model parameters extracted are shown in Table II.

The Cauer TN in Fig. 9 is calculated from the Forster TN in device datasheet and the heatsink structure used in this article. The transferring method from Forster to Cauer network is conventional and not mentioned here. In this article, only heatsink is used because the interruption time is short and nonperiodic.

TABLE II
KEY PARAMETERS IN THE PROPOSED IGBT MODEL

Parameter	Value
τ_L	5 μs
τ_H	0.2 μs
N_L	1.6×10^{13} cm^{-3}
N_H	1×10^{16} cm^{-3}
W_L	440 μm
W_H	20 μm
λ_1	0.15
λ_2	0.85

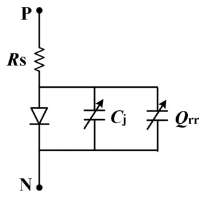

Fig. 12. Freewheeling diode model in simulation.

TABLE III
COMPARISON OF SIMULATION AND DATASHEET OF THE PROPOSED MODEL

Tj / Parameter	25°C		125°C	
	Proposed model	datasheet	Proposed model	datasheet
t_{don} (μs)	0.73	0.82	0.64	0.69
t_r (μs)	0.56	0.53	0.60	0.54
t_{doff} (μs)	3.2	3.99	4.00	4.41
t_f (μs)	0.73	0.71	0.88	0.80
E_{on} (mJ)	7680	8110	10260	9960
E_{off} (mJ)	7860	7670	10910	9790

V. EXPERIMENT RESULTS

A. Model Verification of Single Device

The simulation circuit is shown in Fig. 8 and the simulation condition is the same as that in the datasheet: $V_{\rm DC} = 2800$ V, $I_{\rm CE} = 2000$ A, $L_s = 200$ nH, $C_{\rm GE} = 330$ nF, $R_{\rm on} = 1.8\,\Omega$, $R_{\rm off} = 8.2\,\Omega$, and $L_\sigma = 25$ nH. The diode simulation model of D1 and D2 in this article is shown in Fig. 12. The parameters of diode are extracted by curve fitting in Saber using the datasheet values.

To verify the proposed model, different temperatures are used as shown in Table III. The key dynamic performances of simulation and datasheet are compared in Table III at 25 and 125 °C. The simulation results of the proposed IGBT model match well with the datasheet under different temperatures, which verifies the proposed modeling method. In addition, simulation waveforms of the proposed model at 25 °C and the most critical case 125 °C are supplied compared with testing waveforms [24], as shown in Fig. 13.

From Fig. 13, the turn-ON and turn-OFF waveforms between simulation and testing under both 25 and 125 °C match well, especially for the N– base punch-through part when the tail current falls rapidly. There are some mismatches for the turn-ON current peak, and this can be improved by a physics-based diode model in future.

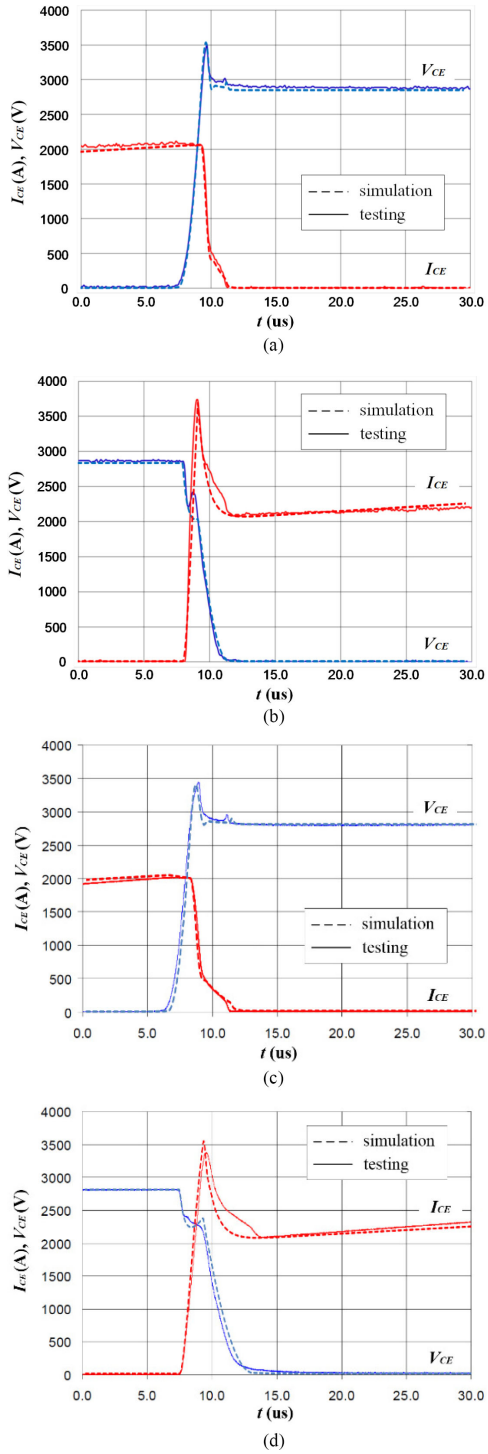

Fig. 13. Double-pulse simulation and testing waveforms at $V_{\rm DC} = 2800$ V, $I_{\rm CE} = 2000$ A. (a) Turn-OFF transient: $T_j = 25$ °C. (b) Turn-ON transient: $T_j = 25$ °C. (c) Turn-OFF transient: $T_j = 125$ °C. (d) Turn-ON transient: $T_j = 125$ °C.

B. Model Verification in HVdc Interruption

After verifying the single IGBT model, the HVdc interruption in this article is then simulated using the proposed electrothermal

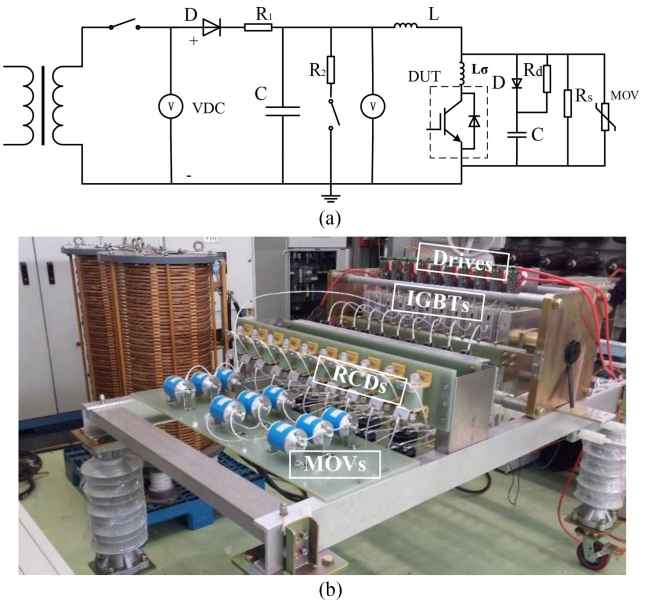

Fig. 14. Circuit schematic and testing platform of HVdc interruption. (a) Simulation circuit schematic. (b) Testing platform of ten IGBTs in series connection.

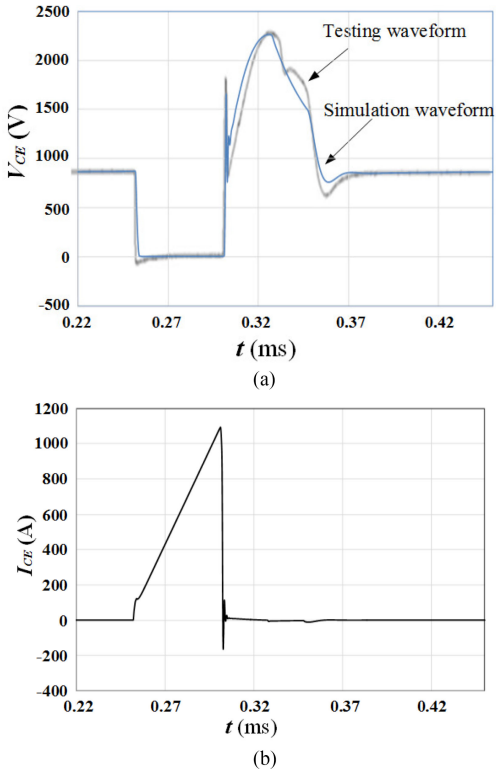

Fig. 15. Simulation and testing waveforms of single IGBT. (a) Simulated and tested V_{CE} waveforms. (b) Simulated I_{CE} waveform.

model and tested in a solid breaker prototype [25] as shown in Fig. 14. Because there are no efficient ways to direct measure the junction temperature at fast switching transient, we use an indirect way to verify the electrothermal effect of the model at switching transient by comparing the electric waveforms since the temperature variation is coupled in the electric characteristics through the TN as shown in Fig. 10. The Cauer TN of the device itself is directly transferred from the Foster TN in the device datasheet using the typical method. The TN of heatsink is also calculated from its structure using the typical method. The calculation of the TN is actually normal and thus being ignored in the article.

To be simple, the device under test in Fig. 14(a) is drawn as one IGBT which is actually several series-connected IGBTs as shown in Fig. 11. R_1 is the current limitation resistor which is eliminated in the large current experiment. R_2 is discharging resistor. L is the inductive load. R_s is the static voltage balancing resistor and R_d is the dynamic voltage balancing resistor. The testing includes three conditions: single IGBT, three IGBTs in series connection, and ten IGBTs in series connection. The setting method of the above components is already introduced in [25]. The series-connected IGBTs are all switched simultaneously in simulations.

1) Single IGBT Testing: The testing condition is: $V_{\mathrm{DC}} = 800$ V, triggering pulse width is 50 μs, and $L = 40$ μH. As shown in Fig. 15, the whole turn-OFF process is 80 μs, and the simulation and testing waveforms of voltage and current during HVdc interruption match well. The detailed values are shown in Table IV.

2) Three IGBTs in Series Connection: The testing condition is: $V_{\mathrm{DC}} = 3000$ V, triggering pulsewidth is 50 μs, and $L = 40$ μH. As shown in Fig. 16, the whole turn-OFF process is 50 μs, and the simulation and testing waveforms of the total voltage and current through the three IGBTs during HVdc interruption match well.

TABLE IV
COMPARISON BETWEEN SIMULATION AND TESTING OF HVDC INTERRUPTION

IGBT connection	Simulation		Testing		Error (%)	
	Vpeak	Ipeak	Vpeak	Ipeak	Vpeak	Ipeak
1 IGBT	2.33 kV	1.056 kA	2.3 kV	1.093 kA	1.3	3.4
3 IGBTs in series	9 kV	3.41 kA	8.8 kV	3.4 kA	2.3	0.3
10 IGBTs in series	28.62 kV	5.2 kA	29.04 kV	5 kA	1.5	4

The mismatch during current shifting is mainly introduced by the *RCD* circuit. The detailed values are shown in Table IV.

3) Ten IGBTs in Series Connection: The testing condition is: $V_{\mathrm{DC}} = 10$ kV, triggering pulsewidth is 1.3 ms, and $L = 1.5$ mH. As shown in Fig. 17, the whole turn-OFF process is around 1 ms and the voltage is clamped to 23 kV of ten IGBTs after the metal oxide varistors (MOV) acts. The simulation and testing waveforms of the total voltage and current during HVdc interruption match well. The detailed values are shown in Table IV.

From Figs. 15–17, the proposed electrothermal model of the press-pack IGBT exhibits the accurate current and voltage during the HVdc interruption. The voltage and current peak in Table IV shows good consistency between the model simulation and the measurements, which further proves the accuracy at the switching transient and even in the series connection simulation.

The difference between the test and simulation results as shown in Table IV is explained as follows. For the current peak difference, it is mainly caused by the circuit settings such as V_{DC}, L, and turn-ON pulsewidth (tpulse) since I_{peak}

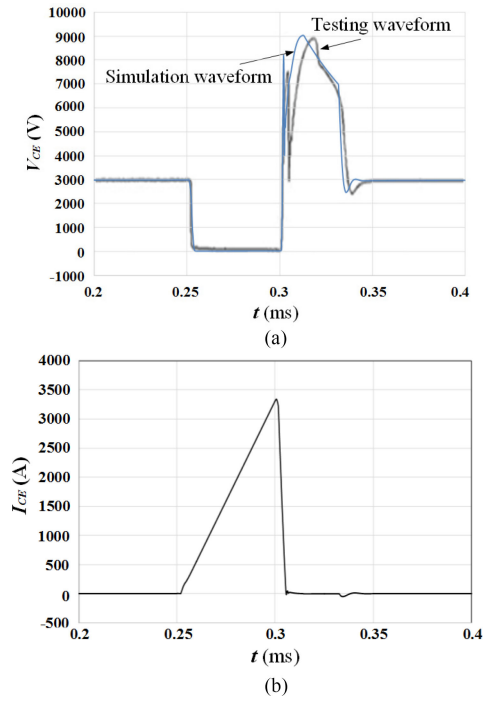

Fig. 16. Simulation and testing waveforms of three IGBTs in series connection. (a) Simulated and tested $V_{\rm CE}$ waveforms. (b) Simulated I_{CE} waveform.

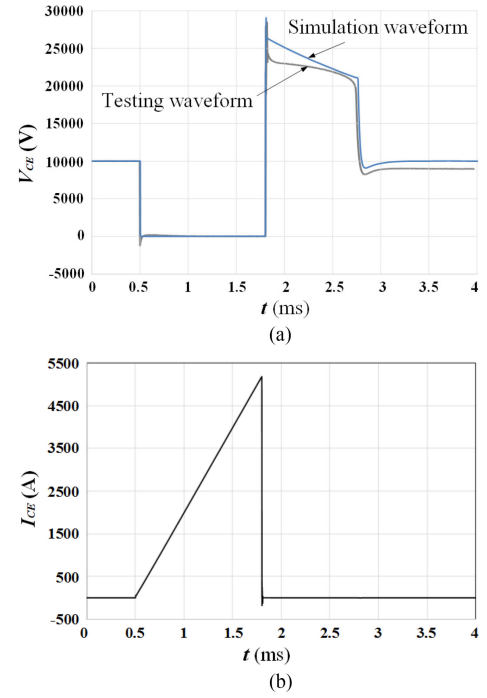

Fig. 17. Simulation and testing waveforms of ten IGBTs in series connection. (a) Simulated and tested $V_{\rm CE}$ waveforms. (b) Simulated $I_{\rm CE}$ waveform.

$= V_{\rm DC}/L$*tpulse. L could be a little more sensitive since it is in the denominator. For the voltage peak difference, it is more complicated and mainly caused by three factors: 1) the error of device model itself as shown in Table III; 2) stray inductance of the IGBT current branch which includes the stray inductance of the module's package and of the heatsink; and 3) the inevitable voltage-sharing unbalance for series-connected IGBTs. Because

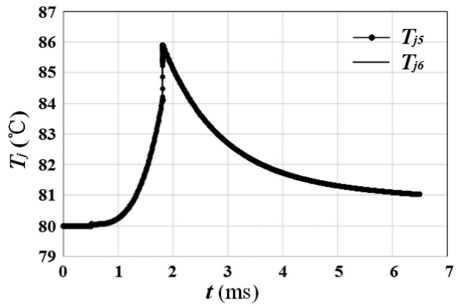

Fig. 18. Junction temperature simulation results of the middle two IGBTs under case 3.

the equal voltage sharing cannot be guaranteed in practical applications, the practical turn-OFF sequence of each IGBT could be a little different. The first turn-OFF device endures higher voltage, making the total turn-OFF time longer than simultaneous turn-OFF which is the case in simulations. Therefore, for real system design in case of much more press-pack modules connected in serial under HVdc interruption event, the simulation accuracy could be improved from three aspects: 1) improve the model accuracy especially for turn-OFF transient under specific HVdc conditions; 2) measure the stray inductance of modules and heatsink used in the breaker accurately; and 3) considering the inconsistency of actual gate signals of each IGBT in serial in the simulation. In addition, effective voltage-sharing strategy is necessary for large amount of IGBTs in serial, which can also be accurately designed using the proposed device model.

The method of model verification in this article can be concluded as follows: first, verify the electropart and its temperature dependence using double pulse testing; then further verify the TN in the solid breaker under longer interruption time which reflects the temperature variation; finally comparing the electric waves to prove the electro and thermal effects because the temperature variation is coupled in the electric characteristics during the switching transient through the relationship shown in Fig. 10.

After the verification of the model, we could evaluate the junction temperature variation at switching using the proposed model. We choose case 3 as an example because it has higher current and longer turn-ON pulse to present more obvious temperature variation. Fig. 18 shows the junction temperature simulation results of the middle two IGBTs (the fifth and sixth out of the ten IGBTs) under case 3 using the proposed electrothermal model configuration in Fig. 11. The ambient temperature is set to 80 °C. The simulated junction temperature rise at the interruption transient is about 6 K for both devices.

For higher current, this temperature rise could be more because of the coupling effect in Fig. 10. Furthermore, unbalanced voltage sharing could also lead to higher temperature rise of partial IGBTs in serial.

VI. Conclusion

In this article, a physics-based electrothermal transient model of a high-voltage press-pack IGBT has been established based on the semiconductor structure and the press-pack package structure. The proposed model of the press-pack HVIGBT

takes into account the carrier recombination in the wide base region, the different injection level in the SPT buffer layer, and the double-sided heat transfer of the package structure. The presented model is also implemented in common software and verified first by the double-pulse testing. A solid breaker with series-connected IGBTs is then built to further verify the proposed model under HVdc interruptions. The simulation and testing results of voltage and current show good consistency, which proves that the proposed model can be used to assist the accurate design of the solid breaker in HVdc transmissions with good prediction of the voltage and current margin.

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