A Gate Drive Circuit and Dynamic Voltage Balancing Control Method Suitable for Series-Connected SiC MOSFETs

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***Abstract*—Compared with silicon insulated-gate bipolar transistor, silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) presents good features that it clearly shows on its switching and thermal performance. However, the fast switching speed of SiC MOSFET makes it much more difficult for solving the dynamic voltage imbalance problem caused by the parameter fluctuations of the SiC MOSFETs and drive circuits when they are connected in series. This article proposes an effective gate drive circuit and its dynamic voltage balancing control method to tackle this issue. The proposed method not only balances the dynamic voltage during high-speed switching but also adapts to the variation of the dc-bus voltage by utilization of overdrive control method (ODCM). Furthermore, to widen the control range of the ODCM, a switched-capacitor compensation method by switching and combining different drive capacitors into different values is proposed. The operation principles and the parameter design method are discussed in detail. The performance of the proposed series-connected SiC MOSFETs gate drive circuit and its dynamic voltage balancing control method is validated by experimental results. The dynamic voltage can be well balanced within the design range.**

***Index Terms*—Dynamic voltage balancing, gate drive circuit, series connected, silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs).**

I. Introduction

COMPARED with silicon material, silicon carbide (SiC) material has many excellent properties, such as reasonable electron mobility, larger critical electric field, and greater thermal conductivity, providing lower ON-resistance, higher blocking voltage, higher operation temperature, and higher switching frequency capability when used in the field of power semiconductor devices [1]–[5]. All of these are beneficial to further improve the performance of power electronic equipment.

Despite that the maximum voltage rating of SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) in laboratories has reached over 10 kV [5]–[9], due to the limitations of manufacture craft and cost, the maximum voltage rating of commercial available SiC MOSFETs is only 1.7 kV. In some high-voltage applications, in order to increase the blocking voltage of SiC MOSFETs, series connection is essential. However, due to the parameter fluctuations of the power devices and external circuits and the different propagation delays of the gate drive circuits, the dynamic imbalance problem will occur when direct connected MOSFETs are in series. In addition, as the switching speed of power devices increases, the dynamic imbalance problem becomes more serious. Therefore, it is necessary to solve the dynamic imbalance problem by using drive technology for series-connected power devices.

The drive technology for series-connected power devices has been studied since the 1990s [10]–[12]. Two main tasks of series operation of power devices are static and dynamic voltage balancing. The general solution for static voltage balancing is to parallelize static voltage balancing resistors with each power devices in series [13]–[19], [22]–[28]. The resistance selection of the static voltage balancing resistors requires a tradeoff between power consumption and OFF-state voltage imbalance ratio [24]. Methods of dynamic voltage balancing for series-connected power devices can be classified into three categories: passive snubber method [9], [13], active control method [14]–[21], and capacitive coupling method [22]–[28].

The passive snubber method implements passive devices in parallel with each power devices. Using the snubber capacitors, whose capacitance is at least five to ten times of the output capacitance of power devices [9], could minimize the dynamic voltage imbalance but increase snubber power loss and device commutation time.

The active control method is a major way to balance the dynamic voltage of series-connected insulated-gate bipolar transistors (IGBTs). In [14] and [15], a gate signal delay method is proposed to compensate the dynamic voltage imbalance caused by the inconsistent characteristics of the driving circuits and IGBTs. But the control resolution is affected by the performance of the controller and the delay of the sensing and the A/D

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conversion circuit. In the work proposed in [16], all the gate wires of the series-connected IGBTs are magnetically combined with gate-balancing core to synchronize the gate drive current so that the gate delay difference of the IGBTs can be effectively controlled. However, this method provides little optimization for the voltage unbalancing caused by voltage slope differences [17]. In [18], an active voltage control method for the series-connected IGBTs is proposed, which allows dv_{ce}/dt adaptive variation in switching transients. But, a preconditioning step is required in this method, which is not suitable for SiC MOFETs. An active voltage control method [19] achieves dynamic voltage control for both turn-ON and turn-OFF periods by introducing a current source at the gate side of the low-side device, but only controls the switching performance of the low-side device. An improved hybrid active gate control method is proposed in [17]; by controlling a digital-controlled current-source driver, it can both reduce the switching losses and balance the dynamic voltage of the series-connected IGBTs. However, a considerable output delay generated from the current source is unacceptable in series-connected SiC MOSFETs. When active control method is used, two main problems will deteriorate the control performance of the series-connected SiC MOSFETs. The first problem is the control delay, which is mainly caused by the control loop. For SiC MOSFETs that only have tens or hundreds of nanoseconds rise and fall time, the delay of active control is normally large. The second problem is that the overvoltage caused by dynamic voltage imbalance during the start-up period may cause permanent damaged to SiC MOSFETs before the active control method works. Therefore, the normal active control methods need some improvement and are not the best choice for series SiC MOSFETs. An active gate delay control method that uses delay line IC has been reported in [20] to adapt the fast switching speed of SiC MOSFET; the minimum delay control step is 150 ps. But, this control method does not consider the overvoltage caused by dynamic voltage imbalance during start-up period. To solve this problem, a voltage balancing control strategy under steady state and start-up condition based on digital time delay circuit is proposed [21]. By updating the initial delay time, the voltage imbalance at start-up period can be reduced. However, the initial delay time may vary due to the parameter fluctuations of the power devices and gate drive circuit.

The capacitive coupling method was first reported in 1994 [21] and optimized in [22]–[25]. The capacitive coupling method uses only one external gate driver and several drive capacitors to drive the series string of voltage-driven devices, such as IGBTs and MOSFETs. In [21], diodes and *RC* networks couple the drive signal to the gate sides of series MOSFETs. However, its voltage balancing performance still needs to be optimized during static and dynamic periods. The circuit is optimized in [22]. The static voltage balancing resistors are introduced to balance the static voltage and a capacitor is inserted to fast trigger the entire series stack reliably. A quasi-active gate control circuit has been reported in [24]. The initial turn-OFF delay, dynamic voltage sharing, and sustainability of the gate voltage are further optimized. In [25], capacitive coupling method is optimized to obtain a negative voltage during the turn-OFF period and applied to a dc breaker with constant dc-bus voltage.

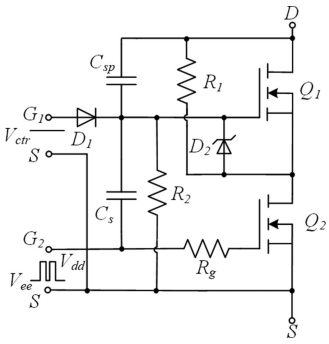

Fig. 1. Series-connected gate drive circuit for SiC MOSFETs.

Compared with the passive snubber and active control method, the capacitive coupling method has a simpler circuit structure and a faster response speed, and is more suitable for series SiC MOSFETs. However, the driving capability of this approach is directly affected by the dc-bus voltage, and it is difficult to achieve perfect dynamic voltage balancing when the dc-bus voltage changes. To handle this problem, papers [27] and [28] use passive snubber circuits in the capacitive coupling series-connected SiC MOSFETs gate drive circuit, which sacrifices the switching speed of the SiC MOSFETs and results in considerable snubber loss.

In this article, to accommodate fast switching speed and achieve a good dynamic voltage balance of SiC MOSFETs in series, a simple and effective SiC MOSFETs series-connected gate drive circuit based on capacitive coupling method is proposed. Meanwhile, to handle the dynamic voltage imbalance problem when the dc-bus voltage changes, a dynamic voltage balancing control method (DVBCM) composed of overdrive control method (ODCM) and switched-capacitor compensation method (SCCM) is proposed. ODCM utilizes a controllable voltage source $V_{\rm ctr}$ to change the overdrive depth of the high-side SiC MOSFETs and compensate for the effect of dc-bus voltage variation on drive capability of drive capacitor. SCCM is proposed to widen the control range of DVBCM by switching and combining different driving capacitors into different values. In this article, within the design range, the dynamic and static voltages between the series-connected SiC MSOFETs are well balanced.

The rest of this article is organized as follows. The turn-ON transient, turn-OFF transient, and steady state of the proposed series-connected SiC MOSFET gate drive circuit are analyzed in Section II. In Section III, DVBCM consisting of ODCM and SCCM is discussed. Section IV presents the discussion about the parameter calculations. The gate drive circuit and control method are evaluated by experimental results in Section V. Finally, Section VI concludes this article.

II. Series-Connected Circuit for SIC MOSFET

Fig. 1 shows the proposed gate drive circuit for series-connected SiC MOSFETs. SiC MOSFETs Q_1 and Q_2 are connected in series. R_1 and R_2 are static voltage balancing resistors. Only an external driver for SiC MOSFET Q_2 is needed in this circuit. The external gate driver drives Q_2 directly. SiC MOSFET Q_1 is

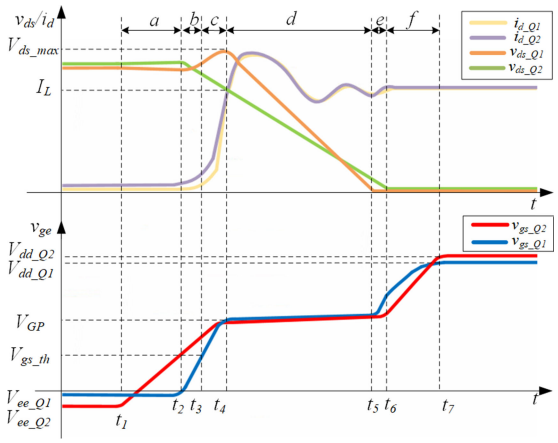

Fig. 2. Analyzed waveforms during the turn-ON transient.

driven by a well-designed high-voltage capacitor C_s. A transient voltage suppressor (TVS) D_2 is used to protect gate–source of Q_1 from overvoltage and provide a current path during the OFF-state. Due to the speed-up capacitor $C_{\rm sp}$ is connected in parallel with the C_{gd} of Q_1, only the C_{gd} of Q_1 is considered in this section. The effect of $C_{\rm sp}$ is discussed in Section III, and the selection method of $C_{\rm sp}$ is introduced in Section IV. The turn-ON transient, turn-OFF transient, and steady state for the proposed circuit under the clamped inductive load are described in detail. Each switching transient includes five periods, respectively.

A. *Turn-ON Transient*

As shown in Fig. 2, the turn-ON transient can be divided into five stages: turn-ON delay period of Q_2, turn-ON delay period of Q_1, current rise period, voltage fall period, and positive overdrive period. In Fig. 2, $V_{ds\_\max}$ is the maximum drain–source voltage of Q_1 during turn-ON process, I_L is the load current, V_{dd_Q1} and V_{dd_Q2} are the positive driving voltage of Q_1 and Q_2, respectively, V_{ee_Q1} and V_{ee_Q2} are the negative driving voltage of Q_1 and Q_2, respectively, $V_{\rm GP}$ is the Miller platform voltage, and $V_{gs\_\rm th}$ is the gate threshold voltage of SiC MOSFETs.

1) Turn-ON Delay Period of Q_2 *[see Fig. 3(a)]:* Q_1 and Q_2 are in the OFF state and withstand one half the dc-bus voltage due to the static voltage balancing resistors R_1 and R_2 before t_1. The turn-ON signal makes the turn-ON operation of Q_2, at t_1. V_{dd_Q2} forms a gate drive current i_g via the gate drive resistor R_g and charges Q_2's input capacitor $C_{\rm iss}$, which is composed of C_{gs} and C_{gd} ($C_{\rm iss} = C_{gs} + C_{gd}$), and the gate–source voltage of Q_2 $v_{gs\cdot Q2}$ rises. The expression of $v_{gs\cdot Q2}$ at this period is shown in the following equation:

$$v_{gs\_Q2}(t) = (V_{ee\_Q2} - V_{dd\_Q2})\, e^{\frac{t_1 - t}{R_g\left(C_{gs\_Q2}+C_{gd\_Q2}\right)}} + V_{dd\_Q2} \tag{1}$$

where C_{gs_Q2} and C_{gd_Q2} present the gate–source capacitance and gate–drain capacitance of Q_2, respectively.

2) Turn-ON Delay Period of Q_1 *[see Fig. 3(b)]:* At t_2, v_{gs_Q2} reaches the gate threshold voltage $V_{gs\_\rm th}$. Since Q_1 is still in the OFF state, the drain–source voltage of Q_2 v_{ds_Q2} begins to fall,

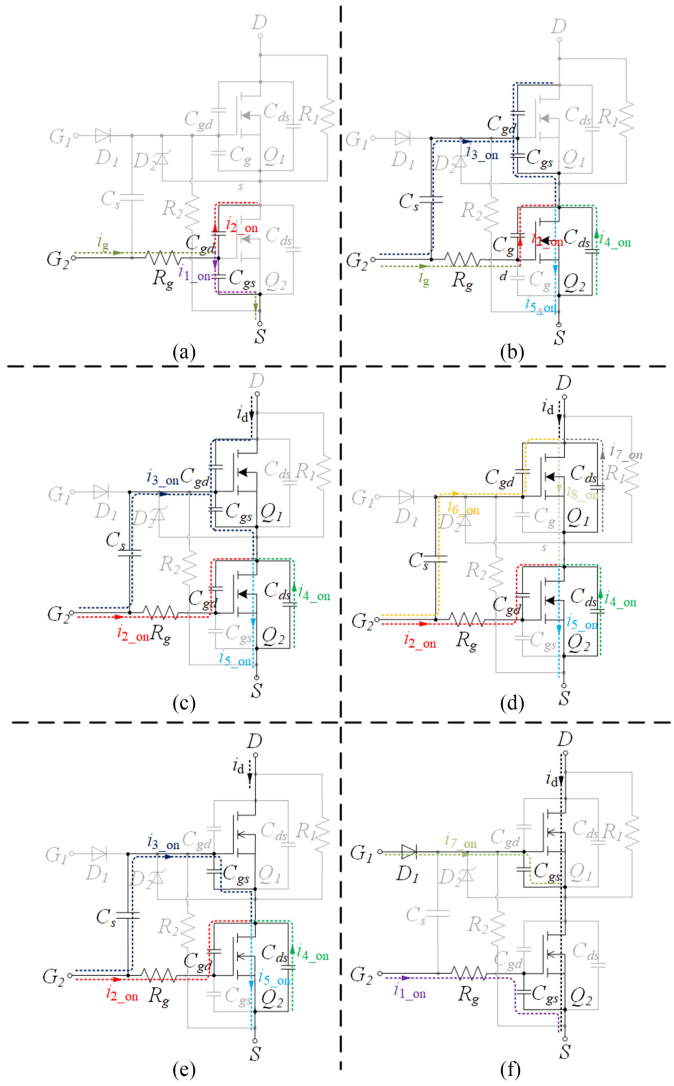

Fig. 3. Turn-ON transient of the series-connected SiC MOSFETs. (a) t_1–t_2. (b) t_2–t_3. (c) t_3–t_4. (d) t_4–t_5. (e) t_5–t_6. (f) t_6–t_7.

whereas the drain–source voltage of Q_1 v_{ds_Q1} rises accordingly and $\Delta V_{ds\_Q2} = \Delta V_{ds\_Q1}$. As v_{ds_Q2} drops rapidly, C_s begins to discharge through Q_1's $C_{\rm iss}$, producing the gate drive current of Q_1 $i_{3\_\rm on}$ and the gate–source voltage of Q_1 v_{gs_Q1} rises

$$i_{3\_\rm on} = C_s \frac{dv_{Cs}}{dt} = C_s \frac{dv_{ds\_Q2}}{dt} \tag{2}$$

where v_{Cs} is the voltage on drive capacitor C_s.

3) Current Rise Period [see Fig. 3(c)]: Once v_{gs_Q1} reaches $V_{gs\_\rm th}$ at t_3, the current i_d flowing through Q_2 begins to increase until i_d increases to the load current. During this period, v_{ds_Q2} drops and continues providing gate current $i_{3\_\rm on}$ for Q_1. Until t_4, v_{gs_Q1} reaches $V_{\rm GP}$ and the current rise period ends.

4) Voltage Fall Period [see Fig. 3(d) and (e)]: When Q_1 enters the Miller plateau at t_4, v_{ds_Q1} reaches its maximum value $V_{ds\_\max}$ and begins to decrease. By adjusting the parameters of the drive circuit, v_{ds_Q1} is reduced to the conduction voltage drop, which is close to zero slightly before v_{ds_Q2}, and Q_1 exits

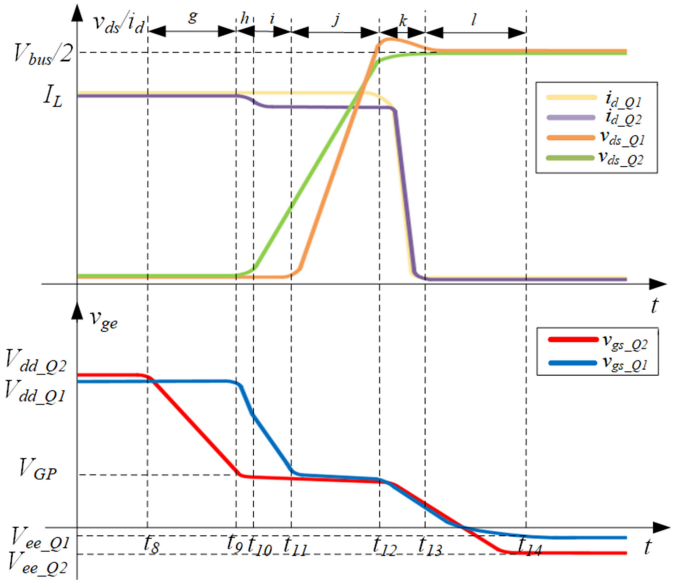

Fig. 4. Analyzed waveforms during the turn-OFF transient.

the Miller plateau and enters into the gate overdrive period

$$v_{ds\_\max} = \frac{V_{\text{bus}}}{2} + \Delta v_{ds\_Q1} = \frac{V_{\text{bus}}}{2} + \frac{C_{\text{iss}}}{C_s}\left(V_{ee\_\text{Q1}} + V_{gs\_\text{th}} + \frac{I_L}{g_m}\right). \quad (3)$$

5) Positive Overdrive Period [see Fig. 3(f)]: v_{cs} follows v_{ds_Q2} and goes to zero. Then, the diode D_1 turns ON. The driving voltages V_{dd_Q2} and V_{ctr} provide drive currents i_{7_on} and i_{1_on} for Q_1 and Q_2, respectively, driving v_{gs_Q1} to V_{dd_Q1} and v_{gs_Q2} to V_{dd_Q2}.

B. Turn-off Transient

As shown in Fig. 4, the turn-OFF transient can be divided into five stages: turn-OFF delay period of Q_2, turn-OFF delay period of Q_1, voltage rise period, current fall period, and negative overdrive period.

1) Turn-off Delay Period of Q_2 *[see Fig. 5(g)]:* When a turn-OFF signal occurs at t_8, C_{iss} of Q_2 begins to discharge and v_{gs_Q2} starts to decrease as the gate drive voltage steps from V_{dd} to $-V_{ee}$.

2) Turn-off Delay Period of Q_1 *[see Fig. 5(h) and (i)]:* At t_9, v_{gs_Q2} drops to V_{GP}, Q_2 enters the saturation region, its drain–source voltage v_{ds_Q2} starts to rise, and v_{Cs} rises accordingly. The generated drive current $i_{3\cdot\text{off}}$ causes $v_{gs\cdot Q1}$ to drop rapidly. When v_{cs} rises to V_{dd1}, diode D_1 begins reverse recovery, producing a reverse recovery current $i_{2\cdot\text{off}}$. At this time, $i_{2\cdot\text{off}}$ and $i_{3\cdot\text{off}}$ work together to turn Q_1 OFF. At t_{10}, the reverse recovery ends and $i_{3\cdot\text{off}}$ continues turning the Q_1 OFF.

3) Voltage Rise Period [see Fig. 5(j)]: At t_{11}, V_{gs_Q1} drops to V_{GP}, Q_1 enters the saturation region, and the drain–source voltage v_{ds_Q1} starts to rise. Through the adjustment of the drive circuit parameters, v_{ds_Q1} and v_{ds_Q2} reach half of the dc-bus voltage almost simultaneously at t_{12}, and the voltage rise period ends. That is, the dynamic voltage is balanced during the turn-OFF transient. In order to balance the dynamic voltage between Q_1 and Q_2, the drive capacitor C_s should provide a continuous driving force for Q_1 at least before t_{12}. The selection method of the gate drive circuit parameters is introduced in detail in Section IV.

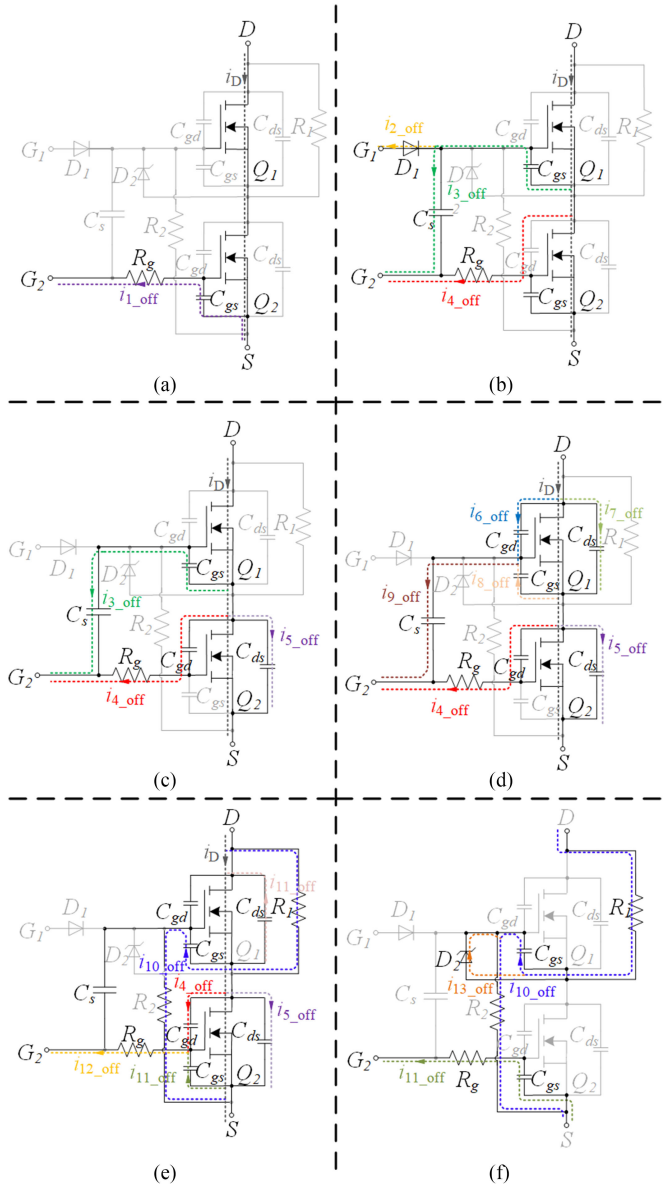

Fig. 5. Turn-OFF transient of the series-connected SiC MOSFETs. (g) t_8-t_9. (h) t_9-t_{10}. (i) $t_{10}-t_{11}$. (j) $t_{11}-t_{12}$. (k) $t_{12}-t_{13}$. (l) $t_{13}-t_{14}$.

4) Current Fall Period [see Fig. 5(k)]: At t_{12}, Q_1 and Q_2 exit the Miller plateau, the current drop period begins. v_{gs_Q2} is driven by i_{12_off} and v_{gs_Q1} is driven by i_{10_off}. It should be noted that in this circuit, the work of switching OFF the load current during the turn-OFF transient is mainly done by Q_1.

5) Negative Overdrive Period [see Fig. 5(l)]: After the end of the current drop period, under the action of Q_2's negative driving voltage $-V_{ee}$ and the clamp diode D_2, v_{gs_Q1} continues to drop to -0.7 V, and v_{gs_Q2} drops to $-V_{ee}$. The turn-OFF process ends.

C. Steady State

R_1 and R_2 are static voltage balancing resistors. In the OFF state, the voltage balancing current forms a path through the voltage balancing resistors R_1 and R_2 and the voltage clamping diode D_2. D_2 clamps V_{gs_Q1} at -0.7 V, which is the forward voltage of D_2. The resistance selection of R_1 and R_2 requires a tradeoff between power consumption and OFF-state voltage imbalance ratio. To obtain the optimum performance, the parameters selection method is described in detail in Section IV.

III. Dynamic Voltage Balancing Control Method

A. Overdrive Control Method

By analyzing the turn-ON and turn-OFF transients of the proposed series-connected SiC MOSFET drive circuit in Section II, it can be found that Q_1 is mainly driven by the current caused by voltage change of C_s, and the voltage variation of C_s during turn-ON and turn-OFF processes is equal to one half of dc-bus voltage when the dynamic voltage is balanced. When the dc-bus voltage changes, the driving capability of C_s changes accordingly, resulting in a dynamic voltage imbalance of Q_1 and Q_2.

Fig. 2 shows that during turn-ON transient, the maximum imbalance occurs at t_4. In order to minimize the voltage spike at t_4, a 24-pF speed-up capacitor is connected in parallel at the drain–source of Q_1. From (3), a larger C_s means a smaller voltage spike. With the speed-up capacitor $C_{\rm sp}$, the drive capacitor C_s can be a larger one while achieving the dynamic voltage balancing. The selection methods and the relationship between the speed-up capacitor and the voltage spike are discussed in detail in Section IV. The voltage spike can be controlled within a certain range with appropriate parameter selection. Therefore, the voltage imbalance problem during the turn-ON transient in this circuit is not critical.

During the turn-OFF transient, the controllable voltage source ($V_{\rm ctr}$ in Fig. 1) directly affects the turn-OFF speed of Q_1 by changing the overdrive depth of Q_1 in the ON state. When the dc-bus voltage changes, the driving capacity of C_s changes accordingly. Dynamic voltage balancing is achieved by changing $V_{\rm ctr}$ thus adjusting the overdrive depth of Q_1, and compensate for the effect of dc-bus voltage variation on C_s drive capability. For example, when the dc-bus voltage increases, the driving capacity of C_s increases. The dynamic voltage imbalance will occur due to the faster turn-OFF of Q_1. At that time, adding $V_{\rm ctr}$ appropriately to offset the increase in the driving capacity of C_s balances the dynamic voltage at turn-OFF transient.

However, the maximum value of $V_{\rm ctr}$ is determined by the absolute maximum values of gate–source voltage $V_{gs\max}$ and therefore $V_{\rm ctr}$ must be less than $V_{\rm ctr\_max}$, which is shown in (4). In order to ensure fully open of the SiC MOSFET Q_1, it is necessary to ensure that V_{gs_Q1} is greater than 15 V; we can obtain the minimum value of $V_{\rm ctr}$, which is shown in (5)

$$V_{\rm ctr\_max} = i_d R_{d\rm son} + V_{D1\_\rm on} + (V_{gs\max} - V_{gs\_\rm sm}) \quad (4)$$

$$V_{\rm ctr\_min} = i_d R_{d\rm son} + V_{D1\_\rm on} + V_{gs\,\rm min} \quad (5)$$

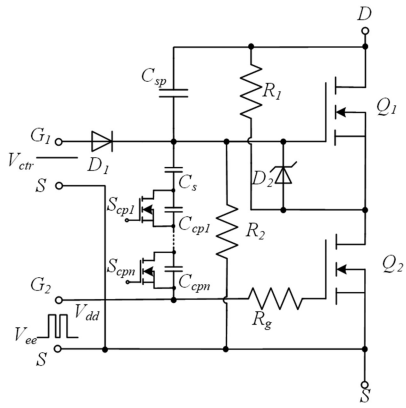

Fig. 6. Series-connected drive circuit for SiC MOSFETs with switched capacitor.

where $R_{d\rm son}$ is the drain–source ON-state resistance of the SiC MOSFET, $V_{D1\_\rm on}$ is the forward voltage of D_1, $V_{gs\_\rm sm}$ is the safety margin of V_{gs}, and in this article $V_{gs\_\rm sm}$ is set to 3 V.

B. Switched-Capacitor Compensation Method

The dynamic voltage can be controlled by ODCM when the dc-bus voltage changes. However due to the limitations of $V_{\rm ctr}$, the effective range of the dynamic voltage balancing control method is limited. Therefore, the SCCM is carried out to widen the control range of ODCM.

Fig. 6 shows the gate drive circuit for series-connected SiC MOSFET with switched capacitor $C_{\rm cp1},\ldots,C_{{\rm cp}n}$, which can be switched by $S_{\rm cp1},\ldots,S_{{\rm cp}n}$, respectively. By controlling the switch state of $S_{\rm cp1},\ldots,S_{{\rm cp}n}$, different switched capacitors and C_s can be combined into different driving capacitor. For some applications, the dc-bus voltage fluctuates within a certain range. Therefore, whether the switched capacitor is needed and how many switched capacitors are needed depend on the applications. In this article, series-connected SiC MOSFET gate drive circuit with single switched capacitor is designed and tested.

C. Dynamic Voltage Balancing Control Method

As shown in Fig. 7, DVBCM is comprised by two loops. First, the overdrive control loop is illustrated. The aim of the overdrive control loop is to control the dynamic voltage balancing by controlling the output of an insulated dc–dc converter, which is named $v_{\rm ctr}$ in this article. Its output command $v^*_{\rm ctr}$ is also given to the second loop, switched-capacitor control loop. If the change of dc-bus voltage causes $v^*_{\rm ctr}$ to exceed its limited range, the drive signal of $S_{\rm cp1}$ will change to control the state of the switched capacitor $C_{\rm cp1}$. In higher voltage, due to the drive capability of the drive capacitor is proportional to the dc-bus voltage, a smaller drive capacitor is needed to guarantee the dynamic voltage balancing between the two SiC MOSFETs. In this case, $S_{\rm cp1}$ is turn-OFF and the drive capacitor consists of C_s and $C_{\rm cp1}$ in parallel. In contrast, $S_{\rm cp1}$ is turned ON to bypass $C_{\rm cp1}$ and the drive capacitor is C_s.

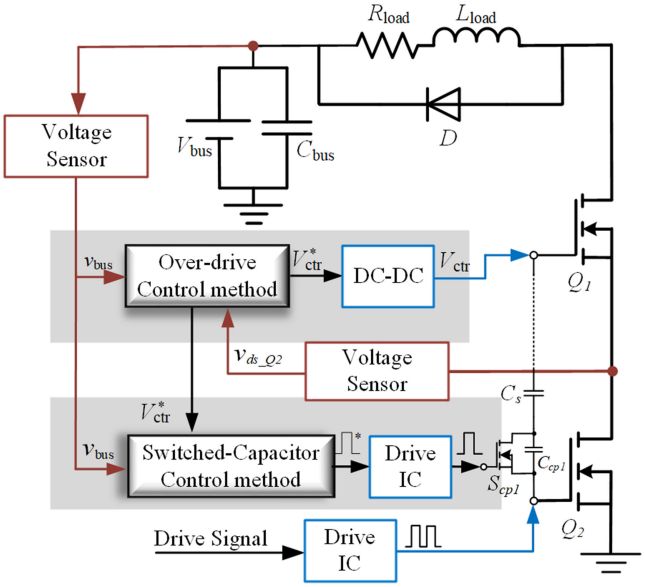

Fig. 7. Structure of the control method for dynamic voltage balancing and the setup used for experiments.

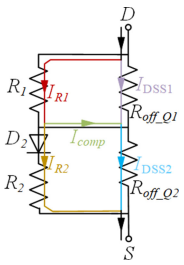

Fig. 8. Equivalent circuit model for steady-state voltage balancing.

IV. Parameter Selection and Calculation

In this section, the parameters are calculated under the rated condition, which is defined as: dc-bus voltage $V_{\rm bus} = 1.2$ kV, $I_D = 2$ A, and $V_{gs\_Q1} = -0.7/20$ V.

A. Steady-State Voltage Balancing Resistors

The equivalent circuit model for steady-state voltage balancing is shown in Fig. 8, where $I_{\rm DSS1}$ and $I_{\rm DSS2}$ are the leakage currents of SiC MOSFETs Q_1 and Q_2, respectively, and $R_{\rm off\_Q1}$ and $R_{\rm off\_Q2}$ present the equivalent resistance of Q_1 and Q_2, respectively. To simplify the analysis, we assume that $I_{\rm DSS2}$ is greater than $I_{\rm DSS1}$. In order to ensure that the steady-state voltage imbalance ratio is less than 5%

$$\frac{I_{R1}\cdot R_1 - (I_{R1} - I_{\rm comp})\cdot R_2}{I_{R1}\cdot R_1} \le 5\% \tag{6}$$

where $I_{\rm comp}$ is defined by

$$I_{\rm comp} = I_{\rm DSS2} - I_{\rm DSS1}. \tag{7}$$

In this case, we can easily find that

$$I_{R1}\cdot R_1 > I_{R2}\cdot R_2. \tag{8}$$

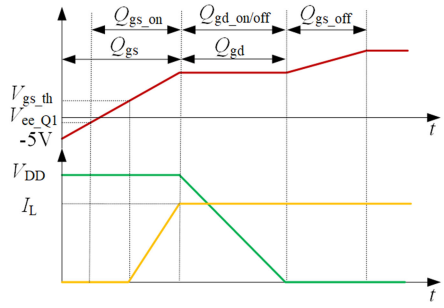

Fig. 9. Basic gate charge definitions.

Combining (6)–(8), we can obtain

$$I_{R1} \ge 20\cdot(I_{\rm DSS2} - I_{\rm DSS1}). \tag{9}$$

Then, R_1 and R_2 can be selected by the following equation:

$$R_1 = R_2 \le \frac{V_{\rm bus}/2}{20\cdot(I_{\rm DSS2} - I_{\rm DSS1})}. \tag{10}$$

From datasheet, $I_{\rm DSS(max)}$ is 100 μA, and we assume that $I_{\rm DSS(min)}$ is 0 A to guarantee even in the worst case the result is practical. Then, we can obtain

$$R_1 = R_2 \le 300\,{\rm k}\Omega. \tag{11}$$

R_1 and R_2 are set to be 300 kΩ to minimize the power dissipation while achieving static voltage balancing.

B. Drive Capacitor C_s

In order to simplify the parameter selection and calculation of the speed-up capacitor and the drive capacitor, we make the following assumptions and statements.

1) During the turn-ON process, the charges in the drive capacitor transfer to the parasitic capacitor of Q_1 without dissipation. During the turn-OFF process, all of the charges filled in the drive capacitor are supplied by the discharge of parasitic capacitor of Q_1.
2) Parasitic parameters of the gate drive circuit are not considered.
3) C_{gs} is a linear capacitance. C_{gd} is a nonlinear capacitance, but has a constant value when V_{ds} is high.
4) Fig. 9 shows the definitions of basic gate charge in datasheet and this article including Q_{gs}, Q_{gd}, Q_{gs_on}, Q_{gs_off}, Q_{gd_on}, and Q_{gd_off}. And the positive and negative of these symbols present charge inflow or outflow.
5) The speed-up capacitor $C_{\rm sp}$ is not considered in the calculation of C_s. The effect of $C_{\rm sp}$ in the gate drive circuit is discussed later. In this article, SiC MOSFETs C2M1000170D from Cree/Wolfspeed are selected for our design and testing.

During the turn-ON process, in order to ensure reliable turn-ON of Q_1, the drive capacitor C_s should provide at least the driving charge until Q_1 exits the Miller plateau at t_5, as shown in Fig. 2. We can obtain that

$$C_s \ge \frac{Q_{gs\_on} + Q_{gd\_on}}{V_{\rm bus}/2}. \tag{12}$$

Q_{gs} can be found in the datasheet of C2M1000170D, which is 4.7 nC in the condition of $V_{gs} = -5/20$ V. Thus, under the condition of $V_{gs} = -0.7/20$ V, Q_{gs_on} can be estimated to be 3.5 nC.

Q_{gd_on} is defined as

$$Q_{gd\_on} = \int_{v_{gd}=-V_{bus}/2}^{v_{gd}=0} C_{gd} dv_{gd}. \tag{13}$$

To ensure the dynamic voltage balancing during the turn-OFF process, C_s should provide driving charge to drive Q_1 exits the voltage rise period at t_{12}, as shown in Fig. 4. We can obtain that

$$C_s \geq \frac{|Q_{gs\_off} + Q_{gd\_off}|}{V_{bus}/2}. \tag{14}$$

From the figure "gate charge characteristics" in the datasheet, the minimum Q_{gs_off} is -2.9 nC, and Q_{gd_off} is defined as

$$Q_{gd\_off} = \int_{v_{gd}=0}^{v_{gd}=-V_{bus}/2} C_{gd} dv_{gd}. \tag{15}$$

The nonlinear parasitic capacitance C_{gd} can be described by the following equation when V_{gd} is larger than zero [29]–[31]:

$$C_{gd} = A\tanh(aV_{gd} + b) + B \tag{16}$$

where the constant parameters A and B are calculated depending on $C_{gd\min}$ and $C_{gd\max}$ values. Parameter A is the slope of the tan$h$ curves when $V_{gd} = 0$. Parameter B determines the crossover value when $V_{gd} = 0$. Parameters a and b are tuned to fit the slope of C_{gd} with the datasheet graph. The parameters can be obtained by fitting the graph "capacitances versus drain–source voltage" in the datasheet of SiC MOSFET.

From (16), C_{gd} nearly has a constant value when the drain–source voltage v_{gd} is high. For C2M1000170D when v_{gd} is higher than 400 V, C_{gd} can be approximated as a constant value C_{gd_cons}. From the datasheet, Q_{gd} is 5.4 nC, and it can be expressed as

$$Q_{gd} = \int_{v_{gd}=-1200}^{v_{gd}=0} C_{gd} dv_{gd}. \tag{17}$$

Thus, (13) and (15) can be simplified to

$$Q_{gd\_on} = Q_{gd} - \int_{v_{gd}=-1200}^{v_{gd}=-V_{bus}/2} C_{gd\_cons} dv_{gd} \tag{18}$$

$$Q_{gd\_off} = \int_{v_{gd}=-1200}^{v_{gd}=-V_{bus}/2} C_{gd\_cons} dv_{gd} - Q_{gd}. \tag{19}$$

Combining (12), (17), and (18), we can obtain the drive capacitor under 1.2 kV $C_{s\_1.2k}$

$$C_{s\_1.2k} \geq 13.5 \text{ pF}. \tag{20}$$

Combining (14), (17), and (19), we can obtain the drive capacitor under 1.2 kV $C_{s\_1.2k}$

$$C_{s\_1.2k} \geq 12.5 \text{ pF}. \tag{21}$$

Thus, when the dc-bus voltage is 1.2 kV and without the effect of the speed-up capacitor, the drive capacitor should be larger than 13.5 pF. Using the same method, when the dc-bus voltage is 800 V and without the effect of the speed-up capacitor, the drive capacitor $C_{s\_0.8k}$ should be larger than 19.65 pF. In addition, according to the above calculation results and the experimental test, $C_{s\_1.2k}$ and $C_{s\_0.8k}$ are selected as 18 and 30 pF, respectively, to guarantee the dynamic voltage balancing under rated condition.

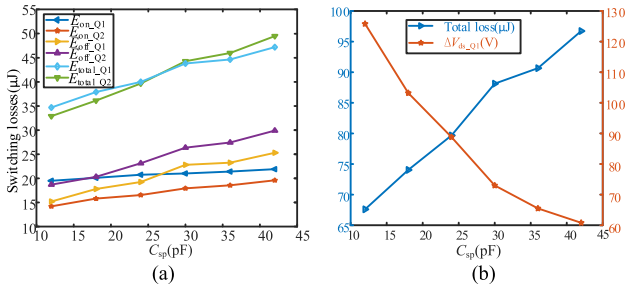

Fig. 10. Effect of C_{sp} on switching loss and voltage spike.

C. Speed-Up Capacitor C_{sp}

As discussed in Section III, the speed-up capacitor C_{sp} is needed in this circuit to reduce the voltage spike during the turn-ON transient.

The gate charge during the switching transient is related to the change in capacitor voltage and capacitance, and the relationship is

$$Q_{charge} = C_s \Delta V_{Cs} - C_{sp} \Delta V_{Csp}. \tag{22}$$

When the dynamic voltage is well balanced, we can obtain that

$$\Delta V_{Cs} = \Delta V_{Csp} = V_{bus}/2. \tag{23}$$

Combining (22) and (23), we can obtain

$$Q_{charge} = (C_s - C_{sp}) V_{bus}/2. \tag{24}$$

It can be seen from (24) that the effect of C_{sp} on dynamic voltage imbalance can be completely offset by increasing the value of C_s. And from (3), the increase in C_s can reduce the voltage spike during the turn-ON process. In addition, the larger speed-up capacitor will increase the driving loss. Therefore, the capacitance of C_{sp} is a tradeoff between driving loss and the voltage spike.

In order to demonstrate the relationship between C_{sp} and switching losses and voltage spike during the turn-ON transient, more experiments have been carried out and the experimental results are shown in Fig. 10. Fig. 10(a) shows the turn-ON, turn-OFF, and total switching loss of Q_1 and Q_2. It can be seen from the experimental results that each loss increases with the increase of C_s. The turn-ON or turn-OFF loss between Q_1 and Q_2 is quite different, but the difference of total switching loss between Q_1 and Q_2 is not significant. This is mainly because the drain–source voltage change of Q_1 lags behind Q_2, resulting in turn-ON loss of Q_1 is greater than Q_2 and turn-OFF loss of Q_1 is less than Q_2. The total switching loss of Q_1 and Q_2 is similar when C_{sp} is 20–35 pF. Fig. 10(b) shows the relationship between total loss, which is the sum of total switching loss of Q_1 and Q_2, and the voltage spike with the change of C_{sp}. When C_{sp} increases, the total loss increases, whereas the voltage spike decreases. According to the experimental results, C_{sp} is set to

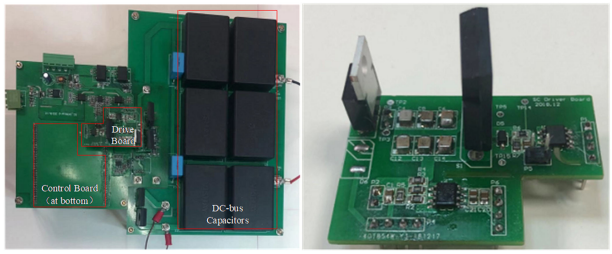

Fig. 11. Photograph of experimental setup (left) and driver board (right).

TABLE I
COMPONENT PARAMETERS IN THE EXPERIMENTAL SETUP

Components	Values	Descriptions
Q_1,Q_2, S_{cp1}	1700 V, 4.9 A	C2M1000170D from CREE/Wolfspeed
C_S	54 pF, 1kV	MLCC from Vishay
C_{cp1}	176 pF, 1kV	MLCC from Vishay
R_g	10 Ω	0805 resistor from Yageo
D	1700V,10A	C3D10170H from CREE/Wolfspeed
D_1	1200V, 2A	C4D02120A from CREE/Wolfspeed
D_2	22V, 600W	SMAJ22A from Littelfuse
R_1,R_2	300 kΩ	2512 resistors from TE

24 pF, a tradeoff between the switching losses and overshoots can be achieved. That is, in our design, considering the output capacitance of Q_1, C_s is set to 54 pF, $C_{\rm cp1}$ is set to 176 pF, and $C_{\rm sp}$ is set to 24 pF.

V. EXPERIMENTS AND RESULTS

To validate the proposed series-connected SiC MOSFETs gate drive circuit and its dynamic voltage balancing control method, the experimental setup was built and three test schemes were carried out. The circuit of the setup is shown in Fig. 7, and the DVBCM with a switched capacitor $C_{\rm cp1}$ is designed and tested. The photographs of the series-connected gate drive and the experimental setup are shown in Fig. 11. The parameters of the components in the experimental setup are shown in Table I. The static voltage balancing resistors R_1 and R_2 are composed of three 100 kΩ resistors connected in series, and the drive capacitors C_s and $C_{\rm cp1}$ are composed of several multilayer ceramic capacitors (MLCCs) connected in parallel. The three test schemes are double-pulse test (DPT) under inductive load in open-loop mode, resistive and inductive load tests in open-loop mode, and dc-bus changes test in close-loop mode, which are described in detail in the following sections.

A. Double-Pulse Test

In order to validate the dynamic and static voltage balancing performance of the proposed series-connected SiC MOSFET gate drive circuit under 1.2 kV dc-bus voltage, the first test DPT is done. The load in this test is a 2.5 mH inductive load. The $V_{\rm crt}$ is set to 22 V. The gate–source voltage of Q_2 is set to −5 V when turned OFF and 19 V when turned ON. The experimental results of DPT are shown in Fig. 12. It can be seen from Fig. 12(a) that the proposed series-connected SiC MOSFETs gate drive circuit can achieve good static and dynamic voltage balancing. Fig. 12(a) shows, when the drain–source voltage of Q_2 changes during the switching transient, the driving capacitor drives Q_1 almost without delay. In the steady state, there is almost no voltage difference between the two SiC MOSFETs due to the effort of R_1 and R_2. Thus, the proposed drive circuit has a good dynamic and static voltage balancing performance. Fig. 12(b) shows the zoom-in view of the turn-ON process. During the turn-ON process, Q_1 quickly follows the change of Q_2, and the maximum drain–source voltage of Q_1 is 688 V. The drain–source voltages of Q_1 and Q_2 reach 0 V almost simultaneously. Fig. 12(c) shows the zoom-in view of the turn-OFF process. The drain–source voltage of Q_1 rises slightly later than the rise of Q_2, but they rise to 600 V almost simultaneously. Before Q_1 enters the Miller platform, Q_1's gate–source voltage has a voltage valley. This is mainly caused by the rapid discharge of $C_{\rm sp}$ and the internal gate resistor of Q_1. The design value of C_s guarantees that Q_1 can exit the Miller platform. After that, the gate–source voltage of Q_1 is clamped to −0.7 V under the action of the static voltage balancing resistors and D_2. If Q_1 requires a lower negative driving voltage, it is recommended to connect several low voltage TVSs in series as D_2.

B. Open-Loop Test Under Resistive and Inductive Loads

In order to validate the effectiveness of the proposed ODCM and SCCM, the second test is an open-loop test under resistive and inductive loads. The load is a 360 Ω power wire-wound resistor, equivalent inductance of which is about 2.1 mH. The gate–source voltage of Q_2 is set to −5 V when turned OFF and 19 V when turned ON. The experimental results under different $V_{\rm bus}$ are shown in Fig. 13. Fig. 13(a)–(c) shows the experimental results under 1200, 1000, and 700 V dc-bus voltage, respectively. Dynamic and static voltage balancing are well achieved by adjusting $V_{\rm ctr}$ and switching the switched capacitor $C_{\rm cp1}$. In Fig. 13(a) and (b), the $S_{\rm cp1}$ is in the OFF state. As shown in Fig. 7, $C_{\rm cp1}$ and $C_{\rm oss}$ of $S_{\rm cp1}$ are connected in parallel and then in series with C_s to obtain a smaller drive capacitance, which is suitable for higher voltage conditions. At 1200 and 1000 V dc-bus voltage, the v_{gs_Q1} before turn-OFF is 19.5 and 17.5 V, respectively. By adjusting the overdrive depth of Q_1, the imbalanced dynamic voltage caused by the dc-bus voltage changes can be controlled. In Fig. 13(c), as the dc-bus voltage further reduced to 700 V, only adjusting the drive depth of Q_1, the dynamic voltage balancing cannot be achieved. In this case, $S_{\rm cp1}$ is turned ON to bypass the $C_{\rm cp1}$ to get a larger drive capacitance, and v_{gs_Q1} before turn-OFF is 18.2 V. Therefore, with SCCM, the dynamic voltage can be further balanced by ODCM when the dc-bus voltage fluctuates greatly.

Fig. 14 shows the $V_{\rm ctr}$ and V_{gs} of Q_1 under different $V_{\rm bus}$ when the dynamic voltage is balanced during the turn-OFF transient. It can be seen from Fig. 14 that with the rise of $V_{\rm bus}$, the increase of $V_{\rm ctr}$ makes the corresponding changes of $V_{\rm gs}$, resulting in a deeper overdrive depth of Q_1, which can offset the effect of the dc-bus voltage increase on dynamic voltage balancing at the turn-OFF transient.

The dynamic voltage balancing can be achieved from 900 to 1500 V when the $S_{\rm cp1}$ is OFF. When the $S_{\rm cp1}$ is ON, the dynamic voltage balancing can be achieved from 500 to 900 V. In both the

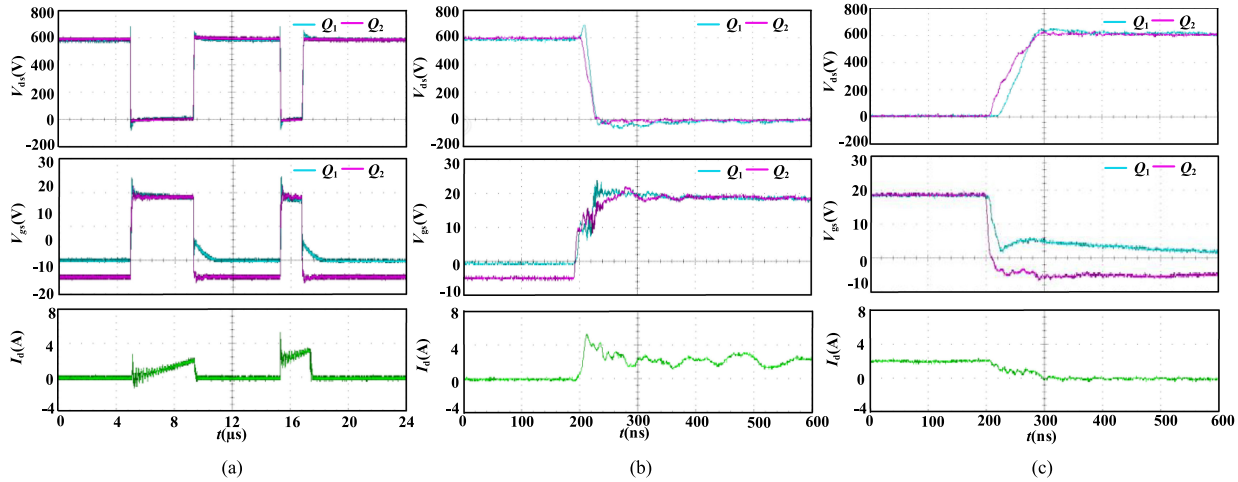

Fig. 12. Experimental result of DPT under 1200 V. (a) DPT waveforms. (b) Zoom-in view of turn-ON transient. (c) Zoom-in view of turn-OFF transient.

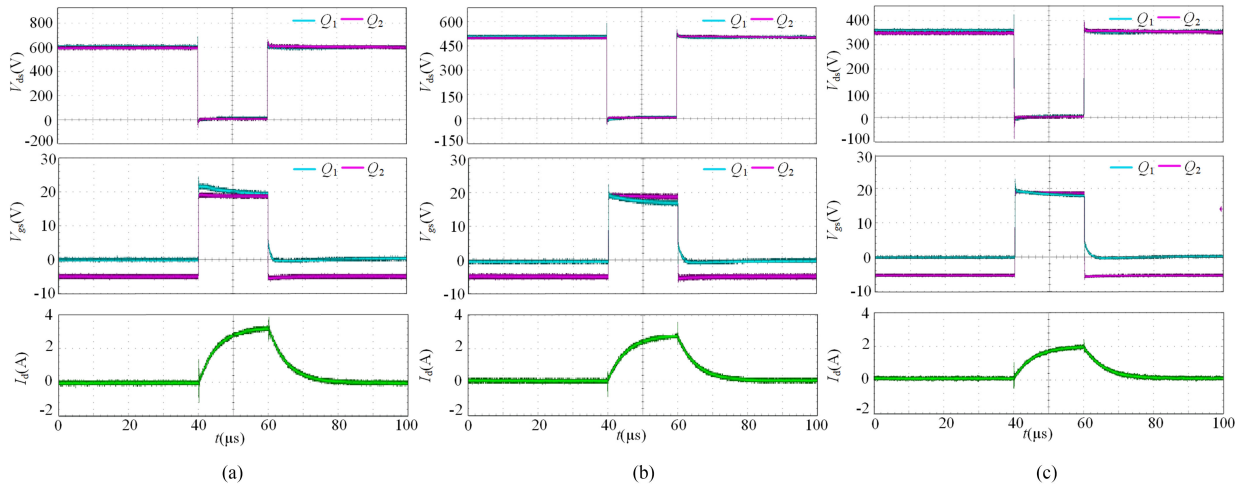

Fig. 13. Experimental results under different V_{bus}. (a) 1200 V. (b) 1000 V. (c) 700 V.

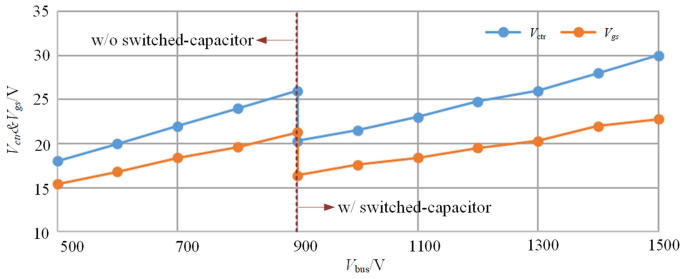

Fig. 14. V_{ctr} and V_{gs} of Q_1 under different V_{bus}.

cases, the V_{gs} of Q_1 has a certain margin. In addition, the higher the dc-bus voltage, the wider the adjustment range of ODCM.

The ODCM realizes dynamic voltage balancing between 900 and 1500 V dc-bus voltage with switched capacitor, and the control range is 600 V. While the ODCM realizes dynamic voltage balancing control between 500 and 900 V without switched capacitor, the control range is 400 V. This is because at higher voltage, a smaller drive capacitance is required, which means that the drive capacity of the drive capacitor changes slowly with the change of voltage. Therefore, ODCM has a wider control range in high-voltage applications.

C. DC-Bus Voltage Change Test

In order to validate the effectiveness of DVBCM, the third test is designed as dc-bus voltage change test. The parameters of the test circuit are same as the second test. The experimental results when dc-bus voltage changes from 600 to 1200 V are shown in Fig. 15. Fig. 15(a) shows the test results without the DVBCM. V_{ctr} is set to 20 V and S_{cp1} turns ON to balance the dynamic voltage at 600 V. Fig. 15(a) shows that as the dc-bus voltage changes, the dynamic voltage imbalance occurs. The maximum unbalanced voltage between the two SiC MOSFETs is 377 V. Fig. 15(b) shows the close-loop test when the dc-bus voltage changes from 600 to 1200 V. The switching point of S_{cp1} is set at 900 V. When the dc-bus voltage is larger than 900 V, S_{cp1} turns OFF and connects C_{cp1} into the gate drive circuit. Fig. 15(c) and (d) shows the zoom-in views during and after the dc-bus voltage change, respectively. In both the cases, the dynamic and static voltages are well balanced. Thus, the DVBCM achieves the dynamic voltage balancing when the

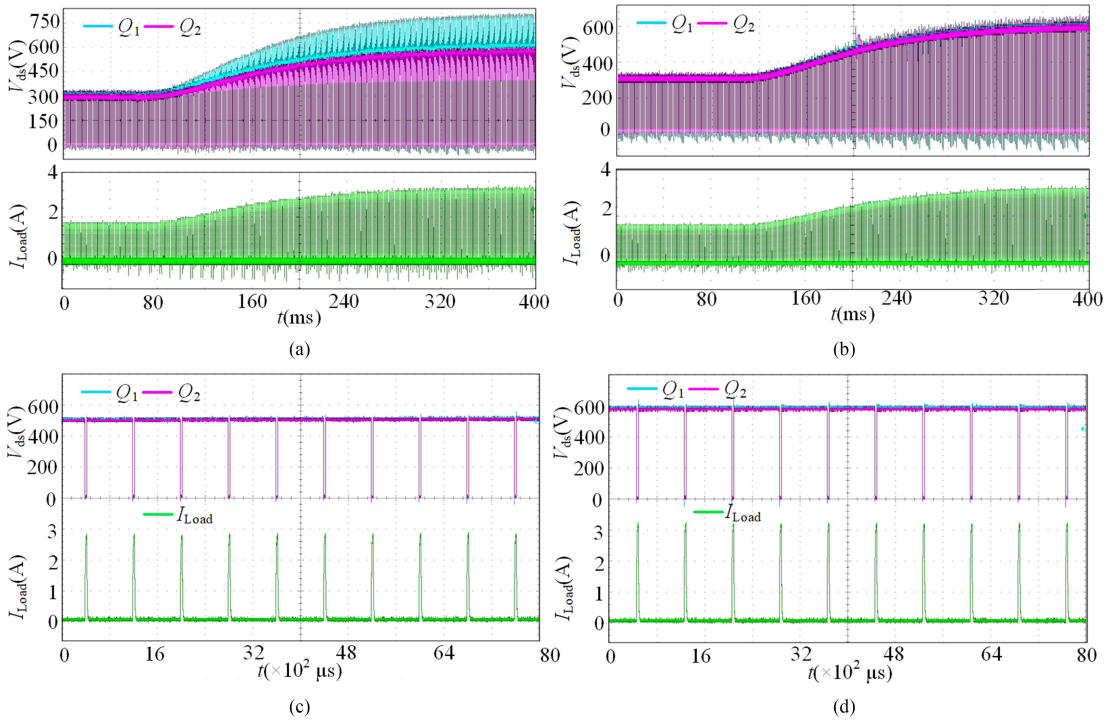

Fig. 15. Experimental results when the dc-bus voltage changes from 600 to 1200 V. (a) Without dynamic voltage balancing method. (b) With dynamic voltage balancing method. (c) Zoom-in view during the dc-bus voltage changes. (d) Zoom-in view after the dc-bus voltage changes.

dc-bus voltage changes. The critical target of the DVBCM is achieved.

VI. Conclusion

This article presents a simple and effective gate drive circuit to realize dynamic voltage balancing during the fast switching transient of series-connected SiC MOSFETs. The DVBCM is proposed to balance the dynamic voltage when the dc-bus voltage changes and this method is more suitable for high-voltage applications. In this method, the ODCM makes full use of the overdrive feature to achieve the dynamic voltage balancing. The SCCM based on ODCM is proposed to widen the control range and it is available for selection according to the applications. The experimental results validated the analysis and showed the availability of the proposed series-connected gate drive circuit for SiC MOSFETs and DVBCM.

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