10-kV SiC MOSFET Power Module With Reduced Common-Mode Noise and Electric Field

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***Abstract*—The advancement of silicon carbide (SiC) power devices with voltage ratings exceeding 10 kV is expected to revolutionize medium- and high-voltage systems. However, present power module packages are limiting the performance of these unique switches. The objective of this research is to push the boundaries of high-density, high-speed, 10-kV power module packaging. The proposed package addresses the well-known electromagnetic and thermal challenges, as well as the prominent electrostatic and electromagnetic interference (EMI) issues associated with high-speed, 10-kV devices. The high-speed switching and high voltage rating of these devices causes significant EMI and high electric fields. Existing power module packages are unable to address these challenges, resulting in detrimental EMI and partial discharge that limit the converter operation. This article presents the design and testing of a 10-kV SiC MOSFET power module that switches at a record 250 V/ns without compromising the signal and ground integrity due to an integrated screen reduces the common-mode current by ten times. This screen connection simultaneously increases the partial discharge inception voltage by more than 50%. With the integrated cooling system, the power module prototype achieves a power density of 4 W/mm^3.**

***Index Terms*—Electromagnetic interference, partial discharges, semiconductor device packaging, wide band gap semiconductors.**

I. Introduction

WIDE-BANDGAP (WBG) semiconductors, such as silicon carbide (SiC), have demonstrated improved efficiency, reduced size and weight, and lower system cost compared to silicon [1]–[5]. SiC semiconductors have also demonstrated superior high-voltage capability [3]–[6]. While silicon devices have proven reliability and ruggedness, they have limited voltage ratings (typically 6.5 kV or less), thus requiring complex series connection of devices or multilevel converter topologies [7]. Moreover, medium-voltage silicon devices have slow switching speeds, which constrain the efficiency and switching frequency of the power converter [8], [9].

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10-kV SiC MOSFETs are of great interest due to their high blocking voltage, fast switching speed, simple drivability, reverse conduction capability, and moderate ON-state losses. These features can increase the efficiency, reliability, and switching frequency, and reduce the complexity, size, and weight of medium- and high-voltage power conversion systems [10], [11]. Applications include electric ships [12], traction [9], [13], data center distribution, direct renewables integration [14], fast charging stations [15], HVdc [16] and FACTS [17], [18], and transformer-less intelligent power substations [11], [14], [19]–[21].

Due to the vast possibilities for $\geq$10-kV SiC devices, many resources have been devoted to their development. To date, the majority of the reports on these devices have been focused on the characterization [6], [11], [19], [22], [23], gate driver design [24]–[27], and converter evaluation [11], [23], [28]. However, the packaging of the semiconductor dies has a significant impact on the performance, and is currently hindering their switching speed, voltage rating, current rating, and operating temperature. It is nontrivial to design a suitable package for 10-kV SiC MOSFETs. In addition to the well-known electromagnetic and thermal challenges associated with packaging WBG devices, the high voltage rating creates impeding electrostatic and electromagnetic interference (EMI) issues, which must be addressed to utilize the full capabilities of these devices.

The first-generation 10-kV SiC MOSFETs were assembled into a power module using a modified 6.5-kV silicon nsulated gate bipolar transistor (IGBT) package [29]. Upon analysis and testing of the power module, it was found that the parasitic inductances and capacitances were large and unbalanced [30], limiting the dynamic performance and causing significant EMI. An improved package for third-generation 10-kV SiC MOSFETs was presented in [31]. This package has lower and more symmetrical parasitic inductances [31], though the improvement in the EMI is unknown.

EMI arises from the voltage and current transitions occurring during operation of the switching cell, and can be conducted through the electrical connections, or radiated into the surrounding space. Typically, filters are added to reduce the EMI; however, these increase the cost, size, and complexity of the power conversion system. Adding large external filters diminishes the power density and simplicity benefits gained by using 10-kV SiC MOSFETs.

In particular, conducted common-mode (CM) noise is a major issue with high-speed devices. CM noise is caused by the high-*dv/dt* switching of the semiconductor devices, which

causes current to flow through the parasitic capacitances. These capacitances exist in the power module and auxiliary circuitry, such as the gate driver isolation. The latter has been addressed in other works by reducing the isolation capacitance of the gate driver power supply [24]–[27].

To address the issue of current flowing through the parasitic capacitances within the package, [32] proposed a method for diverting the current back to the dc bus by using two stacked direct-bonded-copper (DBC) substrates, where the intermediate metal layer is connected to the positive or negative dc bus. The amount of current that is diverted will depend on the high-frequency impedance of the connection back to the dc bus. Accordingly, the implementation of this screen is critical. In [32], wire bonds are used for the interconnections, and lugs are used for the terminals. These connection methods may have large parasitic inductances, which could reduce the effectiveness of the screen.

In [33], a similar screen is proposed. The 1.2-kV SiC MOSFET power module in [33] uses a multilayer DBC substrate, and dc-link capacitors located close to the dies. Vias in the multilayer substrate create a low-inductance connection between the middle metal layer and the negative dc bus [33]. The module has a 14 dB reduction compared to the reference module [33], [34]. While this module has several advantageous features, there are some areas for improvement. First, by connecting the middle metal to the negative dc bus, as in [32], the top ceramic is providing all the voltage isolation, and thus the second ceramic is not being fully utilized. Second, by placing the capacitors on the same plane as the MOSFETs, the footprint of the module is increased. Third, the module parasitics are not well balanced, which has been shown to cause greater high-frequency noise compared to balanced designs [35].

The high-voltage rating of the 10-kV SiC MOSFETs poses a challenge for the electrostatic performance. If the electric field exceeds the breakdown field strength of the insulation materials, such as the encapsulation or insulating substrate, then partial discharge (PD) can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate, as shown in [36], which could cause a short circuit between the dc bus and ground. Furthermore, the PD inception voltage (PDIV) has been shown to decrease with increased *dv/dt* and switching frequency [37]. Due to the high-speed switching capabilities of these 10-kV SiC MOSFETs, measures must be taken to reduce the electric field concentration within the power module to ensure sufficient PDIV and breakdown voltage.

In this work, a high-voltage power module package was designed, prototyped, and tested using 10-kV SiC MOSFETs. With the proposed package, the 10-kV SiC MOSFETs are able to switch at record speeds with minimal ringing and voltage overshoot. This fast switching results in significantly reduced switching losses compared to medium-voltage silicon transistors, and allows the switching frequency of medium- and high-voltage converters to be increased by orders of magnitude, which drastically reduces the size of passive components, thereby increasing the system power density. To mitigate the conducted EMI that could result from this high *dv/dt*, this work proposes to fully integrate a low-inductance screen into the package that limits the amount of CM current that flows out of the power module. In this implementation, the screen layer is connected to the dc bus midpoint, which evenly distributes the electric field in the ceramic substrates and reduces the peak electric field at the critical triple points. The dc bus midpoint connection is made through embedded series capacitors that are arranged above each MOSFET switch pair. Thus, the proposed implementation will mitigate the CM current, while also improving the voltage isolation, increasing the PDIV of the power module, and maintaining a small footprint for high power density.

In this article, the EMI issues encountered during testing of the first-generation 10-kV SiC power modules from [29] will be presented, followed by a description of the proposed power module for 10-kV SiC MOSFETs. The analysis, implementation, and preliminary testing of the integrated CM screen will then be discussed. Methods for reducing the electric field concentration within the power module will be reviewed, and the proposed technique will be analyzed. Finally, the experimental switching tests that demonstrate the high-speed transients and low CM current of the proposed package will be presented. Partial discharge tests validating the improved voltage capability provided by the CM screen will also be shown.

II. EMI Limitations for High-Voltage SiC Power Modules

The development of 10-kV SiC MOSFETs [38] and 10-kV SiC junction barrier Schottky (JBS) diodes [40] gave rise to the first 10-kV SiC power module [29]. The half-bridge modules comprise 12 parallel 10-kV, 10-A SiC DMOSFETs, and six parallel 10-kV, 10-A SiC JBS diodes, per switch position, yielding a current rating of 120 A [29]. These 10-kV SiC modules demonstrated higher efficiency and switching frequency potential than 6.5-kV silicon IGBT modules [8], and were critical components in the development of a high-density 1 MVA solid-state power substation, which employed soft switching techniques and was capable of switching up to 20 kHz [40]. These modules were also used to demonstrate the first medium-voltage impedance measurement unit capable of characterizing in-situ source and load impedances of dc and ac networks up to 4160 V ac, 6000 V dc, 300 A, and 2.2 MVA [41]. Unfortunately, the full voltage and power levels could not be achieved due to significant, unresolvable EMI. Upon further evaluation, it was found that substantial current was flowing through the system ground. The contaminated ground was causing the controller to malfunction, thereby limiting the operating conditions.

During voltage transients, parasitic capacitances can become a path for CM current to flow. Within the power module, parasitic capacitances exist across the ceramic substrate that isolates the semiconductor devices from the cooling system. Since the cooling system is generally grounded for safety, under high-speed voltage transients, this parasitic capacitance becomes a path for CM current to flow through the system ground [35]. Therefore, this capacitance should be minimized, especially for fast-switching devices.

From ANSYS Q3D simulations, the parasitic capacitance between the output node of the half-bridge and the module baseplate is approximately 300 pF. Discrete switching tests were conducted on these power modules to characterize the dynamic

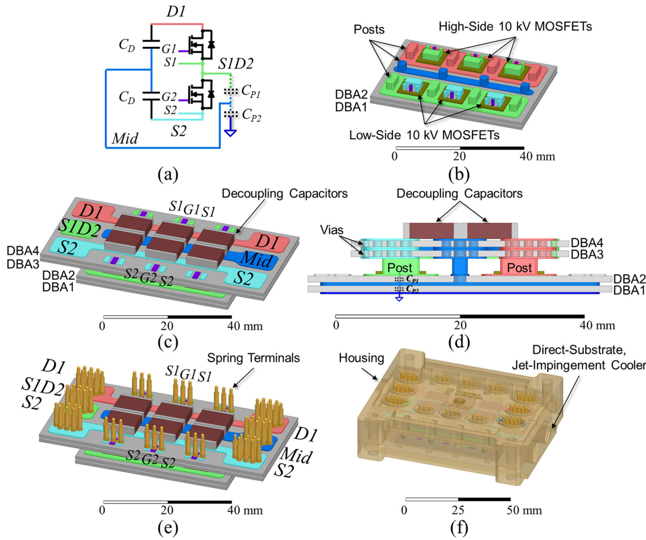


Fig. 1. (a) Schematic and 3-D models of the (b) bottom and (c) complete assemblies, (d) side-view of the module, (e) terminal arrangement, and (f) housing with integrated cooler. The colors in the 3-D models correspond to the nodes in the schematic with the same color.

performance [42]. At 4.7 kV and 100 A, the power modules had a maximum *dv/dt* of 22 V/ns [42]. This measured *dv/dt* and simulated parasitic capacitance give a calculated peak current of nearly 7 A. It should be noted that the 22 V/ns switching speed was achieved with internal and external gate resistances slowing down the devices. If these resistances were reduced or eliminated, then the switching speed would increase, which would raise the efficiency, but worsen the CM current. Therefore, this capacitance is limiting the operation of the 10-kV SiC MOSFETs. The package proposed in this work reduces this EMI without sacrificing the efficiency by minimizing the parasitic capacitance, and integrating a screen that contains the generated CM current within the power module.

III. Module Overview

Fig. 1 shows the designed half-bridge power module, which has three 10 kV, 350-mΩ SiC MOSFET dies in parallel per switch position. No external anti-parallel diodes are used. The module has a planar, sandwich structure, using metal posts and direct-bonded-aluminum (DBA) substrates as the die interconnection instead of wire bonds. Similar structures were proposed in [43] and [44] for lower voltage silicon IGBTs. This type of structure allows for increased power density, and reduces the parasitic inductances and capacitances in the module, thereby improving the dynamic performance. Furthermore, by eliminating the wire bonds, the module will be able to withstand higher energy faults, as shown in [45]. This structure also allows decoupling capacitors to be embedded within the module to further improve the dynamic performance without increasing the module footprint.

In total, four substrates are used in the power module: two beneath the dies (DBA1 and DBA2) and two on top (DBA3 and DBA4). DBA1 and DBA2 are used to reduce the CM current flowing through the system ground and to decrease the peak electric field strength within the power module. With the housing and integrated cooler, the module dimensions are 70 mm × 80 mm × 20 mm. Details on the design and prototyping of this power module are reported in [46]–[47].

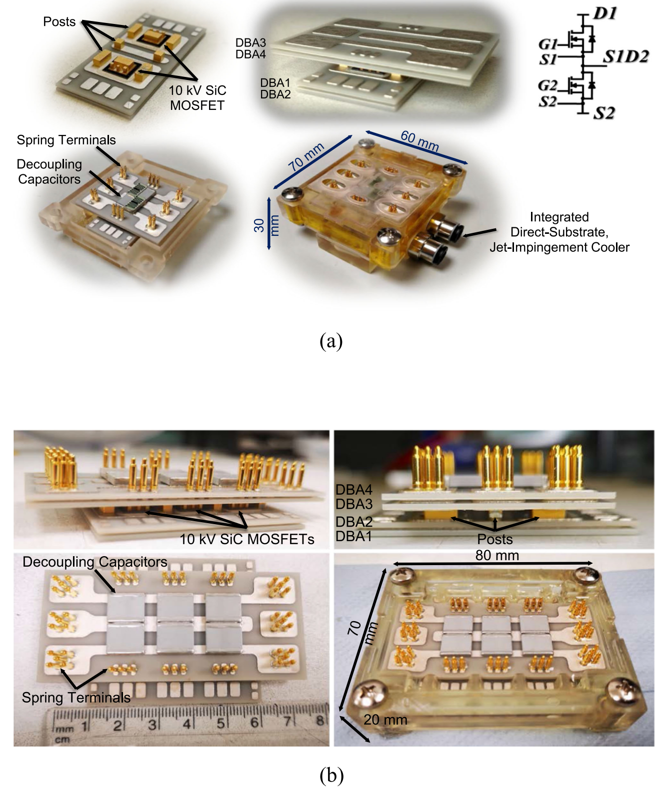


Fig. 2. 10-kV SiC MOSFET module prototypes with (a) two 10-kV SiC MOSFET dies, and (b) six 10-kV SiC MOSFET dies.

Fig. 2 shows two module prototypes: a low-current module with two dies [see Fig. 2(a)], and a high-current module with six dies [see Fig. 2(b)]. The low-current module was fabricated to test the prototyping procedures, and was used for initial testing. The testing of these module prototypes will be presented in Section VI.

IV. Common-Mode Screen

A. Impedance Analysis

In this section, the CM path impedances will be analyzed. Fig. 3 shows a schematic of the power module with the key impedances that will be considered. For the generated CM current to be diverted from the ground to the screen, the impedance of the screen path must be much lower than that of the ground path, especially at high frequency. The condition required for the screen to effectively divert the CM current from the ground path to the dc bus may be summarized as follows:

$$Z_{\text{screen}} \ll Z_{\text{gnd}} \tag{1}$$

where Z_{screen} and Z_{gnd} are the impedances of the screen and ground paths, respectively. Considering the parasitic elements shown in Fig. 3, these impedances can be defined as follows:

$$Z_{\text{screen}} = \omega L_{\text{screen}} + 1/(j\omega C_D) + R_{\text{screen}} \tag{2}$$

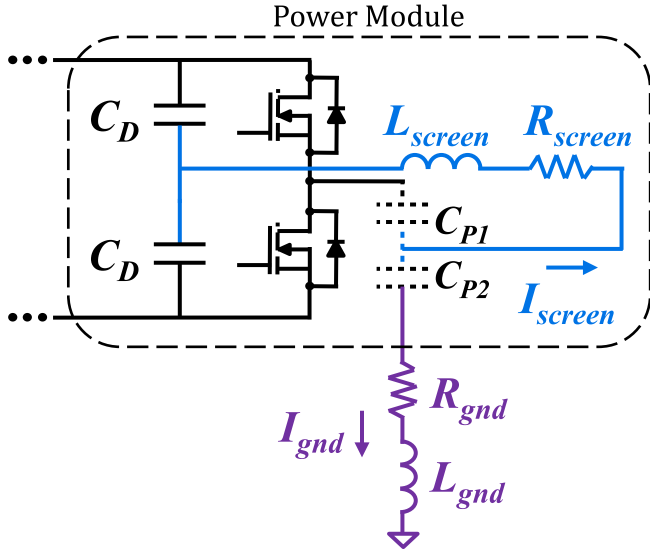


Fig. 3. Power module schematic with parasitic impedances of the ground (purple) and screen (blue) paths.

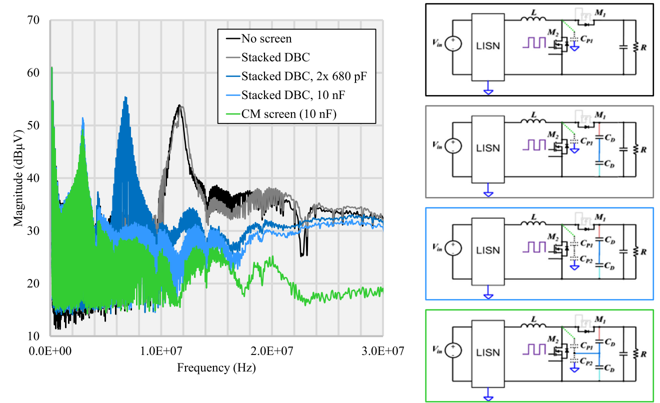


Fig. 4. Measured LISN current in 1.2-kV SiC-based boost converter with (green waveform) and without (black, grey, and blue waveforms) the proposed CM screen.

$$Z_{\text{gnd}} = \omega L_{\text{gnd}} + 1/(j\omega C_{P2}) + R_{\text{gnd}} \tag{3}$$

where L_{screen} and L_{gnd} are the parasitic inductances in the screen and ground paths, respectively. R_{screen} and R_{gnd} are the parasitic resistances in the screen and ground paths, respectively. C_D is the decoupling capacitance and C_{P2} is the parasitic capacitance of the bottom substrate, which is connected to ground [see Fig. 1(d)]. As shown by (2), to minimize Z_{screen}, L_{screen} should be as small as possible, while C_D should be large. From (3), it can be seen that a smaller C_{P2} results in a greater Z_{gnd}. Substituting (2) and (3) into (1) gives the following:

$$\omega L_{\text{screen}} + 1/(j\omega C_D) + R_{\text{screen}} \ll \omega L_{\text{gnd}} + 1/(j\omega C_{P2}) + R_{\text{gnd}}. \tag{4}$$

From (4), it can be seen that the effectiveness of the screen is dependent on the parasitic elements, which are determined by the implementation. To effectively reduce the CM current, the power module should be compact such that C_{P2} and L_{screen} are small, yet capable of accommodating sufficient decoupling capacitance C_D. The L_{gnd} and R_{gnd} will vary depending on the system integration, and are therefore out of the control of the power module designer. Accordingly, this work focuses on minimizing C_{P2} and L_{screen}, and maximizing C_D. A more general theoretical analysis of CM impedances is presented in [49].

B. Preliminary Testing

Prior to constructing the 10-kV SiC MOSFET power modules, it was desirable to understand the effects of the proposed screen on the CM noise. Accordingly, a half-bridge module with 1.2-kV, 80-mΩ SiC MOSFETs (C2M0080120D) was built and tested in a boost converter. For the test, the module substrate was directly mounted onto a copper ground plane. No cooling system was added between the substrate and the ground plane to improve the measurement results. Due to the absence of a cooling system, the tests were conducted at low power (360 W). The output voltage was 60 V, and the switching frequency was 50 kHz.

For the prototyped 1.2-kV SiC modules, the parasitic capacitance from the output node to the middle metal layer, C_{P1}, was 20 pF, and the parasitic capacitance from the middle metal layer to the ground, C_{P2}, was 150 pF. These values were measured on the prototype using an impedance analyzer, and were verified by calculation and Q3D simulation. C_{P2} is larger than C_{P1} because the middle and bottom metal layers cover the entire substrate area, whereas the output terminal makes up a small portion of the footprint.

For the tests, a high-frequency current transformer (HFCT) was used to measure the current of the line impedance stabilization network (LISN). The output of the HFCT was connected to an EMC analyzer. The measured current for five cases is shown in Fig. 4. The first case has a single substrate and no decoupling capacitors. The second case has two stacked substrates and no decoupling capacitors. The third case has two stacked substrates and two 680-pF decoupling capacitors in parallel and two in series, but the middle metal layer of the substrate stack is left floating. The fourth case is similar to the third, but has two series 10 nF capacitors. The fifth case connects the middle metal layer of the substrate stack to the midpoint of the series decoupling capacitors.

When two substrates are stacked together (case 2), the noise decreases by just a few decibels compared to case 1 with a single substrate. This indicates that the reduction in the parasitic capacitance offered by the second substrate is not sufficient to lower the CM noise. The addition of 680-pF decoupling capacitors in case 3, on the other hand, reduces the high-frequency noise by more than 10 dB compared to case 1 with a single substrate. The decoupling capacitors also cause the resonant frequency to decrease. When the decoupling capacitance is increased to 10 nF (case 4), then the resonant frequency further decreases, and the high-frequency noise is reduced by a few more decibels. This is in agreement with (2), which shows that increasing the decoupling capacitance reduces the high-frequency impedance of the screen path. When the middle metal of the substrate stack is connected to the midpoint of the two series 10-nF capacitors (case 5), then the high-frequency noise decreases by more than

15 dB over a larger frequency range. This is because there is now a low-impedance, high-frequency path for the generated CM current to flow. This preliminary testing demonstrates the potential of the screen to reduce the CM noise.

The gate–source and drain–source voltages and drain current of the 1.2-kV SiC MOSFET were also monitored during the testing. By adding decoupling capacitors, the ringing frequency in the drain–source voltage reduced, and the *di/dt* increased, resulting in greater current overshoot and higher-amplitude ringing. This ringing and overshoot can be reduced by decreasing the power-loop inductance, which was not optimized in this module prototype. Connecting the middle metal layer to the decoupling capacitor midpoint did not cause noticeable changes in the MOSFET voltage and current waveforms. Therefore, if the parasitic inductances and decoupling capacitors are carefully designed, the proposed CM screen will have minimal impact on the MOSFET losses.

C. Implementation

To achieve a low-impedance implementation for the CM screen in the 10-kV power module, it is proposed to embed capacitors, and to use vias within the insulating ceramic substrates to make the connection between the middle metal layer and the capacitor potentials. In [49], the capacitors are placed above the semiconductor devices, creating a vertical high-frequency power loop that does not increase the module footprint, as it takes advantage of the third dimension. In this work, this vertical-capacitor-loop concept was adopted with some modifications. Each 10-kV SiC MOSFET switch pair has its own set of decoupling capacitors located above it [see Fig. 1(c)], resulting in a symmetric power loop inductance of just 4.4 nH for each. In this embodiment, two capacitors are placed in series, and the midpoint, which is at half of the dc bus voltage, is connected to the middle metal of the substrate stack. By connecting the screen to the decoupling capacitors within the power module, the influence of the parasitic impedances external to the package are diminished thereby improving the effectiveness of the screen.

According to ANSYS Q3D simulations, this connection method has less than 2 nH parasitic inductance, allowing for a high proportion of the CM current to be diverted to the dc bus and contained within the power module. Additionally, the S1D2 pad area was designed as small as possible to minimize C_{P1}. For the proposed high-current 10-kV power module shown in Figs. 1 and 2(b), C_{P1} is 46 pF, and C_{P2} is 160 pF, according to ANSYS Q3D simulations. For the decoupling capacitors (C_D), a surface-mount 680-pF C0G 5-kV multilayer ceramic capacitor was selected. As shown in Fig. 1(c), there are three capacitors in parallel—one above each MOSFET switch pair—giving an equivalent capacitance of 2.04 nF.

V. Electric Field Reduction

To address the enhanced electric field associated with a high-voltage, high-density package, the ceramic substrate must be thoughtfully designed and evaluated. In power modules, the electric field concentrates at the intersection of the ceramic, metal, and encapsulation [51]–[54]. This is known as the triple point. If this electric field exceeds the breakdown field strength of the insulation materials, such as the ceramic or encapsulation, then PD can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate as shown in [36], thus destroying the power module.

In the literature, it has been shown that the PDIV for standard 1-mm thick aluminum nitride (AlN) DBC substrates is less than 10-kV rms [36], and can be as low as 5-kV rms [55]. This does not provide sufficient margin for 10-kV SiC MOSFETs. Accordingly, methods for reducing the peak electric field within the power module need to be explored. There have been several proposed solutions to reduce the electric field strength at the triple point, including increasing the ceramic thickness [36]; varying the metal pad size [36], pad corner curvature [36], offset between the top and bottom pads [36], and metal-ceramic interface geometry [56]–[58]; and stacking multiple substrates [55]. None of these previously proposed solutions were implemented and tested in an actual power module, and several of them may complicate the module manufacturing. The method proposed in this work, is an adaptation of the latter method. It effectively increases the PDIV, and is simple to implement.

In [55], it was shown that stacking DBC substrates reduces the electric field strength within the bulk ceramic and at the critical triple points. The PD tests revealed that the PDIV could be increased by 94% by stacking two 0.32-mm Al_2O_3 substrates compared to having a single 0.63-mm substrate [55]. However, the practical implementation of this method was not explored. In a power module, the top and bottom metal layers are not symmetrical; the top metal is patterned to create the circuit (e.g., half bridge), and the various traces are at different potentials during the module operation. As a result, it is not clear what potential should be applied to the middle metal layer to achieve a meaningful reduction in the electric field strength. This key factor in the realization of this method is explored in this work.

Fig. 5 shows the simulated two-dimensional electric field distribution for the case when the top metal is patterned and has two different potentials. One of the potentials represents the drain of the high-side switch, and the other represents the drain of the low-side switch. The former is consistently at the positive dc bus potential while the latter switches between the positive and negative dc bus potentials. The worst-case scenario is when the low-side switch is conducting and its drain is at the negative dc bus potential. This worst-case was simulated. The positive dc bus is set to 10 kV, and the negative is set to 0 V. The bottom-most metal is at the same potential as the cooling system, which is grounded (0 V).

Fig. 5(a) shows the simulated electric field plot for a single DBA substrate. It can be seen that the electric field distribution is non-uniform within the bulk of the ceramic, and that the peak electric field occurs at the triple points. The peak electric field exceeds 20 kV/mm, which is the typical breakdown field strength for ceramic substrates.

Fig. 5(b) shows the simulated electric field plot for two stacked DBA substrates with the middle metal layer connected to the negative dc bus (0 V), as proposed in [32] and [33] Comparing Fig. 5(a) and (b), it can be seen that connecting the middle metal to the negative dc bus does not reduce the peak electric field

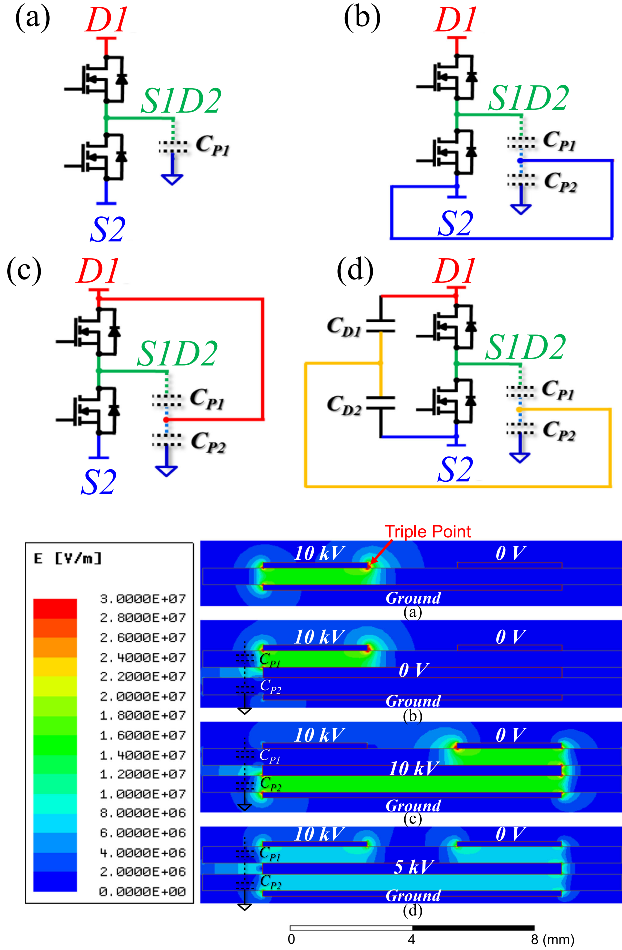
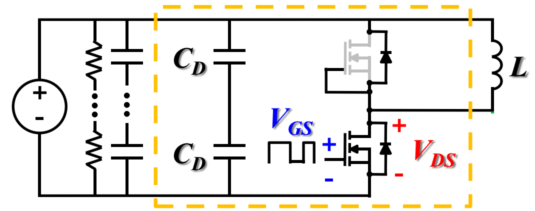
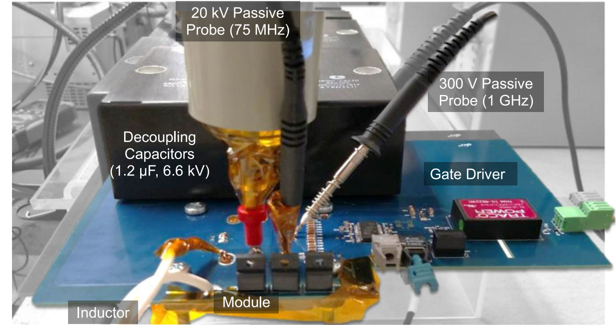


Fig. 5. Simulated 2-D electric field distribution for (a) a single substrate, and two stacked substrates with the middle metal at the (b) negative dc bus, (c) positive dc bus, and (d) dc bus midpoint.



(a)

(b)



(c)

Fig. 6. Double-pulse test (a) schematic with the power module indicated by the yellow box, (b) hardware setup, and (c) module connection.

at the triple point, nor does it improve the distribution within the bulk ceramic, compared to the single substrate case. This is because the bottom substrate has 0 V across it, while the top substrate has 10 kV. In this implementation, the bottom substrate is not helping to support the voltage, and is therefore not being fully utilized.

If the middle metal is connected to the positive dc bus, as proposed in [32], then the triple points at which the peak electric field occur will change, and the electric field distribution within the bulk ceramic will shift. This is shown in Fig. 5(c). Although the distribution and critical triple points have changed, the peak electric field, and therefore the PDIV, are similar to the case with a single substrate. This is because both the top and bottom substrates have 10 kV across them.

If instead the middle metal is connected to half of the applied voltage, then both the top and bottom substrates have a potential of 5 kV across them. The simulated electric field distribution for this case is shown in Fig. 5(d). The simulated peak electric field is reduced by 58% compared to the single-substrate case [see Fig. 5(a)], and the electric field in the bulk ceramic is uniformly distributed in the two substrates. Therefore, in this work, the middle metal layer of the DBA stack is connected to half of the bus voltage.

The connection of the middle metal layer to half of the bus potential can be realized with the embedded decoupling capacitors. Each set of decoupling capacitors shown in Fig. 1(c) consists of two, 5-kV ceramic capacitors placed in series. From Fig. 1(d), it can be seen that the midpoint of the capacitors is connected to the middle metal layer of the bottom DBA stack through vias and metal posts. This connection allows the middle metal layer to be connected to half of the bus voltage, thus reducing the peak electric field in the power module.

VI. Experimental Results

A. Switching Testing

To evaluate the switching performance of the proposed 10-kV power module, double-pulse tests (DPT) were performed on the low-current prototype shown in Fig. 2(a). The DPT schematic and setup are shown in Fig. 6. The gate driver used for the DPTs was adapted from the one presented in [59]. The low-side

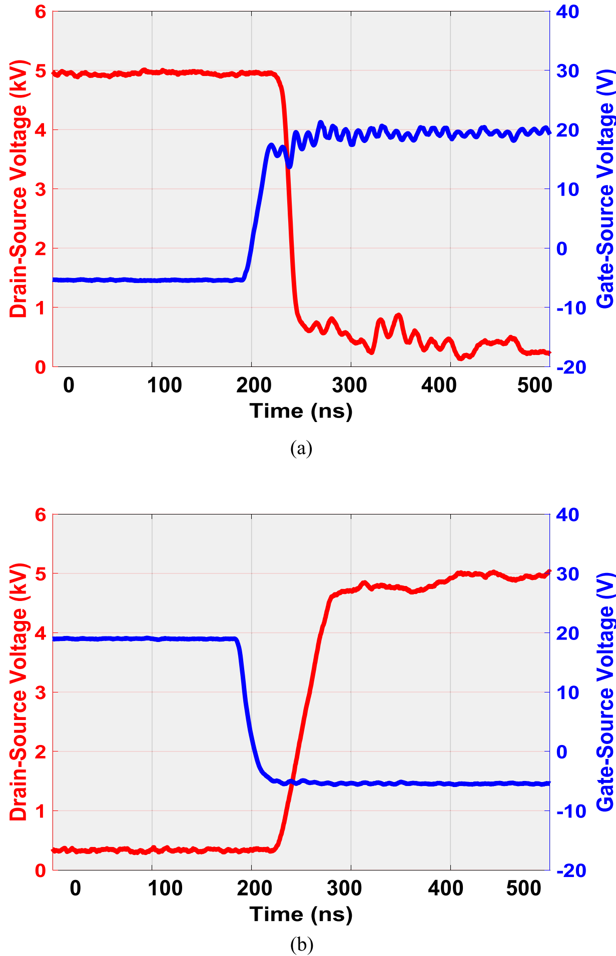


Fig. 7. (a) Turn-ON and (b) turn-OFF gate-source (blue, right axis) and drain–source (red, left axis) voltages.

10-kV SiC MOSFET was driven from +20 V in the ON-state to −5 V in the OFF-state. The body diode of the high-side 10-kV SiC MOSFET was used as the free-wheeling diode. The gate driver PCB is mounted on top of the power module to achieve small gate-loop inductance between the driver and the module.

The gate–source and drain–source voltages of the low-side SiC MOSFET were monitored using a 300-V passive probe with a bandwidth of 1 GHz, and a 20-kV passive probe with a bandwidth of 75 MHz, respectively. As shown in Fig. 6(c), these probes are placed directly above the MOSFET terminals to minimize the parasitic inductance in the measurement loop. Due to the embedded decoupling capacitors, the drain current of the SiC MOSFETS could not be measured. A 15-kV power supply was used to charge the external decoupling capacitors. Each capacitor is 0.82 μF and rated at 3.3 kV (MP80CV824K [60]). Six total capacitors were used—two in series and three in parallel for a total capacitance of 1.2 μF and voltage rating of 6.6 kV. Three capacitors were put in parallel to increase the capacitance and to reduce the inductance; each capacitor has an equivalent series inductance of 30 nH [60].

Fig. 7 shows the gate–source and drain–source voltage waveforms for the turn-ON and turn-OFF transients for the DPTs performed on the module shown in Fig. 2(a). The switching tests were performed up to 5 kV and 20 A with turn-ON and turn-OFF gate resistances of 0.33 and 0.17 Ω, respectively. Table I lists the measured overshoot, undershoot, rise and fall times, and switching rates from the DPTs. During the turn-ON transient, the fall time of the drain–source voltage is 16 ns, giving a *dv/dt* of 250 V/ns. At turn-OFF, the voltage rise time is 50 ns, which is a *dv/dt* of 80 V/ns. The voltage rise time is longer because it is controlled by the output capacitance and load current. Negligible voltage overshoot and ringing were measured, indicating low power- and gate-loop inductances. This is due to the low-inductance module design, as well as careful layout and connection of the gate driver, bus bar, external decoupling capacitors, and measurement probes.

TABLE I
10 kV, 350-mΩ SiC mosfet MODULE PROTOTYPE SWITCHING RESULTS

Parameter	Value	
	Gate-Source Voltage	Drain-Source Voltage
Overshoot	None	None
Undershoot	None	None
Rise Time	24 ns	50 ns
Rise *dv/dt*	0.9 V/ns	80 V/ns
Fall Time	26 ns	16 ns
Fall *dv/dt*	0.8 V/ns	250 V/ns

To the author’s knowledge, these are the fastest switching speeds reported for similarly rated SiC MOSFETs and IGBTs. In fact, this is more than two times faster than those reported in [23], [31], [61], and [62]. In [31], switching results for a module populated with a single die had turn-ON and turn-OFF transition times of approximately 80 and 120 ns, respectively, giving switching speeds of 88 and 58 V/ns at a bus voltage of 7 kV, drain current of 15 A, and gate resistance of 21 Ω. The switching waveforms also showed a moderate voltage overshoot of approximately 300 V (4.3%) [31].

For a discrete 4-kV silicon IGBT, the datasheet reports voltage rise and fall times of 146 and 514 ns at 1.25 kV, 30 A, and 2 Ω external gate resistance [63]. These switching times result in *dv/dt* values of 8.6 and 2.4 V/ns for the rise and fall, respectively, which are 10 and 100 times slower than the switching speeds achieved in this work. Accordingly, the proposed power module can enable faster switching, higher voltage power converters while maintaining high efficiency.

B. Common-Mode Screen Testing

To evaluate the effectiveness of the integrated CM current screen on the 10-kV power module, switching tests were performed. As mentioned earlier, the CM current increases as the *dv/dt* and parasitic capacitances increase. To improve the signal-to-noise ratio of the CM current measurement, the *dv/dt* was reduced. This was achieved by lowering the dc bus voltage to 2 kV. To ensure sufficient CM current could be measured, the larger power module with three 10-kV SiC MOSFET dies in parallel per switch position was used [see Fig. 2(b)] [64]. The C_{P1} and C_{P2} of this 10-kV prototype are 47 and 162 pF, respectively.

Fig. 8(a) shows the schematic of the tests when the CM screen is not connected (the middle metal layer of the bottom substrate

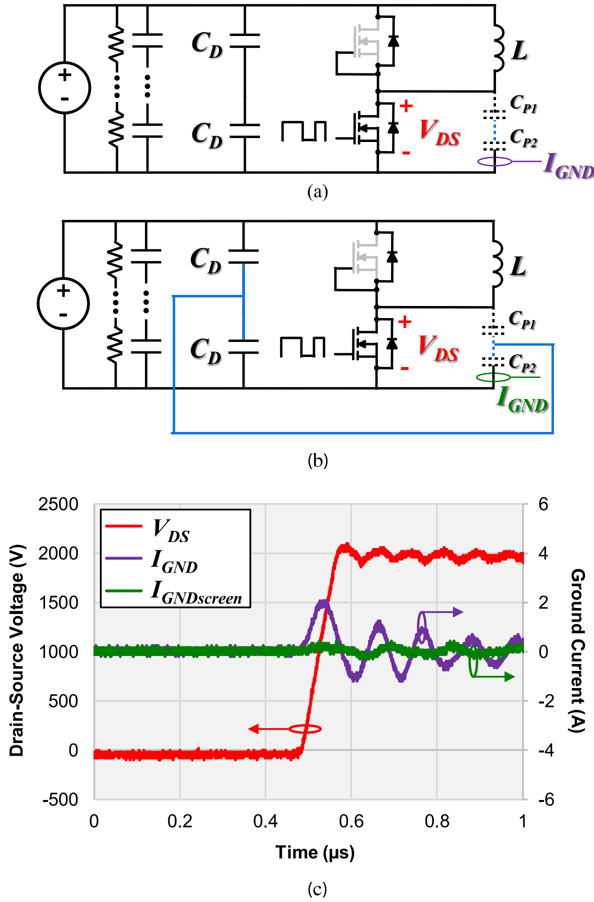


Fig. 8. Schematic of the testing setup when the screen is (a) not connected and (b) connected, and (c) drain–source (red, left axis) and ground current (right axis) waveforms with (green) and without (purple) the common-mode screen.

stack is floating). Fig. 8(b) shows the schematic of the tests when the CM screen is connected to the capacitor midpoint. An inductor with high-voltage wire for the winding was connected across the high-side switch of the half-bridge module. The body diode of the high-side SiC MOSFET was used to freewheel the current in the inductor when the low-side switch was OFF.

To validate the performance of the CM screen, the current through the ground path, I_{gnd}, was measured, as shown in Fig. 8, using an RF current transformer with a bandwidth of 200 MHz. For these tests, the middle metal layer was connected to the midpoint of the two series 680-pF decoupling capacitors. Three capacitors were placed in parallel.

Fig. 8(c) shows the turn-OFF drain–source voltage and ground current waveforms with and without the screen at 2 kV and 20 A with no external gate resistance. The voltage rise time at turn OFF is 66 ns, which gives a *dv/dt* of 24 V/ns. This *dv/dt* is lower than the previous switching tests because of the lower bus voltage and larger device capacitance due to the three MOSFET dies in parallel. The measured peak current through the ground path without the proposed screen is 2 A. This peak current will increase as the dc bus voltage, and therefore the *dv/dt*, increases. With the CM screen connected, the measured peak current through the ground path is reduced to 0.2 A. This is an order of magnitude reduction.

TABLE II
PARTIAL DISCHARGE TESTING SUMMARY

Sample	Voltage of Middle Metal	Surrounding Medium	S1D2 Potential	PDIV (rms)
Single Substrate	N/A	Air	D1	1.7 kV
Stacked Substrates	N/A	Air	S2	1.7 kV
	½ × V_{AC}	Air	D1	2.6 kV
	½ × V_{AC}	Air	S2	2.6 kV
Encapsulated Stacked Substrates	0 V	SilGel 612	S2	7.4 kV
	½ × V_{AC}	SilGel612	S2	>10.5 kV

C. Partial Discharge Testing

PD tests were conducted to validate the electrostatic simulation results. The PD tests were performed using a 50 kV, 100 mA, 60 Hz power supply as the excitation source. To detect the PD events, a Doble PD Smart with HFCT-300 sensor was used [65]. The Doble PD Smart complies with IEC 60270 and VDE 0434, among other standards [65]. PD signals at frequencies from 35 kHz to 20 MHz and an apparent charge as low as 0.2 pC can be measured [65].

PD tests were performed on a patterned, 1-mm thick AlN-DBA substrate. The spacing between metal traces and from the metal traces to the edge of the ceramic was 2 mm. The following three cases were tested:

1) a single substrate;
2) two stacked substrates with the middle metal connected to the source ground;
3) two stacked substrates with the middle metal connected to half of the applied excitation voltage.

Each case was tested under two conditions: 1) S1D2 = D1 (the high-side switch is conducting and the low-side switch is blocking), and 2) S1D2 = S2 (the high-side switch is blocking and the low-side switch is conducting).

First, the PD tests were performed with the samples in air to have a high signal-to-noise ratio. These tests revealed that, as was shown in the electrostatic simulations, the PD for the DBA substrates will occur at the triple points. Specifically, the PD will take place along the edge of the metal pad where the high potential is applied. The resulting PDIV for the cases when the samples are tested in air are listed in Table II. When S1D2 is equal to D1 (the applied voltage), and the middle metal is connected to half of the applied voltage, the PDIV increases by 53% compared to the single-substrate case [64]. The same increase in PDIV was observed when S1D2 is equal to S2 (ground). These results, which are in good agreement with the simulations, demonstrate that connecting the middle metal to half of the applied voltage gives predictable, consistent results for both switching states.

Since the power module will be encapsulated, PD tests were also performed on a stacked substrate sample that was encapsulated with SilGel 612 from Wacker. For this sample, the S1D2 potential was connected to S2 (the worst case). The measured PDIVs for this sample are listed in Table II. When the middle metal is connected to the source ground, the PDIV

is 7.4 kV rms (10.5 kV peak). For this same case, breakdown occurred at 8.5 kV rms (12.0 kV peak). This means if the middle metal is connected to ground, or if a single substrate is used, then there is 20% margin between the peak breakdown voltage and the voltage rating of the 10-kV SiC MOSFETs.

When the middle metal is connected to half of the applied voltage, no PD could be measured up to 10.5 kV rms (14.8 kV peak). The testing was stopped at 10.5 kV rms due to the reduced signal-to-noise ratio. This suggests that encapsulated stacked substrates with the middle metal connected to half of the applied voltage will have more than a 40% higher PDIV compared to a single substrate or a stacked substrate with the middle metal connected to ground. Therefore, it is advantageous to use the stacked substrate structure with the middle metal connected to half the applied voltage to increase the high-voltage performance of the power module.

VII. Conclusion

This work proposed a high-density power module for 10-kV SiC MOSFETs with reduced CM current and electric field strength. The optimal layout and system interface enable the module to switch 5 kV in tens of nanoseconds with negligible ringing and voltage overshoot. This is the fastest switching speed reported to date for 10-kV SiC MOSFETs. To reduce the adverse EMI effects of this high-speed switching, a CM screen was incorporated into the power module design. This screen was realized by stacking two DBA substrates and connecting the middle metal to the midpoint of embedded decoupling capacitors through vias and metal posts. This proposed method creates a low-impedance path at high frequency, and contains the current that would normally flow to the system ground within the power module. With this screen, the measured CM current leaving the power module decreases by ten times. This proposed integrated screen will reduce the need for filtering at the system level, thereby increasing the power density, lowering the cost, and simplifying the design of power electronic systems. Moreover, it will permit the operation of the 10-kV SiC MOSFETs at faster speeds, thereby reducing losses and increasing efficiency.

This screen also increases the voltage rating of the power module. PD tests showed that stacking two substrates and connecting the middle metal to half of the applied voltage increases the PDIV by 53% compared to a single substrate. When testing two encapsulated stacked substrates with the middle metal connected to the source ground, breakdown occurred at 8.5 kV rms (12.0 kV peak). This breakdown voltage limits the voltage rating of the package. When the middle metal of the encapsulated substrates is connected to half of the applied voltage, the PDIV exceeds 10.5 kV rms. This method for reducing the electric field is effective and simple to implement, and will enable high-voltage packages with greater power density.

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References

[1] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 912–921, Mar./Apr. 2011.

[2] A. Bindra, "SiC-based PV inverters display reduced size, weight and cost," *How2Power Today*, May 2013.

[3] J. Rabkowski, D. Peftitsis, and H. P. Nee, "Silicon carbide power transistors- A new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012.

[4] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[5] "Train trial shows a 40% energy saving for SiC inverters," *Drives and Controls*, Jun, 2015.

[6] J. W. Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. IEEE Int. Symp. Semicond. Devices IC's*, Jun. 2014, pp. 79–82.

[7] T. Lu, Z. Zhao, S. Ji, H. Yu, and L. Yuan, "Parameter design of voltage balancing circuit for series connected HV-IGBTs," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, Jun. 2012, pp. 1502–1507.

[8] H. Mirzaee, A. De, A. Tripathi, and S. Bhattacharya, "Design comparison of high-power medium-voltage converters based on a 6.5-kV Si-IGBT/Si-PiN diode, a 6.5-kV Si-IGBT/SiC-JBS diode, and a 10-kV SiC-MOSFET/SiC-JBS diode," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2728–2740, Jul/Aug. 2014.

[9] J. Casarin, P. Ladoux, and P. Lasserre, "10 kV SiC MOSFETs versus 6.5kV Si-IGBTs for medium frequency transformer application in railway traction," in *Proc. IEEE Int. Conf. Elect. Syst. Aircr., Railway, Ship Propulsion, Road Veh.*, Mar. 2015, pp. 1–6.

[10] K. Hatua, S. Dutta, A. Tripathi, S. Baek, G. Karimi, and S. Bhattacharya, "Transformer less intelligent power substation design with 15kV SiC IGBT for grid interconnection," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 4225–4232.

[11] S. Madhusoodhanan *et al.*, "Solid state transformer and MV grid tie applications enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs based multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3343–3360, Aug. 2015.

[12] *IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships*, IEEE Standard 1709-2010, Nov. 2010.

[13] C. Zhao *et al.*, "Power electron traction transformer- medium voltage prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, Aug. 2013.

[14] D. C. Patel *et al.*, "15 kV SiC IGBT based three-phase three-level modular-leg power converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 3291–3298.

[15] S. Srdic, X. Liang, C. Zhang, W. Yu, and S. Lukic, "A SiC-based high-performance medium-voltage fast charger for plug-in electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–6.

[16] M. S. Chinthavali, L. M. Tolbert, and B. Ozpineci, "4H-SiC GTO thyristor and p-n diode loss models for HVDC converter," in *Proc. IEEE Ind. Appl. Conf.*, Oct. 2004, pp. 1238–1243.

[17] Y. Koyama, Y. Nakazawa, H. Mochikawa, A. Kuzumaki, K. Sano, and N. Okada, "A transformerless 6.6-kV STATCOM based on a hybrid cascade multilevel converter using SiC devices," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7411–7423, Nov. 2017.

[18] P. Wolfs, F. Yang, and Q.-L. Han, "Distribution level SiC FACTS devices with reduced dc bus capacitance for improved load capability and solar integration," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 2014, pp. 1353–1358.

[19] M. K. Das *et al.*, "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2689–2692.

[20] R. Chattopadhyay *et al.*, "Low-voltage PV power integration into medium voltage grid using high-voltage SiC devices," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 3225–3232.

[21] A. Q. Huang, Q. Zhu, L. Wang, and L. Zhang, “15 kV SiC MOSFET: An enabling technology for medium voltage solid state transformers,” *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 118–130, Aug. 2017.

[22] V. Pala *et al.*, “10 kV and 15 kV silicon carbide power MOSFETs for next-generation energy conversion and transmission systems,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 449–454.

[23] K. Vechalapu, S. Bhattacharya, E. Van Brunt, S.-H. Ryu, D. Grider, and J. W. Palmour, “Comparative evaluation of 15-kV SiC MOSFET and 15-kV SiC IGBT for medium-voltage converter under the same dv/dt conditions,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 469–489, Mar. 2017.

[24] A. Kadavelugu, “Medium voltage power conversion enabled by 15 kV SiC IGBTs,” Ph.D. dissertation, North Carolina State Univ., Raleigh, NC, USA, 2015.

[25] X. Zhang *et al.*, “A gate drive with power over fiber-based isolated power supply and comprehensive protection functions for 15-kV SiC MOSFET,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 946–955, Sep. 2016.

[26] A. Tripathi, K. Mainali, S. Madhusoodhanan, A. Yadav, K. Vechalapu, and S. Bhattacharya, “A MV intelligent gate driver for 15kV SiC IGBT and 10kV SiC MOSFET,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 2076–2082.

[27] D. Berning, T. Duong, J. Ortiz-Rodfriguez, A. Rivera-Lopez, and A. Hefner, “High-voltage isolated gate drive circuit for 10 kV, 100 A SiC MOSFET/JBS power modules,” in *Proc. IEEE IAS Annu. Meeting*, 2008, pp. 1–7.

[28] S. Moballegh, S. Madhusoodhanan, and S. Bhattacharya, “Evaluation of high voltage 15 kV SiC IGBT and 10 kV SiC MOSFET for ZVS and ZCS high power DC -DC converters,” in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 656–663.

[29] M. Das, D. Grider, S. Leslie, R. Raju, M. Schutten, and A. Hefner, “10 kV SiC power MOSFETs and JBS diodes: Enabling revolutionary module and power conversion technologies,” *Mater. Sci. Forum*, vol. 717–720, pp. 1225–1228, May 2012.

[30] Z. Chen, R. Burgos, D. Boroyevich, F. Wang, and S. Leslie, “Modeling and simulation of 2 kV 50 A SiC MOSFET/JBS power modules,” in *Proc. IEEE Electric Ship Technol. Symp.*, Apr. 2009, pp. 1–10.

[31] B. Passmore *et al.*, “The next generation of high voltage (10 kV) silicon carbide power modules,” in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Nov. 2016, pp. 1–4.

[32] D. Domes, “Semiconductor arrangement,” U.S. Patent 2013/0043593 A1, Feb. 21, 2013.

[33] T. Huber, A. Kleimaier, S. Polster, and O. Mathieu, “Low inductive SiC power module design using ceramic multilayer substrates,” in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Jun. 2018.

[34] T. Huber, A. Kleimaier, and R. Kennel, “Ultra-low inductive power module design with integrated common mode noise shielding,” in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2017, pp. P.1–P.9.

[35] A. Domurat-Linde and E. Hoene, “Analysis and reduction of radiated EMI of power modules,” in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Mar. 2012, pp. 1–6.

[36] C. Bayer, U. Waltrich, R. Schneider, A. Soueidan, E. Baer, and A. Schletz, “Enhancing partial discharge inception voltage of DBCs by geometrical variations based on simulations of the electric field strength,” in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Mar. 2016, pp. 1–5.

[37] P. Wang, A. Cavallini, and G. C. Montanari, “The influence of repetitive square wave voltage parameters on enameled wire endurance,” *IEEE Trans. Dielect. Elect. Insul.*, vol. 21, no. 3, pp. 1276–1284, Jun. 2014.

[38] S. H. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, and A. Hefner, “10 kV, 5 A 4H-SiC power DMOSFET,” in *Proc. Int. Symp. Power Semicond. Devices IC’s*, 2006, pp. 1–4.

[39] B. A. Hull *et al.*, “Performance and stability of large-area 4H-SiC 10-kV junction barrier Schottky rectifiers,” *IEEE Trans. Electron. Devices*, vol. 55, no. 8, pp. 1864–1870, Aug. 2008.

[40] D. Grider *et al.*, “10 kV/120 A SiC DMOSFET half H-bridge power modules for 1 MVA solid state power substation,” in *Proc. IEEE Elect. Ship Technol. Symp.*, 2011, pp. 131–134.

[41] M. Jaksic *et al.*, “Medium-voltage impedance measurement unit for assessing the system stability of electric ships,” *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 829–841, Apr. 2017.

[42] C. DiMarino, I. Cvetkovic, Z. Shen, R. Burgos, and D. Boroyevich, “10 kV, 120 A SiC MOSFET modules for a power electronics building block (PEBB),” in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Oct. 2014, pp. 55–58.

[43] S. Haque *et al.*, “An innovative technique for packaging power electronic building blocks using metal posts interconnected parallel plate structures,” *IEEE Trans. Adv. Packag.*, vol. 22, no. 2, pp. 136–144, May 1999.

[44] B. Mouawad, J. Li, A. Castellazzi, and C. M. Johnson, “Hybrid half-bridge package for high voltage application,” in *Proc. IEEE Int. Symp. Semicond. Devices IC’s*, Jun. 2016, pp. 147–150.

[45] I. Yaqub, J. Li, and C. M. Johnson, “Dependence of overcurrent failure modes of IGBT modules on interconnect technologies,” *Microelectron. Reliab.*, vol. 55, no. 12, pp. 2596–2605, Dec. 2015.

[46] C. DiMarino *et al.*, “Design of a novel, high-density, high-speed 10 kV SiC MSOFET module,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2017, pp. 4003–4010.

[47] C. DiMarino *et al.*, “Fabrication and characterization of a high-power-density, planar 10 kV SiC MOSFET power module,” in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Mar. 2018, pp. 1–6.

[48] C. DiMarino *et al.*, “Design and experimental validation of a wire-bondless 10 kV SiC MOSFET power module,” *IEEE J. Emerg. Spec. Topics Power Electron.*, to be published.

[49] Z. Zhang and C. M. Johnson, “Suppression of electromagnetic interference using screening and shielding techniques within the switching cells,” in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Apr. 2017, pp. 1–5.

[50] E. Hoene, A. Ostmann, and C. Marczok, “Packaging very fast switching semiconductors,” in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Feb. 2014, pp. 1–7.

[51] J. H. Fabian, S. Hartmann, and A. Hamidi, “Analysis of insulation failure modes in high power IGBT modules,” in *Proc. 40th Ind. Appl. Soc. Annu. Meeting*, Oct. 2005, pp. 799–805.

[52] J. H. Fabian, S. Hartmann, and A. Hamidi, “Partial discharge failure analysis of AlN substrates for IGBT modules,” *Microelectron. Rel.*, vol. 44, pp. 1425–2430, 2004.

[53] G. Mitic and G. Lefranc, “Localization of electrical-insulation-and partial-discharge failures of IGBT modules,” *IEEE Trans. Ind. Appl.*, vol. 38, no. 1, pp. 175–180, Jan./Feb. 2002.

[54] C. F. Bayer, E. Baer, U. Waltrich, D. Malipaard, and A. Schletz, “Simulation of the electric field strength in the vicinity of metallization edges on dielectric substrates,” *IEEE Trans. Dielect. Elect. Insul.*, vol. 22, no. 1, pp. 257–265, Feb. 2015.

[55] O. Hohlfeld, R. Bayerer, T. Hunger, and H. Hartung, “Stacked substrates for high voltage applications,” in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Mar. 2012, pp. 1–4.

[56] H. Hourdequin, L. Laudebat, M.-L. Locatelli, and P. Bidan, “Design of packaging structures for high voltage power electronics devices: Electric field stress on insulation,” in *Proc. IEEE Int. Conf. Dielect.*, Jul. 2016, pp. 999–1002.

[57] D. Frey, J. L. Schanen, J. L. Auge, and O. Lesaint, “Electric field investigation in high voltage power modules using finite element simulations and partial discharge measurements,” in *Proc. 30th IAS Annu. Meeting Conf. Rec. Ind. Appl. Conf.*, Oct. 2003, pp. 1000–1005.

[58] H. Reynes, C. Buttay, and H. Morel, “Protruding ceramic substrates for high voltage packaging of wide bandgap semiconductors,” in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Nov. 2017, pp. 404–410.

[59] C. DiMarino, J. Wang, R. Burgos, and D. Boroyevich, “A high-power-density, high-speed gate driver for a 10 kV SiC MOSFET module,” in *Proc. IEEE Elect. Ship Technol. Symp.*, Aug. 2017, pp. 629–634.

[60] Electronic Concepts, “MP80 series metallized polypropylene,” MP80 datasheet, Rev. 4. [Online]. Available: https://www.ecicaps.com/film-capacitors/mp80-series

[61] A. Kadavelugu *et al.*, “Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 2528–2535.

[62] D. Johannesson, M. Nawaz, and K. Ilves, “Assessment of 10 kV, 100 A silicon carbide MOSFET power modules,” *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5215–5225, Jun. 2018.

[63] IXYS, “High voltage IGBT for capacitor discharge applications,” IXGF30N400 datasheet, 2009. [Online]. Available: http://ixapps.ixys.com/DataSheet/DS99978C(IXGF30N400).pdf

[64] C. DiMarino *et al.*, “A wire-bond-less 10 kV SiC MOSFET power module with reduced common-mode noise and electric field,” in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Jun. 2018, pp. 74–80.

[65] Doble Engineering Company, “Doble in-service testing & assessment PD-Smart partial discharge analyzer,” PD-Smart datasheet, Mar. 2016.

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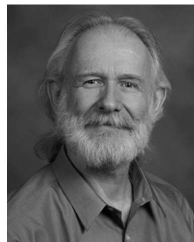
From 1990 to 1992, he was a Research Associate with the University of Cambridge and in 1992 he was appointed as a Lecturer in the University of Newcastle, U.K., where his research included the design, analysis, and characterization of power semiconductor devices, resonant power conversion and instrumentation. From 1998 to 2001, he managed the U.K. national programme on silicon carbide electronics, and in 2000, he became a Reader of Power Electronics at the University of Newcastle. In 2003, he was appointed as a Rolls-Royce/RAEng Research Professor of Power Electronic Systems at the University of Sheffield and in 2006 he was appointed to a Personal Chair at the University of Nottingham, where he leads research into power semiconductor devices, power device packaging, reliability, thermal management, power module technologies, and power electronic applications.

He is the Director of the U.K. Engineering and Physical Sciences Research Council (EPSRC) Centre for Power Electronics, which combines the U.K.'s best academic talent to address the key research challenges underpinning power electronics innovation plasma applications. He holds two patents.

Dr. Johnson is an Associate Editor of the journal *Earth*, *Moon*, *Planets*.



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Dr. Dushan was the President of the IEEE Power Electronics Society (PELS) for 2011–2012. He was the recipient of numerous awards, including the IEEE William E. Newell Power Electronics Technical Field Award, the IEEE PELS Harry A. Owen Distinguished Service Award, the European Power Electronics Association (EPE) Outstanding Achievement Award, and the Award for Outstanding Achievements and Service to Profession by the European Power Electronics and Motion Control Council. He is an Honorary Professor at the Xi'an Jiaotong University in Xi'an, China, and received the K.T. Li Chair Professor Award at the National Cheng Kung University, Tainan, Taiwan. He was elected to the US National Academy of Engineering in 2014 for advancements in control, modeling, and design of electronic power conversion for electric energy and transportation.

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