Switching and Conduction Loss Reduction of Dual-Buck Full-Bridge Inverter Through ZVT Soft-Switching Under Full-Cycle Modulation

Baoquan Kou, *Member, IEEE*, Jian Wei, and Lu Zhang, *Member, IEEE*

***Abstract*—Based on the no blanking time characteristic, voltage error does not occur in the pulsewidth modulated output stage of dual-buck full-bridge inverter (DBFBI), resulting in lower total harmonic distortion (THD) of the output current. The two main modulations applied in the topology are half-cycle modulation and full-cycle modulation. Compared with the half-cycle modulation, the full-cycle modulation does not have the zero-crossing problem, but the inverter requires a bias current to guarantee better output waveform. The circulation current loop caused by bias current has a great influence on inverter efficiency. This article proposes a novel zero voltage transition (ZVT) soft-switching topology to increase efficiency by reducing the switching losses and conduction losses resulting from low bias current. The advantages of the DBFBI are included in the proposed inverter. The soft-switching condition is achieved by the snubber cells, and the energy stored in the passive snubber capacitors can be transferred effectively. The topology deduction, operating principles, and design guidelines are presented in detail. An 800-W experimental prototype operating with a 100-kHz switching frequency is implemented to verify the theoretical result.**

***Index Terms*—Conduction losses, dual-buck full-bridge inverter (DBFBI), efficiency, full-cycle modulation, switching losses, zero voltage transition (ZVT) soft-switching.**

I. Introduction

MOTION control systems have increasingly strict demands for power converter performance, especially in ultraprecision positioning application, for instance, advanced numerical control machines require power converter with high-precision output current generation capabilities, which are used to provide the output currents to drive the electromechanical actuators, such as voice coil motors and linear motors [1], [2]. Nonlinearity errors produced by the converter influence the stationary and dynamic positioning accuracy of the high-precision mechatronic system. Furthermore, as an inner loop of the position servo control system, improving the output current precision of power converter is important to the optimization design of the mechatronics system. To achieve the high performance of the motion systems, power converters must meet the requirements of high precision. In fact, the dead-time effect is a dominant source of output current distortion to traditional full-bridge inverters [3]–[5]. To compensate for the dead-time effect, many research works have been conducted on full-bridge pulsewidth modulated (PWM) inverters [6]–[11]. These methods can reduce the problem but are not capable of completely removing it. The topology of dead-time elimination is a primary method to solve the aforementioned problems, which make the dual-buck full-bridge topology attractive to power converter. Therefore, it has been widely used in many power conversion systems, such as photovoltaic grids and LED drivers [12]–[18].

Modulation strategies of dual-buck full-bridge inverter (DBFBI) include the full-cycle mode and the half-cycle mode. When the inverter operates in the half-cycle mode, the switch and diode conduction times decrease, which can achieve relatively high efficiency [19], [20]. However, zero-crossing distortion occurs due to the inductor current on the state of discontinuous conduction mode. Some articles analyzed and tried to remove the zero-crossing distortion problem [21], [22], but the effect is less obvious. Total harmonic distortion (THD) of DBFBI under the half-cycle modulation can meet the requirement of grid-connected field. Accordingly, the characteristics of relatively high efficiency make it suitable for that. When the inverter operates in the full-cycle mode, a bias current is applied, and the continuous conduction mode (CCM) of the filter inductor current is maintained to eliminate the zero-crossing distortion completely. A key advantage of DBFBI under the full-cycle modulation is the high precision output current capability, which is important for the application of ultraprecision positioning. At the same time, a circulating current exists between the inductor and the switches (diodes), which reduces the efficiency of the inverter. With the growing demands on power density, how to improve the efficiency has become an increasingly important problem.

The soft-switching technique is efficient approach to solve the dissipation problem and to improve system efficiency [23]. A coupled-magnetic structure as the resonant snubber circuit achieved zero-voltage switching (ZVS) was proposed in [24]. The auxiliary switches meet with low current and ZCS, which resulted in low conduction and switching losses. In [25] and [26], soft-switching condition was achieved to decrease switching losses in the full-bridge grid-connected inverter, and the zero voltage transition (ZVT) zero current transition (ZCT) resonant

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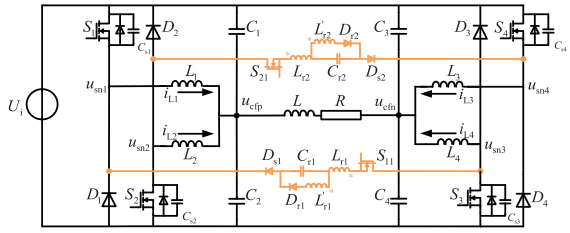

Fig. 1. Proposed ZVT DBFBI topology.

tank has no influence on the common-mode characteristics of the former transformerless topologies. In [27], Xiao *et al.* proposed a soft switching for the H6 inverter with self-compensation that reduced switching losses with few passive devices. Xiao *et al.* [28] introduced integrated resonant circuits for the highly efficient reliable inverter concept (HERIC) topology to reduce switching losses, and the added resonance cell increases the current stress of the active and passive components. In [29], an interleaved boost-integrated *LLC* resonant converter with full loads was analyzed, and switches were operated with ZVS over full-load range leading to reduced switching losses. A two-stage quasi-resonant dual-buck LED driver not suitable for full-cycle modulation was proposed in [30], and the system efficiency was improved to some extent in low-power application. In [31], a passive lossless snubber circuit was added to DBFBI to improve the efficiency, and the inverter was operated in the half-cycle modulation. Besides, the voltage error caused by rise- and fall-time due to the ZVT snubber cell in full-bridge topology was analyzed in [32].

The research of soft-switching mainly focuses on the grid-connected photovoltaic system to improve efficiency, and high precision is not a major issues. Furthermore, the existing soft-switching of the DBFBI topology does not achieve low THD while improving system efficiency. Therefore, a novel ZVT DBFBI topology shown in Fig. 1 is proposed to improve efficiency with low THD in the ultraprecision positioning application. The main contributions of this article are as follows. First, a new topology is proposed to improve the system efficiency, and the characteristic of low THD is achieved. Second, a design method is summarized by modeling and analyzing the resonant snubber cell. Third, the effect of resonant circuit and bias current on output voltage error is analyzed.

This article is organized as follows. In Section II, the basic topology of the ZVT DBFBI is presented, and the operation principle of the converter is analyzed. Modal operation diagrams of the soft switching are shown when the inductor operates in CCM. Section III introduces the parameters design and analysis of the conduction losses. Section IV shows the features of the converter compared with other similar converters, and the parameters of the ZVT DBFBI prototype are provided. Section V shows the experimental results of an 800-W ZVT DBFBI prototype.

II. Operation Principles and Analysis

A. Operation Modes of ZVT DBFBI

The resonant branch (S_{11}, L_{r1}, L'_{r1}, C_{r1}, D_{s1}, D_{r1}) corresponds to switches S_1 and S_3, whereas the resonant

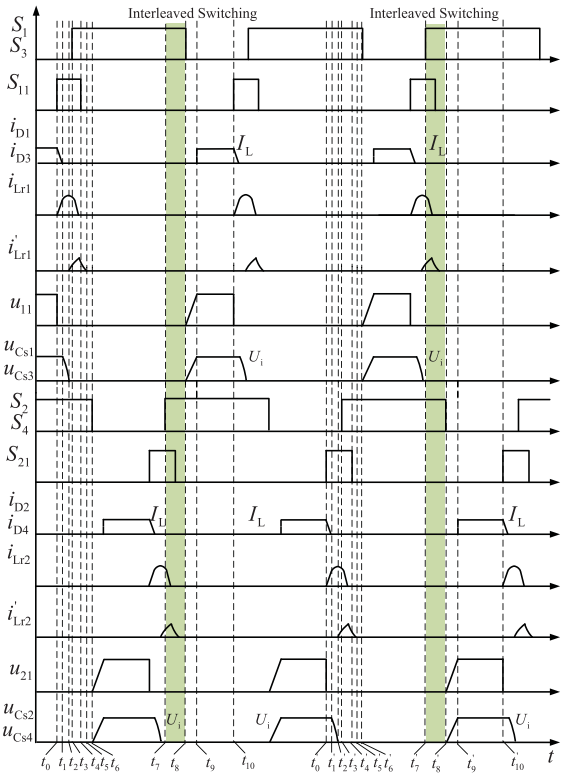

Fig. 2. Key waveforms of operation stages in the proposed converter.

branch (S_{21}, L_{r2}, L'_{r2}, C_{r2}, D_{s2}, D_{r2}) corresponds to switches S_2 and S_4. Cs1, Cs2, Cs3, and Cs4 are equal to Cs, which are equivalent parallel capacitances of the main switches. The switching period is divided into ten working stages when inductors operate in CCM. The behavior of the converter in each mode is explained in detail in this section. Equations that define the operation of the converter are derived. The operation stages of the soft-switching cells are shown in Fig. 2. The equivalent circuits of each operation mode are shown in Fig. 3.

Due to the symmetry characteristics of the ZVT DBFBI topology, the two soft-switching cells operate in the same way, so only one auxiliary branch is selected for analysis. When analyzing the operation state of the soft-switching cell corresponding to S_1 and S_3, the operation state of the soft switching cell corresponding to S_2 and S_4 is not considered for the convenience of analysis. The control signals of S_1 and S_3 overlaps with the control signals of S_2 and S_4.

Mode 1 [$t_0 < t < t_1$: Fig. 3(a)]: Before the initial moment t_0, switches S_1 and S_3 are in OFF state, whereas switches S_2 and S_4 are in ON state. The overlap between S_1 (S_3) and S_2 (S_4) is related to the bias current. Diode D_1 (D_3) fully conducts the inductor L_1 (L_4) current, and the current of filter inductor L_1 (L_4) can be considered as a constant within a soft-switching period. At the same time, $i_{S1} = 0$, $i_{S3} = 0$, $i_{Lr1} = 0$, and $u_{Cs1} = u_{Cs3} = U_i$. At $t = t_0$, due to the existence of the resonant inductor L_{r1}, auxiliary switch S_{11} turns ON under ZCS. Therefore, the inductor current i_{Lr1} increases linearly from 0. Besides, due to capacitor voltage u_{Cr1}, diode D_{r1} is in the reverse blocking state, and diode current i_{D1} (i_{D3}) decreases when current i_{L1} starts increasing.

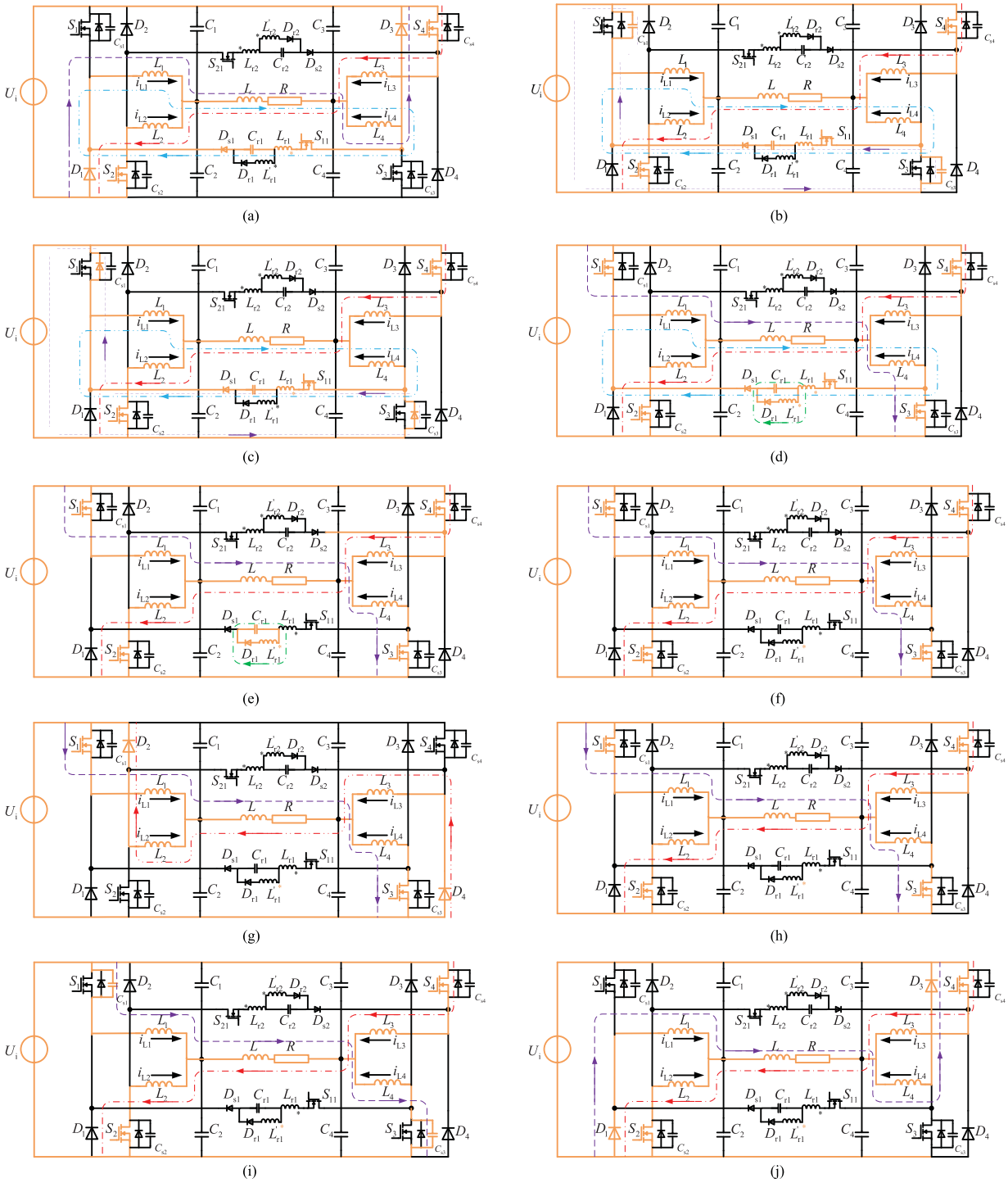

Fig. 3. Equivalent circuit schemes of the CCM in the proposed converter. (a) $t_0 < t < t_1$. (b) $t_1 < t < t_2$. (c) $t_2 < t < t_3$. (d) $t_3 < t < t_4$. (e) $t_4 < t < t_5$. (f) $t_5 < t < t_6$. (g) $t_6 < t < t_7$. (h) $t_7 < t < t_8$. (i) $t_8 < t < t_9$. (j) $t_9 < t < t_{10}$.

The equations for this stage are obtained as follows:

$$i_{\mathrm{Lr1}}(t) = \frac{U_{\mathrm{i}} + u_{\mathrm{Cr1}}(t_0)}{L_{\mathrm{r1}}}(t - t_0) \tag{1}$$

$$i_{\mathrm{D1}}(t) = I_{\mathrm{L1}} - i_{\mathrm{Lr1}}(t) = I_{\mathrm{L1}} - \frac{U_{\mathrm{i}} + u_{\mathrm{Cr1}}(t_0)}{L_{\mathrm{r1}}}(t - t_0). \tag{2}$$

When $t = t_1$, i_{Lr1} is equal to I_{L1}, this mode ends, and the duration is given as follows.

$$T_{01} = \frac{L_{\mathrm{r1}} \cdot I_{\mathrm{L1}}}{U_{\mathrm{i}} + u_{\mathrm{Cr1}}(t_0)}. \tag{3}$$

Mode 2 [$t_1 < t < t_2$: Fig. 3(b)]: At $t = t_1$, $i_{\mathrm{D1}}(t_1) = i_{\mathrm{D3}}(t_1) = 0$, $i_{\mathrm{Lr1}}(t_1) = I_{\mathrm{L}}$, and $u_{\mathrm{Cs1}}(t_1) = U_{\mathrm{i}}$. D_1 (D_3) realizes

ZCS turn-OFF. In this interval, a resonance begins between L_{r1}, C_{r1}, D_{s1}, S_{11}, C_{s1}, $C_{s3,}$ and U_i. The resonance starts via the path $L_{r1}\rightarrow C_{r1}\rightarrow C_{s1}\rightarrow U_i\rightarrow C_{s3}$. Resonant inductor current L_{r1} continues to increase with the voltage $u_{Cs1}(u_{Cs3})$ reduced by the resonant principle. Since the resonant inductor current i_{Lr1} is basically in the rising state, therefore the diode D_{r1} is in reverse blocking state. For this resonance, the following equations are obtained:

$$i_{Lr1}(t) = \left(U_i + u_{Cr1}(t_1)/\sqrt{2L_{r1}/C_s}\right)\sin\omega_0(t-t_1) + I_0\cos\omega_0(t-t_1) + I_{L1} \tag{4}$$

$$u_{Cs1}(t) = u_{s1}(t) = \frac{U_i - u_{Cr1}(t_1)}{2} + \frac{U_i + u_{Cr1}(t_1)}{2}\cos\omega_0(t-t_1) - (I_0/\sqrt{2C_s/L_{r1}})\sin\omega_0(t-t_1). \tag{5}$$

In the equations, I_0 is the initial resonant current of inductor L_{r1}. In order to compare with other ZVT circuits, I_0 was introduced

$$\omega_0 = \sqrt{\frac{2}{L_{r1}C_s}} \tag{6}$$

Eq. 7 shown at the bottom of this page.

For the proposed ZVT snubber cell, the initial resonant current I_0 is equal to 0, and therefore

$$T_{12} = \frac{\pi - \arccos((U_i - u_{Cr1}(t_1))/(U_i + u_{Cr1}(t_1)))}{\sqrt{2/L_{r1}C_s}}. \tag{8}$$

Mode 3 [$t_2 < t < t_3$: Fig. 3(c)]: At $t = t_2$, $u_{Cs1}(u_{Cs3})$ decreases to zero. During this stage, the resonant inductor should obtain enough current that is more than the filter inductor current through the resonant circuit. The body diodes of S_1 and S_3 conducts the excess of the resonance current from inductor current, and the control signal must be applied to switches S_1 and S_3. Thus, ZVS turn-ON for S_1 and S_3 will be achieved. It can be seen that time duration of this stage is called ZVT time. For this stage, the following equations are obtained:

$$i_{D_{S1}} = i_{Lr1}(t_2) - i_{L1} \tag{9}$$

$$T_{23} = L_{r1}(i_{Lr1}(t_2) - i_{L1})/(U_i - u_{Cr1}). \tag{10}$$

Mode 4 [$t_3 < t < t_4$: Fig. 3(d)]: The main switch S_1 (S_3) turns on under ZVS condition. The voltage of resonant inductor i_{Lr1} reaches U_i-u_{Cr1}, and the current i_{Lr1} decreases due to the reverse voltage U_i. Current of coupled inductor L'_{r1} begins increasing at the same time. When the current i_{Lr1} flowing through Diode D_{S1} is zero, the current i'_{Lr1} also reaches its maximum value simultaneously. When current i_{Lr1} drops to zero, the control signal of S_{11} should be removed, and this stage ends. The following equations are formed for this stage and M is the mutual inductance

$$i_{Lr1}(t) = i_{Lr1}(t_3) - \frac{L'_{r1}U_i - (L'_{r1}+M)u_{Cr1}(t_3)}{L_{r1}L'_{r1} - M^2}(t-t_3) \tag{11}$$

$$i_{L'_{r1}}(t) = \frac{MU_i - (L_{r1}+M)u_{Cr1}(t_3)}{L_{r1}L_{r1}' - M^2}(t-t_3) \tag{12}$$

$$T_{34} = \frac{i_{Lr1}(t_3)(L_{r1}L'_{r1} - M^2)}{L'_{r1}U_i - (L'_{r1}+M)u_{Cr1}(t_3)}. \tag{13}$$

Mode 5 [$t_4 < t < t_5$: Fig. 3(e)]: This stage starts when the control signal of S_{11} is removed and ZCS turn-OFF for S_{11} is achieved. S_1 and S_3 conduct current i_{L1} and i_{L4} to the load, and the time of this interval is determined by the PWM control. A resonance starts between the L'_{r1} and C_{r1} via the path $L'_{r1}\rightarrow D_{r1}\rightarrow C_{r1}$. i_{Lr1} drops to zero at t_5, and this stage ends

$$i_{L'r1}(t) = 2\cdot\sqrt{\left(\frac{i_{L'r1}(t_4)}{2}\right)^2 + \left(\frac{u_{Cr1}(t_4)}{2}\right)^2\frac{C_{r1}}{L'_{r1}}} \times\cos(\omega_1(t-t_4)+\theta_1) \tag{14}$$

$$T_{45} = \left(\frac{\pi}{2} - \theta_1\right)\Big/\,\omega_1. \tag{15}$$

In these equations, ω_1 is determined as follows:

$$\omega_1 = \frac{1}{\sqrt{L'_{r1}C_{r1}}} \tag{16}$$

$$\theta_1 = \arctan\left(\frac{C_{r1}u_{Cr1}(t_4)}{L'_{r1}i_{L'r1}(t_4)}\right). \tag{17}$$

Mode 6 [$t_5 < t < t_6$: Fig. 3(f)]: The initial conditions at $t = t_5$ are $i_{S1} = i_{L1}$, $i_{S2} = i_{L2}$, $i_{S3} = i_{L4}$ $i_{S4} = i_{L3}$, $i'_{Lr1} = 0$, and $i_{Lr1} = 0$. This stage starts when the current of inductor L'_{r1} drops to zero. The switches S_1 and S_3 are in ON state, so the energies of inductors L_1 and L_4 are given by the source U_i via the main switches S_1 and S_3. The main switches S_2 and S_4 turn OFF at the end of this interval. For this stage, equation can be given as follows:

$$i_{S1} = i_{L1}. \tag{18}$$

Mode 7 [$t_6 < t < t_7$: Fig. 3(g)]: At $t = t_6$, $i_{S1} = i_{L1}$, $i_{S3} = i_{L4}$, $u_{Cs2} = U_i$, and $u_{Cs4} = U_i$. At this stage, the snubber cell is inactive, and main switches S_1 and S_3 continue to conduct the inductor currents i_{L1} and i_{L4}. Diodes D_2 and D_4 turn ON

$$T_{12} = \frac{\pi - \arccos\left(\dfrac{(U_i - u_{Cr1}(t_1))/2}{\sqrt{\left(\dfrac{I_0}{\sqrt{2C_s/L_{r1}}}\right)^2 + \left(\dfrac{U_i + u_{Cr1}(t_1)}{2}\right)^2}}\right) - \arctan\left(\dfrac{I_0/\sqrt{2C_s/L_{r1}}}{U_i/2}\right)}{\sqrt{2/L_{r1}C_s}}. \tag{7}$$

to conduct currents i_{L2} and i_{L3} for freewheeling. This stage is normal duration of the PWM converter.

Mode 8 [$t_7 < t < t_8$: Fig. 3(h)]: The initial conditions at $t = t_7$ are $i_{\mathrm{S1}} = i_{\mathrm{L1}}$, $i_{\mathrm{D2}} = 0$, $i_{\mathrm{S3}} = i_{\mathrm{L4}}$, $i_{\mathrm{D4}} = 0$, $i'_{\mathrm{Lr1}} = 0$, and $i_{\mathrm{Lr1}} = 0$. The main switches S_2 and S_4 turn ON at the beginning of this interval. The overlap between S_1 (S_3) and S_2 (S_4) is related to bias current. This stage ends with removing control signals of S_1 and S_3.

Mode 9 [$t_8 < t < t_9$: Fig. 3(i)]: At $t = t_8$, $i_{\mathrm{S1}} = 0$, $i_{\mathrm{S3}} = 0$, $i_{\mathrm{S2}} = i_{\mathrm{L2}}$, $i_{\mathrm{S4}} = i_{\mathrm{L3}}$, $u_{\mathrm{Cs1}} = u_{\mathrm{Cs3}} = 0$, and $u_{\mathrm{Cd1}} = u_{\mathrm{Cd3}} = U_{\mathrm{i}}$ are valid. In this interval, C_{s1} (C_{s3}) is charged and C_{d1} (C_{d3}) is discharged by the line current, simultaneously. At the end of this stage, C_{s1} (C_{s3}) voltage is equal to U_{i}, and C_{d1} (C_{d3}) voltage is equal to zero. The following equations can formed for this stage:

$$U_{\mathrm{i}} = \frac{i_{\mathrm{Cs1}}(t)}{C_{\mathrm{s}}}(t - t_8) + \frac{i_{\mathrm{Cd1}}(t)}{C_{\mathrm{d1}}}(t - t_8). \tag{19}$$

Mode 10 [$t_9 < t < t_{10}$: Fig. 3(j)]: In this stage, the control signals of S_1 and S_3 are negative half-cycle. This stage is OFF state duration of the PWM converter, and diodes D_1 and D_3 turn ON to conduct current I_{L} for freewheeling. At $t = t_{10}$, one switching period is completed, and a new switching period begins

$$i_{\mathrm{D1}} = i_{\mathrm{L1}}. \tag{20}$$

B. Control Method of the Proposed Inverter

The operation of the auxiliary resonant circuit depends on the state of the main circuit, and the proposed soft switching is compatible with the operation of the main circuit. Based on the average switching node voltage u_{sn}, the state-space average model and equations are given as in (21) shown at the bottom of this page.

$$y = \mathrm{C}x = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{out}} \\ i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ i_{\mathrm{L3}} \\ i_{\mathrm{L4}} \\ u_{\mathrm{Cfp}} \\ u_{\mathrm{Cfn}} \end{bmatrix}, \tag{22}$$

where x is the state variable, u is the input variable. A, B, and C are constant matrices. Besides, L_{f} and R_{f} are the filter inductance and resistance, respectively. The assumption $C_1 = C_2 = C_3 = C_4 = C_{\mathrm{f}}/2$ is made. In order to realize decoupling control of output current i_{out} and bias current i_{bias}, the decoupling equations are defined as follows:

$$\begin{cases} \left.\begin{aligned} u_{\mathrm{outp}} &= \tfrac{1}{2}(u_{\mathrm{sn1}} + u_{\mathrm{sn2}}) \\ u_{\mathrm{outn}} &= \tfrac{1}{2}(u_{\mathrm{sn4}} + u_{\mathrm{sn3}}) \\ u_{\mathrm{biasp}} &= (u_{\mathrm{sn1}} - u_{\mathrm{sn2}}) \\ u_{\mathrm{biasn}} &= (u_{\mathrm{sn4}} - u_{\mathrm{sn3}}) \end{aligned}\right\} \Rightarrow \begin{bmatrix} u_{\mathrm{outp}} \\ u_{\mathrm{outn}} \\ u_{\mathrm{biasp}} \\ u_{\mathrm{biasn}} \end{bmatrix} = \mathrm{G} \begin{bmatrix} u_{\mathrm{sn1}} \\ u_{\mathrm{sn2}} \\ u_{\mathrm{sn4}} \\ u_{\mathrm{sn3}} \end{bmatrix} \\ \left.\begin{aligned} i_{biasp} &= \tfrac{1}{2}(i_{L1} - i_{L2}) \\ i_{biasn} &= \tfrac{1}{2}(i_{L3} - i_{L4}) \end{aligned}\right\} \Rightarrow \begin{bmatrix} i_{biasp} \\ i_{biasn} \end{bmatrix} = \mathrm{Q} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \end{bmatrix} \end{cases}. \tag{23}$$

By combining the decoupling equation with the state equation, the new state equation is derived as in (24) shown at the bottom of the next page.

$$\begin{aligned} y' &= \begin{bmatrix} i_{\mathrm{out}} \\ i_{\mathrm{biasp}} \\ i_{\mathrm{biasn}} \\ i_{\mathrm{Cfp}} \\ i_{\mathrm{Cfn}} \end{bmatrix} = \mathrm{C}'x \\ &= \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/2 & -1/2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/2 & -1/2 & 0 & 0 \\ -1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{out}} \\ i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ i_{\mathrm{L3}} \\ i_{\mathrm{L4}} \\ u_{\mathrm{Cfp}} \\ u_{\mathrm{Cfn}} \end{bmatrix}. \end{aligned} \tag{25}$$

Therefore, the equation between input and output after decoupling can be obtained as

$$\begin{aligned} y'(s) &= \mathrm{C}'(s\mathrm{I} - \mathrm{A})^{-1}\mathrm{B}'u' \\ &= \begin{bmatrix} \mathrm{p}_{\mathrm{out}} & -\mathrm{p}_{\mathrm{out}} & 0 & 0 \\ 0 & 0 & \mathrm{p}_{\mathrm{bias}} & 0 \\ 0 & 0 & 0 & \mathrm{p}_{\mathrm{bias}} \\ \mathrm{p}_{\mathrm{iCf}} & \mathrm{p}'_{\mathrm{iCf}} & 0 & 0 \\ \mathrm{p}'_{\mathrm{iCf}} & \mathrm{p}_{\mathrm{iCf}} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} u_{\mathrm{outp}} \\ u_{\mathrm{outn}} \\ u_{\mathrm{biasp}} \\ u_{\mathrm{biasn}} \end{bmatrix}. \end{aligned} \tag{26}$$

From the aforementioned equations, i_{out} is determined by u_{outp} and u_{outn}; however, i_{bias} is determined by u_{biasp} and u_{biasn}. Therefore, output current and bias current can be controlled separately by decoupling.

$$\dot{x} = \mathrm{A}x + \mathrm{B}u = \begin{bmatrix} -R/L & 0 & 0 & 0 & 0 & 1/L & -1/L \\ 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & 0 & 0 & -1/L_{\mathrm{f}} & 0 \\ 0 & 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & 0 & -1/L_{\mathrm{f}} & 0 \\ 0 & 0 & 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & 0 & -1/L_{\mathrm{f}} \\ 0 & 0 & 0 & 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & -1/L_{\mathrm{f}} \\ -1/C_{\mathrm{f}} & 1/C_{\mathrm{f}} & 1/C_{\mathrm{f}} & 0 & 0 & 0 & 0 \\ 1/C_{\mathrm{f}} & 0 & 0 & 1/C_{\mathrm{f}} & 1/C_{\mathrm{f}} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{out}} \\ i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ i_{\mathrm{L3}} \\ i_{\mathrm{L4}} \\ u_{\mathrm{Cfp}} \\ u_{\mathrm{Cfn}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1/L_{\mathrm{f}} & 0 & 0 & 0 \\ 0 & 1/L_{\mathrm{f}} & 0 & 0 \\ 0 & 0 & 1/L_{\mathrm{f}} & 0 \\ 0 & 0 & 0 & 1/L_{\mathrm{f}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} u_{\mathrm{sn1}} \\ u_{\mathrm{sn2}} \\ u_{\mathrm{sn4}} \\ u_{\mathrm{sn3}} \end{bmatrix} \tag{21}$$

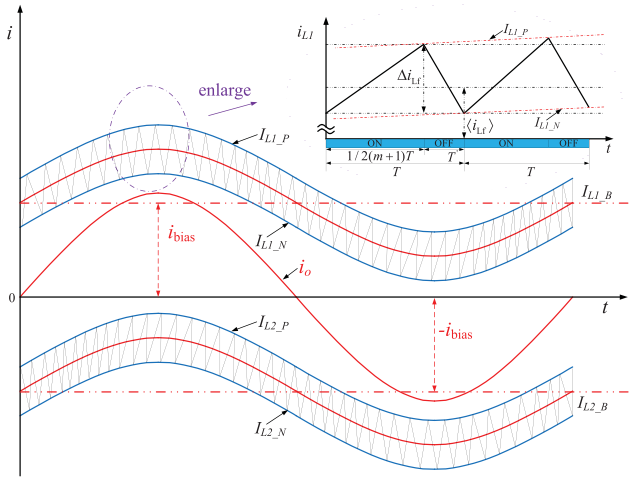

Fig. 4. Main waveforms with decoupling control based on bias current.

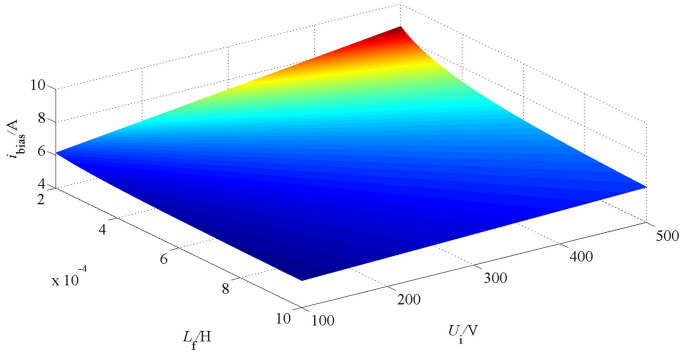

Fig. 5. Bias current under 100 kHz switching frequency.

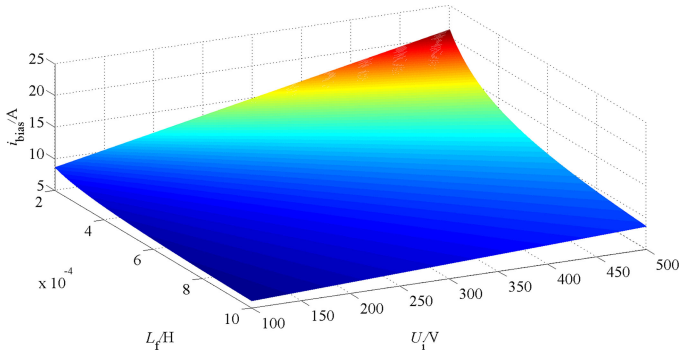

Fig. 6. Bias current under 20 kHz switching frequency.

In order to eliminate the zero-crossing distortion, the filter inductor should operate in CCM. Therefore, a bias current is necessary to keep the inductor currents continuous, which is analyzed in Fig. 4

$$\Delta i_{\mathrm{Lf}} = \frac{\frac{1}{2}(m+1)(U_{\mathrm{i}} - u_{\mathrm{cfp}})T}{L_{\mathrm{f}}} = \frac{(1-m^2)TU_{\mathrm{i}}}{4L_{\mathrm{f}}} \tag{27}$$

$$\Delta I_{\mathrm{Lf}} = \frac{TU_{\mathrm{i}}}{4L_{\mathrm{f}}} \tag{28}$$

$$i_{\mathrm{bias}} \geq \frac{1}{2}\left|i_{\mathrm{omax}}\right| + \frac{1}{2}\Delta I_{\mathrm{Lf}} = \frac{1}{2}\left|i_{\mathrm{omax}}\right| + \frac{TU_{\mathrm{i}}}{8L_{\mathrm{f}}} \tag{29}$$

where m is the carrier modulation ratio. Switching period T and dc bus voltage U_{i} are proportional to bias current, whereas filter inductance and bias current are inversely proportional. The variation of bias current is shown in Figs. 5 and 6.

Due to the bias current, there are two circulation current loops, which increase the conduction losses and have a great influence on efficiency. In addition, bias current is important to the design of inductors, which affects the operating point of the magnetic core. With the increase in bias current, the dc magnetization of the magnetic core will be further enhanced, which may cause the saturation, especially in the case of large dc bus voltage. Although the bias current can be reduced by increasing the inductance, the bias current is still relatively large. In the case, it is difficult to obtain the magnetic core with high filter

$$\dot{x} = \mathrm{A}x + \mathrm{B}'u' = \begin{bmatrix} -R/L & 0 & 0 & 0 & 0 & 1/L & -1/L \\ 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & 0 & 0 & -1/L_{\mathrm{f}} & 0 \\ 0 & 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & 0 & -1/L_{\mathrm{f}} & 0 \\ 0 & 0 & 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & 0 & -1/L_{\mathrm{f}} \\ 0 & 0 & 0 & 0 & -R_{\mathrm{f}}/L_{\mathrm{f}} & 0 & -1/L_{\mathrm{f}} \\ -1/C_{\mathrm{f}} & 1/C_{\mathrm{f}} & 1/C_{\mathrm{f}} & 0 & 0 & 0 & 0 \\ 1/C_{\mathrm{f}} & 0 & 0 & 1/C_{\mathrm{f}} & 1/C_{\mathrm{f}} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{out}} \\ i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ i_{\mathrm{L3}} \\ i_{\mathrm{L4}} \\ u_{\mathrm{Cfp}} \\ u_{\mathrm{Cfn}} \end{bmatrix}$$
$$+ \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1/L_{\mathrm{f}} & 0 & 1/(2L_{\mathrm{f}}) & 0 \\ 1/L_{\mathrm{f}} & 0 & -1/(2L_{\mathrm{f}}) & 0 \\ 0 & 1/L_{\mathrm{f}} & 0 & 1/(2L_{\mathrm{f}}) \\ 0 & 1/L_{\mathrm{f}} & 0 & -1/(2L_{\mathrm{f}}) \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} u_{\mathrm{outp}} \\ u_{\mathrm{outn}} \\ u_{\mathrm{biasp}} \\ u_{\mathrm{biasn}} \end{bmatrix} \tag{24}$$

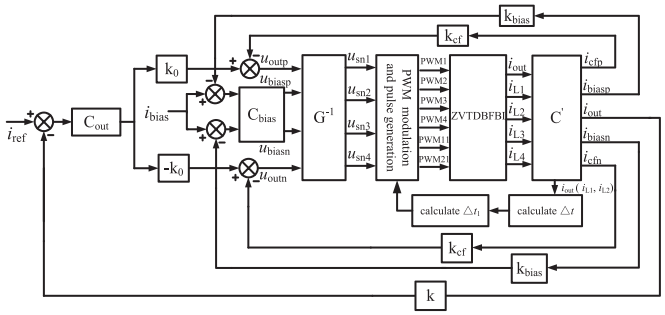

Fig. 7. Control diagram of the proposed ZVTD BFBI.

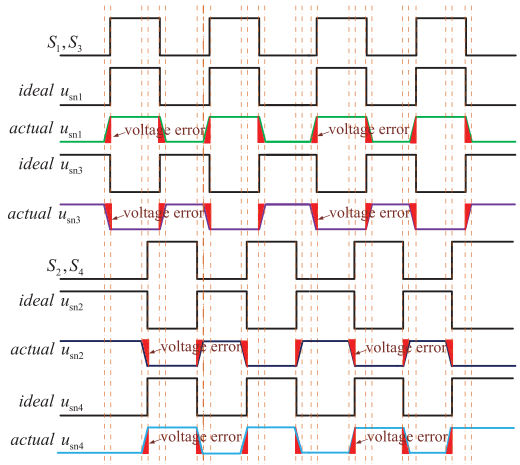

Fig. 8. Voltage error of ZVT DBFBI.

performance and strong resistance ability of dc magnetization. Therefore, reducing the bias current is needed.

Based on the abovementioned analysis, the decoupling control diagram of the proposed converter is shown in Fig. 7. According to the control diagram, the soft-switching snubber cell is compatible with the decoupling control algorithm, and it is important to ensure high performance of the proposed inverter.

To the auxiliary soft-switching cells of ZVT DBFBI, a time interval Δt is necessary for the auxiliary switches to turn ON in advance of the main switches. In addition, after the main switches turning on, the auxiliary switches needs to delay a time interval Δt_1 for realizing ZCS turn-OFF. The turn-ON signals of S_{11} and S_{21} are determined by the charging time and resonance time of resonant inductors. The turn-OFF signals of S_{11} and S_{21} are determined by the time of the resonant inductor current falling to zero. These times can be derived and calculated, so the pulse of the auxiliary switches can be obtained.

III. Design Procedure

A. ZVT Snubber Cells Design

1) The voltage error caused by rise time and fall time due to ZVT snubber cell exists in the drain-to-source voltage of main switches, which possibly causes the nonlinearity of the inverter and increases output harmonic. The voltage error introduced by the ZVT snubber cell in the proposed topology is analyzed as Fig. 8.

Combined the decoupling equations (23) and (26) and the symmetry of the proposed topology, the voltage error caused by the soft-switching snubber cell is eliminated. Besides, the ZVT snubber cell has no resonant component in the main current path, and the resonant process does not cause the oscillation of the filter inductance current. Therefore, the proposed ZVT circuit can maintain the low THD output of the inverter.

2) To determine the steady-state switching node voltage error as a function of the bias current and output voltage, the steady-state duty cycles are determined by an averaged model, which is valid for an ideal triangular inductor current ripple, Eq.30 shown at the bottom of this page, where $< >$ represents a cycle average value, and R_{onm} is the on-resistance of MOSFET. v_{f} and R_{ond} are the forward voltage and resistance of diode, respectively. Based on the nonideal circuit model, the duty cycles are substituted by the desired steady-state averaged switching node voltages using $<i_{\mathrm{Lf}}>$.

Therefore, the output voltage error under nonideal circuit conditions can be calculated according to decoupling equation (26), and the linear reference is removed.

From Fig. 9, it can be seen that the voltage error is small and almost does not vary with the bias current when the on-resistance is less than 50 mΩ. With the increase in on-resistance of MOSFET, the bias current will affect the nonlinear error of output voltage, which will increase the harmonic component of the output current. Of course, the voltage error can be compensated to a great extent by the feed-back control. In conventional converters, these effects are, in practice, often neglected, since their contribution is relatively small compared with the effect of blanking time, or simply because high accuracy is not an issue.

The operation of soft-switching cells is related to the performance of the converter, which should be further analyzed. Based

$$
\begin{cases}
u_{\mathrm{sn1}} = \underbrace{(v_{\mathrm{f}} + (R_{\mathrm{ond}} - R_{\mathrm{onm}}) \cdot \langle i_{\mathrm{Lf1}} \rangle) \cdot (u_{\mathrm{Cfp}} + \langle i_{\mathrm{Lf1}} \rangle \cdot R_{\mathrm{f}})/U_{\mathrm{i}} - (v_{\mathrm{f}} + R_{\mathrm{ond}} \cdot \langle i_{\mathrm{Lf1}} \rangle)}_{\text{Nonlinear errors}} + \underbrace{(u_{\mathrm{Cfp}} + \langle i_{\mathrm{Lf1}} \rangle \cdot R_{\mathrm{f}})}_{\text{Linear reference}} \\
u_{\mathrm{sn2}} = \underbrace{((R_{\mathrm{ond}} - R_{\mathrm{onm}}) \cdot \langle i_{\mathrm{Lf2}} \rangle - v_{\mathrm{f}}) \cdot (U_{\mathrm{i}} - u_{\mathrm{Cfp}} - \langle i_{\mathrm{Lf2}} \rangle \cdot R_{\mathrm{f}})/U_{\mathrm{i}} + (v_{\mathrm{f}} - R_{\mathrm{ond}} \cdot \langle i_{\mathrm{Lf2}} \rangle)}_{\text{Nonlinear errors}} + \underbrace{(u_{\mathrm{Cfp}} + \langle i_{\mathrm{Lf2}} \rangle \cdot R_{\mathrm{f}})}_{\text{Linear reference}} \\
u_{\mathrm{sn3}} = \underbrace{((R_{\mathrm{ond}} - R_{\mathrm{onm}}) \cdot \langle i_{\mathrm{Lf4}} \rangle - v_{\mathrm{f}}) \cdot (U_{\mathrm{i}} - u_{\mathrm{Cfn}} - \langle i_{\mathrm{Lf4}} \rangle \cdot R_{\mathrm{f}})/U_{\mathrm{i}} + (v_{\mathrm{f}} - R_{\mathrm{ond}} \cdot \langle i_{\mathrm{Lf4}} \rangle)}_{\text{Nonlinear errors}} + \underbrace{(u_{\mathrm{Cfn}} + \langle i_{\mathrm{Lf4}} \rangle \cdot R_{\mathrm{f}})}_{\text{Linear reference}} \\
u_{\mathrm{sn4}} = \underbrace{(v_{\mathrm{f}} + (R_{\mathrm{ond}} - R_{\mathrm{onm}}) \cdot \langle i_{\mathrm{Lf3}} \rangle) \cdot (u_{\mathrm{Cfn}} + \langle i_{\mathrm{Lf3}} \rangle \cdot R_{\mathrm{f}})/U_{\mathrm{i}} - (v_{\mathrm{f}} + R_{\mathrm{ond}} \cdot \langle i_{\mathrm{Lf3}} \rangle)}_{\text{Nonlinear errors}} + \underbrace{(u_{\mathrm{Cfn}} + \langle i_{\mathrm{Lf3}} \rangle \cdot R_{\mathrm{f}})}_{\text{Linear reference}}
\end{cases}
\tag{30}
$$

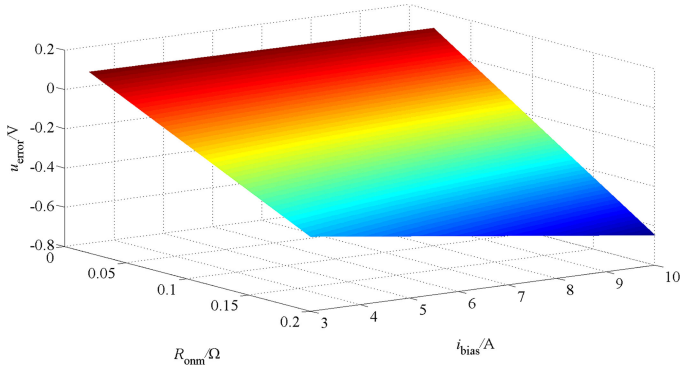

Fig. 9. Output voltage error with different bias currents.

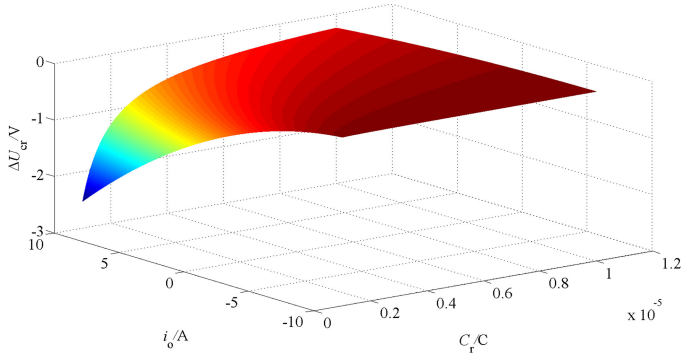

Fig. 10. Relations of $\Delta U_{\rm cr}$, $i_{\rm o}$, and $C_{\rm r}$ under interval T_{01}.

on this, snubber components should be designed according to the following analysis.

3) ZVT soft-switching needs to meet the conditions that auxiliary switches (S_{11}, S_{21}) turn ON in advance of main switches for a short interval Δt determined by the following formula:

$$\begin{aligned}&\underbrace{\frac{L_{\rm r1}\cdot I_{\rm L1}}{U_{\rm i}+u_{\rm Cr1}(t_0)}}_{T_{01}}\\&+\underbrace{\frac{\pi-\arccos((U_i-u_{\rm Cr1}(t_1))/(U_i+u_{\rm Cr1}(t_1)))}{\sqrt{2/L_{r1}C_s}}}_{T_{12}}\\&+\underbrace{\frac{L_{\rm r1}(i_{\rm Lr1}(t_2)-i_{\rm L1})}{U_{\rm i}-u_{\rm Cr1}}}_{T_{23}}\geq\Delta t\\&\geq\underbrace{\frac{L_{\rm r1}\cdot I_{\rm L1}}{U_{\rm i}+u_{\rm Cr1}(t_0)}}_{T_{01}}\\&+\underbrace{\frac{\pi-\arccos((U_i-u_{\rm Cr1}(t_1))/(U_i+u_{\rm Cr1}(t_1)))}{\sqrt{2/L_{r1}C_s}}}_{T_{12}}.\end{aligned}\tag{31}$$

The variables in formula (31) are $u_{\rm cr1}$ (t) and $I_{\rm L1}$, so the two variables need to be analyzed. First, $I_{\rm L1}$ can be obtained by sampling or the output current $i_{\rm o}$. Second, if $u_{\rm cr1}$ (t) can be considered as a dc voltage source, then it does not require sampling. Accordingly, it is necessary to select an appropriate capacitance to maintain the capacitor voltage $u_{\rm cr1}$ fluctuating in a small range. The variation of capacitor voltage $u_{\rm cr}$ and its effect on the soft switching are analyzed, as shown in Figs. 10–12, respectively. Based on the theoretical analysis, the capacitor voltage remained basically invariable, and its effect on the soft switching was also small. Therefore, the capacitor voltage $u_{\rm cr}$ (t) can be treated as a constant when calculating the time interval Δt, and the calculation error of time interval caused by voltage fluctuation ($\Delta u_{\rm cr}$) will not affect the operation of soft switching.

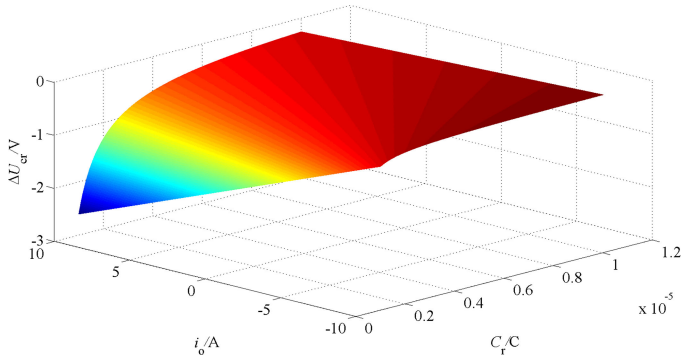

Fig. 11. Relations of $\Delta U_{\rm cr}$, $i_{\rm o}$, and $C_{\rm r}$ under interval T_{12}.

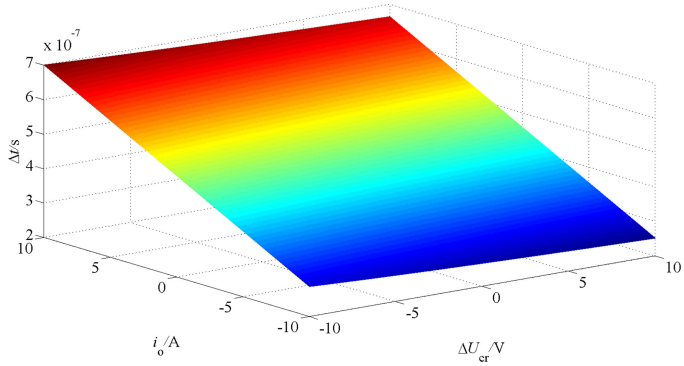

Fig. 12. Relations of interval Δt, $i_{\rm o}$, and $\Delta U_{\rm cr}$.

4) After the main switches turn ON, the auxiliary switches needs to delay a time interval Δt_1 determined by formula (32) to realize ZCS. Therefore, the turn-ON and turn-OFF time of the auxiliary switches can be obtained by formula (31) and (32), and the pulse of the auxiliary switches can be obtained

$$DT-t_{\rm ch}\geq\Delta t_1\geq\underbrace{\frac{i_{\rm Lr1}(t_3)(L_{\rm r1}L'_{\rm r1}-M^2)}{L'_{\rm r1}U_{\rm i}-(L'_{\rm r1}+M)u_{\rm Cr1}(t_3)}}_{T_{34}}.\tag{32}$$

The effect of capacitor voltage variation $\Delta U_{\rm cr}$ and coupling coefficient k on interval Δt_1 is shown in Figs. 13 and 14,

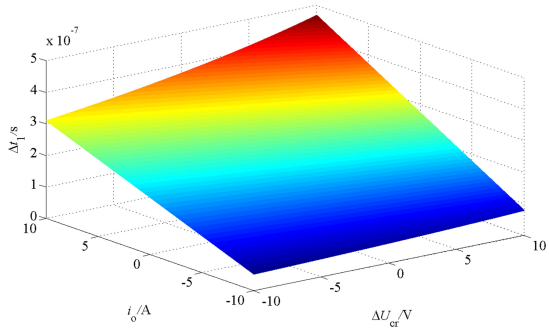

Fig. 13. Relations of interval Δt_1, $i_{\rm o}$, and $\Delta U_{\rm cr}$.

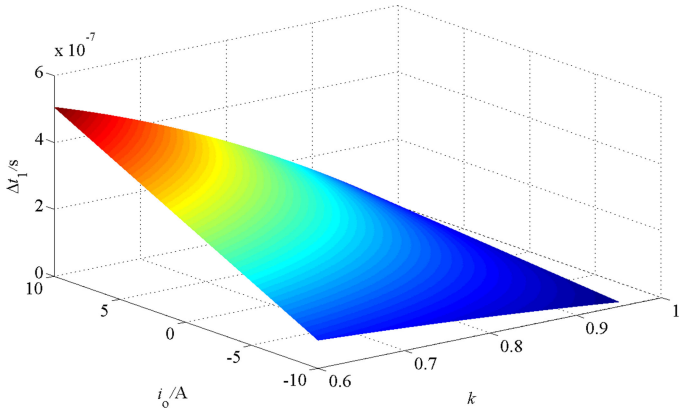

Fig. 14. Relations of interval Δt_1, $i_{\rm o}$, and k.

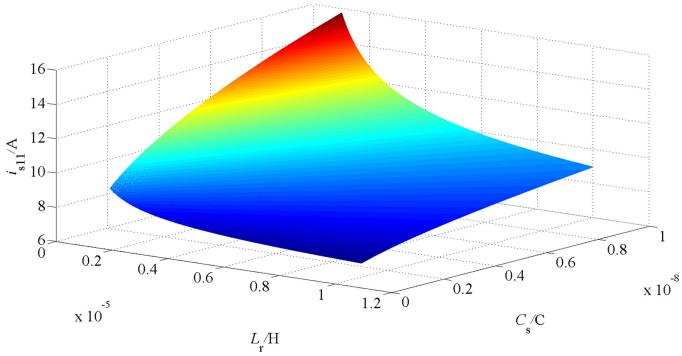

Fig. 15. Current stress of the auxiliary switch S_{11}.

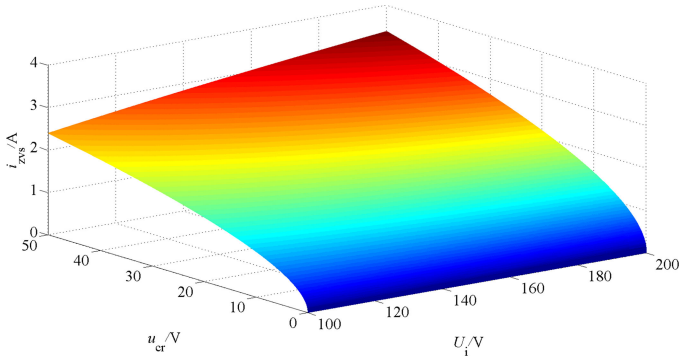

Fig. 16. Current $i_{\rm ZVS}$ of the diodes parallel with main switches.

respectively. It can be seen that the fluctuation of capacitor voltage has small influence on Δt_1 within certain range of output current. Moreover, increasing the coupling coefficient can reduce the time interval Δt_1. When voltage $u_{\rm cr}$ is treated as a constant, the only variable in formula (32) is $i_{\rm Lr1}$. $i_{\rm Lr1}$ (t_3) can be obtained by the formula given in the third mode. But the calculation will increase the burden of the digital system and consume more controller resources. By analyzing the operation of the soft-switching snubber cell, it is not necessary to calculated Δt_1 accurately. When the resonant inductance current $i_{\rm Lr1}$ decreases to zero under the effect of reverse voltage, $i_{\rm Lr1}$ is equal to zero for relatively long time interval. Therefore, auxiliary switches can realize ZCS when it turns off in this time intervals, and there is a relatively large margin of turn-OFF time. Based on the abovementioned analysis, the auxiliary switches can turned off before turning off the main switches to realize ZCS, and a small time interval $t_{\rm ch}$ should be reserved for charging the junction capacitance of the auxiliary switches.

5) The resonant capacitance and inductance have influence on the current stress of auxiliary devices, and the current stress of the auxiliary switch is analyzed, as shown in Fig. 15.

Large resonant inductance helps to suppress the current stress of auxiliary switching devices. However, the enough resonant current is needed because the excess of the resonance current from inductor current should be large enough to flow through the antiparallel diodes of main switches to realize ZVS. Therefore, the current stresses of the auxiliary circuit and operating state of soft switching should be simultaneously considered when designing the resonant capacitors and inductors.

6) Formula (33) is a necessary condition for ZVS. The resonant inductor $L_{\rm r1}$ $(L_{\rm r2})$ should have enough current to flow through the diodes parallel with main switches, so that the main switches can realize ZVS

$$(U_i + u_{\rm Cr1}(t_1) \Big/ \sqrt{2L_{r1}/C_s}\,) \sin\omega_0(t_2 - t_1) + I_0 \cos\omega_0(t_2 - t_1) \geq 0. \tag{33}$$

Initial resonant current I_0 is equal to zero in the proposed topology, and the effect of capacitor voltage $u_{\rm cr1}$ on current $i_{\rm ZVS}$ that flow through the diodes parallel to main switches is analyzed, as shown in Fig. 16.

Based on Fig. 16, capacitor voltage $u_{\rm cr}$ is very important for the realization of ZVS, which affects the operation of the soft switching. $u_{\rm cr}$ can help to resist the influence of dc voltage source on the resonance process, so that the resonant current can get higher amplitude at the end of discharge of resonant capacitors, which is key for the main switches to turn ON with ZVS.

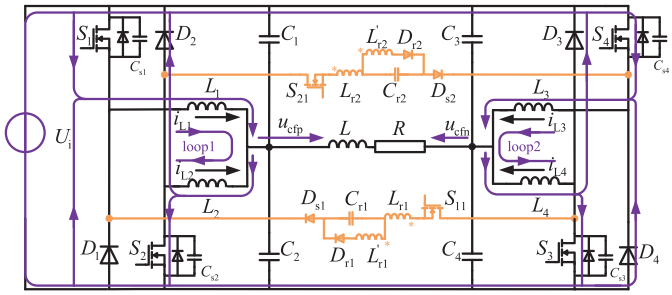

Fig. 17. Current circulations of ZVT DBFBI.

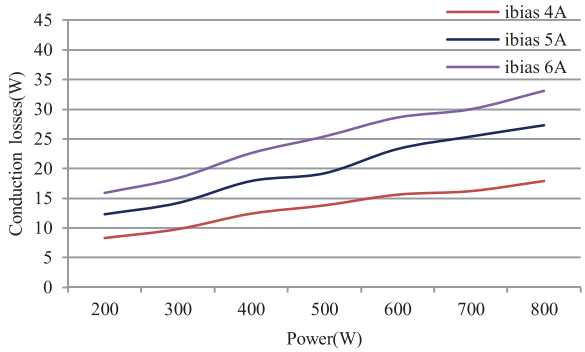

Fig. 18. Conduction losses of different bias currents.

B. Conduction Losses

In the full-cycle modulation, two circulation current loops exist in the converter. One is between the inductors L_1 and L_2, another is between the inductors L_3 and L_4. The corresponding circulation currents are shown in Fig. 17. Conduction losses mainly result from circulation current that affect the efficiency of the system. Considering the main operation state of the circuit, the conduction losses associated with two of the four current paths can be calculated as follows:

$$P_H = \left(\frac{1}{DT}\int_0^{DT}\left(\frac{1}{2}i_o + i_{bias} - \frac{(U_\mathrm{i}-u_\mathrm{cfp})DT}{2L_\mathrm{f}} + \frac{U_{\mathrm{i}-u_\mathrm{cfp}}}{L_\mathrm{f}}t\right)^2\right) + \frac{1}{D'T}\int_0^{D'T}\left(-\frac{1}{2}i_o + i_{bias} - \frac{(U_\mathrm{i}-u_\mathrm{cfn})D'T}{2L_\mathrm{f}} + \frac{U_\mathrm{i}-u_\mathrm{cfn}}{L_\mathrm{f}}t\right)^2 \cdot (R_{onm}+R_\mathrm{f})dt \quad (34)$$

$$P_{H'} = \left(\frac{1}{(1-D)T}\int_0^{(1-D)T} \times\left(\frac{1}{2}i_o + i_{bias} + \frac{(U_\mathrm{i}-u_\mathrm{cfp})DT}{2L_\mathrm{f}} - \frac{u_\mathrm{cfp}}{L_\mathrm{f}}t\right)^2 + \frac{1}{(1-D')T}\int_0^{(1-D')T} \times\left(-\frac{1}{2}i_o + i_{bias} + \frac{(U_\mathrm{i}-u_\mathrm{cfn})D'T}{2L_\mathrm{f}} - \frac{u_\mathrm{cfn}}{L_\mathrm{f}}t\right)\right) \cdot (R_{on\_dio}+R_\mathrm{f})dt, \quad (35)$$

where $R_{\mathrm{on\_dio}}$ represents the equivalent on-resistance of the diode. P_H and $P_\mathrm{H}{}'$ represent the conduction losses of the bridge, which include the switches S_4 and S_1. In (34) and (35), a large L_f and small i_{bias} can result in small conduction losses. By reducing bias current i_{bias}, the conduction losses of the system can be reduced as a result of reducing the circulation current. Therefore, in order to minimize conduction losses, i_{bias} should be designed as small as possible.

Similarly, the conduction losses of the other two current paths can be calculated as follows:

$$P_L = (R_{onm}+R_\mathrm{f})\left(\frac{1}{D'T}\int_0^{DT} \times\left(-\frac{1}{2}i_o + i_{bias} - \frac{u_\mathrm{cfp}D'T}{2L_\mathrm{f}} + \frac{u_\mathrm{cfp}}{L_\mathrm{f}}t\right)^2 + \frac{1}{DT}\int_0^{DT}\left(\frac{1}{2}i_o + i_{bias} - \frac{u_\mathrm{cfn}DT}{2L_\mathrm{f}} + \frac{u_\mathrm{cfn}}{L_\mathrm{f}}t\right)^2\right)dt \quad (36)$$

$$P_{L'} = \left(\frac{1}{(1-D')T}\cdot\int_0^{(1-D')T} \times\left(-\frac{1}{2}i_o + i_{bias} + \frac{u_\mathrm{cfp}D'T}{2L_\mathrm{f}} - \frac{U_\mathrm{i}-u_\mathrm{cfp}}{L_\mathrm{f}}t\right)^2 + \frac{1}{(1-D)T}\int_0^{(1-D)T}\left(\frac{1}{2}i_o + i_{bias} + \frac{u_\mathrm{cfn}DT}{2L_\mathrm{f}} - \frac{U_\mathrm{i}-u_\mathrm{cfn}}{L_\mathrm{f}}t\right)^2\right). \cdot (R_{on\_dio}+R_\mathrm{f})dt \quad (37)$$

According to the main operation of the circuit, the conduction losses consist of four parts

$$P_{cond} = P_H + P_{H'} + P_L + P_{L'} \quad (38)$$

The relation between conduction losses and bias current is shown in Fig. 18. By analyzing the conduction losses of the converter, it can be seen that bias current i_{bias} is an important factor affecting conduction losses. When the bias current reduced from 5 to 4 A under present power rating, the conduction loss will reduce about 10 W. Therefore, in order to reduce conduction losses, reducing the bias current through soft-switching is a reasonable solution. Furthermore, with the increase in switching frequency, the magnetic flux density B of the filter magnetic core will generally decrease. It means that the losses of inductors possibly do not increase with the increase within a certain range of switching frequency in ZVT DBFBI. The conduction loss is the main part of the losses, so the selection of switching frequency mainly considers reducing the conduction losses as much as possible and balancing the core losses of inductors.

TABLE I
COMPARISON OF CHARACTERISTICS OF SIMILAR CONVERTERS

Characteristics	THD	Efficiency	Complexity
ZVT DBFBI under full-cycle modulation	low	high	medium
DBFBI under full-cycle modulation	low	low	medium
DBFBI under half-cycle modulation	medium	high	low
FBI without dead-time compensation	high	high	low
FBI with dead-time compensation	medium	high	low

IV. CONVERTER FEATURES

The features of the proposed soft-switching converter are briefly summarized as follows.

1) All of the switches turn ON and OFF under ZVS or ZCS. All snubber diodes operate under soft-switching conditions.
2) The proposed soft-switching converter is compatible to decoupling control algorithm under full-cycle modulation, and it acts as a conventional PWM converter during the switching cycle.
3) The proposed topology has high quality output voltage and current.
4) A soft-switching operation of the converter is maintained during the full-load range.
5) The main switches are not subjected to additional voltage stress. The current stress of switches is within the allowable range.
6) Diodes (D_{s1}, D_{s2}) are inserted in the auxiliary circuit to eliminate the parasitic loop current and improve the efficiency of the circuit. This also ensures the normal operation of soft switching.
7) There is no additional component on the main converter current path.

The comparison of characteristics of similar converter is shown in Table I. ZVT DBFBI under the full-cycle modulation has the characteristics of high efficiency and low total harmonic distortion. The efficiency of ZVT DBFBI is higher compared with DBFBI under the full-cycle modulation.

Some values of the main components used in the ZVT dual-buck full-bridge converter are listed in Table II with reference to the manufacturer datasheets.

V. VERIFICATION AND EXPERIMENT RESULT

An 800-W prototype with a switching frequency of 100 kHz shown in Fig. 19 is used to verify the theoretical analysis of the proposed ZVT DBFBI.

The inductor current waveforms (i_{L4}, i_{L3}) and output current (i_o) are given in Fig. 20 with a switching frequency of 20 kHz. The inductor current waveforms (i_{L4}, i_{L3}) operating with a switching frequency of 100 kHz are shown in Fig. 21. Comparing Fig. 20 with Fig. 21, the envelope of inductor current will decrease as the switching frequency increases, and the bias current corresponding to 100 kHz switching frequency is about 1 A less than that corresponding to 20 kHz. Besides, 0.5 A is the margin. Thus, reducing the bias current can still ensure the inductor currents in the CCM when the inductor current envelope becomes smaller. Lower bias current can reduce the conduction losses, and the current stress of the main switches is also reduced. Due to high switching frequency and low oscillation of drain–source voltage resulting from snubber circuits, the THD of output current is somewhat improved by comparing Fig. 22 with Fig. 23.

TABLE II
VALUES OF MAIN COMPONENTS USED IN THE PROTOTYPE

Item	Symbol	Value
DC input voltage	U_i	120 V
Switching frequency	f_{sw}	100 kHz
Filter inductors	L_1, L_2, L_3, L_4	450 μH
Filter capacitors	C_1, C_2, C_3, C_4	1 μF
Resonant capacitors	C_{s1}, C_{s2}, C_{s3}, C_{s4}	3.3 nF
Storage capacitors	C_{r1}, C_{r2}	1 μF
Resonant inductors	L_{r1}, L_{r2}	5.78 μH
Coupled-inductors	L'_{r1}, L'_{r2}	5.70 μH
MOSFETs	S_1, S_2, S_3, S_4, S_{11}, S_{21}	IRFB4227
Diodes	D_1, D_2, D_3, D_4, D_{s1}, D_{s2}, D_{r1}, D_{r2}	IDH12SG60C

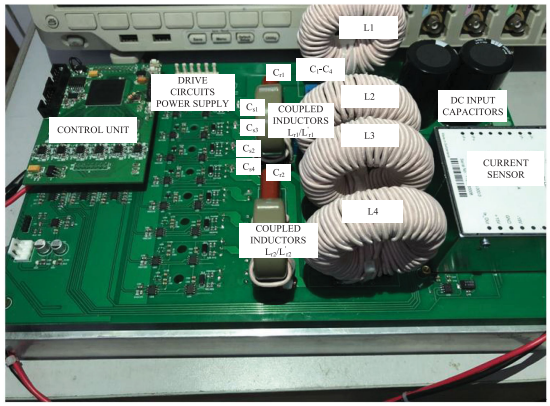

Fig. 19. Prototype of the proposed ZVT DBFBI.

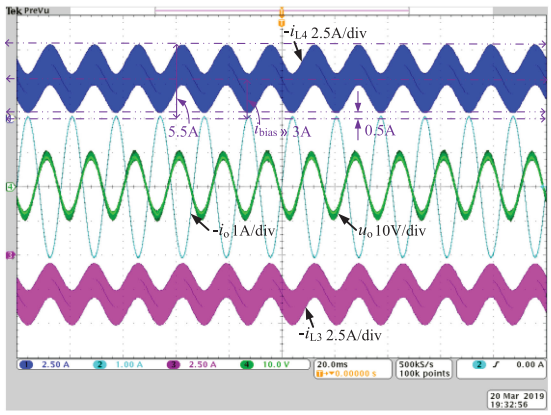

Fig. 20. Current waveforms of inductors (L_3, L_4) and output (i_o, u_o) with 20 kHz switching frequency.

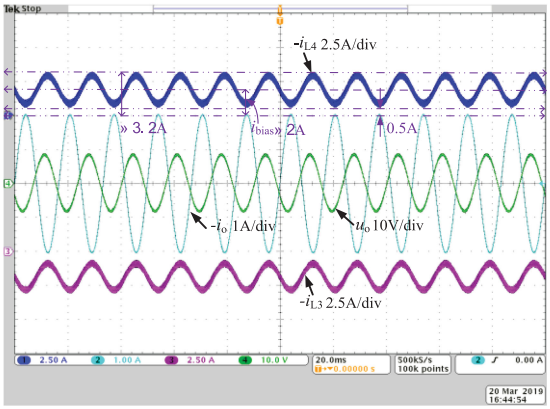

Fig. 21. Current waveforms of inductors (L_3, L_4) and output (i_o, u_o) with 100 kHz switching frequency.

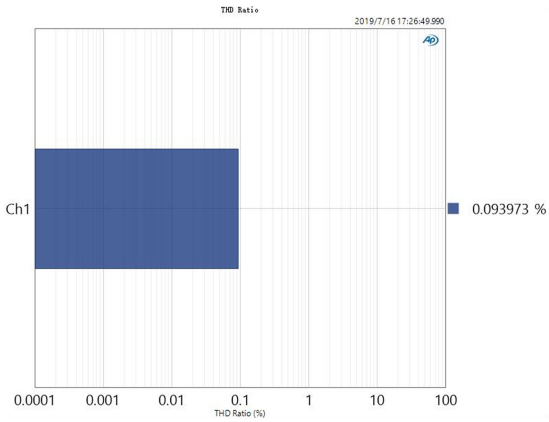

Fig. 22. THD of output current i_o under 20 kHz switching frequency.

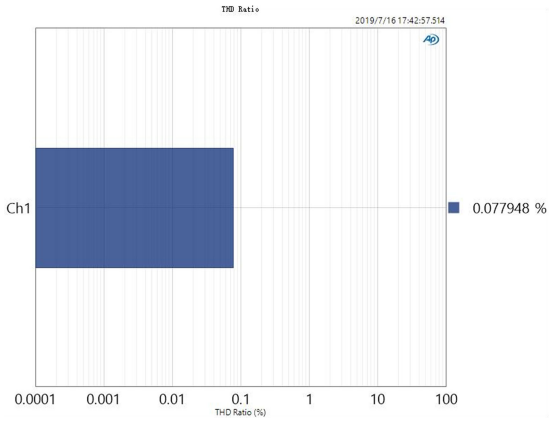

Fig. 23. THD of output current i_o under 100 kHz switching frequency.

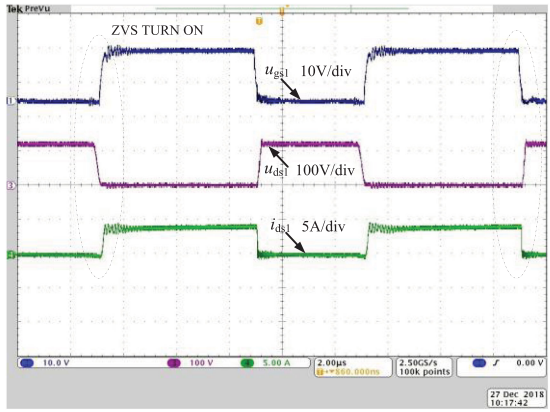

Fig. 24. Waveforms of u_{ds1}, u_{gs1}, and i_{ds1} under the full-cycle mode.

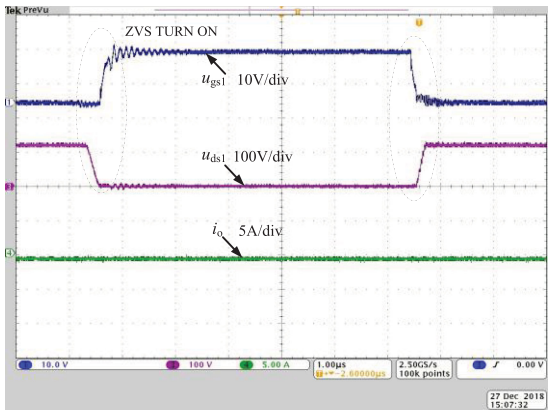

Fig. 25. Waveforms of u_{ds1}, u_{gs1}, and i_o with light load under the full-cycle mode.

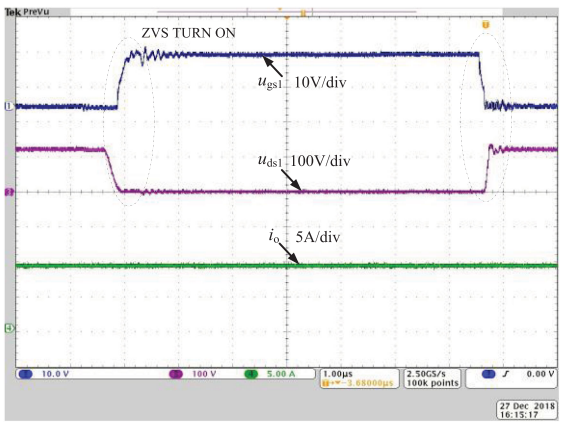

Fig. 26. Waveforms of u_{ds1}, u_{gs1}, and i_o with high load under the full-cycle mode.

Fig. 24 shows the soft-switching process of the main switch S_1. Before the gate turn-ON signal, the voltage (u_{ds1}) of the main switch has reached zero. After the gate turn-OFF signal, the voltage of the main switch gradually increases. When the inductor operates in the CCM, the voltage and current of the main switch S_1 have basically no overlap region.

The measured waveforms of the main switch (S_1) with control signals are given under high- and light-load conditions in Figs. 25 and 26. It is shown that ZVS turn-ON is achieved under both load conditions. The extra capacitance paralleled with junction capacitance can delay the turn-OFF process of the main switch. When the gate voltage decreases from u_{dr} to the

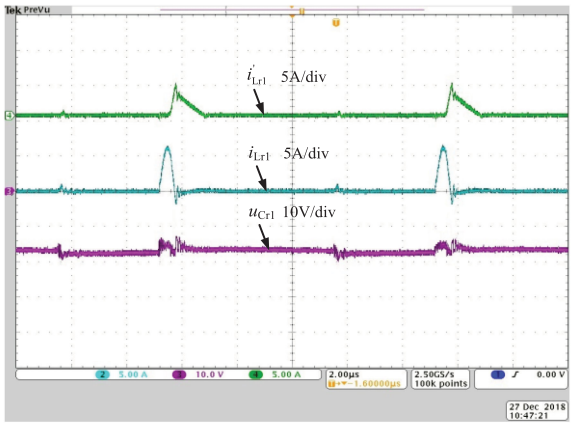

Fig. 27. Waveforms of currents i_{Lr1} and i'_{Lr1} and capacitor C_{r1} voltage.

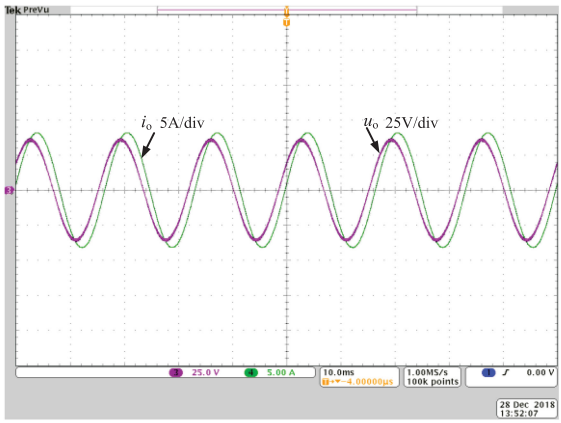

Fig. 29. Output waveforms under the full-cycle modulation.

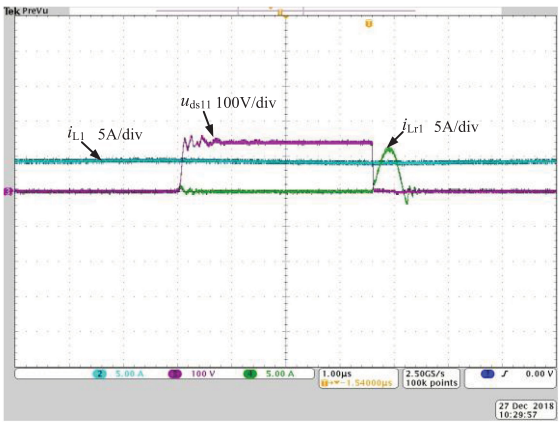

Fig. 28. Waveforms of voltages u_{ds11} and inductor currents i_{L1} and i_{Lr1}.

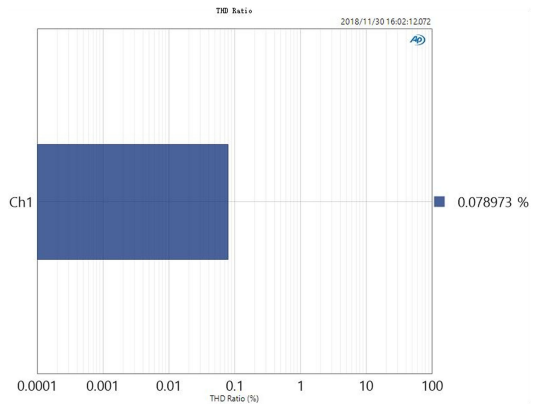

Fig. 30. THD analysis of output current i_o under the full-cycle modulation.

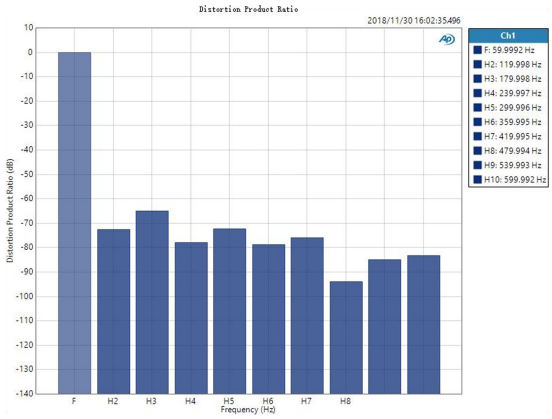

Fig. 31. Spectrum analysis of output current under the full-cycle modulation.

threshold voltage u_{th}, the drain-to-source voltage u_{ds1} is small, which can reduce the turn-OFF loss. There is no additional voltage stresses, and low electromagnetic interfere noise is achieved.

Some of the main waveforms (i_{Lr1}, i'_{Lr1}, u_{Cr1}, u_{ds11}, i_{L1}) are shown in Figs. 27 and 28 to verify the operation of soft switching. When the auxiliary branch turns on, the current i_{Lr1} of the inductor begins increasing, which makes the auxiliary switch (S_{11}) achieve ZCS. When the current of the auxiliary branch is equal to I_L, the resonant capacitor and inductor begin resonating and D_1 turns on with ZCS. It can be seen that $Lr1$ current falls to zero, and $L'r1$ current continues to fall linearly. Besides, the analysis of capacitance voltage u_{cr1} is consistent with the experimental result. Finally, i_{Lr1} and i'_{Lr1} drop to zero, and D_{s1} and D_{r1} turn OFF under ZCS. The switch S_{11} turns off under ZCS.

Fig. 29 shows waveforms of output voltages u_o and current i_o under coil load ($R = 3.7\ \Omega$, $L = 4.9$ mH). The output current amplitude is 8 A when the bus voltage is 120 V and the switching frequency is 100 kHz. Fig. 30 shows the THD ratio of output current under the full-cycle modulation, and the THD ratio is equal to 0.078973% measured by APX515. The spectrum of output current of ZVT DBFBI is shown in Fig. 31 with 60 Hz of fundamental frequency. With the increase in H ($H = 1, 2, 3, \ldots 10$), basically the amplitude A_H of harmonic gets smaller (A_H is the amplitude of H-order harmonic), and the former harmonic is higher than the latter. The amplitude of the harmonic is less than -60 dB. By comparison, the current shown in Fig. 32 has obvious zero-crossing distortion under half-cycle modulation with the same output current, and the corresponding voltage also has distortion. The THD of output current under the half-cycle modulation is equal to 4.108038%, which is shown in Fig. 33. The spectrum of output current is shown in Fig. 34 with 60 Hz of fundamental frequency. Moreover, the harmonic amplitude is

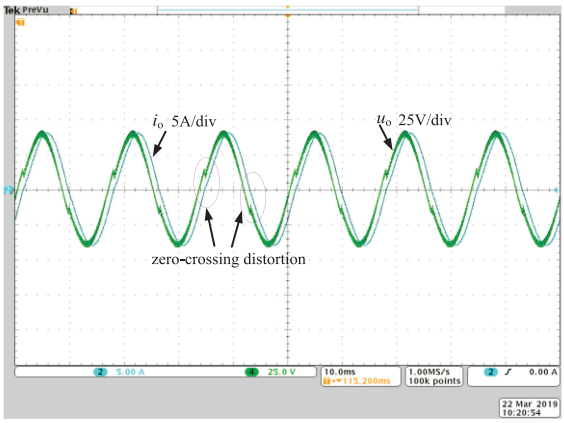

Fig. 32. Output waveforms under the half-cycle modulation.

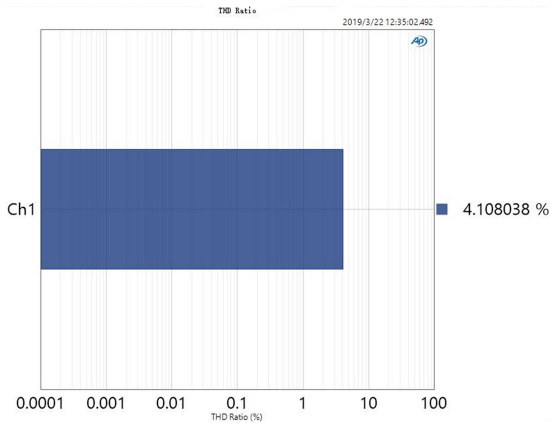

Fig. 33. THD analysis of output current i_o under the half-cycle modulation.

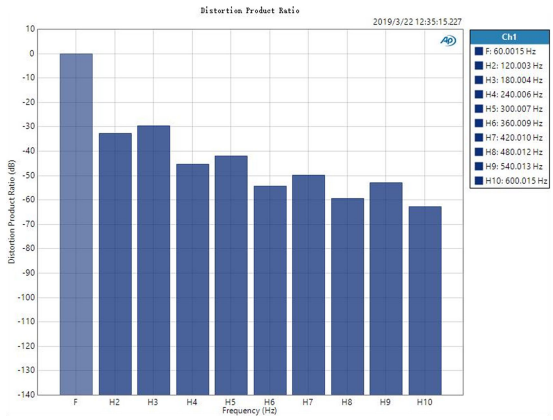

Fig. 34. Spectrum analysis of output current under the half-cycle modulation.

relatively large, and the amplitude $A_H\,(H = 1, 2 \ldots 5)$ of harmonic is more than -50 dB. Therefore, the ZVT DBFBI has the high performance of output voltage and current.

Figs. 35 and 36 show the load transient waveforms. From those results, it can be seen that the proposed inverter can follow the reference signal quickly and it can achieve fast dynamic response. Moreover, the overshoot of the system is about 15%.

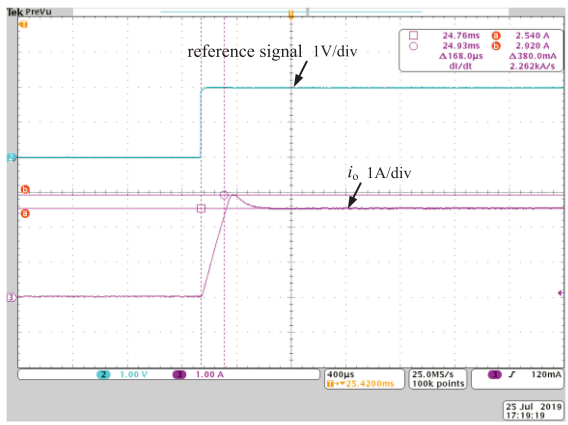

Fig. 35. Load transient waveforms under step reference signal.

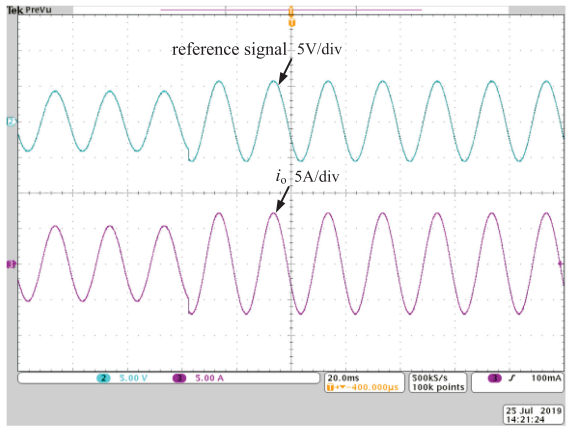

Fig. 36. Load transient waveforms under sinusoidal reference signal.

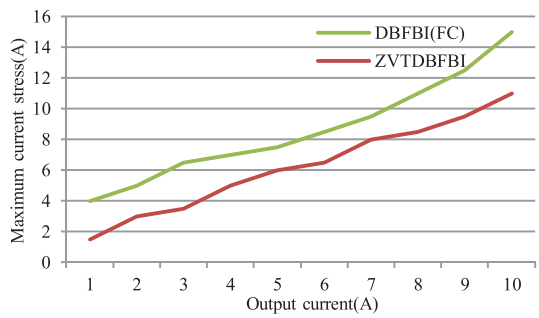

Fig. 37. Current stress comparison of ZVT DBFBI and DBFBI(FC).

Fig. 37 shows the comparison of the main switch current stresses of ZVT DBFBI and DBFBI under the full-cycle modulation [DBFBI (FC)]. The current stress of the ZVT soft-switching topology is less than that of the original topology that can be verified by Figs. 20 and 21. The minimum values are one-third of the original current stress.

Fig. 38 shows the difference between the efficiency of ZVT soft-switching DBFBI topology and DBFBI topology. The novel ZVT-DBFBI converter has a higher efficiency than the hard-switched converter. The input power is measured by

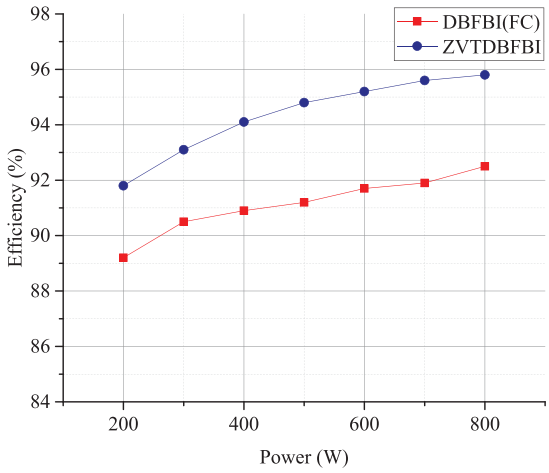

Fig. 38. Efficiency comparison of ZVT DBFBI and DBFBI (FC).

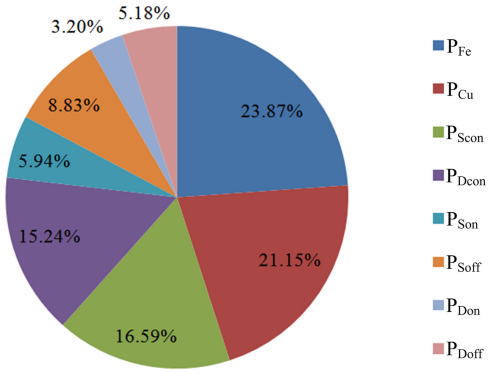

Fig. 39. Loss distribution of ZVT DBFBI.

PWR1201 MH, and the output power is measured by Tektronix 4034B. The efficiency of the converter is effectively improved, and the maximum efficiency is 95.8%. The distribution of losses of the proposed inverter is shown in Fig. 39. The core losses (P_{Fe}) and copper losses (P_{Cu}) are 23.87% and 21.15%, respectively, of the whole losses. Besides, the conduction losses (P_{Scon}, P_{Dcon}) and switching losses (P_{Son}, P_{Soff}, P_{Don}, P_{Doff}) of the power switches and diodes is 31.83% and 23.15% of the whole losses, respectively. Furthermore, the inverter losses are mainly conduction losses (P_{Scon}, P_{Dcon}, and P_{Cu}), which account for 52.98%.

VI. Conclusion

This article presents a ZVT soft-switching topology that inherits the advantages of the DBFBI with the full-cycle control method. Specifically, all of the switches and snubber diodes operate under soft-switching condition. Due to the high switching frequency, inductors can operate in the CCM under a small bias current, and the conduction losses are reduced. With the realizing of soft switching, the efficiency of the converter system is effectively improved. Moreover, the output voltage and current quality is advantageous due to the control algorithm compatibility and soft switching. The experimental results of the proposed ZVT DBFBI prototype correspond with the theoretical analysis.

However, the bias current still exists in the proposed topology, which limits the further improvement of efficiency. Anyway, the proposed topology is attractive in the high-precision applications. Despite the fact that the experimental results are based on the power rating of 800 W, the characteristics of ZVT DBFBI can be further embodied with the increase in power rating.

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