Power Losses and Current Distribution Studies by Infrared Thermal Imaging in Soft- and Hard-Switched IGBTs Under Resonant Load

Manuel Fernández, Xavier Perpiñà, Miquel Vellvehi, Oriol Aviñó-Salvadó, Sergio Llorente, and Xavier Jordà

***Abstract*—A test bench is proposed to study, at die-level, the power losses and current distribution in power devices. It is based on an infrared camera and a flexible half-bridge resonant inverter with a tunable resonance frequency $f_{\rm res}$. With this setup, the die surface temperature is acquired in steady state, while the device is under real operation. The power losses are derived from the temperature mean value averaged, first, over a few switching cycles and, then, across the die surface. By contrast, the current distribution is inferred from the spectral component of the surface thermal map at the switching frequency ($f_{\rm Sw}$). As a proof of concept, two case studies are reported considering 650 V-40 A insulated gate bipolar transistors (IGBTs) soft- and hard-switched within and outside the zero voltage switching condition. First, the power losses are analyzed under switching conditions representative of domestic induction heating applications ($f_{\rm res} = 29.6$ kHz) at $f_{\rm Sw} = 40$ kHz and $f_{\rm Sw} = 20$ kHz. Second, the power losses and local current distribution are investigated when $f_{\rm res} = 9.25$ kHz at $f_{\rm Sw}$ ranged from 8.91 to 9.51 kHz. Such results are assessed with power losses electrical measurements and simulations, obtaining a satisfactory agreement. Moreover, hot spots are identified as current crowding points at $f_{\rm Sw}$, whose location is fixed by the bonding wires attachment to the die and the device edge termination. As main benefits of this technique, a higher spatial resolution is achieved and problems related with noisy electrical measurements resulting from the insertion of the used probes or transducers, power circuit stray elements, or device packaging parasitics are avoided.**

***Index Terms*—Current distribution sensing by lock-in thermography, infrared (IR) imaging, insulated gate bipolar transistors (IGBTs), power losses measurement, thermal measurements.**

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I. Introduction

INDUSTRIAL power converters are designed to operate under rated conditions of voltage, current, frequency, and temperature. However, they are susceptible to change according to the load and operating environment, as observed in many applications [1], [2]. In this scenario, the power system designer should be able to identify the limitations of the power semiconductor devices when functioning within or outside of their nominal conditions to ensure an efficient and safe operation of the power converter. In this sense, failure mode and effects analysis (FMEA) assist to identify potential failure modes and provide useful information to evaluate the reliability at system level. In particular, power semiconductor devices are a key part to warrant the converter requirements in terms of performance, efficiency, and reliability. Usually, these devices are submitted to a high electro-thermal stress [1], which, in combination with an operation out of their nominal switching conditions, provokes system failure [2]. Under such situations, the devices reach destruction due to an overtemperature event or a local high electric field resulting from current crowding or focalization effects [1], which are manifested in both cases, on the die surface with a temperature increase. Therefore, an adequate method not only to measure the power devices local temperature under real operation [3], but also to sense the current distribution at the switching frequency, becomes crucial when designing a power converter for reliability. Apart from a selection criterion for thermal management purposes, this approach would be crucial to determining the most rugged devices for a given appliance or to redesigning their layout or packaging strategy to make them suitable for the considered scenario.

Unfortunately, solutions directly addressing such demands are not currently available. Nowadays, this problem is tackled gathering simulation and experimental approaches aiming at determining first, the device power losses and after, their associated compact thermal model (CTM). Traditionally, the device power losses are directly measured by electrical means, based on using current or voltage oscilloscope probes or other transducers [4]–[10]. The main strengths of this method are its ease of use and high repeatability, being suitable either for stationary or transient state measurements. However, there are drawbacks that

make them sometimes unsuitable [4], [10]. First, the noise due to electrical couplings resulting from the power circuit stray elements, the device packaging parasitics, or the insertion of either oscilloscope probes or transducers can significantly affect the sensitivity of digital instruments induced by a high rate of current (*dI/dt*) and/or voltage (*dV/dt*), which introduce radio frequency interference/electro-magnetic interference issues. Second, the delays of the different current and voltage oscilloscope probes or transducers impact on their accuracy, since phase shifts between channels, nonlinearities of analog-to-digital converters, sampling errors, or thermal drifts in their offset values take place during the measurements. Third, soft-switching techniques used for extremely reducing losses and electromagnetic emission make the electrical measurements of power losses difficult. Finally, when multiple chips or circuit components are connected in parallel, classical techniques do not always allow accessing to an individual die or circuit component. For instance, this is the case when multiple insulated gate bipolar transistors (IGBTs) are connected in parallel or when the dissipation of a snubber capacitor is intended to be monitored. Therefore, such nonlocal strategies can be invasive or/and unsuitable. One of the less invasive solutions is the use of accurate calorimeters [10]–[14], inspired on those employed for power converters efficiency evaluation [15]–[21]. Although their sensitivity and accuracy have been improved at cost of lengthening the acquisition time, they require slightly modifying the converter geometry without locally accessing to the die (die-level measurement). In such cases, the local temperature extraction in the die could even be useful for validating CTMs commonly used for design purposes [22], especially in highly efficient converters using soft-switching driving strategies as in induction heating (IH) appliances [12]–[14]. In conclusion, a direct access to the chip surface for temperature monitoring with short acquisition times is mandatory to offer a solution to the aforementioned needs and reduce the design time. Besides, such an approach is useful for circuit-level simulations to investigate the device packaging and power circuit parasitics interactions.

In response to this, this article proposes an experimental approach to study, locally accessing to the die, the power losses and current distribution in IGBTs used in resonant soft-switching power converters. Such circuits connect in parallel an IGBT, a free-wheel diode, and a snubber capacitor (C_{snub}), making the power losses determination in each component difficult. Besides, for a given pair of switching (f_{Sw}) and resonance (f_{res}) frequencies, the IGBTs have been studied when working within and outside the zero voltage switching (ZVS) condition. Operating at ZVS condition means that the IGBT is gated on just as its corresponding free-wheel diode is under conduction state [23], [24]. By contrast, when the device is commutated outside the diode conduction window, i.e., before C_{snub} is fully discharged and diode conduction starts, or after diode conduction finishes; a commutation outside ZVS takes place. Eventually, this occurs just by setting $f_{\mathrm{Sw}} < f_{\mathrm{res}}$, when dead times and C_{snub}'s with sufficiently high values are used [23], [24]. From a reliability point of view, the influence of the ZVS condition on the current distribution within an IGBT is of concern. Switching them outside ZVS condition can yield to more degrees-of-freedom in the converter design, but resulting into a local overstress in the device as the turn ON and conduction power losses can be significantly increased [25], [26]. This fact provokes a higher current concentration at the weakest spots of the device, manifested as hot spots. To inspect all this, a half bridge has been designed to set the semiconductor power device under nominal operation conditions (i.e., high voltage and current levels). The thermal field is acquired on top of the die surface with an infrared (IR) thermographic system that makes possible thermal measurements at the die-level. Among all existing techniques for noninvasive thermal measurements [21], [22], [27]–[33], IR thermography [34]–[36], combined with a lock-in detection strategy (IR Lock-In Thermography (IR-LIT)) [31], has been selected because of its commercial availability, high thermal resolution (below 1 m°C) and high rejection to noise and thermal boundary conditions [37]–[43]. With this IR system, power losses and current distribution at the die-level can be carried out as follows. To derive the power losses, the junction temperature (T_{j}) is determined as the mean value of temperature averaged first per switching period and after across the die surface. In contrast, the surface current distribution is detected by lock-in strategies [31], which extract the temperature map spectral component at f_{Sw}. In comparison to prior works, the proposed approach differs from [44] to [46] in the test circuit and intended scope. Here, the device is studied under real operation conditions, rather than reporting an IGBT selection criterion or an FMEA on repetitive stressful switching conditions for safe operating area definition. Therefore, this article focuses on reproducing the regular operating conditions of a power device in a real power converter, i.e., current and voltage ratings at a given f_{Sw}, with a specifically designed high voltage circuit. Thanks to the proposed approach, the power device can be studied at die-level in a controlled way in the lab. Moreover, when multiple chips are encapsulated together, e.g., the case of an IGBT copackaged with a free-wheeling diode, all dies can be simultaneously measured, depending on the field of view of the lens employed with the camera. This provides an added value to the proposed approach and can speed up the acquisition process. According to all stated, the article is organized as follows. Section II describes all the details of the proposed approach, also including how a window is opened in the device package to have visual access to the dies. Section III presents the electro-thermal modeling of the test bench. Section IV reports on both the power losses measured and current distribution analyzed at f_{Sw} in a soft- and hard-switched IGBT when operated within or outside the ZVS condition. Finally, Section V draws the main conclusions.

II. Approach, Test Bench and Device Preparation

A. Approach Theoretical Aspects

The methodology followed to extract, at die-level, power losses (P_{gen}) and current distribution at f_{Sw} exploits the Joule effect inherent to power devices operation. On the one hand, P_{gen} is the sum of the power dissipated per switching period in on-state (P_{On}) and the transitions from on to off and viceversa (P_{Sw}). According to a reference temperature (T_{Ref}), T_{j} and P_{gen}

are related through the thermal impedance $Z_{\mathrm{th(j-Ref)}}$ as [41]

$$\Delta T_{\mathrm{(j-Ref)}}(t) = \int_0^t P_{\mathrm{gen}}(\tau)\left(\frac{dZ_{\mathrm{th(j-Ref)}}(t-\tau)}{dt}\right)\cdot d\tau \quad (1)$$

where $\Delta T_{\mathrm{(j-Ref)}}(t) = T_{\mathrm{j}}(t) - T_{\mathrm{Ref}}(t)$. In (1), T_{j}, T_{Ref}, and P_{gen} represent die mean values. Thus, known $\Delta T_{\mathrm{(j-Ref)}}(t)$ and $Z_{\mathrm{th(j-Ref)}}(t)$, P_{gen} (t) is thus inferred by solving (1) in steady state, i.e., $P_{\mathrm{gen}} = P_{\mathrm{gen}}(t \to \infty) = \Delta T_{\mathrm{(j-Ref)}}(t \to \infty)/R_{\mathrm{th(j-Ref)}}$, where $R_{\mathrm{th(j-Ref)}}$ corresponds to the thermal resistance and relates with $Z_{\mathrm{th(j-Ref)}}(t)$ as $R_{\mathrm{th(j-Ref)}} = Z_{\mathrm{th(j-Ref)}}(t \to \infty)$. To simplify the extraction of P_{gen}, it is possible to experimentally fix an isotherm at the T_{Ref} measurement location when $t \to \infty$ (see Section II-C), which means that $T_{\mathrm{j}}(t \to \infty)$ and $T_{\mathrm{Ref}}(t \to \infty)$ are constants different to zero. Under steady state conditions, the IR camera measures a $T_{\mathrm{j}}(\mathrm{x},\mathrm{y},t)$ and for P_{gen} it is required the mean value of $T_{\mathrm{j}}(\mathrm{x},\mathrm{y},t)$ averaged, first, over a certain number n_{c} of switching cycles $(n_{\mathrm{c}}/f_{\mathrm{Sw}})$ and, after, across the die surface S with a total area A, i.e., $T_{\mathrm{j}} = T_{\mathrm{j}}(t \to \infty) = f_{\mathrm{Sw}}/(n_{\mathrm{c}}A)\int_0^{n_{\mathrm{c}}/f_{\mathrm{Sw}}} dt \iint_{\mathrm{S}} dS\, T_{\mathrm{j}}(\mathrm{x},\mathrm{y},t)$. To do this, IR acquisitions are performed with a camera integration time (t_{int}) considering several switching periods $(n_{\mathrm{c}}/f_{\mathrm{Sw}})$. By this procedure, notice that P_{On} and P_{Sw} can be inferred from P_{gen} by appropriately configuring the specifically designed test circuit described in Section II-B, in such a way that, first, $P_{\mathrm{gen}} = P_{\mathrm{On}} + P_{\mathrm{Sw}}$ and, after, $P_{\mathrm{gen}} = P_{\mathrm{On}}$. As a notation to distinguish between electrical and thermal results, P_{gen}, P_{On}, and P_{Sw} are, respectively, referred to as $P_{\mathrm{gen}}^{\mathrm{Elec}}$, $P_{\mathrm{On}}^{\mathrm{Elec}}$, and $P_{\mathrm{Sw}}^{\mathrm{Elec}}$ when determined by electrical means. Conversely, when thermally inferred, P_{gen}, P_{On}, and P_{Sw} are designated as $P_{\mathrm{gen}}^{\mathrm{IR}}$, $P_{\mathrm{On}}^{\mathrm{IR}}$, and $P_{\mathrm{Sw}}^{\mathrm{IR}}$, respectively.

On the other hand, the die-level current distribution representative of the switching behavior can be studied and inferred from the detection and location of the hot spots generated by current crowding or focalization problems at f_{Sw}, since a nonhomogenous current distribution on top of the device occurs at the areas of localized lowered resistance or in areas where the field strength is concentrated, especially at the vicinity of the chip top contacts with the bonding wires (lower resistance/impedance case) [47], [48] and/or over the device internal PN junctions (high electric field case) [1]. In our case, such phenomena affect differently depending on the physical processes taking place when the spectral components at f_{Sw} of P_{On} $(P_{\mathrm{On},f_{\mathrm{Sw}}})$ or P_{Sw} $(P_{\mathrm{Sw},f_{\mathrm{Sw}}})$ are produced. Thus, $P_{\mathrm{On},f_{\mathrm{Sw}}}$ is related with current focalization around the bonding wires contact on top of the device, while $P_{\mathrm{Sw},f_{\mathrm{Sw}}}$ originates from the charge removal of PN junctions to support voltage, which mainly occurs at the device edge terminations. Consequently, several hot spots appear at the device top surface and superpose to the mean or dc value of the surface thermal field (T_{S}), giving rise to a surface thermal field spectral component at f_{Sw} $[\Delta T_{\mathrm{surf}}(\vec{r},\vec{r}_n,t,f_{\mathrm{Sw}})]$ as [42]–[46], [49]

$$\begin{aligned}\Delta T_{\mathrm{surf}}&(\vec{r},\vec{r}_n,t,f_{\mathrm{Sw}})\\ &= |P_{\mathrm{gen},f_{\mathrm{Sw}}}| \times \sum_{n=1}^{N}\iint_{S_{HS,n}} dS_{HS,n}\\ &\quad\times\left[a_n \times \frac{C}{|\vec{r}-\vec{r}_n|}\times e^{-\phi_{\tau,n}}\times\cos\left(2\pi f_{\mathrm{Sw}}t - \phi_{\tau,n} - \frac{\pi}{4}\right)\right]\end{aligned} \quad (2)$$

where $|\vec{r}-\vec{r}_n|$ is the distance between each location $\vec{r}$ from the coordinate origin of the thermal field and each hot spot location $(\vec{r}_n)$, $dS_{HS,n}$ is the differential of surface of the n-th hot spot, and C is a boundary condition constant. $|P_{\mathrm{gen},f_{\mathrm{Sw}}}|$ is the amplitude of the spectral component of the total active power dissipated at f_{Sw} by all hot spots, and obeys $|P_{\mathrm{gen},f_{\mathrm{Sw}}}| = |P_{\mathrm{On},f_{\mathrm{Sw}}} + P_{\mathrm{Sw},f_{\mathrm{Sw}}}|$. a_n corresponds to the fraction of $|P_{\mathrm{gen},f_{\mathrm{Sw}}}|$ dissipated by each hot spot. $\phi_{\tau,n}$ is the thermal phase lag related with the heat propagation around a nth hot spot, defined as $\phi_{\tau,n} = |\vec{r}-\vec{r}_n|/\rho$. ρ is the thermal diffusion characteristic length at f_{Sw} and writes as $\rho = \sqrt{D(\pi f_{\mathrm{Sw}})^{-1}}$ where D is the thermal diffusivity of the media. From its comparison to the die thickness h, ρ is one of the main parameters in such measurements. It establishes when the external boundary conditions do not affect IR-LIT measurements ($\rho < h$, thermally thick condition) [49], [50], also confining the thermal field around the hot spots (spatial resolution improvement). Such an approach is supported by the fact that, under working conditions, the current, dissipated power and thermal field are periodic functions of time, which allow their Fourier expansion. Concretely, this analysis focuses on the detection of the thermal field spectral component at f_{Sw}; which will provide spatial information about the same spectral component of current and dissipated power.

For the detection of such surface hot spots at f_{Sw}, lock-in strategies are commonly performed, as they allow recovering under thermal steady state these low thermal signals in the frequency domain [31]. One of them is the two channel lock-in correlation. As presented in [31], it consists of multiplying a signal $F(t)$ containing a broad frequency information

$$\begin{aligned}F(t) &= F_0 + A_j\sin(2\pi f_j t + \varphi_j)\\ &\quad + \sum_{l\neq j}^{\infty} X_n \sin(2\pi f_l t + \varphi_l)\end{aligned} \quad (3)$$

by a reference signal in phase $[K^{0^\circ}(t)]$ and quadrature $[K^{90^\circ}(t)$, $+90^\circ$ in advance of $K^{0^\circ}(t)]$ with respect to j-th spectral component of $F(t)$ at a frequency f_j

$$K^{0^\circ}(t) = 2\sin(2\pi f_j t) \quad (4)$$

$$K^{90^\circ}(t) = 2\cos(2\pi f_j t) \quad (5)$$

and integrating the result to carry out a low-pass filtering. The in-phase (S^{0°) and quadrature (S^{90°) components of $F(t)$ at f_j are obtained as follows [31]:

$$S^{0^\circ} = \frac{1}{t_{\mathrm{acq}}}\int_0^{t_{\mathrm{acq}}} F(t)\,K^{0^\circ}(t)\,dt = A_j\cos(\varphi_j) \quad (6)$$

$$S^{90^\circ} = \frac{1}{t_{\mathrm{acq}}}\int_0^{t_{\mathrm{acq}}} F(t)\,K^{90^\circ}(t)\,dt = A_j\sin(\varphi_j) \quad (7)$$

where A_j and φ_j are the amplitude and phase lag of the harmonic component of $F(t)$ corresponding to f_j, respectively. X_l and φ_l are the amplitude and phase lag of the other harmonic components of $F(t)$ corresponding to f_l. F_0 is the dc level of $F(t)$. As it can be inferred from (6) and (7), F_0 and all other

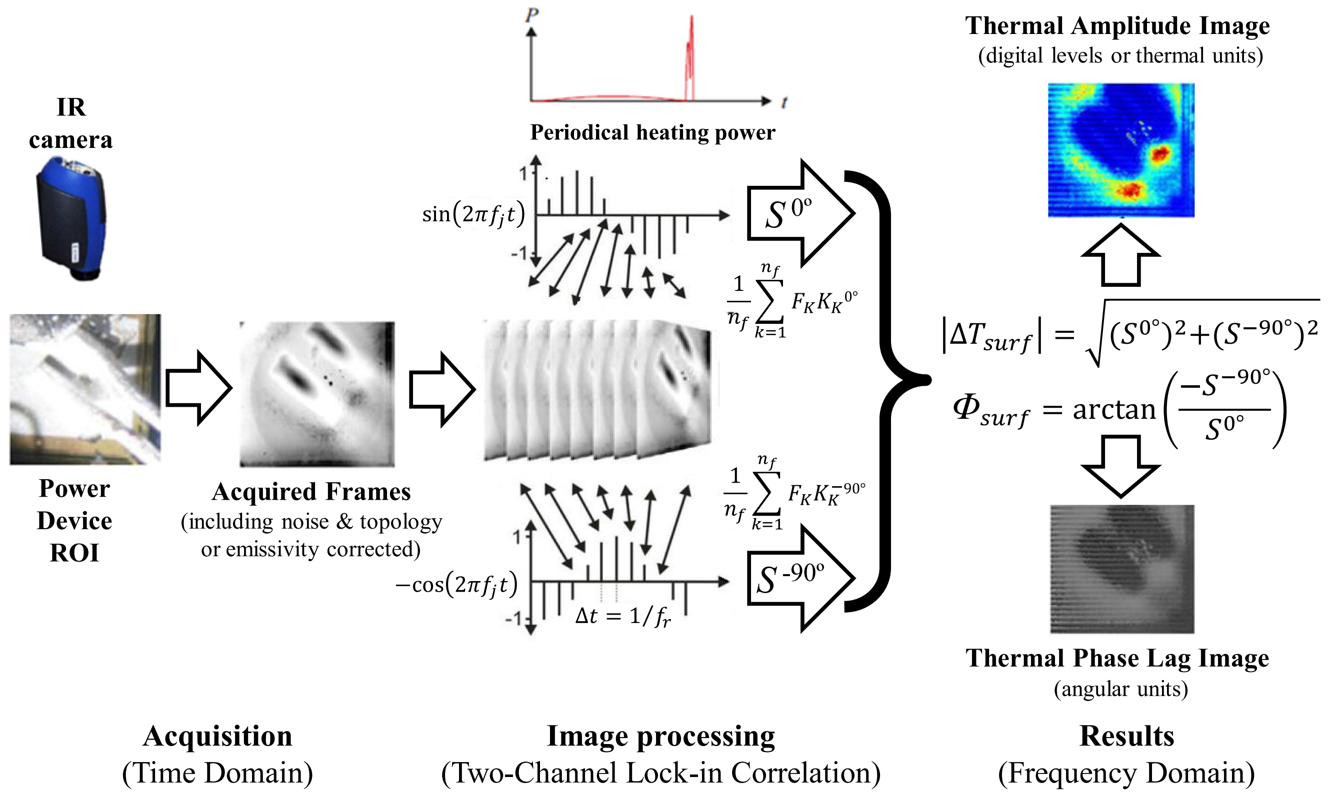


Fig. 1. Procedure followed for the extraction of $|\Delta T_{\mathrm{surf}}|$ and Φ_{surf} at f_{Sw} after sampling n_{f} thermal images under a thermal steady state, based on the method described in [31] and [51].

harmonics different to f_j are suppressed in $S^{0°}$ and $S^{90°}$ when a high acquisition time (t_{acq}) is considered (i.e., $t_{\mathrm{acq}} \gg 1/f_j$). Therefore, A_j and φ_j can be derived from $S^{0°}$ and $S^{90°}$ [31]:

$$A_j = \sqrt{(S^{0°})^2 + (S^{90°})^2} \tag{8}$$

$$\varphi_j = \arctan\left(\frac{S^{90°}}{S^{0°}}\right). \tag{9}$$

To have a satisfactory lock-in correlation, measuring a defined phase lag is required. In other words, reliable lock-in detection is performed when no phase lag noise occurs. In the case of a signal sampled or discretized in time $K(k)$ as the camera does, $S^{0°}$ and $S^{90°}$ writes as follows [31]:

$$S^i = \frac{1}{n_{\mathrm{f}}} \sum_{k=1}^{n_{\mathrm{f}}} F(k)\, K^i(k) \tag{10}$$

where i refers to 0° or 90°, and n_{f} is the number of samples acquired. This relationship is used in our case to determine the thermal amplitude $|\Delta T_{\mathrm{surf}}|$ and phase lag Φ_{surf} of $\Delta T_{\mathrm{surf}}(\vec{r}, \vec{r}_n, t, f_{\mathrm{Sw}})$ at f_{Sw}, as depicted in Fig. 1 [31], [51]. Fig. 1 summarizes the two channel lock-in approach followed by the IR-LIT system, relating the theory previously presented with the discrete case when the sampling frequency is lower than $1/f_{\mathrm{Sw}}$ (oversampling case). In this case, the quadrature correlation is performed with a phase shift of −90°, instead of 90°. Notice that in IR-LIT measurements, two interesting results deserve to be stressed. First, $|\Delta T_{\mathrm{surf}}|$ and Φ_{surf} have thermal and angular units, respectively. Second, to appropriately determine the $|\Delta T_{\mathrm{surf}}|$ value, an emissivity correction is required (see Fig. 1) [31], whereas in the case of Φ_{surf}, it is unnecessary, as it is calculated by the ratio $S^{0°}/S^{-90°}$ (see Fig. 1) and Φ_{surf} is not modulated by the surface emissivity [31]. Thus, Φ_{surf} is a good indicator for detecting $\Delta T_{\mathrm{surf}}(\vec{r}, \vec{r}_n, t, f_{\mathrm{Sw}})$, i.e., thermal signal at f_{Sw}. As a main restriction for $|\Delta T_{\mathrm{surf}}|$ and Φ_{surf} detectability, f_{Sw} must be within the bandwidth of the IR-LIT system, and ensure certain levels of signal to noise ratio (S/N) at the camera output [52]. In the present case, t_{int} establishes both conditions, as it fixes, according to the Nyquist theorem, the sampling frequency of the sensed IR radiation [i.e.,: $t_{\mathrm{int}} < 1/(2f_{\mathrm{Sw}})$] and the images S/N [52]. Moreover, the approach for image acquisition will be phase-locked with the devices excitation to avoid phase noise and performed by undersampling at a frame rate (f_{r}) nonmultiple of f_{Sw}, to allow the recovery of several periods and properly reconstruct the product $F(k)K^i(k)$ discretized for a given $1/f_{\mathrm{Sw}}$. Finally, the used criteria for hot spot location is to determine the position where a local maximum, in $|\Delta T_{\mathrm{surf}}|$, and a well-defined Φ_{surf} are concurrently observed [31].

B. Test Circuit Presentation and Capabilities

Fig. 2 depicts the schematic of the test circuit specifically designed for the intended experiments at high voltage and current ratings, and implemented on a printed circuit board (PCB).

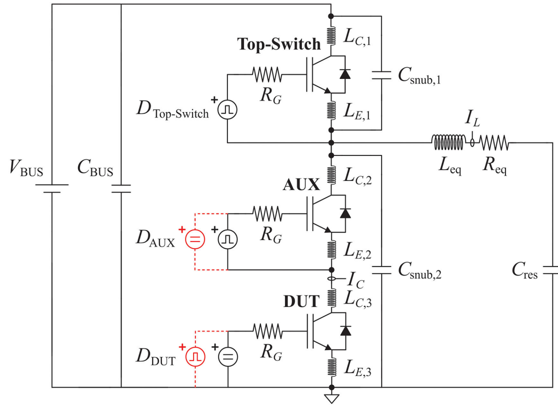


Fig. 2. Schematic of the test circuit designed for $P_{Sw} = 0$ (black) and $P_{Sw} \neq 0$ (red) in the DUT, considering its parasitic elements.

Fig. 2 also highlights the IGBTs parasitic collector $(L_{C,i})$ and emitter $(L_{E,i})$ inductances used in Sections III-B and IV-A. This circuit is based on a half-bridge resonant inverter with a flexible resonant load, formed by a resistor (R_{eq}), capacitor (C_{res}) and inductor (L_{eq}). In this configuration, a single device is located on the upper branch (Top-Switch) and gate-controlled with a driver ($D_{Top\text{-}Switch}$), while the device under test (DUT) is connected in series to an IGBT on the lower branch acting as an auxiliary switch (AUX). Depending on the driver settings of the DUT (D_{DUT}) and AUX (D_{AUX}), this circuit allows adjusting, in the DUT, $P_{Sw} = 0$ (i.e., $P_{gen} = P_{On}$) or $P_{Sw} \neq 0$ (i.e., $P_{gen} = P_{On} + P_{Sw}$). For $P_{Sw} = 0$ measurements, D_{DUT} keeps the DUT at a constant gate-emitter voltage (V_{GE}), while D_{AUX} drives the AUX with a V_{GE} square waveform (see Fig. 2, black color). Conversely, $P_{Sw} \neq 0$ measurements interchange the drivers' role, i.e., the DUT is switched, while AUX remains under conduction state (see Fig. 2, red color). From the comparison of both results, P_{Sw} can be inferred. Additionally, this circuit presents, on the PCB, some monitoring points for electrical measurements in the DUT and resonant load (see Fig. 2). Together with a current transformer, the DUT's collector current (I_C) and load current (I_L) have been monitored with a Tektronix Hall probe TCP202 and a Pearson current monitor model 2877, respectively. As for the rest of electrical parameters, the DUT collector-emitter voltage (V_{CE}) and V_{GE} have been acquired with Tektronix voltage probes P5050. All such probes are connected to a Tektronix TDS5034B oscilloscope, which allow finally deriving P_{gen}^{Elec}, P_{On}^{Elec}, and P_{Sw}^{Elec}.

Several elements can be configured in this circuit to provide a higher versatility for addressing different case studies. The BUS voltage (V_{BUS}) can be ranged up to 800 V. The BUS capacitor (C_{BUS}) can be also modified, as its discharge allows reaching the current levels required for a given case study. The snubber capacitors $(C_{snub,i})$ can be modified for hard- or soft-switching studies. The gate resistors (R_G) and drivers can be set to control the IGBTs under different switching conditions. Especially, the drivers allow easily adjusting the amplitude and polarity (unipolar/bipolar) of the device control gate voltage. Finally, the resonant load can be tuned within the following ranges: $R_{eq} = \{3$ to $6\ \Omega\}$, $L_{eq} = \{24$ to $274\ \mu H\}$, and $C_{res} = \{1$ to $4.5\ \mu F\}$. Consequently, f_{res} and I_L (up to 50 A) can be easily set. Even, this load can be transformed into a pure inductive or resistive one, commonly employed in other switching tests. Such degrees of freedom permit reproducing operation conditions of several final applications corresponding to medium voltage range, e.g., those of domestic IH. In this case, R_{eq} and L_{eq} should be set according to the inductor-recipient interaction, which fix an equivalent typical power factor in the range of 0.40–0.60 for commercial recipients. These values are based on the quality factor of a series R_{eq}-L_{eq} load [53]. Then, the power supplied to the load at $V_{BUS} = 300$ V is controlled by modifying f_{Sw}, with respect to f_{res}, in the range of 35–80 kHz.

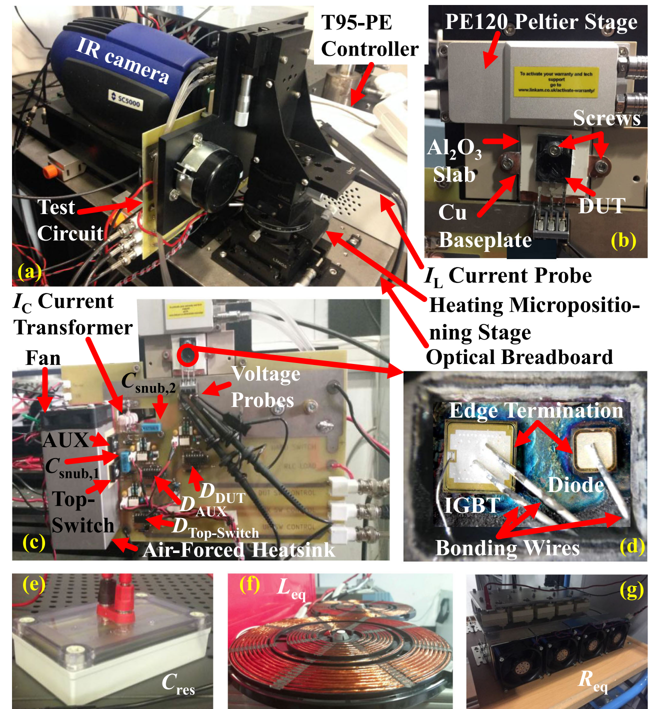


Fig. 3. (a) Experimental test bench for die-level analysis. (b) Heating part of the heating micropositioning stage. (c) Test circuit mounted on the heating micropositioning stage. (d) Detailed view of the DUT, and the flexible resonant load: (e) C_{res}; (f) L_{eq}; and (g) R_{eq}.

C. Test Bench Description

Fig. 3 depicts the main parts of the test bench developed to extract the power losses and to study the current distribution at die-level. Fig. 3(a) and (b) present, placed on top of an optical breadboard, the IR camera, the test circuit described in Section II-B, and a heating micropositioning stage [54]. The IR measurements have been performed using a FLIR SC5500 camera with an internal lock-in module and a set of microscopic lenses with lateral resolutions down to 6 μm, in particular, lenses G1X and G3X are used in the tests. It should be noted that for LIT measurements, the IR-camera acquisition must be synchronized with the IGBT driving by using two waveform generators in a phase-locked configuration. An Agilent 33522A, presenting two output channels, is used to control the switching devices of the

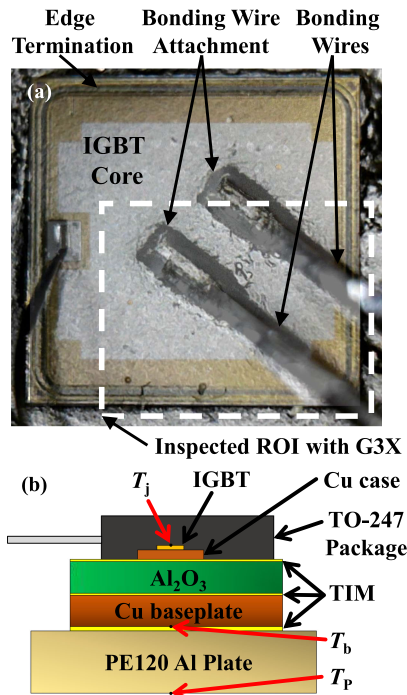


Fig. 4. (a) Top view of the IGBT die, highlighting the bonding wires, their attachment, the edge termination, and the area inspected with G3X. (b) Device layers structure including the TO-247 package, TIM, Al_2O_3 thin slab, Cu baseplate, and Al plate of PE120.

test circuit, supplying to the drivers a 5-0 V square waveform at the f_{Sw} values for the intended lock-in detection indicated in Section IV.B. During IR measurements, an Agilent 33220A is used to synchronize the acquisition of the camera with the Agilent 33522A by means of a sinusoidal waveform. To do this, the Agilent 33522A and 33220A are phase-locked through their rear-panel connections [55]. As a result of this, both signals are at the same frequency and phase-locked, i.e., maintaining a constant phase offset from each other without any phase drift.

As for the used lenses, several aspects should be taken into account. When measuring T_{j} for power losses extraction, the spatial resolution is not a main requirement and monitoring both the IGBT and diode is mandatory. This can be performed with a microscopic lens (G1X), which shows the highest field of view and worst spatial resolution (30 µm) of all available lenses, being possible to inspect the window opened in the device package of Fig. 3(d). Conversely, for current distribution analyses at die-level, a higher spatial resolution is required, at least 10 µm, to detect hot spots due to current distribution. For this reason, a smaller region of interest (ROI), as shown in Section IV-B and Fig. 4(a), has been analyzed. Fig. 4(a) depicts a top view of the IGBT die, jointly with the bonding wires, their attachment to the emitter top metallization, the edge termination, and the ROI. The ROI has been fixed around the bonding wire attachment areas close to the device right lower corner, as the current is focused there for its extraction through the bonding wires [see Fig. 4(a)]. For this reason, a FLIR microscope lens (G3X) has been used.

As for the camera settings, all IR images have been acquired at $f_{\mathrm{r}} = 376$ Hz to minimize the read-out noise, whereas different values have been considered for the rest of the acquisition parameters depending on the analysis performed. For power losses measurements, t_{int} is kept at 262 µs to determine the mean value over ten switching cycles (see Section IV-A, $f_{\mathrm{Sw}} = 40$ kHz and $n_{\mathrm{c}} = 10$), while, for current distribution studies at f_{Sw} (i.e., IR-LIT measurements), t_{int} is set for 49 µs according to the Nyquist condition $t_{\mathrm{int}} < 1/(2\, f_{\mathrm{Sw}})$ and a total of 5×10^4 IR images have been acquired at each test ($t_{\mathrm{acq}} = 134$ s) (see Section IV-B, $f_{\mathrm{Sw}} < 10$ kHz). In summary, all such values are selected since they are the highest f_{r}, the shortest t_{int}, and the smallest image number n_{f} to rapidly achieve a proper S/N in the final image. With regards to the aspects related with camera safety or external IR reflections mitigation, any special approach has been performed aside from coating the chip surface with a high emissivity material, as described further on. Neither the camera nor the lens have been protected by any optical window when performing the IR measurements; as the V_{BUS} voltage ratings involved in the tests avoid electric arcing between the device and the camera. On the other hand, IR radiation coming from the surroundings have not altered the performed measurements, as the dies have been covered with a high emissivity coating, and the considered operating temperatures have been higher than 50 °C, as presented in Section IV-A. Moreover, LIT measurements have not been affected by them thanks to the followed lock-in strategy [31].

Fig. 3(c) shows a zoomed view of the test circuit highlighting all the parts presented in Section II-B (e.g., drivers, $C_{\mathrm{snub},i}$, electrical probes and power devices). In the test circuit, top-switch and AUX are cooled down with an air-forced heatsink, while the DUT (packaged chips, IGBT and Diode) is mounted on the heating micropositioning stage. This stage presents five degrees of freedom (X–Y–Z positioning, rotation and tilt), which allows accurately displacing and focusing the IGBT and diode. Moreover, this system also heats up them to an initial operating temperature (T_{P}), which aids to improve the IR images S/N [31], [33]. Concretely, this heating part is implemented with a Linkam PE120 Peltier stage [see Fig. 3(b)] and T_{P} is adjusted in closed loop with a Linkam T95-PE controller. The PE120 is based on a water cooled Peltier cell soldered on top of the ends of a tinned aluminum plate. The rest of the available surface is used to heating up the DUT by conduction and fix the DUT backside temperature, while extracts the power dissipated by the DUT under operation (up to 30 W RMS). For the PE120 control, T_{P} is measured with a PT100 sensor embedded in an indentation at the plate backside close to the middle, so as to properly carry out the closed loop regulation from -25 °C to 125 °C. Furthermore, this plate ensures a uniform heating and heat removal for both dies, which, jointly with the other described characteristics, allows keeping an isotherm at the monitoring point T_{P}.

Fig. 3(d) presents a detailed view of the packaged devices, as shown in Fig. 3(b) and (c), where both chips are visually accessible and prepared as detailed in Section II-D. Fig. 3(d) also indicates some parts of the packaging and the devices: the bonding wires attached on the dies top surface and the devices edge terminations. Both chips are fixed to the PE120 stage with a multiple material stack [see Fig. 3(b)]. The device is screwed onto a copper (Cu) baseplate, including an alumina (Al_2O_3) thin slab between them to electrically isolate the device from

the PE120 stage. In all material interfaces, silicone grease is disposed as a thermal interface material (TIM) to improve the thermal contact. A sectional view of this assembly is reported in Fig. 4(b). Finally, C_{res}, L_{eq} and R_{eq} are presented in Fig. 3(e)–(g), respectively.

D. Devices Preparation and Electro-Thermal Characterization

For the proposed tests, five units of commercially available 650 V-40 A IGBTs have been used and studied as a demonstrator. Such components are encapsulated with free-wheel diodes in a TO-247 package. Prior to measuring them by IR means, several actions have been performed to have visual access to both dies. Thus, the molding compound covering the dies has been removed in four of them, opening a window on top of the package. An individual sample has not undergone such a procedure in order to be used as a reference to analyze possible effects of such a removal process in the devices electrical performance. This window has been performed combining physical and chemical processes. First, a laser etching has been carried out to create a container on top. After, the container has been filled in of 4–5 droplets of 98% nitric acid, which finally removes the rest of molding compound in 20–30 s.

To increase the IR camera sensitivity, the dies have been coated by spraying a high emissivity matt black paint [see Fig. 5(a)], which adheres to metals or polymeric materials on top of the dies and package substrate. According to the characteristics given by the manufacturer, such a coating is a carbon-free pigment rich paint composed out of a semiflexible film that features a very high corrosion, electrical insulation, and temperature resistance of up to 700°C. Unfortunately, a highly uniform coating is not obtained, and depending on the used IR lens, such a fact may influence on thermal measurements. To show this, Fig. 5 presents the field of view corresponding to lenses G1X [see Fig. 5(a) and (b)] and G3X [see Fig. 5(c) and (d)], jointly with their associated emissivity maps ε [see Fig. 5(b) and (d)]. As a result of the coating deposition, a higher emissivity than that of the top metallization (typically 0.2–0.3) is ensured in all cases [see Fig. 5(b) and (d)]. However, in the case of G3X lens, a higher emissivity variation is observed [between 0.94 and 0.74, see Fig. 5(d)] than in the case of G1X [between 0.94 and 0.87, see Fig. 5(b)]. This dispersion in the ε values appears during the paint spraying, as the bonding wires, surface roughness and die edges make difficult to obtain a uniform thickness of material coating over the whole surface, leaving certain areas partly covered. Concretely, such areas along the edge termination and below the bonding wires present ε values on top of the die ranging from 0.84 to 0.74 [see Fig. 5(d)] in G3X, whereas in the case of G1X, a maximum variation between 0.94 to 0.87 is measured. To overcome such an effect in both cases, the emissivity contrast has been performed in all images according to the method described in [33]. It should be noticed that in all images, four spots close to the bonding wires, referred in Fig. 5(d) and (e) to as A, B, C, and D, have resulted from the package window opening and coating processes. They could be related with remaining molding compound material on top of the die. Fortunately, they have been excluded in the performed calculations of T_{j} and do not affect to the results on power losses measurement presented further on.

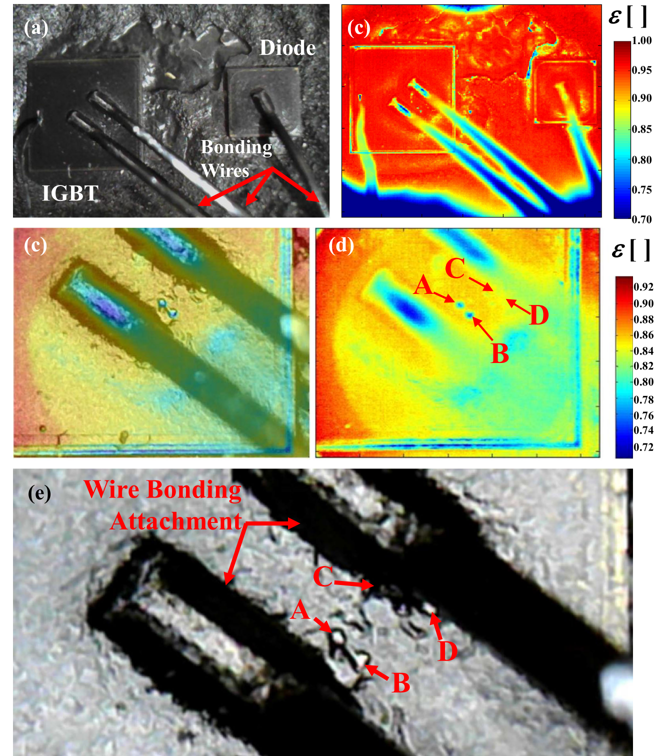


Fig. 5. Surface emissivities depending on the field of view, superposed to a picture, and compared to a picture of the inspected area. (a) Picture of the full view with G1X. (b) Emissivity map for this lens. (c) Superposition of emissivity map parameters with a picture of the ROI inspected with lens G3X. (d) Emissivity map alone. (e) Area identifying the elements affecting $|\Delta T_{\mathrm{surf}}|$ determination.

To deepen on the effect of nonhomogeneous ε on the final results, the device presented in Fig. 5 has been recoated after performing all tests presented in Section IV and measured again. The device has been submitted under the operation conditions of test B-III presented in Section IV-D; i.e., resonant load has been reconfigured to $L_{\mathrm{eq}} = 274$ µH, $C_{\mathrm{res}} = 1080$ nF, and $R_{\mathrm{eq}} = 6.6\ \Omega$, leading to $f_{\mathrm{res}} = 9.25$ kHz, $V_{\mathrm{BUS}} = 300$ V, $f_{\mathrm{Sw}} = 9.31$ kHz and without snubber. Fig. 6 presents before and after recoating the device, a picture of the inspected ROI showing the coated surface [see Fig. 6(a) and (b)], ε [see Fig. 6(c) and (d)], T_{S} [see Fig. 6(e) and (f)], $|\Delta T_{\mathrm{surf}}|$ at $f_{\mathrm{Sw}} = 9.31$ kHz [see Fig. 6(g) and (h), and Φ_{surf} at $f_{\mathrm{Sw}} = 9.31$ kHz [see Fig. 6(i) and (j)]. In Fig. 6(a) and (b), the spots A, B, C, and D with a lower emissivity (singularities in ε) identified in Fig. 5 are also highlighted. Fig. 6(c) and (d) show how the coating process has decreased and made more uniform the emissivity in the area between the bonding wire attachments, totally suppressing the singularities in ε. As a result, Fig. 6 demonstrates how spots A and B [singular emissivity points, see Fig. 6(e)] are perfectly corrected by emissivity contrast in T_{S} image. In spite of this interesting result, thick coatings introduce a noticeable attenuation in $|\Delta T_{\mathrm{surf}}|$, as the heat diffuses through the coating and experiences a decay fixed by ρ. Another consequence of this appears in Φ_{surf}, which presents a more

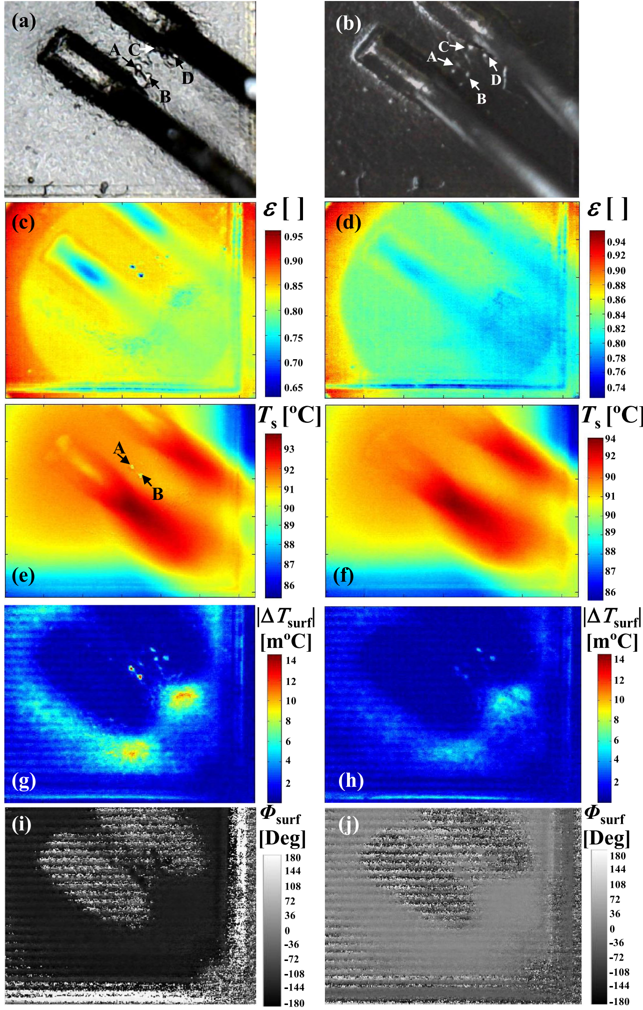


Fig. 6. Measurements performed for a thinner (a), (c), (e), (g), (i) and a thicker (b), (d), (f), (h), (j) coating layer on top of the IGBT surface depicting in each case: (a) and (b) Picture of the surface. (c) and (d) Surface emissivity ε. (e) and (f) Mean or dc temperature T_{S}. (g) and (h) Thermal amplitude $|\Delta T_{\mathrm{surf}}|$. (i) and (j) Phase lag Φ_{surf}.

uniform distribution across the die top surface. Both effects are observed in Fig. 6(g), (h), (i), and (j). However, the pattern of $|\Delta T_{\mathrm{surf}}|$ and Φ_{surf} at f_{Sw} remain equal. As for the singular points A, B, C, and D extremely present in Fig. 6 (g), (h) are still visible, but less stressed. Singular points C and D can be attributed to a thinner metal of the bonding wire attachment areas, where thermal measurements are still possible. For the case of points A and B, they could be related with another material (molding compound, as previously indicated), which is heated up at the same rate of the chip giving a certain signal. Therefore, after carrying out this test, $|\Delta T_{\mathrm{surf}}|$ and Φ_{surf} at f_{Sw} are practically not affected for such effects appeared along the chip preparation.

Next to the devices preparation, their thermal impedance junction to case $(Z_{\mathrm{th(j-C)}})$ has been extracted to check whether their thermal performances have been modified by the window opening process. To this end, the set-up presented in [56] and [57] has been used. The device has been first submitted to a step-like pulse (P) of 21 W until reaching its thermal steady state.

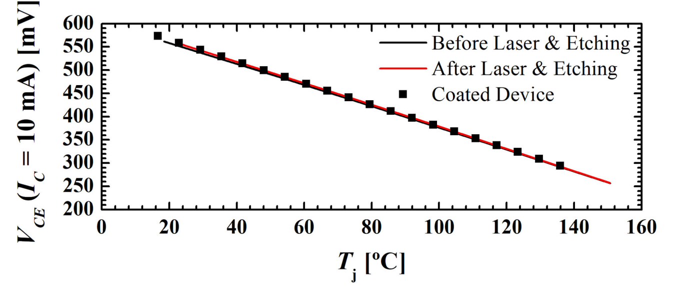


Fig. 7. Sample preparation effects on TSEP calibration.

In that instant, the device dissipation has been stopped, and while the device is cooled down, T_{j} and its case temperature (T_{C}) have been captured simultaneously. T_{j} has been directly measured using a thermo-sensitive electrical parameter (TSEP), while T_{C} has been acquired using a spring-loaded K-type thermocouple. In this article, the TSEP employed is V_{CE} at $I_C = 10$ mA, which has been calibrated from 20 °C to 135 °C in an oven. Thus, known T_{j} and T_{C}, and considering P as a step-like input, $Z_{\mathrm{th(j-C)}}$ has been inferred as follows [41]:

$$Z_{\mathrm{th(j\text{-}C)}}(t) = \frac{T_{\mathrm{j}}(t) - T_{\mathrm{C}}(t)}{P}. \tag{11}$$

Notice that, as a result of such a device preparation process, the devices electro-thermal characteristics have remained practically unaltered. To show this in the case of the used TSEP, Fig. 7 compares the TSEP calibration over the different steps of the sample preparation, demonstrating the invariability of such data from the preparation process.

III. Test Circuit Electro-Thermal Modeling

A. System CTM Extraction by IR and Electrical Means

For the test circuit electro-thermal modeling and $P_{\mathrm{gen}}^{\mathrm{IR}}$ determination, the total thermal impedance and resistance of the set of elements shown in Fig. 4(b) [$Z_{\mathrm{th(j-P)}}$ and $R_{\mathrm{th(j-P)}}$, respectively] is required, i.e.,: the encapsulated device, TIM (silicone grease), both Al_2O_3 and Cu layers, and PE120 Al plate. Unfortunately, this cannot be performed as in Section II-D, since the used set-up is not compatible. Besides, the IR camera does not present a sufficient time resolution to extract T_{j} at timescales below 1 ms. As a solution, electrical and IR measurements have been combined. First, the thermal impedance from junction to Cu baseplate $[Z_{\mathrm{th(j-b)}}]$ has been extracted as performed in Section II-D, taking as a reference the temperature at the Cu baseplate backside [T_{b}, see Fig. 4(b)]. Next, this assembly is mounted on top of the Peltier stage and T_{j} is monitored by IR means, obtaining the contribution of the Al plate of the PE120 stage. From both results, a final $Z_{\mathrm{th(j-P)}}$ is inferred, considering $Z_{\mathrm{th(j-b)}}$ as an offset correction to the IR data. Fig. 8 presents the $Z_{\mathrm{th(j-P)}}$ results (black squared points) and the fifth-order resistive-capacitive (RC) Cauer network, depicted in the inset of Fig. 8, corresponding to $Z_{\mathrm{th(j-b)}}$ (blue dashed line), whose values are given in Table I. Moreover, a CTM also based on a fifth-order RC Cauer network is fitted to $Z_{\mathrm{th(j-P)}}$ (red solid

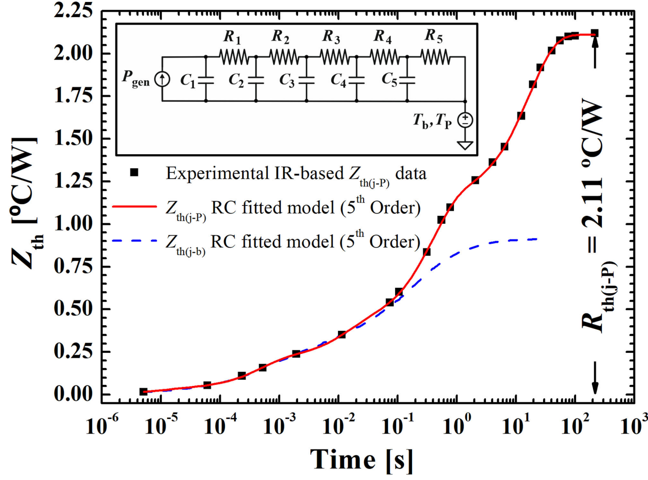


Fig. 8. Experimental IGBT $Z_{\mathrm{th(j-P)}}$ (points) including a model fitting of a fifth-order Cauer network to $Z_{\mathrm{th(j-P)}}$ (red solid line) and $Z_{\mathrm{th(j-b)}}$ (blue dashed line). In the inset, the fifth-order Cauer network schematic is presented.

TABLE I
CAUER NETWORK PARAMETERS FOR $Z_{\mathrm{th(j-Ref)}}$ - R IN [K/W] AND C IN [J/K]

Model	R_1	R_2	R_3	R_4	R_5	C_1	C_2	C_3	C_4	C_5
$Z_{th(j-b)}$	0.053	0.172	0.165	0.300	0.210	$4\cdot10^{-4}$	$2.6\cdot10^{-3}$	0.043	0.313	2.538
$Z_{th(j-P)}$	0.041	0.184	0.235	0.735	0.917	$3\cdot10^{-4}$	$2.4\cdot10^{-3}$	0.561	0.467	17.93

line) and its parameters are given in Table I. From these results $R_{\mathrm{th(j-P)}} = 2.11\,^{\circ}\mathrm{C/W}$ is determined, since it is indispensable for $P_{\mathrm{gen}}^{\mathrm{IR}}$ extraction, as $P_{\mathrm{gen}}^{\mathrm{IR}} = \Delta T_{\mathrm{(j-P)}}/R_{\mathrm{th(j-P)}}$.

B. Test Circuit Modeling for IR Results Assessment

To assess the IR results, the test circuit shown in Fig. 2 has been simulated electrothermally. First, the IGBT model supplied by the manufacturer has been checked. To this end, the $I_C - V_{CE}$ static characteristic curves at $V_{GE} = 20$ V of the prepared devices have been measured at different temperatures (from 25 °C to 125 °C), and compared to the manufacturer model prediction. Besides, the test circuit parasitics (mainly $L_{C,i}$ and $L_{E,i}$) have been extracted from contrasting electrical measurements and simulation results. Finally, the CTM of $Z_{\mathrm{th(j-P)}}$ derived in Section III-A is incorporated in the model.

As for thermal calculation, T_{j} is computed with the following simplification to reduce the simulation time. According to (1), $P_{\mathrm{gen}}(\tau)$ can be written into two terms, periodic and mean value contributions, depending on τ:

$$P_{\mathrm{gen}}(\tau) = P_{\mathrm{Periodic}}(\tau) + P_{\mathrm{Mean}}(\tau) \tag{12}$$

where $P_{\mathrm{Periodic}}(\tau)$ is a fast-varying periodic function of τ and $P_{\mathrm{Mean}}(\tau) = P_0 \cdot f(\tau)$ is a slow-varying function of τ. Thus

$$\Delta T_{\mathrm{(j-Ref)}}(t) = \Delta T_{\mathrm{(j-Ref),Periodic}}(t) + \Delta T_{\mathrm{(j-Ref),Mean}}(t) \tag{13}$$

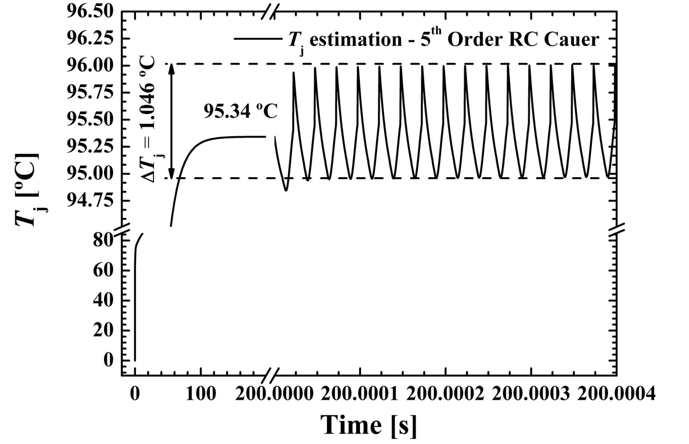


Fig. 9. T_{j} estimation based on the obtained Cauer CTM and considering the superposition principle.

which are

$$\Delta T_{\mathrm{(j-Ref),Periodic}}(t) = \int_0^t P_{\mathrm{Periodic}}(\tau) \cdot \left(\frac{dZ_{\mathrm{th(j-Ref)}}(t-\tau)}{dt}\right) d\tau \tag{14}$$

$$\Delta T_{\mathrm{(j-Ref),Mean}}(t) = P_0 \int_0^t f(\tau) \cdot \left(\frac{dZ_{\mathrm{th(j-Ref)}}(t-\tau)}{dt}\right) d\tau \tag{15}$$

When $t \to \infty$ (steady state) in (15), $\Delta T_{\mathrm{(j-Ref),Mean}}(t) = P_0 \cdot R_{\mathrm{th(j-Ref)}}$, while in (14), $\Delta T_{\mathrm{(j-Ref),Periodic}}(t)$ represents the steady state thermal oscillations. Thus, T_{j} calculation can be addressed in two steps when the goal is to extract the steady state temperature of the device. First, P_{Mean} is considered in the CTM, and, after, P_{Periodic} is applied. Thanks to this, results are rapidly achieved after a few simulation cycles (see Fig. 9). This figure shows the thermal simulation results obtained in steady state after following the superposition approach.

To show the good agreement between the model predictions and experimental data, Fig. 10 compares them and depicts a detailed view of the device commutations to ON and OFF state (i.e., $P_{\mathrm{Sw}} \neq 0$). As test conditions, typical values encountered in domestic IH appliances have been set in the test circuit, i.e.,: $V_{\mathrm{BUS}} = 300$ V, $f_{\mathrm{Sw}} = 40$ kHz, $f_{\mathrm{res}} = 29.6$ kHz, $R_{\mathrm{eq}} = 3\ \Omega$ (i.e., power factor of 0.43), $C_{\mathrm{res}} = 1080$ nF, and $C_{\mathrm{snub}} = 15$ nF. From these results, it has been obtained a similar behavior to the electrical measurements in terms of the parasitic elements modeling. Unfortunately, as Fig. 10(b) highlights, the IGBT tail current behavior ($t_{\mathrm{tail(sim)}}$) slightly differs from the measured waveform ($t_{\mathrm{tail(exp)}}$) and it cannot be corrected by using the model provided by the DUT manufacturer. In such calculations, this introduces a certain error in the power determination of 1.4 W, which signifies an acceptable error of 6% in the prediction. In conclusion, in spite of the IGBT tail current non proper modeling, it is obtained a satisfactory agreement between simulation and measurements, being acceptable for the assessment of the approach presented.

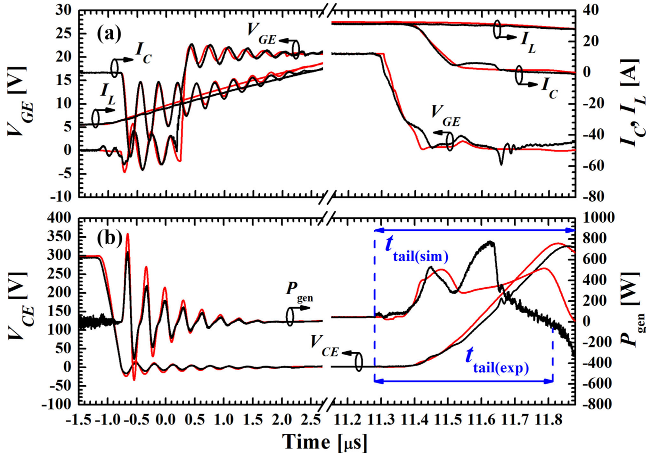


Fig. 10. Detailed view of the turn-ON and turn-OFF commutation corresponding to experimental (black solid line) and simulation (red solid line) electrical waveforms for $P_{\mathrm{Sw}} \neq 0$. (a) V_{GE}, I_C and I_{L}. (b) V_{CE} and P_{gen}.

TABLE II
TEST CONDITIONS AND MEASURED POWER LOSSES

Test Id.	V_{BUS} [V]	f_{Sw} [kHz]	C_{snub} [nF]	$P_{\mathrm{gen}}^{\mathrm{Elec}}$ [W] Meas.	Sim.	$P_{\mathrm{gen}}^{\mathrm{IR}}$ [W]	$P_{\mathrm{On}}^{\mathrm{Elec}}$ [W] Meas.	Sim.	$P_{\mathrm{On}}^{\mathrm{IR}}$ [W]	$P_{\mathrm{Sw}}^{\mathrm{IR}}$ [W]
A-I	300	40	15	23.21	25.02	25.21	14.35	14.71	14.92	10.29
A-II	250	40	15	16.33	17.01	17.21	10.82	9.78	9.66	7.55
A-III	250	40	No	22.93	24.44	21.65	8.02	8.31	7.21	14.44
A-IV	200	20	15	18.36	19.21	17.46	11.12	10.72	11.94	6.42
A-V	200	20	No	11.30	10.60	10.73	10.06	9.31	9.99	0.74

IV. EXPERIMENTAL RESULTS

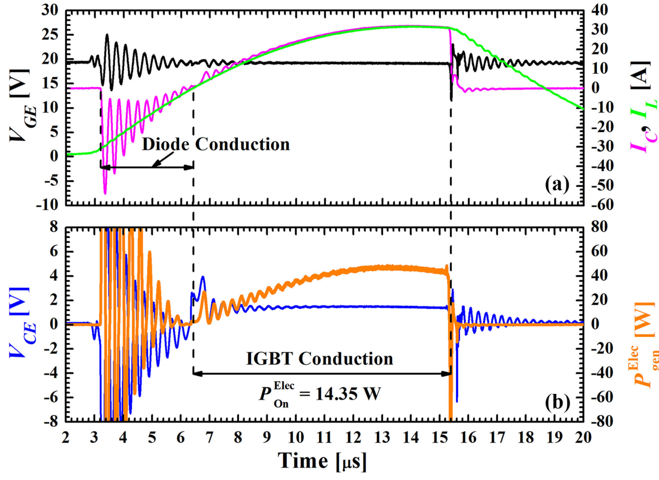
A. Power Losses Extraction From IR Measurements

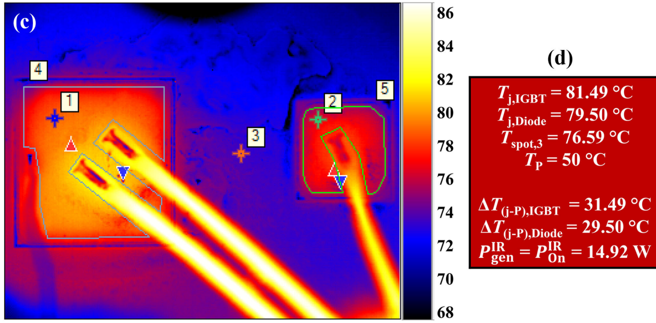
First, the suitability of IR thermography for measuring $P_{\mathrm{gen}}^{\mathrm{IR}}$ has been evaluated by experimentation and simulation in a case study related to a domestic IH appliance. In such an application, a reduced dissipation is ensured under a resonant load by soft-switching IGBTs and following the ZVS condition; while their V_{GE} is unipolar driven with a 20 V amplitude squared waveform. As for test bench conditions, $T_{\mathrm{P}} = 50\,°\mathrm{C}$ has been set, as it allows: thermally stabilizing the Peltier heating system, improving the camera S/N, and reaching close-to-application worst case temperature conditions (at least 75 °C ambient temperatures in domestic IH [58]). Besides, $L_{\mathrm{eq}} = 24.78$ μH, $C_{\mathrm{res}} = 1080$ nF, and $R_{\mathrm{eq}} = 3\ \Omega$ have been fixed in the test circuit, obtaining $f_{\mathrm{res}} = 29.6$ kHz. As for V_{BUS} and f_{Sw} values, they have been varied. Given the studied application resonance and keeping the dead times unchanged, ZVS loss occurs just by setting $f_{\mathrm{Sw}} < f_{\mathrm{res}}$. Table II summarizes all such conditions, jointly with the power losses extracted from electrical (both measurements and simulations) and IR results for one of the prepared IGBTs. Tests A-I to A-III consider the power devices operation within the ZVS condition (i.e., $f_{\mathrm{Sw}} > f_{\mathrm{res}}$, regular operation); whereas, in Tests A-IV and A-V, they are switched outside (i.e., $f_{\mathrm{Sw}} < f_{\mathrm{res}}$). In both ZVS scenarios, the effect of C_{snub} (i.e., soft-switching) on power losses calculation is also analyzed (see tests A-III and A-V).

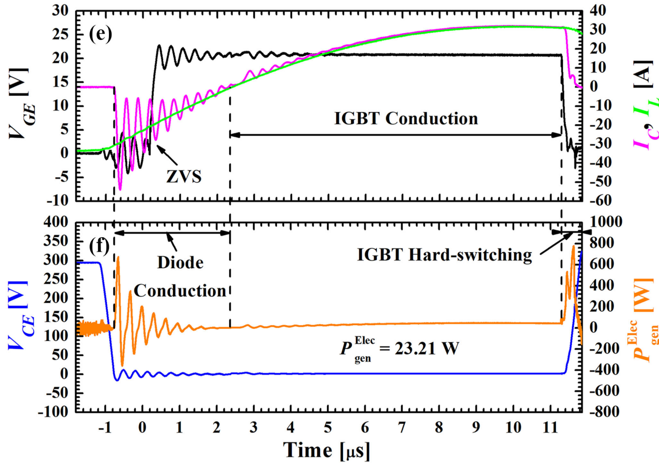
As an example for $P_{\mathrm{gen}}^{\mathrm{IR}}$, $P_{\mathrm{On}}^{\mathrm{IR}}$, and $P_{\mathrm{Sw}}^{\mathrm{IR}}$ extraction, all results corresponding to test A-I are presented when $P_{\mathrm{Sw}} = 0$ and $P_{\mathrm{Sw}} \neq 0$. Fig. 11 (a) and (b) depict the waveforms of V_{GE} (in black), I_C (in magenta), I_{L} (in green), V_{CE} (in blue) and $P_{\mathrm{gen}}^{\mathrm{Elec}}$ (in orange) when $P_{\mathrm{Sw}} = 0$. In the same conditions, Fig. 11(c) and (d) present the IR results with the temperature mean or dc value across the surface of the IGBT ($T_{\mathrm{j,IGBT}}$) and diode ($T_{\mathrm{j,Diode}}$), jointly with a spot in between ($T_{\mathrm{spot,3}}$). Conversely, Fig. 11(e), (f), (g), and (h) provide the electrical and IR information for $P_{\mathrm{Sw}} \neq 0$, respectively. In all such measurements, $T_{\mathrm{j,Diode}}$ remains close to $T_{\mathrm{spot,3}}$ (2.91 °C and 1.53 °C difference). Therefore, the diode practically does not dissipate power due to the adopted driving pattern and the selected values for f_{Sw} and the resonant load, as also observed in the rest of tests given in Table II. As for the IGBT, $T_{\mathrm{j,IGBT}}$ reaches a higher value when $P_{\mathrm{Sw}} \neq 0$ ($T_{\mathrm{j,IGBT}} = 103.20\,°\mathrm{C}$) than in the case that $P_{\mathrm{Sw}} = 0$ is considered ($T_{\mathrm{j,IGBT}} = 81.49\,°\mathrm{C}$), as expected. Subtracting T_{P} to $T_{\mathrm{j,IGBT}}$ and considering $R_{\mathrm{th(j-P)}}$ previously measured, $P_{\mathrm{On}}^{\mathrm{IR}} = 14.92$ W, $P_{\mathrm{On}}^{\mathrm{IR}} + P_{\mathrm{Sw}}^{\mathrm{IR}} = 25.21$ W, and $P_{\mathrm{Sw}}^{\mathrm{IR}} = 10.29$ W are inferred. In comparison to electrical measurements, i.e., $P_{\mathrm{On}}^{\mathrm{Elec}} = 14.35$ W, $P_{\mathrm{On}}^{\mathrm{Elec}} + P_{\mathrm{Sw}}^{\mathrm{Elec}} = 23.21$ W, and $P_{\mathrm{Sw}}^{\mathrm{Elec}} = 8.86$ W, slight differences are observed.

According to Table II results, the power losses behave over the tests as follows. P_{gen} is dissipated in the IGBT, as I_C mainly passes through such a device instead of the diode. Another interesting feature relates with the ZVS condition and C_{snub} presence. Within the ZVS condition and thanks to using C_{snub} (soft-switching during turn-off), the IGBT presents the lowest losses as expected, but this is not the case when the device is commutated outside, as shown from tests A-IV and A-V. Those tests report a higher dissipation when C_{snub} is present. To understand this, Fig. 12 presents the obtained results when $P_{\mathrm{Sw}} \neq 0$ for test A-IV [see Fig. 12(a) and (b)] and for test A-V [see Fig. 12(c) and (d)], showing the same electrical parameters and color codes than in Fig. 11. When the test circuit operates outside the ZVS condition, P_{Sw} is substantially reduced when C_{snub} is removed (i.e., $P_{\mathrm{Sw}}^{\mathrm{IR}}$ changes by 5.68 W), as a consequence of having a faster dV_{CE}/dt; whereas P_{On} are lower due to the reduced oscillations. This behavior, perfectly described by thermal results, is clearly observed after comparing Fig. 12(b) and (d). The same trends have been observed in all analyzed devices.

In general, the results of P_{gen} and P_{On} calculated from the electrical or IR measurements mainly differ between 1% and 10% (≤2 W), which have been calculated according to $\Delta P_{\mathrm{gen}}/P_{\mathrm{gen}} = \sqrt{(P_{\mathrm{gen}}^{\mathrm{Elec}} - P_{\mathrm{gen}}^{\mathrm{IR}})^2 / P_{\mathrm{gen}}^{\mathrm{Elec}}}$ or $\Delta P_{\mathrm{On}}/P_{\mathrm{On}} = \sqrt{(P_{\mathrm{On}}^{\mathrm{Elec}} - P_{\mathrm{On}}^{\mathrm{IR}})^2 / P_{\mathrm{On}}^{\mathrm{Elec}}}$, respectively. The existing discrepancies are linked to the oscillations/noise appeared in the DUT electrical waveforms, especially when the device is soft-switched within the ZVS condition. This is supported by comparing electrical measurements to simulation results in Table II, observing discrepancies between 2.4% and 11% not only coming from the IGBT tail current modeling, but also electrical couplings with the probes. To reduce this difference between approaches, the probes parasitic elements should be first determined, and after their contributions removed from the electrical measurements.







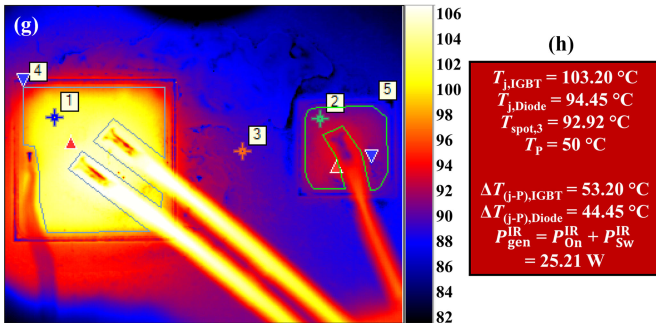


Fig. 11. Test A-I experimental electrical waveforms when (a) and (b) $P_{\mathrm{Sw}} = 0$ and (e) and (f) $P_{\mathrm{Sw}} \neq 0$. Test A-I IR thermographies, $T_{\mathrm{j,IGBT}}$, $T_{\mathrm{j,Diode}}$ and $T_{\mathrm{spot,3}}$ measurements, as well as $T_{\mathrm{j,IGBT}}$ and $T_{\mathrm{j,Diode}}$ increment with respect to T_{P} ($\Delta T_{\mathrm{(j-P),IGBT}}$ and $\Delta T_{\mathrm{(j-P),Diode}}$) for (c) and (d) $P_{\mathrm{Sw}} = 0$, and (g) and (h) $P_{\mathrm{Sw}} \neq 0$.

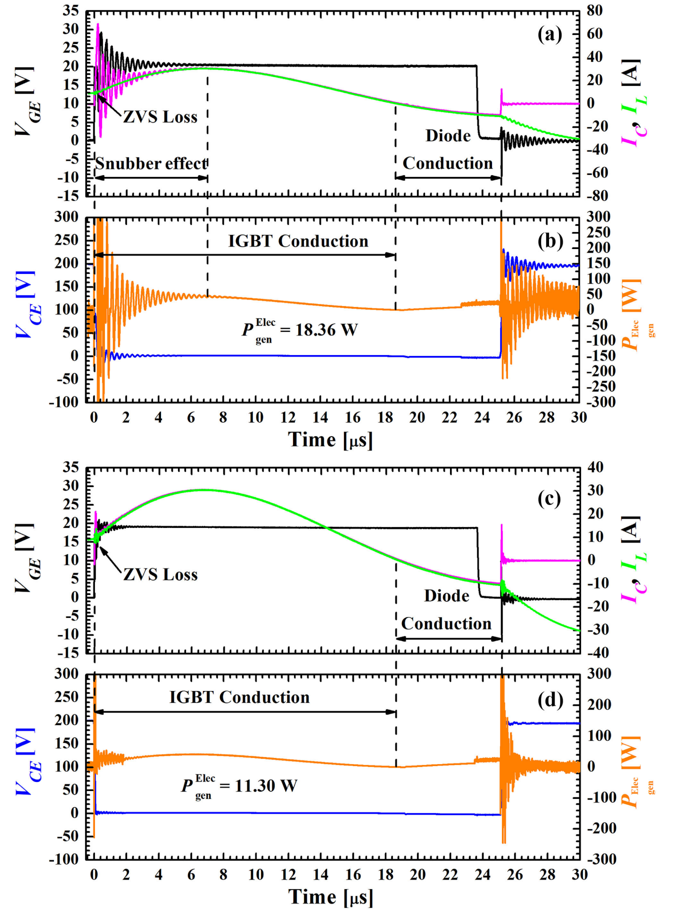


Fig. 12. Tests A-IV and A-V experimental electrical waveforms and $P_{\mathrm{gen}}^{\mathrm{Elec}}$ when $P_{\mathrm{Sw}} \neq 0$ and the DUT is under (a) and (b) soft-switching ($C_{\mathrm{snub}} = 15$ nF) and; (c) and (d) hard-switching (without C_{snub}) conditions.

In summary, the proposed approach based on IR measurements features a better immunity to electrical noise introduced by the test circuit stray elements, the package parasitics or the used probes, as a nonelectrical observable is monitored by a noninvasive and contactless way. Moreover, the effect of thermal drifts and offsets, intrinsically related with current and voltage probes, are more controlled in IR-cameras. In view of such benefits, the strategy presented in this article can be considered an alternative to traditional methods.

B. Die-Level Current Distribution Analysis at f_{Sw} by IR-LIT

The next analysis has been performed adjusting the test circuit at $V_{\mathrm{BUS}} = 300$ V and at lower f_{Sw} and f_{res} values than in Section IV-A to achieve an adequate tradeoff between the device dissipation level (i.e., IR signal) and t_{int} (i.e., camera S/N). Therefore, the resonant load has been reconfigured to $L_{\mathrm{eq}} = 274$ μH, $C_{\mathrm{res}} = 1080$ nF, and $R_{\mathrm{eq}} = 6.6$ Ω, leading to $f_{\mathrm{res}} = 9.25$ kHz. Again, the IGBT has been driven with a 20 V amplitude square waveform for the reasons stated in Section IV-A. The rest of the test conditions are given in Table III, i.e.,: the ZVS condition, C_{snub} presence (i.e., hard- or soft-switching) and f_{Sw} values. Under such conditions, an outside

TABLE III
TEST CONDITIONS AND MEASURED POWER LOSSES FOR CURRENT DISTRIBUTION AT $V_{BUS} = 300$ V

Test Id.	f_{Sw} [kHz]	C_{snub} [nF]	ZVS	P_{gen}^{Elec} [W]	P_{gen}^{IR} [W]	P_{On}^{Elec} [W]	P_{On}^{IR} [W]	P_{Sw}^{Elec} [W]	P_{Sw}^{IR} [W]
B-I	9.51	15	Yes	10.27	10.18	10.08	9.68	0.19	0.50
B-II	9.31	15	Yes	11.45	10.66	10.89	10.34	0.56	0.32
B-III	9.31	No	Yes	10.99	11.03	10.43	9.98	0.56	1.05
B-IV	9.11	15	No	13.21	12.52	13.10	12.18	0.11	0.34
B-V	9.11	No	Yes	10.80	10.66	10.57	9.87	0.43	1.16
B-VI	8.91	15	No	17.29	16.10	17.06	15.80	0.23	0.30

ZVS operation can be carried out when $f_{Sw} < f_{res}$ is verified, as the dead times are also kept constant and the used C_{snub} value is sufficiently high for the considered f_{res} and f_{sw} values. Table III reports the power losses calculated by IR and electrical means, to support the $|\Delta T_{surf}|$ results acquired at f_{Sw}. Moreover, these tests have been performed for the same device analyzed in Section IV-A as presented the highest S/N levels. In this case, electrical and thermal results of P_{gen} and P_{On} present a satisfactory agreement (differences <7.4%). As previously stated, when oscillations appear, the I_C and V_{CE} waveforms could not be properly acquired with the used probes due to the electrical noise resulting from the circuit stray inductances and capacitances, which makes overestimating the power losses value. On the contrary, thermal measurements provide more reliable results, since such an electric noise does not disturb IR acquisitions, as demonstrated in Section IV-A.

To locally deepen into the surface averaged results extracted from dc thermal values and presented in Table III, Fig. 13 provides $|\Delta T_{surf}|$ [(a) and (b)] and Φ_{surf} [(c) and (d)] measured at f_{Sw} in test B-I when $P_{Sw} \neq 0$ [(a) and (c)] and $P_{Sw} = 0$ [(b) and (d)]. Despite the fact that the bonding wires cover part of the chip top surface [see Fig. 4(a)], the thermal field is confined in two main hot spots close to the bonding wires attachment, as a local maximum in $|\Delta T_{surf}|$ and a well-defined Φ_{surf} are concurrently observed in those locations. The bonding wires attachment to the IGBT emitter pad corresponds in all figures to the darkest areas, which matches with the region shown in Fig. 4(a). Concretely, in Fig. 13(c) and (d), Φ_{surf} is undefined (noisy behavior) in this area, demonstrating that in the bonding wires attachment; no lock-in correlation exists. Such a thermal distribution obeys to the current path, as the bonding wires provide to I_C a way to go outside the device [47], [48]. This $|\Delta T_{surf}|$ distribution evidence the crowding effect induced around the bonding wires, mainly focused at their heels (hot spots), similar to that reported in [47], as discussed further on. Besides, a slight $|\Delta T_{surf}|$ increase jointly with a contrasted Φ_{surf} variation is observed at the device edge termination (right and lower part of each image). The variation in Φ_{surf} denotes that one part of the die is dissipating power in phase with the device under on-state, while another one is generating heat only during the IGBT turn-OFF process. However, a lower $|\Delta T_{surf}|$ is detected as switching losses emit IR radiation for a shorter lapse of time.

Such a phenomenon can be acquired with the camera even if $1/f_r$ is much longer. For this acquisition, the critical parameters are t_{int}, where $t_{int} < 1/(2 f_{Sw})$ must be fulfilled, and S/N [31].

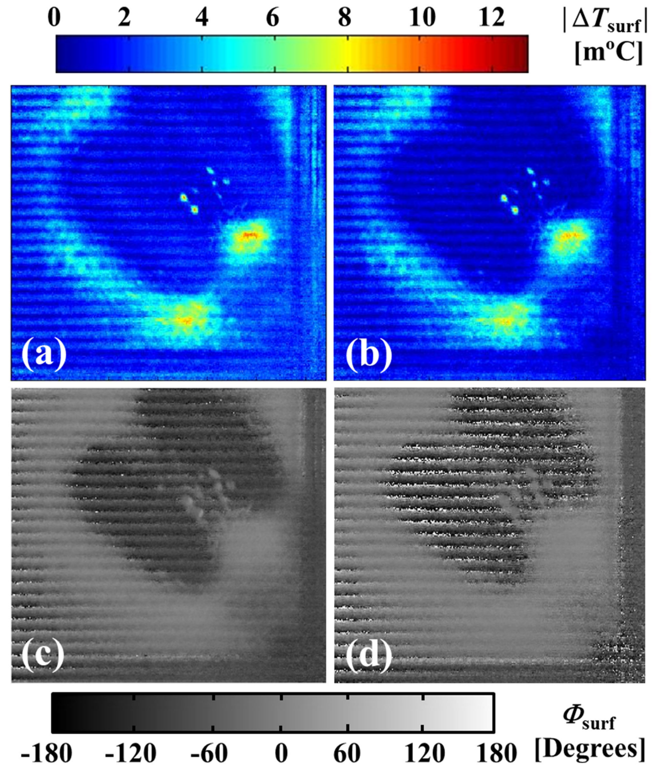


Fig. 13. $|\Delta T_{surf}|$ and Φ_{surf} when commutations are within the ZVS condition (test B-I) at $f_{Sw} = 9.51$ kHz considering (a) and (c) $P_{Sw} \neq 0$ and (b) and (d) $P_{Sw} = 0$.

Therefore, an extremely short IR radiation pulse due to a high power density can be recorded with the camera as long as its intensity, after being integrated by the camera sensor along t_{int}, overcomes a detection threshold fixed by a given S/N. Therefore, f_r is not a limiting factor, as t_{acq} can be extremely extended to undersample this phenomenon along several $1/f_r$ periods, prior to proceeding with the lock-in postprocessing [31], as can be observed in Fig. 13. From the comparison of $|\Delta T_{surf}|$ and Φ_{surf} when $P_{Sw} \neq 0$ [see Fig. 13(a) and (c)] and $P_{Sw} = 0$ [see Fig. 13(b) and (d)], the edge termination shows a less defined Φ_{surf} with a smaller $|\Delta T_{surf}|$ as $P_{Sw} = 0$. This is a consequence of this behavior. When $P_{Sw} \neq 0$, a higher voltage is sustained for a similar I_C level conducted in that area during commutation. Thus, $|\Delta T_{surf}|$ distribution, jointly with Φ_{surf}, provides a map of the current distribution across the die surface.

To better interpret and assess all lock-in images at f_{Sw} by linking them to the inspected ROI and several parts of the die, i.e., edge termination, IGBT core, and bonding wires, Fig. 14 depicts $|\Delta T_{surf}|$ [see Fig. 14(a) and (b)] and Φ_{surf} [see Fig. 14(c) and (d)] maps with a superposition of a ROI picture [see Fig. 14(a) and (c)] and without [see Fig. 14(b) and (d)]. The dots referred to as A, B, C, and D in Fig. 5(d) also appears between the bonding wire attachment areas in Fig. 14(a) and (b). As already explained in Section II-D, they are an optical artifact resulting from local roughness, which cannot be corrected with the followed method for emissivity contrast. Such figures also allow supporting that, at the areas of the bonding wire attachment, no thermal activity

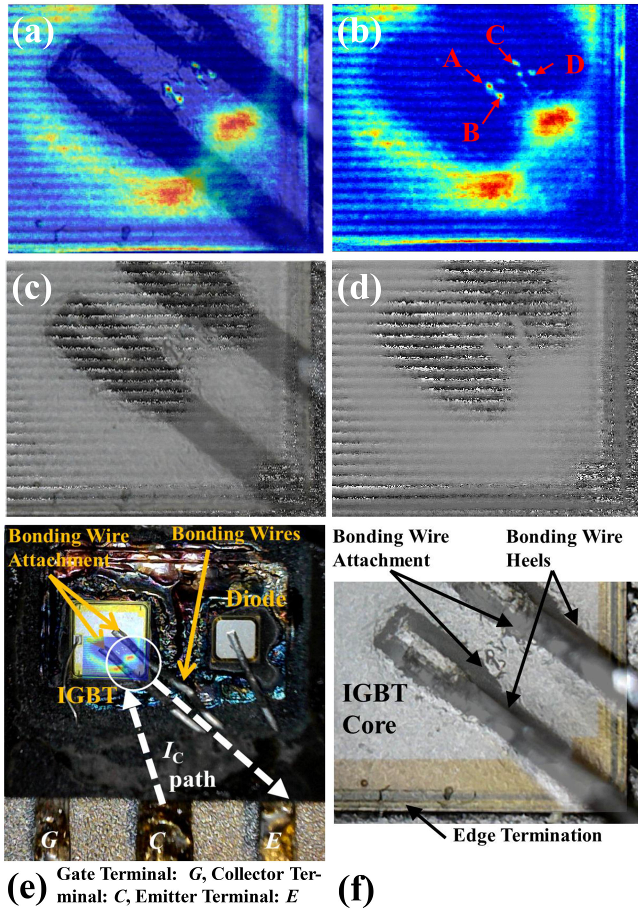


Fig. 14. Lock-in images when commutations are within the ZVS condition (test B-I) at $f_{\mathrm{Sw}} = 9.51$ kHz, considering $P_{\mathrm{Sw}} \neq 0$ and presenting (a) and (b) $|\Delta T_{\mathrm{surf}}|$ and (c) and (d) Φ_{surf}, (a) and (c) with a superposition of a ROI picture, and (b) and (d) without. (e) Top view of an opened package with both dies, observing in the case of the IGBT the terminals and the shortest current path (and less resistive) to go from collector to emitter terminals passing through the device and bonding wires. (f) ROI picture, highlighting the edge termination, IGBT core, and bonding wires parts.

is measured, as no phase correlation is present (noisy/undefined Φ_{surf}). This is due to the fact that G3X lens has a shallow depth of focus and the bonding wires are out of focus. In the case of the bonding wire attachment, the bonding wires contact the die surface and the IR emission is completely shielded. Despite this, Fig. 14(a)–(d) demonstrates that when the bonding wires are out of the camera depth of focus, the IR radiation coming from certain areas below can be partly detected, as each point of the surface emits IR radiation following an all direction pattern. In such areas, the hottest spots are observed and their location is justified by the path followed by the current within the device. This can be perfectly observed in Fig. 14(e) and (f). They present both a top view of an opened package with a $|\Delta T_{\mathrm{surf}}|$ superposed to the IGBT at the ROI [see Fig. 14(e)] and a picture of this ROI, highlighting the edge termination, IGBT core, and bonding wires parts [Fig. 14(f)]. Fig. 14(e) indicates the path of I_C with lower impedance to go from the collector to emitter terminal, expecting, in front of the bonding wire heels, a current crowding or focalization effect [47]. Namely, I_C enters into the IGBT through the die backside (collector side), and comes out through the bonding wires (emitter side).

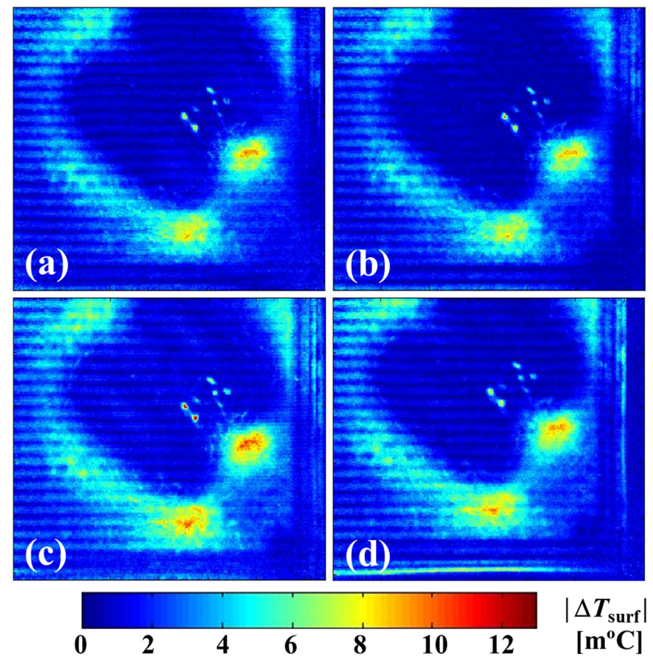


Fig. 15. $|\Delta T_{\mathrm{surf}}|$ when $P_{\mathrm{Sw}} \neq 0$ and the IGBT is: (a) soft-switched within the ZVS condition at $f_{\mathrm{Sw}} = 9.31$ kHz (test B-II); (b) hard-switched within the ZVS condition at $f_{\mathrm{Sw}} = 9.31$ kHz (test B-III); (c) soft-switched outside ZVS condition at $f_{\mathrm{Sw}} = 9.11$ kHz (test B-IV); and (d) hard-switched within the ZVS condition at $f_{\mathrm{Sw}} = 9.11$ kHz (test B-V).

To have a higher insight into such results at f_{Sw} values near f_{res}, Fig. 15 depicts $|\Delta T_{\mathrm{surf}}|$ at f_{Sw} obtained for tests B-II to B-V when $P_{\mathrm{Sw}} \neq 0$. Only $|\Delta T_{\mathrm{surf}}|$ is presented, as Φ_{surf} distributions in these tests are similar to those observed in Fig. 13. In such measurements, Table III presents similar power losses results among them. Again, the bonding wires attachment, close to the wire heels, is revealed as a current focalization area at f_{Sw}. Besides, a temperature increase at f_{Sw} is observed at the device edge termination (right and lower part of each thermal image) when no snubber is used due to the added switching losses. Thanks to this, it can be identified that the device edge terminations are an area with a high potential to generate hot spots under hard-switching conditions, as high voltage is sustained while high I_C levels are passing through. When ZVS operation is fulfilled, the use of C_{snub} does not significantly affect the thermal behavior of the device at the studied test conditions (where f_{Sw} is close to f_{res}), since the current distribution remains almost the same in both cases as shown in Fig. 15(a), (b), and (d). However, when the ZVS condition is lost, the power dissipation raises under soft-switching conditions, as previously described in Section IV-A and observed in Fig. 12. This fact translates into a higher current concentration at the hot spots close to the bonding wires, as shown in Fig. 15(c).

To better understand the hot spots detected at f_{Sw} in the device active area, the analyzed device (die1) is compared with another one (die2) under the operation conditions of test B-III when $P_{\mathrm{Sw}} \neq 0$. Fig. 16 depicts die1 [(a), (c), and (e)] and

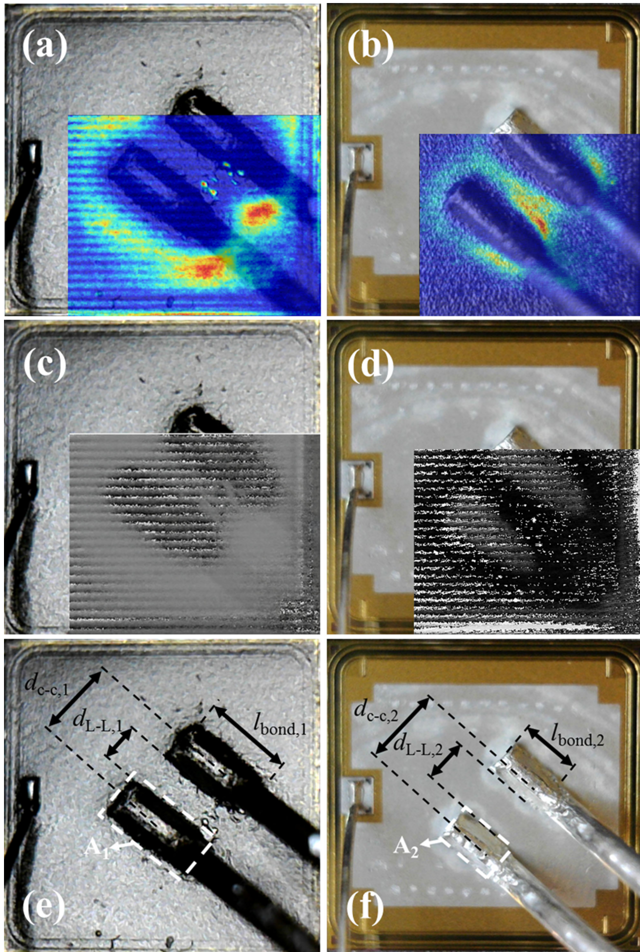


Fig. 16. Results comparison between the (a), (c), (e) analyzed IGBT (b), (d), (f) with another one. Lock-in images superposed to the chip layout when commutations are within the ZVS condition (test B-III) at $f_{\rm Sw} = 9.31$ kHz, considering $P_{\rm Sw} \neq 0$. (a) and (b) $|\Delta T_{\rm surf}|$ and (c) and (d) $\Phi_{\rm surf}$ are presented for each device. (e) and (f) Geometry of the attachment of bonding wires on top of each device is highlighted.

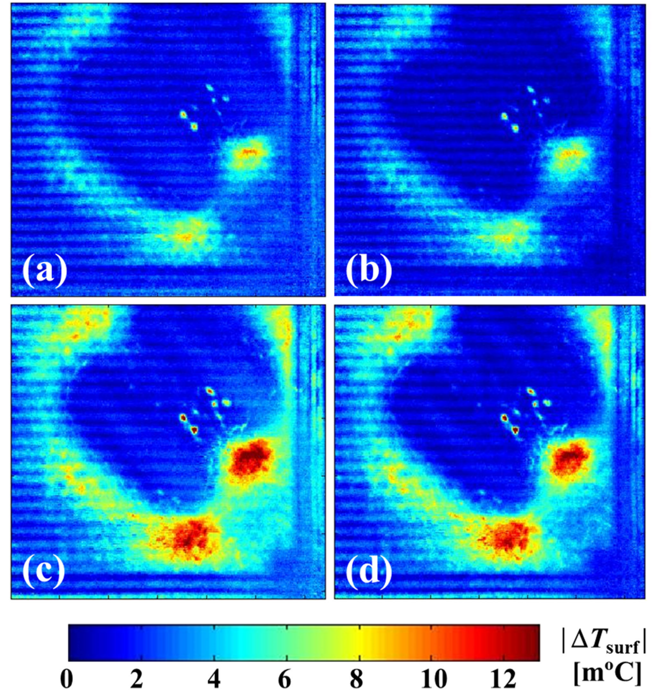


Fig. 17. $|\Delta T_{\rm surf}|$ when commutations are within ZVS condition (test B-I) at $f_{\rm Sw} = 9.51$ kHz considering (a) $P_{\rm Sw} \neq 0$ and (b) $P_{\rm Sw} = 0$, together with when outside ZVS condition (test B-VI) at $f_{\rm Sw} = 8.91$ kHz having (c) $P_{\rm Sw} \neq 0$ and (d) $P_{\rm Sw} = 0$.

die2 [(b), (d), and (f)] superposing $|\Delta T_{\rm surf}|$ [(a) and (b)] and $\Phi_{\rm surf}$ [(c) and (d)] to a picture of each device. Finally, Fig. 16 also highlights the geometry and distribution of the bonding wire attachment on top of die1 (e) and die2 (f). To link this behavior to the bonding wire attachment distribution, Fig. 16(e) and (f) define the following geometrical parameters: the distance between bonding wire centers ($d_{\rm c-c}$), the free space between them ($d_{\rm L-L}$), the area seen from the top of the bonding wire wedge (A), and its length ($l_{\rm bond}$). Fig. 16(a)–(d) shows that the observed hot spots correspond to only one which is partly shielded by the bonding wire. Such hot spot points out the location of a current crowding effect induced by the bonding wires as indicated in [47]. Due to the difference on the geometric parameters of the bonding wire attachment, i.e., $\rm A_1 > A_2$, $l_{\rm bond,1} > l_{\rm bond,2}$, $d_{\rm L-L,1} < d_{\rm L-L,2}$, a different behavior in $\Phi_{\rm surf}$ is observed between die1 and die2. It can be inferred from Fig. 16(c) and (d) that die1 presents a low thermal activity in the areas defined between the bonding wire attachments, differing from die2 results (darker areas in that region in $\Phi_{\rm surf}$). This fact evidences that the bonding wires attachments are very close in die1 and I_C sees them as a unique current collection area. Concretely, the I_C density increases at the heels of the bonding wire attachment, as those locations minimize the impedance of the I_C path, being in agreement with the results shown in [47]. Notice that in both dies, the bond contact at the bottom of the die surface presents the hottest spots (see Fig. 16), as this corresponds to the shortest bonding wire (i.e., lowest impedance path for I_C), and collects more current.

To further examine the hot spots in the edge termination at $f_{\rm Sw}$, Fig. 17 presents $|\Delta T_{\rm surf}|$ corresponding to tests B-I and B-VI when $P_{\rm Sw} \neq 0$ and $P_{\rm Sw} = 0$ are considered. In this figure, the same hot spots appear in the same locations as in Figs. 13 and 14, but with a higher temperature in the case of test B-VI due to its higher power losses (see Table III). In these tests, again, a temperature increase is observed at the device edge termination when $P_{\rm Sw} \neq 0$, since the DUT is commutated and withstands $V_{\rm BUS}$ during a half of the switching period. Additionally, current crowding points close to the wire bonding heels at $f_{\rm Sw}$ appear hotter in tests B-VI due to the higher dissipation reached.

V. Conclusion

A new approach based on IR thermal measurements is proposed to determine at the die-level, the power losses and current distribution. As a case study, soft- and hard-switched IGBTs are analyzed when they are operated under a resonant load and set within and outside the ZVS condition. With this aim, a test bench has been designed, which includes an IR camera and a

specific test circuit. With the IR camera, the temperature on top of the die surface has been averaged (power losses determination) or post processed to extract the spectral component of the surface thermal map at $f_{\rm Sw}$ by using lock-in detection strategies. The test circuit is based on a half-bridge resonant inverter with an adjustable resonant load. It selectively allows measuring $P_{\rm gen}$ when $P_{\rm Sw} = 0$ or $P_{\rm Sw} \neq 0$. To carry out the IR thermal measurements, the inspected devices have been prepared and fully characterized. The top molding compound has been removed from the tested devices without changing their characteristics. Moreover, the IGBT has been electrically and thermally evaluated. To assess the IR experimental results, an accurate electro-thermal model of the test circuit is presented and validated by electrical measurements. The power losses extraction from electrical and IR measurements presented a satisfactory agreement, with an improved performance for IR measurements as the die-level thermal behavior is not affected by electrical couplings. In addition, it is also obtained a good match between simulation and electrical measurements in terms of the parasitic elements modeling and power losses calculation.

The main results found in this article are the following. From the comparison of IR and electrical measurements, the inclusion of $C_{\rm snub}$ in the test circuit (i.e., hard- and soft-switched DUT) influences in the extracted power losses differently depending on whether the ZVS condition is fulfilled. Within the ZVS condition, hard-switched devices present higher losses, whereas when outside ZVS, this situation is reversed. On the other hand, the spectral component of the surface thermal map at $f_{\rm Sw}$ points out current crowding phenomena close to the bonding wires. In addition, when $P_{\rm Sw} \neq 0$ or hard-switching is considered, a temperature increase is observed at the edge termination of the device, as the high current and voltage levels coexist during commutation. Within the ZVS condition, the type of switching does not affect the thermal behavior of the device when $f_{\rm Sw}$ is set close to $f_{\rm res}$, but when outside, the dissipated power is higher for the soft-switched case. This is due to the fact that $P_{\rm Sw}$ is substantially reduced when $C_{\rm snub}$ is removed, induced by the faster dV_{CE}/dt, whereas $P_{\rm On}$ is lower due to the reduced oscillations. A similar behavior is obtained when switching conditions are set in accordance to domestic IH applications, with the exception of an improved thermal behavior when the IGBTs are soft-switched and operated under the ZVS condition.

Thus, the technique presented in this article offers new solutions to inspect, at the die-level, typical situations of power devices under real operating conditions in two ways. First, this approach has a great potential for power losses calculation in high speed switching power devices, avoiding the use of current and voltages transducers whose parasitics usually introduce noise to performed measurements. Moreover, this method is also valid for power losses measurement in RF high power amplifiers. Second, the reliability impact of abnormal situations during the use of the inverter can be studied with the current distribution analysis at the switching frequency. For instance, several aspects related with packaging parasitics or the optimization of bonding wire attachment to the die top surface can be addressed.

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