Half-Bridge Integrated Phase-Shifted Full-Bridge Converter With High Efficiency Using Center-Tapped Clamp Circuit for Battery Charging Systems in Electric Vehicles

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***Abstract*—In this article, a half-bridge (HB) integrated phase-shifted full-bridge (PSFB) converter with a new center-tapped clamp circuit is proposed to achieve high efficiency in electric vehicle battery charging systems. The proposed converter has the benefits of HB integrated PSFB converters, such as the extended zero-voltage-switching range and the reduced conduction loss on the primary side. In addition, by using a new center-tapped clamp circuit, which consists of two diodes and one capacitor, the proposed converter can solve the drawbacks of conventional PSFB converters, such as the substantial circulating current, the severe voltage stress and switching loss in the secondary full-bridge rectifier, and a large output inductor. With these improvements, the efficiency is fairly increased, and the volume of the output inductor is reduced. In order to validate the feasibility of the proposed converter, a 3.3-kW prototype was built and tested.**

***Index Terms*—Circulating current, clamp circuit, electric vehicle (EV), on-board battery charger (OBC), phase-shifted full-bridge (PSFB) converter, zero-voltage and zero-current switching.**

I. Introduction

As THE awareness of global warming and resource depletion increases, there is a growing interest in the sales of ecofriendly electric vehicles (EVs) [1]. A high-voltage rechargeable battery pack is used as energy sources for EVs and is charged through an on-board battery charger (OBC). An OBC is generally made up of a power-factor-corrector (PFC) stage and a dc–dc stage [2]. A PFC stage improves the quality of the input current and regulates the dc bus voltage from the utility grid. A PFC stage is followed by a dc–dc stage, which provides a galvanic isolation between the utility grid and the battery pack and recharges the high-voltage battery pack within the range of 270–420 V.

An *LLC* converter can be a candidate for dc–dc stage in OBC, due to simple structure and the capability of zero-voltage switching (ZVS). However, it has difficulty in operating in a very wide range of output voltage [16]. A phase-shifted full-bridge (PSFB) converter is the most popular topology in the power range of a few kilowatts (1–7 kW) for OBCs [3], [4], due to the capability of ZVS, simple pulsewidth modulation (PWM) control with a fixed switching frequency, and the small rms current of the output capacitor. However, there are drawbacks that need to be resolved. First drawback is the narrow ZVS range for the lagging-leg switch [5], [6]. In order to expand the range of ZVS, the magnetizing inductance L_m should be decreased to increase the energy for ZVS. However, the conduction loss in the primary side can be increased by large rms current. Second drawback is the significant circulating current in the primary side during the freewheeling interval [7], [8]. The circulating current results in a large conduction loss on the primary side and a large turn-OFF switching loss in the lagging-leg switch due to the high turn-OFF current. Third drawback is the large output inductor L_O, increasing the volume and the cost [9], [10]. Fourth drawback is the severe voltage overshoot across a secondary full-bridge rectifier (FBR) [11], [12]. The severe voltage stress results in a large conduction loss in the FBR due to the higher forward-voltage drop V_F of high voltage-rated diodes. Fifth drawback is the significant turn-OFF crossover switching loss $P_{\rm cross}$ in the FBR, where $P_{\rm cross}$ is obtained by multiplying the reverse-recovery current $i_{\rm RR}$ and the reverse voltage of the FBR [13], [20]–[22]. These drawbacks become more serious in OBC applications, where the output voltage is very high, and the range of the output voltage is very wide.

In [14]–[19], half-bridge (HB) integrated PSFB converters have been proposed. This integrated converter is attractive, in which they can overcome some drawbacks of the conventional PSFB converter, such as the narrow range of ZVS for the

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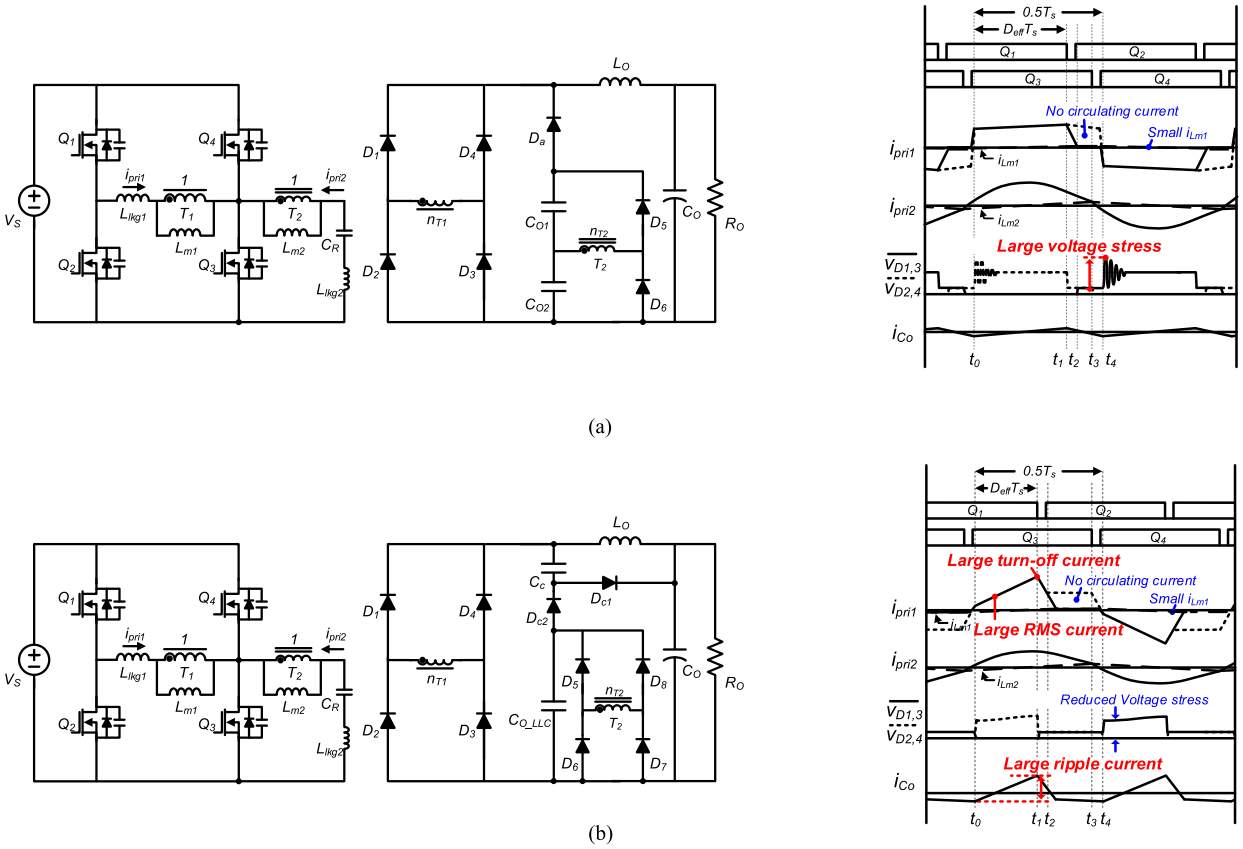

Fig. 1. Previous studies of HB *LLC* integrated PSFB converters. (a) Without clamping circuit [15]. (b) With CDD clamping circuit [19].

lagging-leg switch, the severe circulating current in the primary side, and the large L_O. However, there are still limitations in [14]–[19]. The converters in [14]–[16] cannot clamp the voltage overshoot in the FBR for the PSFB converter, because there is no clamping circuit, as shown in Fig. 1(a). Thus, an additional resistor–capacitor–diode (RCD) circuit is required, causing a large loss in the snubber resistor. In order to solve the aforementioned limitations, a lossless capacitor–diode–diode (CDD) clamp circuit was applied in [17]–[19], as shown in Fig. 1(b). The CDD clamp circuit can clamp the voltage overshoot in the FBR, enabling the use of low voltage-rated diodes. However, the CDD clamp circuit has serious limitations in which there is a current path directly flowing into the output capacitor without passing through L_O, which corresponds to the path through D_{C1} in Fig. 1(b). This makes the converters operate like an output inductorless PSFB converter, causing some problems. The first problem is large rms current and large turn-OFF current due to triangular-shaped current waveform, as shown on the right side in Fig. 1(b). Consequently, since the conduction losses in the primary side and the secondary side are increased, and the turn-OFF switching loss in the leading-leg switch is increased, the efficiency is considerably degraded. The second problem is the significantly increased burden of the output capacitor. This is because substantial current directly flows into the output capacitor without passing through L_O. In order to meet the rating of the rms current in the output capacitor, the volume of the capacitor must be increased, resulting in a low power density and a high cost. In addition, the clamping capacitor is additionally required. Thus, the volume and the cost for the clamping circuit are increased, when compared to the proposed converter.

In this article, a new HB integrated PSFB converter with a center-tapped clamp circuit is presented. The proposed clamp circuit consists of two diodes and one capacitor, and it is connected to the center tap of the transformer on the secondary side. The proposed converter has all the benefits of the previously reported converters in [14]–[19], such as an extended ZVS range of the lagging-leg switch, no circulating current, reduced L_O, clamped voltage overshoot in the FBRs, and the reduced P_{cross} in the FBRs. In addition, since all current flowing into the output capacitor flows through L_O, there are no side effects such as large rms current, large peak current, and large output capacitor. As a result, the proposed converter achieves high efficiency with compact size when compared to the previous researches. In addition, the clamping capacitor is not additionally required, because the output capacitor for the HB converter is also used for the clamping capacitor. Thus, the volume and the cost for the clamping circuit can be further saved, when compared to the previously reported converters, using the CDD clamp circuit in [17]–[19]. The aforementioned characteristics are summarized in Table I.

TABLE I
COMPARISON OF THE CHARACTERISTICS FOR THE PROPOSED CONVERTER WITH THE PREVIOUS RESEARCH

Index	[14]	[15]	[16]	[17]	[18]	[19]	Proposed
Maximum voltage stress on FBR	nV_S+ *ringing*	nV_S+ *ringing*	nV_S+ *ringing*	nV_S	nV_S	nV_S	nV_S
Output capacitor	Small	Small	Small	Very large	Very large	Very large	Small
Clamping circuit	RCD clamp	RCD clamp	RCD clamp	CDD clamp	CDD clamp	CDD clamp	Proposed clamp
Number of additional components	8	10	10	10	10	10	10
Total volume of additional components [cm^3]	95	112	116	124	162	120	82

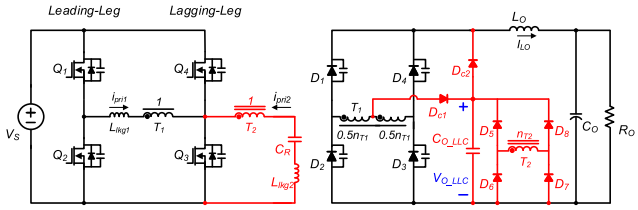

Fig. 2. Circuit diagram of the proposed converter.

II. OPERATION PRINCIPLE

The circuit configuration of the proposed converter is shown in Fig. 2. As shown in the figure, an HB *LLC* converter is integrated into the conventional PSFB converter: 1) in the primary side, the lagging-leg switches are shared; 2) in the secondary side, an FBR for the *LLC* converter is connected in parallel with the FBRs for the PSFB converter. Among several types of resonant tanks, *LLC* topology was employed because it has much higher efficiency due to the availability of ZVS operation and the reduced circulating current [23]. Especially, the proposed clamp circuit, which is composed of two diodes D_{C1} and D_{C2} and the output capacitor of *LLC* converter C_{O_LLC}, is connected to the secondary center tap of the PSFB transformer T_1. The key waveforms are shown in Fig. 3. Each switching period T_s consists of two half-cycles. In this article, only one half-cycle is explained due to its symmetrical operations. A half-cycle is subdivided into seven modes, and the equivalent circuits are shown in Fig. 4. For simplicity, several assumptions are made as follows.

1) The output capacitance of *LLC* converter C_{O_LLC} is large enough to be considered as a constant-voltage (CV) source during T_s.
2) The magnetizing inductance for the PSFB converter L_{m1} is large enough so that the magnetizing current i_{Lm1} is zero.
3) The switch devices are ideal MOSFETs, except for the junction capacitors and the internal body diodes.
4) The junction capacitors of all MOSFETs have the same capacitance of $C_{\rm OSS}$.
5) The junction capacitances of the clamping diodes D_{C1} and D_{C2} and the secondary rectifier diodes for *LLC* converter D_5, D_6, D_7, and D_8 are small enough to be ignored because their voltage rating is much lower than that for FBRs.
6) The external inductor $L_{\rm ext}$ is included into the leakage inductor of the PSFB converter $L_{\rm lkg1}$.

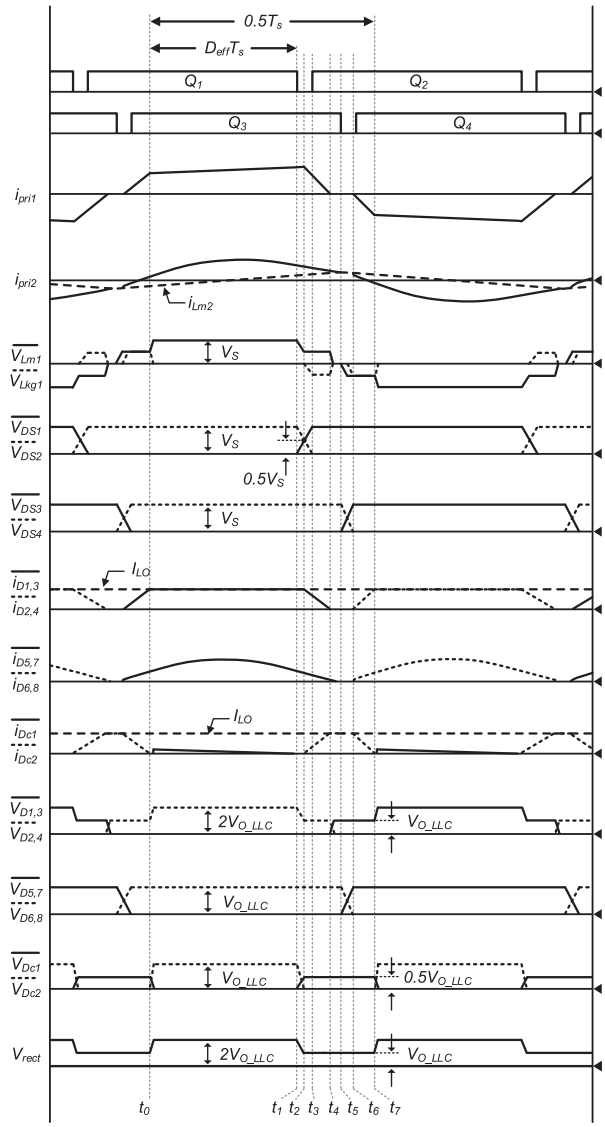

Fig. 3. Key waveforms of the proposed converter.

Mode 1 [t_0–t_1]: This mode begins when the commutation from the clamping diode D_{C2} to the FBR diodes D_1 and D_3 is ended. During this mode, the power is delivered to the output through T_1 and L_O in the same manner of the conventional PSFB converter. At the same time, C_{O_LLC} is charged with the resonant current by the leakage inductor $L_{\rm lkg2}$ and the resonant

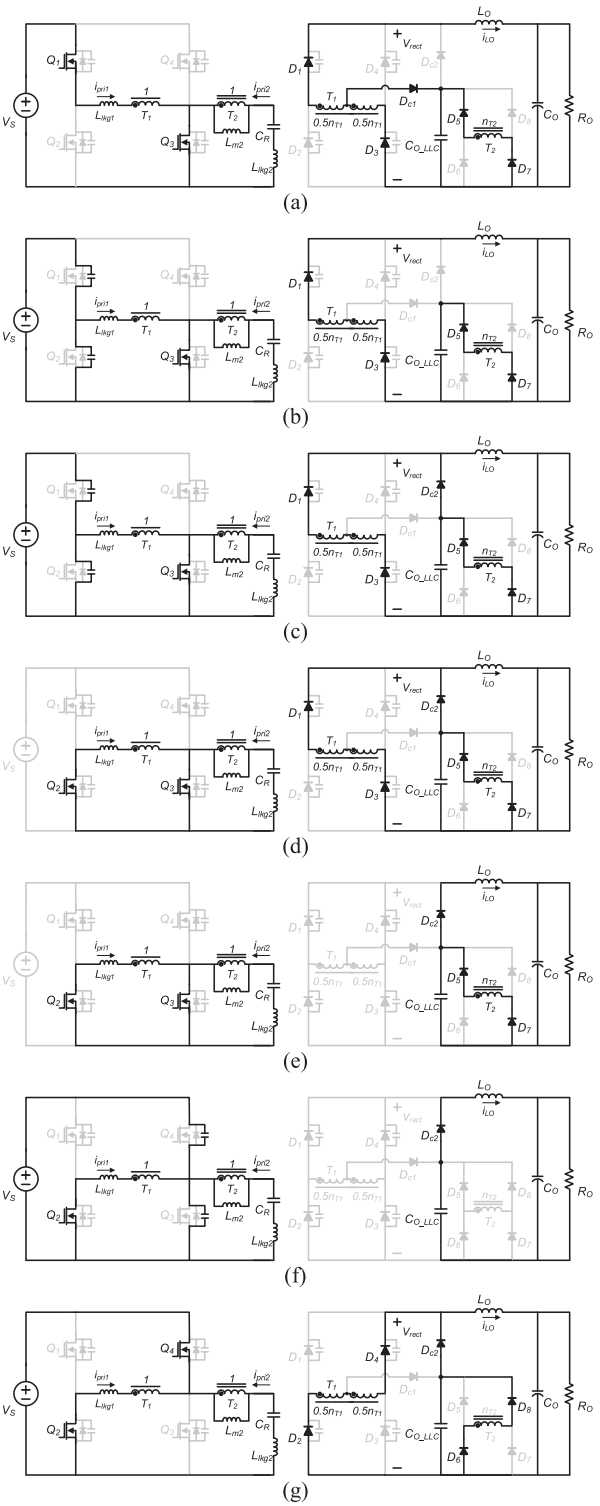

Fig. 4. Equivalent operating circuits of the proposed converter. (a) Mode 1 (t_0–t_1). (b) Mode 2 (t_1–t_2). (c) Mode 3 (t_2–t_3). (d) Mode 4 (t_3–t_4). (e) Mode 5 (t_4–t_5). (f) Mode 6 (t_5–t_6). (g) Mode 7 (t_6–t_7).

capacitor C_R. In this mode, the proposed clamping circuit is utilized to clamp the voltage stress of FBR. Since the clamping diode D_{C1} is turned ON, providing a clamping path, the voltage at the secondary center tap of T_1 is clamped to the output voltage of *LLC*, V_{O_LLC}. This enables the secondary rectifier output voltage $V_{\rm rect}$ to be clamped to $2V_{O\_LLC}$. Thus, it is noted that the maximum voltage stress on the FBR is clamped to $2V_{O\_LLC}$, and the voltage oscillation is eliminated, as shown in Fig. 3. Consequently, the proposed clamp circuit enables the use of lower voltage-rated diodes, resulting in a reduced conduction loss in FBRs. The primary current in the PSFB converter $i_{\rm pri1}$ can be expressed as follows:

$$\begin{aligned} i_{\rm pri1}(t) &= i_{\rm pri1}(t_0) + \frac{V_{\rm Lkg1}}{L_{\rm lkg1}}(t-t_0) \\ &= i_{\rm pri1}(t_0) + \frac{n_{T1}V_S - 2V_{O\_LLC}}{n_{T1}L_{\rm lkg1}}(t-t_0) \end{aligned} \quad (1)$$

where n_{T1} is the turns ratio of the secondary side to the primary side for T_1, $V_{\rm Lkg1}$ is the voltage across $L_{\rm lkg1}$, and V_S is the input voltage.

Mode 2 [t_1–t_2]: Mode 2 begins when the leading-leg switch Q_1 is turned OFF. The junction capacitors of switches Q_1 and Q_2 are charged or discharged by $i_{\rm pri1}$, where $i_{\rm pri1}$ is equal to the primary-reflected output current. In this mode, the ZVS energy comes from L_O in the same manner of the conventional PSFB converter so that $i_{\rm pri1}$ does not change.

Mode 3 [t_2–t_3]: Mode 3 starts when the clamping diode D_{C2} is turned ON. From this mode, freewheeling is started and maintained until mode 7, where clamping diode D_{C2} is turned ON. By turning ON D_{C2}, the voltage across the L_O becomes $V_{O\_LLC}-V_O$, rather than $-V_O$. Thus, much reduced voltage is applied to the output inductor, resulting in a reduced L_O. Thus, the proposed clamp circuit enables the use of much reduced L_O, improving the power density. In addition, since the voltage across L_O is clamped to $V_{O\_LLC} - V_O$, L_O does not participate the resonance for ZVS operation. Thus, the procedure for ZVS is completed by the energy stored in $L_{\rm lkg1}$.

Mode 4 [t_3–t_4]: In this mode, commutation from the FBR diodes to the clamping diode D_{C2} is occurred. Since D_{C2} is turned ON, V_{O_LLC} is reflected to the primary side, and $V_{\rm Lkg1}$ is equal to $-V_{O\_LLC}/n_{T1}$. With the negative $V_{\rm Lkg1}$, $i_{\rm pri1}$ is decreased. Here, there is no circulating current, because the power is still being transferred to the secondary side. Thus, the proposed clamp circuit eliminates the circulating current on the primary side, resulting in a reduced conduction loss. In addition, since $V_{\rm Lkg1}$ is $0.5V_S$, which is half as compared to that in the conventional PSFB converter, the slope of the decreasing $i_{\rm pri1}$ is moderate. This causes the slope of the current in the FBR di_D/dt to be moderate. Consequently, the proposed clamp circuit reduces $i_{\rm RR}$ in the FBR [20]–[22].

During this mode, the commutation occurs from D_1 and D_3 to D_{C2}. The duration of this mode can be expressed as follows:

$$\Delta t_{3-4} = t_4 - t_3 = \frac{n_{T1}^2 I_O L_{\rm lkg}}{V_{O\_LLC}}. \quad (2)$$

Mode 5 [t_4–t_5]: Mode 5 begins when D_1 and D_3 are turned OFF. In this mode, since clamping diode D_{C2} is turned ON, the reverse voltages of D_1 and D_3 are increased up to V_{O_LLC}, which is considerably lower value compared with that in conventional PSFB converters. Thus, $P_{\rm cross}$ in D_1 and D_3 is substantially reduced due to the low reverse voltages and the reduced $i_{\rm RR}$.

Consequently, the proposed clamp circuit reduces $P_{\rm cross}$. Moreover, in this freewheeling interval, $V_{\rm rect}$ is equal to V_{O_LLC} rather than zero. Thus, much lower voltage is applied to L_O, and the burden of L_O can be substantially relieved.

Mode 6 [t_5–t_6]: This mode begins when the lagging-leg switch Q_3 is turned OFF. Since i_{Lm1} was assumed to be zero due to the large value of L_{m1}, $i_{\rm pri1}$ is equal to zero. Thus, the PSFB converter does not participate the ZVS operation for the lagging-leg switch. Instead, the ZVS operation is achieved by the HB *LLC* converter. In addition, the turn-OFF switching loss in Q_3 is considerably reduced due to the low turn-OFF current by the eliminated circulating current.

Mode 7 [t_6–t_7]: This mode begins when the drain–source voltage for Q_4 V_{DS4} reaches zero. In this mode, commutation from D_{C2} to the FBR diodes is occurred. Since D_{C2} is turned ON, V_{O_LLC} is reflected to the primary side, and $V_{\rm Lkg1}$ becomes equal to $-(V_S - V_{O\_LLC}/n_{T1})$. With the negative $V_{\rm Lkg1}$, $i_{\rm pri1}$ started to increase in the negative direction. Here, there is no duty-cycle loss, because V_{Lm1} the power is still being transferred to the secondary side. Thus, the proposed clamp circuit eliminates the duty-cycle loss. At the same time, the resonance between $L_{\rm lkg2}$ and C_R is started, and C_{O_LLC} is charged. During this mode, the commutation from D_{C2} to D_2 and D_4 occurs. Duration of this mode can be expressed as follows:

$$\Delta t_{6-7} = t_7 - t_6 = \frac{n_{T1}^2 I_O L_{\rm lkg}}{n_{T1} V_S - V_{O\_LLC}}. \tag{3}$$

III. Steady-State Analysis

For simple illustration, it is assumed that the duration of the deadtime is narrow enough to be ignored. In this article, the analysis of output filter, circulating current, and $P_{\rm cross}$ in the FBR is omitted, because a similar analysis is well explained in the previous study [12].

A. Voltage Gain

The output voltage V_O is regulated by the phase-shifted PWM with a fixed switching frequency f_S. From Figs. 3 and 4, V_O can be obtained as the averaged voltage of $V_{\rm rect}$ as follows:

$$V_O = V_{O\_LLC}\,(1 + 2D_{\rm eff}) \tag{4}$$

where $D_{\rm eff}$ is the effective duty cycle.

Since the secondary rectifier for *LLC* converter is an FBR, V_{O_LLC} can be obtained as follows:

$$V_{O\_LLC} = n_{T2} V_S M_{LLC} \tag{5}$$

where n_{T2} is the turns ratio of the secondary side to the primary side for the *LLC* transformer T_2, and M_{LLC} is the gain of the HB *LLC* converter.

In this article, the *LLC* converter operates at the resonant frequency f_R to reduce the primary rms current, and to avoid the switch turn-OFF loss and the reverse-recovery problem in the secondary diodes. Thus, with the fixed f_S at f_R, M_{LLC} is equal to 0.5. In that, the achievable minimum voltage stress on the FBR is nT_1V_S, where the voltage overshoot is eliminated, the voltage stress can be minimized by designing the maximum voltage stress of $2V_{O\_LLC}$ to be equal to nT_1V_S. Thus, using (5), n_{T2} is designed to be equal to n_{T1}.

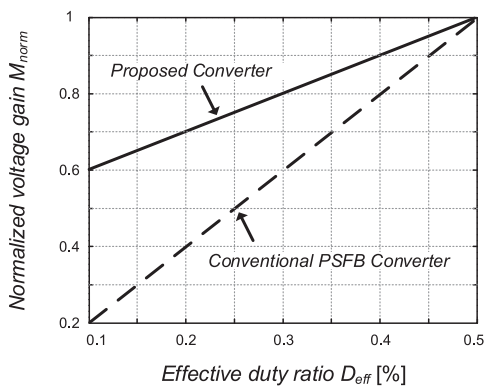

Fig. 5. Normalized voltage gain $M_{\rm norm}$ according to $D_{\rm eff}$.

Finally, from (4) and (5), the voltage gain M is given by

$$M = \frac{V_O}{V_S} = n_{T1}(0.5 + D_{\rm eff}). \tag{6}$$

Normalized voltage gain $M_{\rm norm}$, where n_{T1} is supposed to be 1, is shown in Fig. 5. The figure shows that the proposed converter can achieve a higher voltage conversion ratio for the same $D_{\rm eff}$.

B. Comparison With the Previous Research

Among the previous research works of [14]–[19], the research in [19] is the most similar to this article, in which PSFB stage and HB *LLC* stage are connected in parallel, and it utilized clamp circuit, as shown in Fig. 1(b). Fig. 6 shows the key waveforms of the previous research [19] and the proposed converter. Here, it is assumed that L_m and L_O are large enough, so that i_{Lm} is zero, and the output inductor current has the constant value of I_O. In the case of [19], as shown in Fig. 6(a), the primary current $i_{\rm pri1\_CDD}$ is sharply increasing during $t_A - t_B$. Fig. 7 shows the equivalent circuits of [19] and the proposed converter during $t_A - t_B$. In the case of [19], as shown in Fig. 7(a), since $V_C + V_O$ is reflected to the primary side, $V_{\rm Lkg1}$ is equal to $V_S - (V_C + V_O)/n_{T1}$. Thus, $i_{pri1\_\rm CDD}$ can be expressed as follows:

$$\begin{aligned} i_{\rm pri1\_CDD}(t) &= i_{\rm pri1\_CDD}(t_A) + \frac{V_{\rm Lkg1}}{L_{\rm lkg1}}(t - t_A) \\ &= i_{\rm pri1\_CDD}(t_A) + \frac{n_{T1}V_S - (V_C + V_O)}{n_{T1}L_{\rm lkg1}}(t - t_A). \end{aligned} \tag{7}$$

From (7), it can be noted that as V_O is decreased, the slope of $i_{\rm pri\_CDD}$ is increased. Thus, the rms current and the turn-OFF current in primary side are substantially increased due to the triangular-shaped current waveform. Consequently, the conduction loss on the primary side is increased, and the turn-OFF switching loss in the leading-leg switch is increased, resulting in a degraded efficiency. In addition, since this large current directly flows into the output capacitor through the clamping diode D_{C2}, the volume of the capacitor is considerably increased. On the

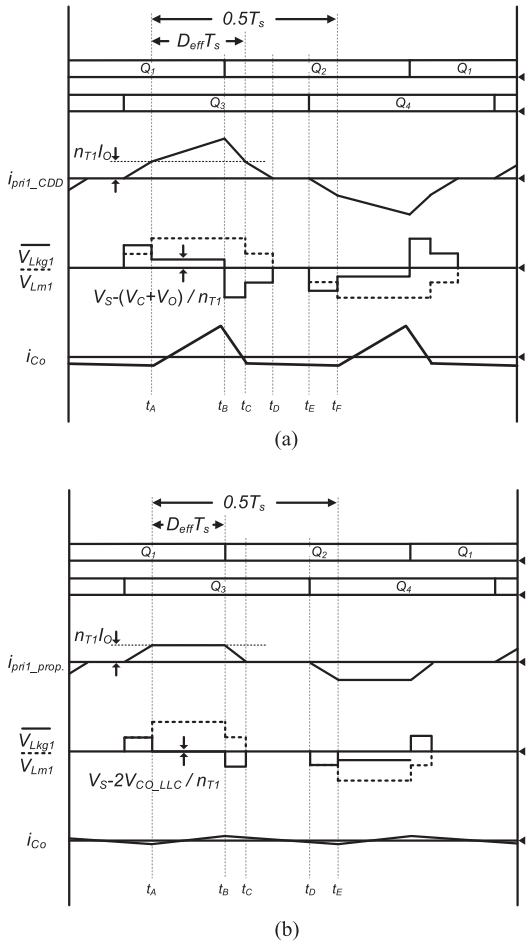

Fig. 6. Key waveforms for the analysis of the performance with the previous study. (a) Previous research in [19]. (b) Proposed converter.

other hand, in the proposed converter, as shown in Fig. 6(b), the primary current $i_{\text{pri1\_prop.}}$ is almost constant during $t_A - t_B$. Fig. 7(b) shows the equivalent circuit of the proposed converter. As shown in the figure, V_{Lkg1} is equal to $V_S - 2V_{O\_LLC}/n_{T1}$. Thus, $i_{\text{pri1\_prop.}}$ can be expressed as follows:

$$\begin{aligned} i_{\text{pri1\_prop.}}(t) &= i_{\text{pri1\_prop.}}(t_A) + \frac{V_{\text{Lkg1}}}{L_{\text{lkg1}}}(t - t_A) \\ &= i_{\text{pri1\_prop.}}(t_A) + \frac{n_{T1}V_S - 2V_{O\_LLC}}{n_{T1}L_{\text{lkg1}}}(t - t_A). \end{aligned} \tag{8}$$

From (8), since V_{O_LLC} is designed to be equal to $0.5n_{T1}V_S$, the slope of $i_{\text{pri\_prop.}}$ is almost zero. Thus, the rms current and the turn-OFF current in primary side are substantially reduced compared to the case in [19]. Consequently, the conduction loss and the turn-OFF switching loss can be fairly reduced, increasing the efficiency. In addition, since all current flows through the output inductor, the volume of the capacitor is considerably decreased.

IV. Design Consideration

In order to validate the feasibility of the proposed converter, a design example is presented. The specifications are as follows: $V_S = 385$ V, $V_O = 270$–420 V, the charging current during constant-current (CC) mode or the maximum output current $I_{O,\max} = 7.85$ A, and $f_s = 50$ kHz. For simple illustration, it is assumed that the magnetizing inductance for the PSFB converter L_{m1} is large enough, so that i_{Lm1} is zero, and the output capacitances of secondary diodes are small enough to be ignored.

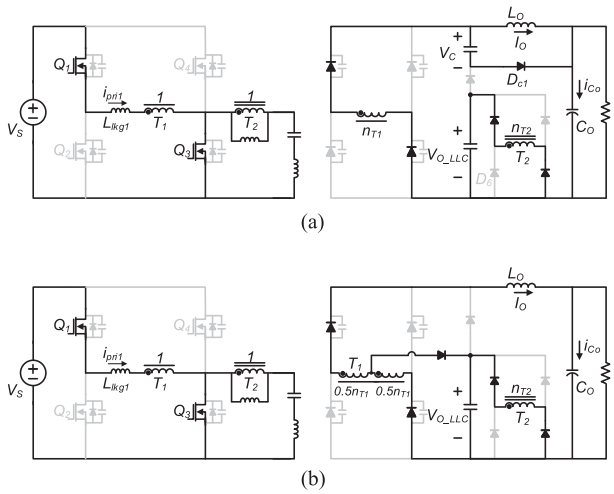

Fig. 7. Equivalent operating circuits during $t_A - t_B$. (a) Previous research in [19]. (b) Proposed converter.

A. Transformer Turns Ratios n_{T1} and n_{T2}

n_{T1} can be obtained through a relational expression with the voltage gain. Since $n_{T1}V_S M_{\text{norm,max}}$ should be larger than the maximum output voltage $V_{O,\max}$, where $M_{\text{norm,max}}$ is the achievable maximum value of M_{norm}, n_{T1} can be expressed as follows:

$$n_{T1} > \frac{1}{M_{\text{norm,max}}}\frac{V_{O,\max}}{V_S}. \tag{9}$$

From (9), it can be noted that, if $M_{\text{norm,max}}$ is supposed to be 0.9, n_{T1} should be larger than 1.21. In this article, n_{T1} is designed as 1.24 by considering the effects of parasitic components such as the voltage drop in the current path.

As for n_{T2}, it is designed to be equal to n_{T1} by considering the maximum voltage stress on the FBRs V_{D_Prop}.

B. Transformer Leakage Inductor L_{lkg1} to Achieve ZVS for Leading-Leg Switches

As shown in Figs. 3 and 4, the ZVS for the leading-leg switch is achieved through two modes: mode 2 and mode 3. In mode 2, the ZVS energy comes from L_O, so that i_{pri1} does not change. Mode 3 starts when the clamping diode D_{C2} is turned ON. Since the voltage across L_O is clamped to $V_{O\_LLC} - V_O$, L_O does not participate in the resonance for ZVS operation. Thus, the procedure for ZVS is completed by the energy stored in L_{lkg1}. The ZVS condition can be obtained as follows:

$$\frac{1}{2}L_{\text{lkg1}}i_{\text{pri1}}(t_2)^2 > C_{\text{oss}}(V_S - V_{O\_LLC}/n_{T1})^2 \tag{10}$$

where

$$i_{\rm pri}(t_2) = I_O/n_{T1} \tag{11}$$

$$V_{O\_LLC} = 0.5 n_{T1} V_S. \tag{12}$$

By substituting (11) and (12) for $i_{\rm pri1}(t_2)$ and V_{O_LLC}, respectively, (10) can be represented as follows:

$$L_{\rm lkg1} > \frac{C_{\rm oss}}{2}\left(\frac{n_{T1}V_S}{I_O}\right)^2. \tag{13}$$

From (13), it can be noted that the condition for $L_{\rm lkg1}$ to guarantee ZVS operation of leading-leg switches is dependent on the load condition. For example, in order to ensure the ZVS operation above 10% load conditions, $0.1\,I_{O,\max}$ is substituted for I_O. Then, $L_{\rm lkg1}$ should be designed to be larger than 13 μH.

C. Transformer Magnetizing Inductor L_{m2} to Achieve ZVS for Lagging-Leg Switches

Mode 6 in Figs. 3 and 4 illustrates the ZVS operation for the lagging-leg switch. Since i_{Lm1} was assumed to be zero due to the large value of L_{m1}, $i_{\rm pri1}$ is equal to zero. Thus, the PSFB converter does not contribute the ZVS operation for the lagging-leg switch. Instead, the ZVS operation is achieved by the HB *LLC* converter. Thus, the ZVS condition can be obtained as follows:

$$i_{Lm2}(t_5) T_{\rm dead} > 2 C_{\rm oss} V_S \tag{14}$$

where $T_{\rm dead}$ is the deadtime.

Since the resonant frequency f_R for the *LLC* converter is equal to the f_s, $i_{Lm2}(t_5)$ can be expressed as follows:

$$i_{Lm2}(t_5) = \frac{1}{4}\frac{V_{O\_LLC}\cdot T_S}{n_{T2} L_{m2}} = \frac{V_S}{8 f_s L_{m2}}. \tag{15}$$

By substituting (15) for $i_{Lm2}(t_5)$, (14) can be presented as follows:

$$L_{m2} < \frac{T_{\rm dead}}{16 f_s C_{\rm OSS}}. \tag{16}$$

From (16), it can be noted that the condition for L_{m2} to guarantee ZVS operation of lagging-leg switches is independent of both the load condition and the $D_{\rm eff}$. Thus, the selection of L_{m2} is very simple. In addition, since the magnetizing current flows only as required for the ZVS operation regardless of $D_{\rm eff}$, the conduction loss resulting from the magnetizing current can be much reduced.

D. Resonant Capacitor C_R

C_R can be designed by considering the resonant period. Since the f_R for the *LLC* converter is equal to the f_s, C_R can be designed as follows:

$$C_R = \left(\frac{1}{2\pi f_S}\right)^2 \frac{1}{L_R} \tag{17}$$

where $L_{\rm lkg2}$ can be simply implemented as the leakage inductor of T_2.

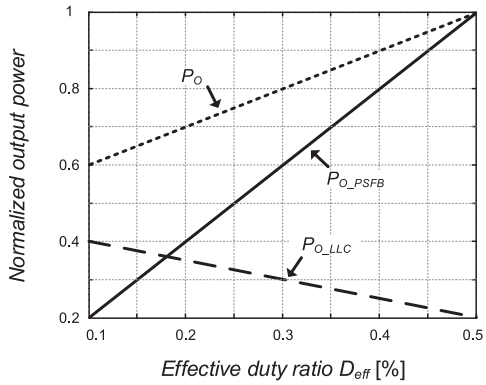

Fig. 8. Normalized output power according to $D_{\rm eff}$.

E. Cost and Volume of LLC Stage Compared to PSFB Stage

In the proposed converter, an *LLC* stage is integrated into a PSFB stage. In the view of the power transfer to the load, two power stages are connected in parallel. During $D_{\rm eff}T_S$, the power is transferred through PSFB stage, and during $(0.5 - D_{\rm eff}T_S)$, the power is transferred through *LLC* stage. Thus, the output power of each power stage can be expressed as follows:

$$\begin{aligned} P_{O\_\rm PSFB} &= V_{\rm rect\_Deff}\cdot\langle I_{O\_\rm Deff}\rangle_{Ts} \\ &= (n_{T1}V_S)\cdot\left(I_O\frac{D_{\rm eff}}{0.5}\right) = 2D_{\rm eff}I_O n_{T1}V_S \\ P_{O\_\rm LLC} &= V_{\rm rect\_(0.5-Deff)}\cdot\langle I_{O\_(0.5-\rm Deff)}\rangle_{Ts} \\ &= (0.5 n_{T1}V_S)\cdot\left(I_O\frac{0.5-D_{\rm eff}}{0.5}\right) \\ &= (0.5 - D_{\rm eff})I_O n_{T1}V_S \end{aligned} \tag{18}$$

where $P_{O\_\rm PSFB}$ and P_{O_LLC} are the output power of PSFB converter and *LLC* converter, respectively, and $V_{\rm rect\_Deff}$ and $V_{rect\_(0.5-D\rm eff)}$ are the instantaneous secondary rectifier output voltage during $D_{\rm eff}T_S$ and $(0.5 - D_{\rm eff})T_S$, respectively, and $\langle I_{O\_D\rm eff}\rangle_{Ts}$ and $\langle I_{O\_(0.5-D\rm eff)}\rangle_{Ts}$ are the averaged output current during $D_{\rm eff}T_S$ and $(0.5 - D_{\rm eff})T_S$, respectively.

From (18), the total output power P_O can be expressed as follows:

$$P_O = P_{O\_\rm PSFB} + P_{O\_LLC} = (0.5 + D_{\rm eff})I_O n_{T1}V_S. \tag{19}$$

From (18) and (19), the normalized output powers, where each power is divided by the maximum output power of $I_O n_{T1} V_S$, are shown in Fig. 8. From Fig. 8, it can be noticed that as $D_{\rm eff}$ is increased, $P_{O\_\rm PSFB}$ is increased. At the maximum $D_{\rm eff}$, almost P_O is transferred through PSFB converter. Thus, when designing the PSFB stage, the power transfer through *LLC* stage can be ignored, and the PSFB stage is designed in the same manner of the conventional PSFB converter. On the other hand, as $D_{\rm eff}$ is decreased, P_{O_LLC} is increased. Since P_{O_LLC} becomes the maximum value at the minimum $D_{\rm eff}$, the *LLC* stage is designed based on the maximum P_{O_LLC} at the minimum $D_{\rm eff}$. Thus, the relative cost and volume of the *LLC* stage compared to the PSFB stage are only dependent on the minimum $D_{\rm eff}$.

TABLE II
COMPONENTS LIST OF PROTOTYPE

Items		Pri. Clamp. PSFB converter	Conventional PSFB converter		Previous Converter [19]	Proposed Converter
			Si diode	SiC diode		
Main switch, Q_1–Q_4		IPP60R074C6 (600 V/31A/74 mΩ/500 pF)				
Transformer for PSFB converter, T_1		Core : PQ5050, L_m=880 μH, L_{lkg}=10 μH $n(N_p{:}N_s)$ = 1.3 (34:44), N_p: 0.1 mm × 150, N_s:0.1 mm × 120			Core : PQ5050, L_{m1} = 2.47 mH, L_{lkg1} = 8 μH $n_{T1}(N_{p1}{:}N_{s1})$ = 1.2 (34:42), N_{p1}: 0.1 mm × 150, N_{s1}:0.1 mm × 120	
External inductor, L_{ext}		Core : PQ2020, L_{ext} = 12 μH N_{ext} = 8 Turns (0.1 mm × 120)			Core : PQ2620, L_{ext} = 21 μH N_{ext} = 10 Turns (0.1 mm × 120)	
Output inductor, L_O		CH358060 × 2EA, L_O = 520 μH			CH358060 × 1 EA, L_O = 250 μH	
FBRfor PSFB converter, D_1–D_4		STTH1512D (1200 V/V_F = 2.0 V)		IDH15S120 (1200V/V_F = 2.2 V)	10ETF06 (600 V/20 A/V_F = 1.2 V)	
Output capacitor, C_O		Film Cap. (450 V, 4.5 A, 1.5 μF)			Film Cap. (450V, 24 A, 11 μF)	Film Cap. (450 V, 4.5 A, 1.5 μF)
HB LLC converter	Transformer, T_2	–			Core : PQ3230 L_{m2} = 527 μH, L_{lkg2} = 6.5μH $n_{T2}(N_{p2}{:}N_{s2})$ = 1.2 (27:34) N_{p2}: 0.1 mm × 80, N_{s2}: 0.61 mm × 120	
	Resonant capacitor, C_R				Film Capacitor (250 V, 680 nF) × 3EA	
	FBR, D_5–D_8				15ETH03 (300 V/15 A/V_F = 1.05 V)	
	Output capacitor, $C_{O\ LLC}$				Film cap. (250 V, 2 μF)	
Clamping circuit	Number of components	5	3	0	3	
	Diode	D_{Cp1} & D_{Cp2}: UF4005 (600V, 1.0 A), D_{snb} : HER108 (1000 V, 1.0 A)	D_{snb} : HER108 (1000V, 1.0A)	-	D_{C1}: 20CTH03 (300 V, 20 A), D_{C2}: U1540G (400 V, 15 A)	
	Capacitor	C_{snb} : Film Cap. (1250 V, 0.1 μF)	C_{snb} : Film Cap. (1250 V, 0.1 μF)		C_C : Film cap. (250 V, 0.2 μF)	-
	Resistor	R_{snb} = 41 kΩ	R_{snb} = 17 kΩ		-	

V. EXPERIMENTAL RESULTS

In order to validate the feasibility of the proposed converter, a 3.3-kW prototype has been built and tested through the charging processes of the CC mode and CV mode, following the battery charging profile in [12].

As a prototype, the converter in [4] using the clamping diode on the primary side was also conducted as a classical solution that reduces RCD snubber loss. In addition, the converter in [19] was also conducted as the most similar converter to the proposed converter. Table II lists the designed parameters. As can be seen in the table, when compared to the converter in [19], clamping capacitor C_C is not additionally required in the proposed converter, and the burden of the output capacitor is much reduced, saving the volume and the cost.

Fig. 9 shows the key waveforms in the CC mode where the range of V_O is from 270 to 420 V with I_O of 7.85 A, and Fig. 10 shows the key waveforms in the CV mode where the load condition is from 10% to 100% with V_O of 420 V. From the figures, there is no circulating current in the primary side, and the turn-OFF current in the lagging-leg switch is very low.

Fig. 11 shows the ZVS waveforms for lagging-leg switches. Fig. 11(a) shows the waveforms in the CC mode where V_O is 270 V with I_O of 7.85 A, and Fig. 11(b) shows the waveforms in the CV mode at 10% load condition. As can be seen in the figures, ZVS is well achieved.

Fig. 12 shows the key waveforms of [19] and the proposed converter in the CC mode where V_O is 270 V with I_O of 7.85 A. As can be seen in the figure, in the proposed converter, the rms current and the turn-OFF current are considerably reduced, resulting in higher efficiency. In addition, the current through the output capacitor i_{Co} is significantly reduced, resulting in a high power density with low cost.

Fig. 13 shows the measured efficiencies in the CC and CV modes. As can be seen in the figure, the proposed converter achieved much higher efficiency over the entire conditions.

The main reason for the higher efficiency comes from the reduction of the conduction loss and the turn-OFF switching loss in the primary switches Q_1–Q_4, and the reduction of the conduction loss and the $P_{\rm cross}$ in the FBRs D_1–D_4. Although primary clamping PSFB converter improved the efficiency by saving RCD snubber loss, it is still suffering from a severe $P_{\rm cross}$ and large conduction loss in the FBR.

Fig. 14 shows the loss distributions in the CC mode with I_O of 7.85 A at the V_O of 270 and 420 V. In the figure, *Pri. Cond.* is the sum of conduction losses in switches and windings in transformer T_1 on the primary side, and *Second. Cond.* is the sum of conduction losses in FBRs and windings in transformer T_1 on the secondary side. The *Integrated HB LLC* covers the conduction loss in the FBRs for *LLC* converter, the core loss in transformer T_2, and the conduction loss in the windings for T_2.

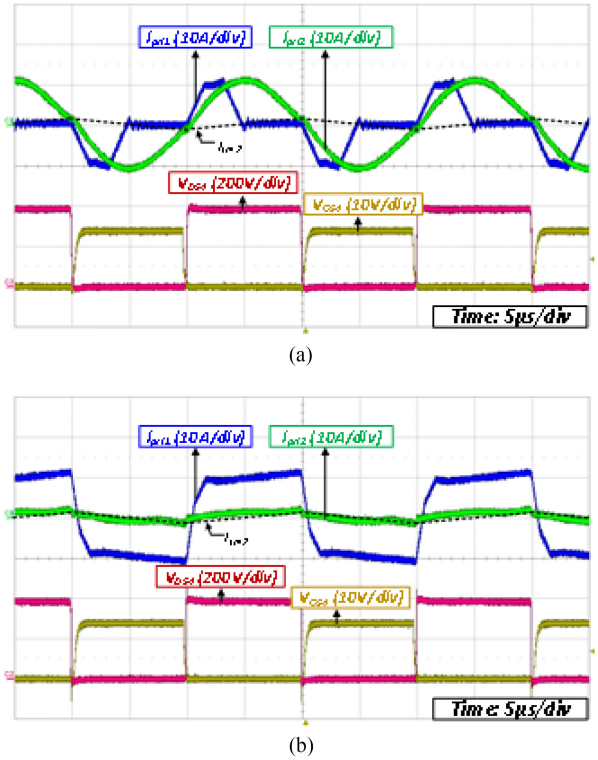

Fig. 9. Key waveforms of the proposed converter during CC mode with the I_O of 7.85 A. (a) $V_O = 270$ V. (b) $V_O = 420$ V.

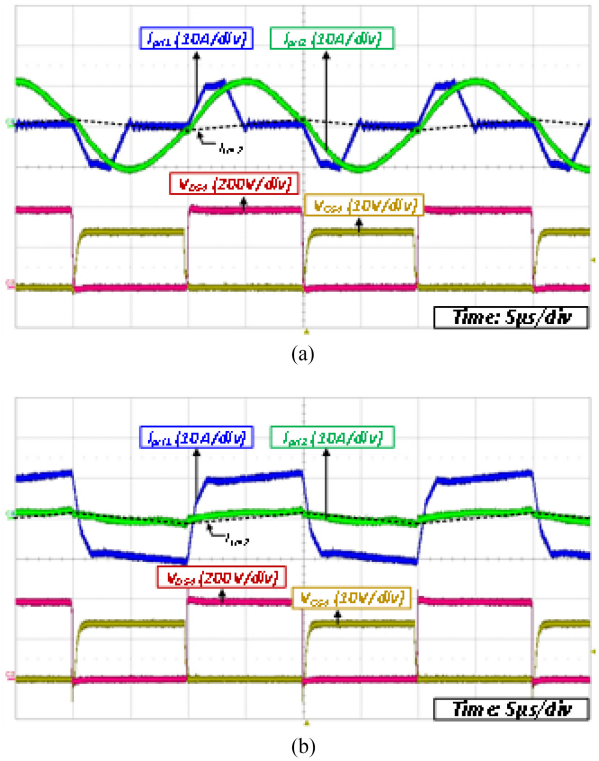

Fig. 10. Key waveforms of the proposed converter during CV mode with the V_O of 420 V. (a) 10% load condition. (b) 70% load condition.

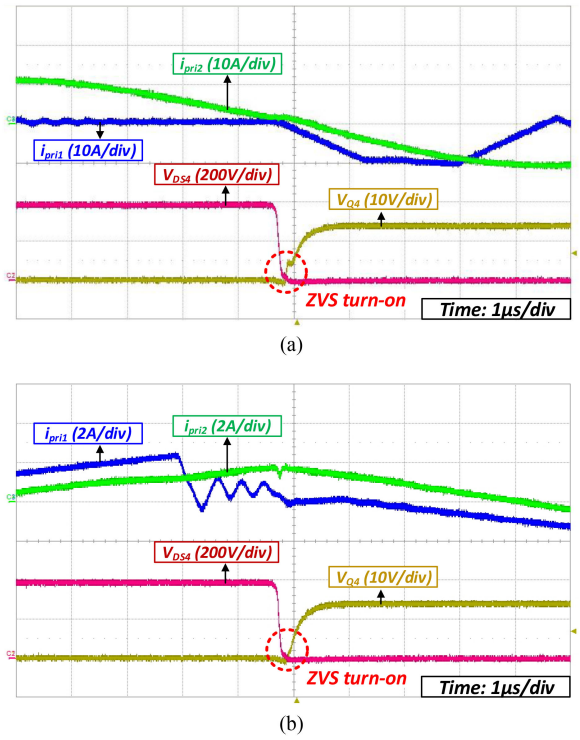

Fig. 11. ZVS waveforms of lagging-leg switches. (a) During CC mode with the I_O of 7.85 A and the V_O of 270 V. (b) During CV mode with the 10% load condition and the V_O of 420 V.

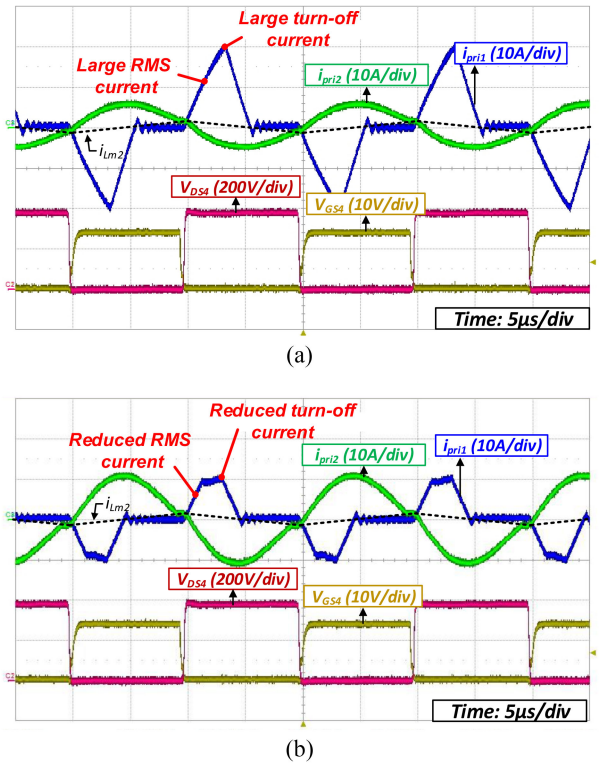

Fig. 12. Key waveforms of the proposed converter in the CC mode where V_O is 270 V with I_O of 7.85 A. (a) Previous research in [19]. (b) Proposed converter.

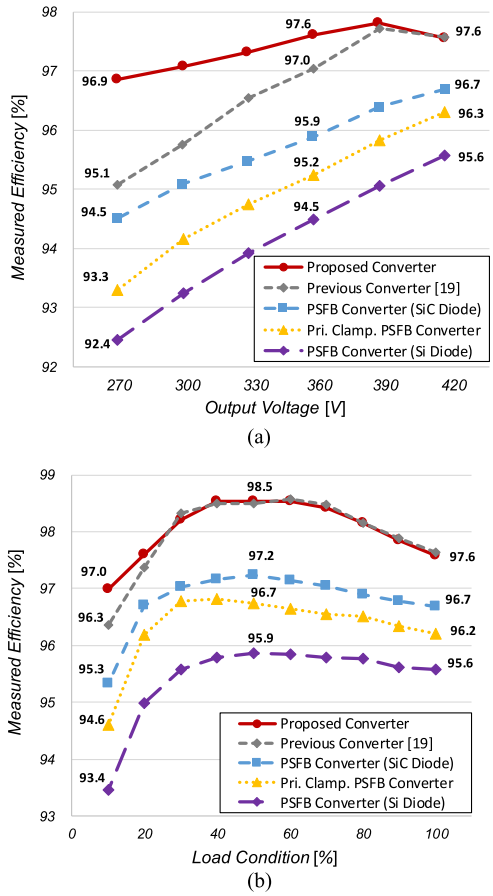

Fig. 13. Measured efficiency. (a) During CC mode with the I_O of 7.85 A. (b) During CV mode with the V_O of 420 V.

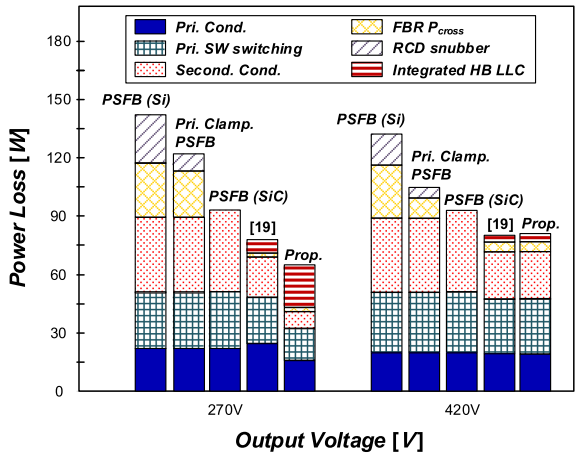

Fig. 14. Loss distributions during CC mode with the I_O of 7.85 A according to V_O.

In both cases of 270 and 420 V, in the proposed converter, the conduction loss on the secondary side and the $P_{\rm cross}$ in the FBR are significantly reduced, and the RCD snubber loss is eliminated. The conduction loss in FBRs is easily obtained by multiplying the averaged current on FBRs by V_F. The averaged current is almost the same in the proposed converter and in the conventional PSFB converter. Instead, different V_F makes a difference in the conduction loss. When SiC diodes are used for the FBRs in the conventional PSFB converter, the $P_{\rm cross}$ and the RCD snubber loss can be eliminated. However, the conduction loss in the FBR is increased due to the higher V_F. Especially, in the case of V_O of 270 V, the conduction loss and the switching loss in the primary switch SW are also significantly reduced in the proposed converter. Although the additional losses by the HB *LLC* converter, which covers the conduction loss in the FBRs for *LLC* converter, the core loss in transformer T_2, and the conduction loss in the windings for T_2 are increased at 270 V, the reduction of the losses in the FBR and the primary SW is more dominant.

Table III lists the comparisons of the volume and the cost, respectively. As can be seen in the tables, the volume and the cost of the proposed converter are similar to those of the PSFB converter with the clamping diode on the primary side and the conventional PSFB converter with Si diodes. This is because although there are additional components in the proposed converter, the size of the output inductor is reduced, the RCD clamp circuit is eliminated, and lower voltage-rated diodes are used for FBR. When compared to the converter in [19], the volume and the cost of the proposed converter are much reduced. This is because the current rating of the output capacitor is much reduced and the additional clamping capacitor is not required. In the case of the conventional PSFB converter with SiC diodes, the volume can be minimized because the RCD clamping circuit can be eliminated. However, the cost is considerably increased due to the expensive SiC diodes.

TABLE III
VOLUME AND COST FOR COMPONENTS OF PROTOTYPE

<table>
<tr><th colspan="2" rowspan="2">Items</th><th rowspan="2">Pri. Clamp. PSFB converter</th><th colspan="2">Conventional PSFB converter</th><th rowspan="2">Previous converter [19]</th><th rowspan="2">Proposed converter</th></tr>
<tr><th>Si diode</th><th>SiC diode</th></tr>
<tr><td colspan="2">External inductor, L_{ext}</td><td colspan="3">PQ2020: 6.2 cm^2, $ 0.8</td><td colspan="2">PQ2620: 10.7 cm^2, $ 1.3</td></tr>
<tr><td colspan="2">Output inductor, L_O</td><td colspan="3">CH358060 × 2EA: 55 cm^2, $ 8.0</td><td colspan="2">CH358060 × 1EA: 25 cm^2, $ 4.0</td></tr>
<tr><td colspan="2">Output capacitor, C_O</td><td colspan="3">Film Cap. (450 V, 4.5 A, 1.5 μF): 6.6 cm^2, $ 1.0</td><td>Film Cap. (450V, 24 A, 11 μF): 37.4 cm^2, $ 4.6</td><td>Film Cap. (450V, 4.5 A, 1.5 μF): 6.6 cm^2, $ 1.0</td></tr>
<tr><td rowspan="4">HB LLC converter</td><td>Transformer, T_2</td><td colspan="3" rowspan="4">–</td><td colspan="2">PQ3230: 22.4 cm^2, $ 2.5</td></tr>
<tr><td>Resonant capacitor, C_R</td><td colspan="2">Film cap. (250V, 680 nF) × 3EA: 8.5 cm^2, $ 1.2</td></tr>
<tr><td>Full-Bridge rectifier, D_5–D_8</td><td colspan="2">20CTH03 × 4EA: 3.4 cm^2, $ 2.1</td></tr>
<tr><td>Output capacitor, $C_{O\ LLC}$</td><td colspan="2">Film Cap. (250 V, 7 A, 2 μF): 7.3 cm^2, $ 1.3</td></tr>
<tr><td colspan="2">FBRfor PSFB converter, D_1–D_4</td><td colspan="2">STTH1512D × 4EA: 3.4 cm^2, $ 7.5</td><td>IDH15S120 × 4EA: 3.4 cm^2, $ 32.5</td><td colspan="2">10ETF06 × 4EA: 3.4 cm^2, $ 4.9</td></tr>
<tr><td colspan="2" rowspan="2">Clamping circuit</td><td>UF4005: 0.06 cm^2, $ 0.2 R_{snb} (41kΩ, 20W): 13.4 cm^2, $ 0.3</td><td>R_{snb} (17kΩ, 30W): 20.2 cm^2, $ 0.7</td><td rowspan="2">-</td><td colspan="2">FE1D: 0.45 cm^2, $ 0.1 U1540G: 0.85 cm^2, $ 0.6</td></tr>
<tr><td colspan="2">HER108: 0.3 cm^2, $ 0.1 Film cap. (1250 V, 0.1μF): 6.1 cm^2, $ 0.4</td><td>Film cap. (160V, 0.4 μF): 1.4 cm^2, $ 0.8</td><td>-</td></tr>
<tr><td colspan="2">Total volume</td><td>91.1 cm^2</td><td>97.8 cm^2</td><td>71.2 cm^2</td><td>120.8 cm^2</td><td>88.6 cm^2</td></tr>
<tr><td colspan="2">Total cost</td><td>$ 18.3</td><td>$ 18.5</td><td>$ 42.3</td><td>$ 23.4</td><td>$ 19</td></tr>
</table>

VI. CONCLUSION

A new HB integrated PSFB converter using a center-tapped clamp circuit was proposed. The proposed converter solved many limitations of the conventional PSFB converters, such as the narrow ZVS range for the lagging-leg switches, the substantial circulating current, the large output inductor, the severe voltage stress in the FBR, and the significant switching loss in the FBR. In addition, the proposed converter solved many side effects of the prior works using CDD clamp circuit, such as large rms current on the primary side, large turn-OFF current for the leading leg switches, and the substantial current stress on the output capacitor. Finally, the proposed converter achieved much higher efficiency with reduced output filter over the conventional PSFB converter and the prior works.

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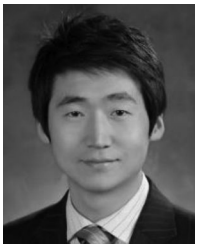

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