Fully Integrated Autonomous Interface With Maximum Power Point Tracking for Energy Harvesting TEGs With High Power Capacity

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***Abstract*—In this article, a novel fully autonomous and integrated power management interface circuit is introduced for energy harvesting using thermoelectric generators (TEGs) to supply power to Internet of Thing nodes. The circuit consists of a self-starting dc–dc converter based on a dual-phase charge pump with *LC*-tank oscillator, a digital MPPT unit, and a 1-V LDO regulator. The novel maximum power point tracking (MPPT) algorithm avoids open-circuit state, and accommodates varying input power and ultra-low voltage conditions. Validation data from the fabricated test-chip in 180 nm standard CMOS technology indicates the circuit start-up voltage is as low as 170 mV. The maximum output power capacity is 0.5 mW, which is the highest noted in the literature for a fully integrated solution. The high output power at low cost is achieved with a peak system efficiency of 30%. The relatively low efficiency is expected, since the focus of the design is high power capacity at low cost. The MPPT algorithm reaches 98% maximum accuracy for a source output resistance of 40 Ω, which is typical for wearable TEG modules.**

***Index Terms*—Integrated *LC*-tank oscillator, low-voltage dc/dc conversion, maximum power point tracking (MPPT), self-powered charge-pump, thermoelectric energy harvesting, wearable sensors.**

I. Introduction

THE real world smart sensor nodes that make up the Internet of Things (IoTs) have typically been powered by small batteries to date. From the point of view of maintenance costs, environmental issues, and aesthetic (system bulkiness) concerns, powering billions of smart nodes with batteries is a significant problem [1] that threatens the sustainable growth of IoT. Fully integrated, adaptable, self-starting circuits with regulated output and sufficient power capacity to eliminate or reduce battery requirement are necessary to achieve energy harvesting sensors with minimum size and cost. A typical IoT smart node includes an embedded processor, sensors, and a wireless data transmission unit. Overall IoT average power budget can be reduced to few hundred μWs range through the use of processor sleep modes [3], [4], duty cycling in wake up radio technology [2], and other system level power management features [5].

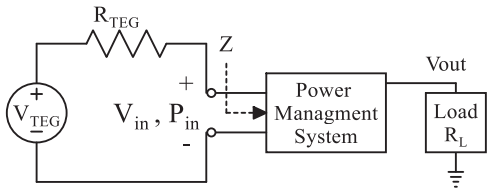

Fig. 1. TEG energy harvesting with integrated power management.

Among the ambient sources, thermoelectric energy can lead to miniaturization due to absence of moving and bulky components. Unlike photovoltaic cells, thermoelectric generators (TEGs) modules can generate power in absence of sunlight, as long as there is a heat source. Fig. 1 depicts a block diagram of the TEG energy harvesting system. Typical wearable thermoelectric microgenerators (of cm^2 scale) deliver ultra-low output voltage (tens to hundreds of mV) depending on environmental temperature, which makes it inevitable to step up the voltage to supply a sensor node. Charge pumps are pre-eminent for fully integrated dc–dc conversion due to absence of large inductors, but carry associated challenges when interfaced with TEGs. First, TEG output levels below the MOSFET threshold voltage, V_T, need to be detected, which sometimes requires external start-up circuits [6]–[8]. Second, the power capacity is limited to some tens of μWs when ultra-low voltage on-die ring oscillators are utilized to stimulate the charge-pumps [9], [10]. Finally, power extraction efficiency from TEG varies significantly under varying load conditions (R_L in Fig. 1), and output power will be affected by varying environmental (varying V_{TEG} in Fig. 1) and load conditions [11]. The effect of all of these problems is lack of sufficient development in fully integrated solutions.

A. Problem of Ultra-Low Input Voltage With High Power Output

Ultra-low voltage *LC*-tank oscillators with voltage gain >1 and capacity to drive 100–1000 μWs can be integrated due

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to low inductance requirement. There are few existing *LC*-tank topologies feasible for the dc–dc converter applications including the ones introduced in [12]–[15]. The impact of the switching resistance on the output impedance of the charge pump is discussed in [16]. An optimization of Dickson charge pump to maximize output current under area constraint is presented in [17]. A model-based optimization method for fully integrated cross-coupled charge pump with an *LC*-tank oscillator for ultra-low voltage dc–dc converter application is first proposed by our group in [18] and [19]. Further optimization based on analytical models is presented in this article, with considerations of power capacity, output voltage, and impedance matching between the *LC*-tank oscillator and the charge pump.

B. Problem of Maximum Power Point Tracking (MPPT)

MPPT for charge pump-based dc–dc converters can be achieved by altering the voltage conversion ratio (VCR), oscillation frequency, or charge pump capacitance [9], [10]. Most of the previous MPPT methods for TEGs involve measuring open circuit voltage, and adjusting the interface circuit input to half of the measured open circuit voltage [6], [20]–[25]. The open-circuit method increases the cost of real-time power delivery to the load through bulky storage devices, and complex circuits. Load current sensing is utilized in [26] to adjust the oscillation frequency, number of stages and the flying capacitance values to attain maximum power point. This method avoids disconnecting the circuit from TEG. However, use of current sensors introduces complexity and power consumption overhead. In general *LC*-tank oscillators have significantly different input and output impedance characteristics compared to traditional ring oscillators, which adds to the challenge of MPPT design for charge pumps with *LC*-tanks as clock generators.

A novel MPPT algorithm (and implementation) is therefore introduced in this article, which ensures maximum output power delivery and efficiency under varying load and ambient conditions. The circuit refrains from disconnecting from the TEG, and is adaptable to varying TEG output and converter efficiency in ultra-low voltage conditions.

C. Section Outline

The article is organized as follows. Section II discusses the dc–dc converter model used for the integrated charge pump design that is stimulated by an on-die *LC*-tank oscillator. The novel MPPT algorithm for integrated TEG interface is outlined in Section III. Section IV presents the circuit implementation details using 180 nm standard CMOS technology. Design validation results are discussed in Section V. Section VI presents the conclusion.

II. DC–DC Converter Model and Optimization

The charge pump topology that is driven by *LC*-tank differential outputs is modeled using two identical half-circuits with lumped elements, where one half-circuit delivers current to the load while the other one is disconnected from the load at any given time. The analytical circuit model is used to optimize

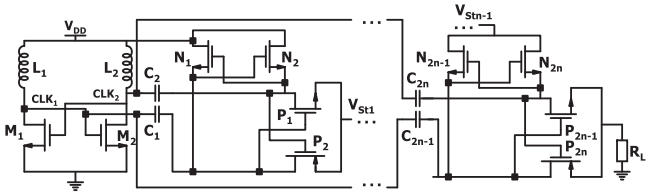

Fig. 2. *n*-stage dc–dc converter with *LC*-tank oscillator.

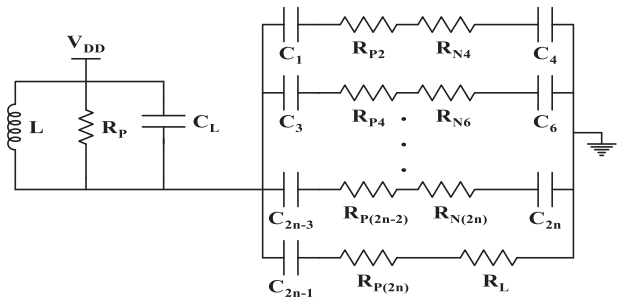

Fig. 3. Lumped element half circuit model of the *n*-stage, dc–dc converter for impedance analysis. For $n = 1$, the charge pump model reduces to load line only.

circuit parameters for maximum power delivery, for enabling the development of a suitable MPPT algorithm, and in prediction of theoretical system efficiency.

A. Simplified Half-Circuit Model for Impedance Analysis

The *n*-stage dc–dc converter is depicted in Fig. 2. The lumped element half circuit model for the system is illustrated in Fig. 3 for impedance analysis. The charge pump MOSFETs are modeled by individual resistors when in ON state. The MOSFET parasitic capacitance is negligible compared to the flying capacitors. Each charge carrying path consists of two resistors and two capacitors except for the last stage. The final stage has a single flying capacitor and two resistors, including the load resistance (R_L). The *LC*-tank half circuit is modeled as a parallel network of inductor (*L*), resistor (R_P), and capacitor (C_L). *LC*-tank parallel resistance and capacitance values are derived as

$$R_P = L/C_L R_S \tag{1}$$

$$C_{P1} = \frac{-A + \sqrt{A^2 + 4LC_{S1}C_0}}{2L};$$

$$A = \left(R_{CS1}^2 C_{S1}^2 + LC_0 - LC_{S1}\right) \tag{2}$$

$$C_L = C_0 + C_{P1} \tag{3}$$

where R_S represents the parasitic series resistance of the inductor, C_{S1} and R_{CS1} represent first stage charge pump capacitance and ON NMOS resistance, respectively. C_0 is the *LC*-tank capacitance corresponding to the resonator frequency without coupled charge pump, and C_{P1} is the parallel capacitance of charge pump capacitor C_1. Further details of the basic model is available in [18]. For the inductor with small self-resistance, the charge pump coupled *LC*-tank oscillator frequency (f_0) can be calculated as in (4). The impedance of each charge carrying

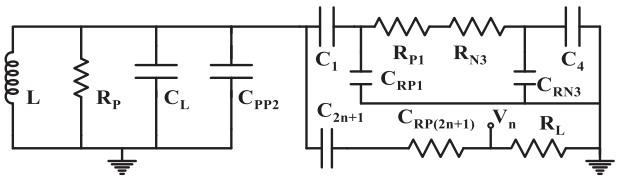

Fig. 4. Lumped element half circuit model of the *n*-stage dc–dc converter for power analysis.

stage network can be written as

$$\omega = \frac{1}{\sqrt{LC_L}} \tag{4}$$

$$Z_1 = (R_{P1} + R_{N3}) - j\,(1/\omega C_1 + 1/\omega C_4) \tag{5}$$

$$Z_2 = (R_{P3} + R_{N5}) - j\,(1/\omega C_3 + 1/\omega C_6) \tag{6}$$

$$Z_{n-1} = \left(R_{P(2n-3)} + R_{N(2n-1)}\right) - j\,(1/\omega C_{2n-3} + 1/\omega C_{2n}) \tag{7}$$

$$Z_n = \left(R_{P2(n-1)} + R_L\right) - j\,(1/\omega C_{2n-1}) \tag{8}$$

where, Z_n is the *n*th charge carrying charge pump stage impedance, with up to *N* stages. C_x, R_{Px} and R_{Nx} represent the *x*th flying capacitor, PMOS and NMOS resistances respectively; $x = 1, 2, \ldots, 2n$. The total impedance of the charge pump network can be described by

$$Z_{CP} = 1 \Big/ \sum\nolimits_1^n (1/Z_n)\,. \tag{9}$$

The charge pump impedance (Z_{CP}) should match with the LC impedance (R_P) at the operating frequency (ω) to achieve maximum power transfer. Considering charge pump *N*-channel and *P*-channel MOSFETs, and capacitors are identical in all stages for design convenience, and using the relation of $Z_{CP} = R_P$, the (1) and (9) can be rearranged as

$$\frac{R_s\,(C_0 + C_{P1})}{L} = \frac{n-1}{(R_{P1} + R_{N1}) - j\,(2/\omega C_{P1})} + \frac{1}{(R_L + R_{N1}) - j\,(1/\omega C_{P1})}. \tag{10}$$

B. Simplified Half-Circuit Model for Power Analysis

The lumped element half circuit of *N*-stage dc–dc converter model consists of *L, R,* and *C* components as illustrated in Fig. 4 for power analysis. As in the case for impedance analysis, all the charge carrying MOSFETs are represented with individual resistors. The parasitic capacitance of the cross-coupled MOSFETs is accounted for the power dissipation calculations; C_{RPx} and C_{RNx} are the parasitic capacitance of *x*th PMOS and NMOS, respectively. The charge carrying NMOS connected capacitor (C_{PP2}) in the first charge pump stage is modeled in parallel with the oscillator capacitor (C_L). For the oscillator output (clock) signal with peak-to-peak swing of V_{pp}, the output voltage of *N*-stage dc–dc converter can be iteratively calculated from (11), considering the voltage boost in each stage. DC–DC converter power output is calculated using

$$V_n = \left(\frac{1}{\sqrt{2}} V_{pp}\, e^{\frac{-t}{C_1(R_{P2}+R_L)}} + V_{n-1}\right) \times e^{\frac{-t}{C_1(R_{P2}+R_L)}} \times \left(1 - \frac{R_{P(2n-1)}}{\left(R_L + R_{P(2n-1)}\right)}\right) \tag{11}$$

$$P_n = \frac{V_n^2}{R_L} \tag{12}$$

where *t* represents the half period of dc–dc converter clock signal and V_0 is the dc–dc converter source voltage (V_{DD}). The total power input of the single-stage dc–dc converter is accumulated from delivered power at the output, losses at the *LC* tank, charge pump capacitors, charge pump MOSFET parasitic capacitors, and charge carrying resistors. The power consumption of MOSFET resistance is negligible due to micro-Amps of through-current. Only the first stage charge pump capacitors are modeled since the others have constant voltage. The total power consumption can be calculated using (13), which shows the summation of the power delivered to the output of the converter, the power stored and dissipated in the *LC*-tank structure and the power dissipated due to parasitic capacitance of charge pump MOSFETs

$$P_{nt} = P_n + \frac{V_{pp}^2}{8}\left[\frac{R_{DS} \times R_P}{(R_{DS} + R_P)} + \frac{C_L \omega}{2\pi}\right] + \left(\frac{V_{pp}}{2\sqrt{2}} - V_{DD}\right)^2 \frac{C_{1P}\omega}{2\pi} + \sum_{n=1}^{n} \frac{V_{pp}^2}{16\pi} C_n \omega \tag{13}$$

where $C_n (C_n = C_{RPn} + C_{RNn})$ is the summation of the parasitic capacitance of charge pump NMOS and PMOS.

C. Optimization Method

The *LC*-tank inductors have significantly higher area requirement compared to the rest of the circuit components, and fundamentally affect oscillation amplitude [27]. Thus, the first step is to select the inductors with the highest power capacity within the die area constraint, leaving sufficient room for the rest of the circuit. Self-resistance (R_S) and parasitic capacitance of the inductors can be extracted from the corresponding technology specifications. Charge pump MOSFET sizes are selected considering resistance-capacitance tradeoff. The number of charge pump stages is selected according to desired boost multiplication factor through a rough estimation of voltage gain using $3 + 1.5(n - 1)$ after losses, where n is the number of stages. Next, the relationship between C_0 and C_{P1} is determined using impedance matching, (10), for selected load resistance, number of stages, and charge pump MOSFET resistance. C_1 is then calculated in terms of C_0 by substituting C_{P1} (use the relation of C_{P1} and C_0 from impedance matching equation) into (2). The half-period time, *t* of the dc–dc converter is calculated in terms of *L* and C_0 by substituting relation of C_0 and C_{P1} into (4). The optimal charge pump capacitance for maximum output power can be calculated by substituting above relation into dP_n/dC_1. C_0 and C_{P1} can be calculated using the optimal C_1. Required minimum transconductance (g_m) of *LC*-tank NMOS is calculated using (14). Then *LC*-tank NMOS capacitance is

determined by simulations or analytical estimation. Equation (10) is reused to calculate the optimal capacitor values in the charge pump

$$g_m \geq \frac{R_S}{R_S^2 + L/(C_0 + C_{P1})} \tag{14}$$

$$L_{\mathrm{MOS}} = \frac{(V_{gs} - V_t)\, W\, k_p}{g_m}. \tag{15}$$

Since the parasitic resistance and capacitance values are expected to be more accurate with post-layout data compared to the pre-layout estimation, the optimization calculations have been iterated after layout extraction.

III. Maximum Power Point Tracking

Increasing the number of stages in the described charge pump increases the load on the oscillator, and hence decreases the oscillation amplitude. While the number of stages is a key factor in determining the VCR of a stand-alone charge pump-based dc–dc converter, this number has an inverse relation with the input impedance of the charge pump as described by (9). On the other hand, higher number of stages results in higher dynamic and static power dissipation. Therefore, changing the number of stages affects the input impedance, output voltage, output power and efficiency of the system all at the same time. The previously derived small signal model [28] reduces the charge pump load to an admittance connected to the *LC*-tank oscillator. Equation (16) is thus derived to model the loading effect of the charge pump on the oscillator

$$\left|\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right| = \frac{g_m}{G_p + G_0} \tag{16}$$

where g_m represents *LC*-tank cross coupled NMOS transconductance as before, $G_p$models the parasitic conductance of both the inductor and the capacitor, and G_0 is the total charge pump admittance ($G_0 = \frac{1}{Z_{CP}}$). V_{out} is the oscillation amplitude and V_{in} is the input voltage. Increasing the number of stages leads to growth in G_0 since it decreases Z_{CP} from (9), decreasing the gain. The output voltage does not linearly increase with the number of stages due to increased loading effect and decreased oscillation amplitude. In fact, for a fixed value of load and input voltage, there is a specific number of stages that leads to the maximum output voltage, which also corresponds to maximum output power for the fixed load. Maximum power transfer from TEG is achieved when the input impedance of the interface circuit is equal to the output resistance of the TEG

$$P_{\mathrm{in,MAX}} = \frac{(V_{\mathrm{TEG}})^2}{4\, R_{\mathrm{TEG}}}. \tag{17}$$

Based on (17), the maximum input power only depends on V_{TEG} and R_{TEG}, and is therefore fixed for any given ΔT (temperature difference between the colder and warmer plates of the TEG). The lower bound for the power efficiency of the system is the amount of power that can be delivered to the load for a particular converter implementation over the maximum extractable power, calculated using (17)

$$\eta_{\mathrm{Lower-bound}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in,max}}} = \frac{\frac{V_{\mathrm{out}}^2}{R_L}}{\frac{(V_{\mathrm{TEG}})^2}{4\, R_{\mathrm{TEG}}}} = \left(\frac{V_{\mathrm{out}}}{V_{\mathrm{TEG}}}\right)^2 \times \left(\frac{4\, R_{\mathrm{TEG}}}{R_L}\right). \tag{18}$$

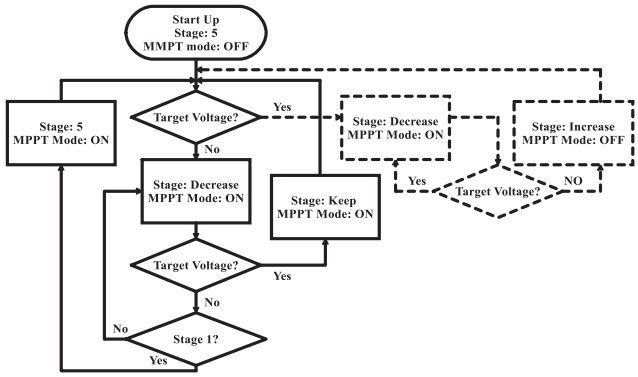

Fig. 5. Proposed MPPT algorithm for charge pump-based dc–dc converters with *LC*-tank oscillator.

Maximizing the output power will maximize efficiency for a given ΔT based on (18). Maximum power point can typically be attained in inductive boost converters through the maximization of input power by matching the input impedance with the output impedance of the power source. However, input impedance matching with TEG output impedance alone will not guarantee maximum output power in this case due to change in efficiency with change in input voltage for ultra-low voltage range. Instead, the output power itself should be maximized for any pair of V_{TEG} and R_L. Furthermore, MPPT needs to target minimization of the number of stages in order to minimize power loss, and deliver a fixed supply potential to the load at the same time.

Fig. 5 illustrates the proposed MPPT algorithm that is compatible with the above requirements. There are two distinct phases in the flow: Search for the stage that can generate the target output voltage (solid lines) and minimize the number of stages while maintaining the output target voltage (dashed lines). MPPT starts with all stages (five in this case) turned ON. This is to account for a potentially very low TEG voltage at cold-start up. If the output voltage is less than the target (1 V in this case), then the number of stages will be decreased by one. Decreasing the number of stages can lead to higher output voltage as a result of reduced loading effect on the oscillator and increased input impedance of the charge pump. If a stage is found for which the target voltage is fulfilled, then the second phase is entered, which checks if the target voltage can be achieved with a smaller number of stages. At the end of the process, the lowest number of stages will be locked, and MPPT will be turned OFF. It is possible that due to very heavy load or very small ΔT across the TEG, which leads to very small TEG voltage, no stage can be found to supply the targeted output voltage. In this case, the algorithm will keep searching until a solution is identified due to a new favorable

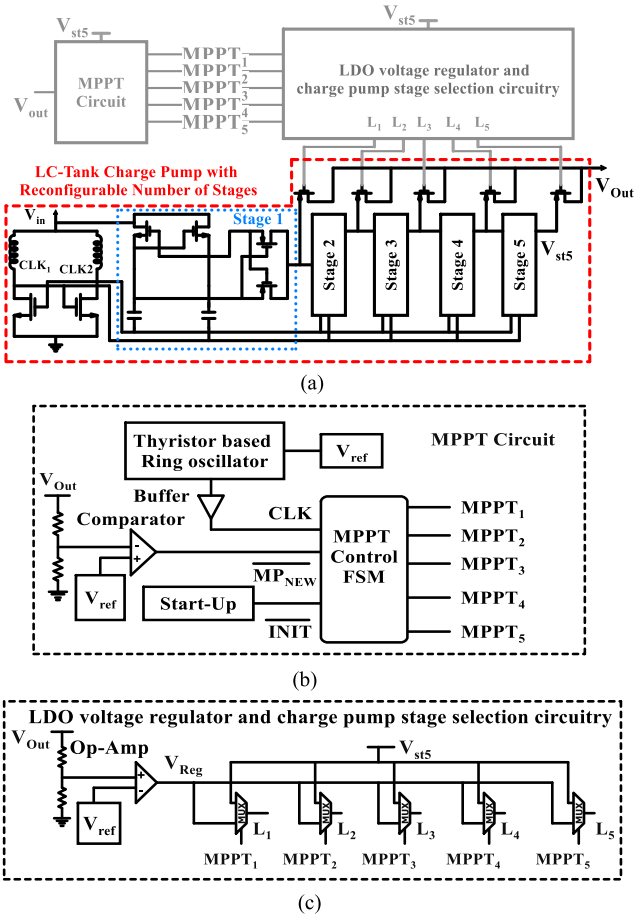

Fig. 6. (a) Power management system architecture. (b) MPPT circuit architecture. (c) LDO voltage regulator and charge pump stage selection circuit.

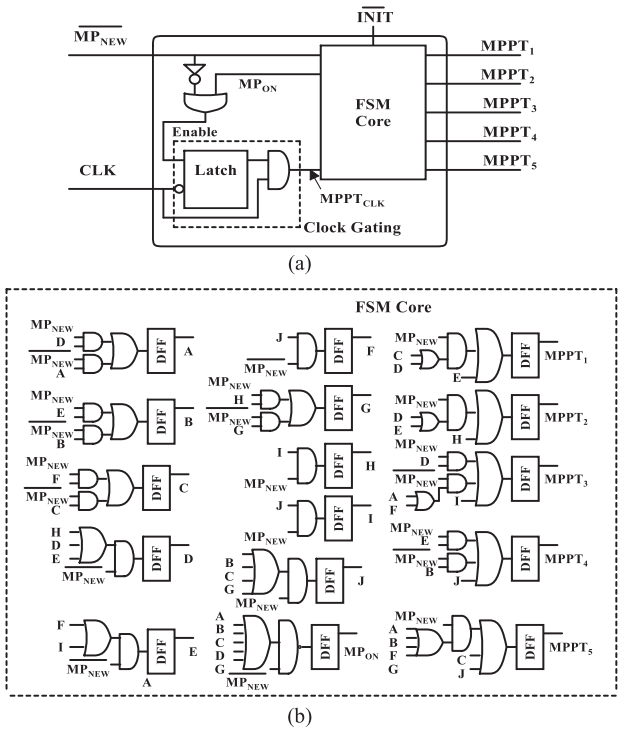

Fig. 7. (a) MPPT Control unit, and (b) gate level implementation of the FSM core circuitry.

condition. After locking to a stage and turning OFF, MPPT unit is reactivated to search for a new maximum power point, when the voltage drops below the target. This is done through a low voltage detector that initializes the MPPT unit.

IV. Implementation

A. System Architecture

The overall architecture of the proposed autonomous system is depicted in Fig. 6(a). MPPT circuit architecture is provided in Fig. 6(b). LDO voltage regulator, enhanced to also select the number of charge pump stages, is detailed in Fig. 6(c). Pass *P*-type MOSFETs driven by this control [shown connected to Vout node in Fig. 6(a)] contribute to LDO regulation, as well as multiplexing among charge pump stages. MPPT unit requires a clock generator as well as a start-up circuit for initialization. These units are further described in the following sections.

B. MPPT Circuit

Fig. 7(a) depicts the MPPT Control circuit. One-hot finite-state machine (FSM) core, which implements the previously discussed algorithm (see Fig. 5), is shown in Fig. 7(b). The active low $\overline{\text{INIT}}$ signal resets the machine to start-up state, whenever the last stage voltage drops below 350 mV (block shown as "start up" in Fig. 5). This may indicate that either the load current demand is too high, or TEG voltage is too low. FSM Core unit is clock gated to be active only when a meaningful event is observed, which minimizes dynamic power consumption. After initialization, MP_{ON} is high. When MP_{ON} switches to low, a maximum power point is found, and FSM clock is turned OFF. Any voltage drop at the output after this point triggers a new MPPT search by activating $\overline{\text{MP}_{\text{NEW}}}$ signal ($\overline{\text{MP}_{\text{NEW}}}$ signal will be high if the output voltage is less than target voltage, which fulfills the condition required by the conditional blocks shown as "target voltage?" in Fig. 5). As in any one hot design, only one MPPT_n signal is high at each clock cycle that configures the charge pump to be n stage. After each successful MPPT cycle, the FSM waits to be reactivated by $\overline{\text{MP}_{\text{NEW}}}$ low-to-high transition. Since the temperature gradient transitions across a TEG occur with a relatively large time constant, MPPT is implemented using slow subthreshold CMOS circuits for ultra-low power consumption. MPPT cycle that lasts for hundreds to thousands of milliseconds is typically tolerable for TE energy harvesting systems [21], [22].

C. Dynamically Configurable Charge Pump

A new charge pump structure is proposed with configurable number of stages, as depicted within the dashed box in Fig. 6(a) so as to enable the previously discussed MPPT scheme. In this topology, only one PMOS switch can be ON at a time to deliver output current. The PMOS switches are large, and are of low V_T (LVT) type to minimize voltage drops typical

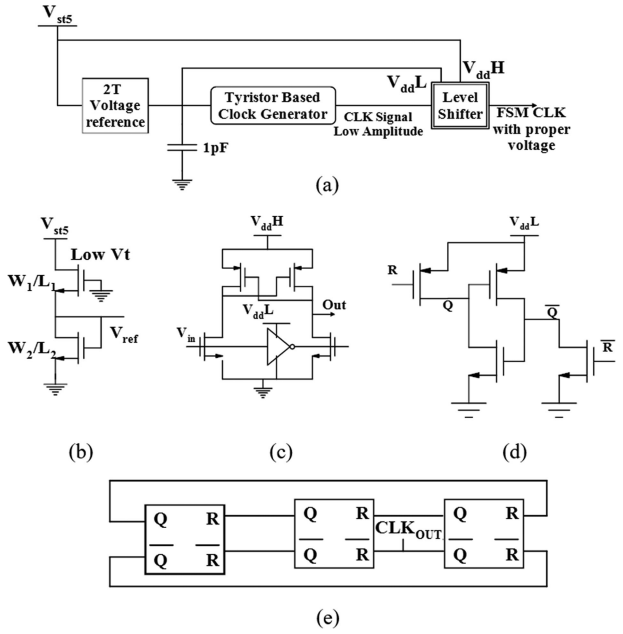

Fig. 8. (a) Ultra-low power FSM clock generator system. (b) 2T subthreshold voltage circuit. (c) Level shifter circuit. (d) One stage of the tyristor-based ring oscillator circuit. (e) Tyristor-based ring oscillator circuit.

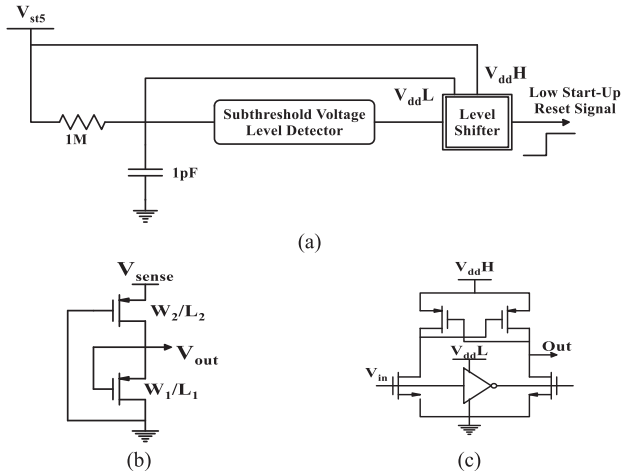

Fig. 9. (a) Circuit that generates the required pulse for initializing the FSM. (b) Subthreshold level detector circuit. (c) Level shifter circuit.

of LDO regulators. This topology offers minimum number of switches. This is essential to minimize leakage, which is already exacerbated due to large LVT MOSFETs. The highest internal voltage available in the system (V_{st5}) from stage 5 is utilized for digital control, reference/biasing, and regulator circuits, even when the regulated output voltage is not at a sufficiently high level.

D. Subthreshold Voltage Reference

FSM clock generator circuit architecture is shown in Fig. 8(a). The subthreshold voltage reference circuit (2T voltage reference) in Fig. 8(b) forms the first stage with two NMOS transistors, and operates based on threshold voltage difference between the devices, as described in [29]. Based on Monte Carlo analysis, the variation is maximum 49 mV at 50 °C with fast devices compared to typical devices at 27 °C. This translates to 77 mV of variation at the output of the system with target voltage 1 V, which is within the generally accepted voltage regulation tolerance of $+/-10\%$. The circuit has ultra-low power consumption, reliability and robustness against power supply variations, and functions correctly with supply voltage as low as 0.5 V.

E. Thyristor-Based Ultra-Low Power Ring Oscillator

Thyristor-based ring oscillator at the second stage is depicted in Fig. 8(e) [30]. This block provides a low frequency clock signal, 1 kHz in our application, with ultra-low power consumption of 124 nW based on the simulation results. The design takes advantage of the low operation frequency to utilize a capacitor at the output of a 2T voltage reference to accumulate sufficient charge and supply instantaneous current for oscillator switching. The output power of the voltage reference is some pWs due to operation in subthreshold region. Low frequency of switching allows sufficient time to charge the capacitor up to the reference voltage value required by each of the three stages [see Fig. 8(d)] in the clock generator. A level shifter circuit [see Fig. 8(c)], supplied by V_{st5} voltage, is utilized to shift clock signal voltage up, to be compatible with the rest of the FSM circuits.

F. Ultra-Low Power Initialization Circuit

MPPT Control Unit will not be activated until the supply voltage reaches a specific level. To overcome this problem, the FSM is initialized to work in five-stage mode to obtain a high voltage at the beginning of the conversion. An active-low signal resets the FSM to "start" state. The initialization signal is generated using the circuit depicted in Fig. 9(a), which is based on the subthreshold voltage level detector (see Fig. 9(b)) introduced in [31].

As the voltage V_{st5} rises during start-up, the subthreshold voltage detector circuit triggers when the RC filtered input reaches V_{Trigger} calculated by

$$V_{\text{Trigger}} = \frac{mkT}{q} \ln\left(\frac{W_1}{W_2} \times \frac{L_2}{L_1}\right) \tag{19}$$

where k is the Boltzman constant, T is absolute temperature, q is the charge of an electron, and m is the subthreshold swing coefficient ($m > 1$). The signal lasts for tens of microseconds due to the high RC time constant, which is sufficient to initialize the FSM. The level shifter [see Fig. 9(c)] ensures voltage compatibility with the FSM unit running on V_{st5} supply.

V. Design Validation Results

Fig. 10 depicts the test chip layout and micrograph of the core circuits illustrated in Fig. 6. The *LC*-tank oscillator occupies 0.79 mm^2 of the area, with two standard inductors of 14 nH, while 0.23 mm^2 is dedicated to the five-stage configurable charge pump, employing two 9.5 pF capacitors for each stage. The

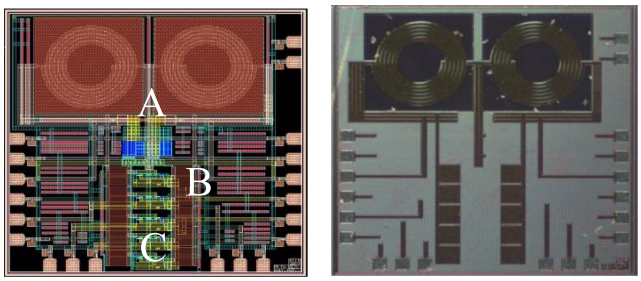

Fig. 10. (a) Chip layout photo with PAD connections. A: Onchip inductors, B: *LC*-tank cross coupled NMOS transistors, and C: Reconfigurable charge pump circuit. (b) 1525 μm $\times$ 1525 μm die micrograph.

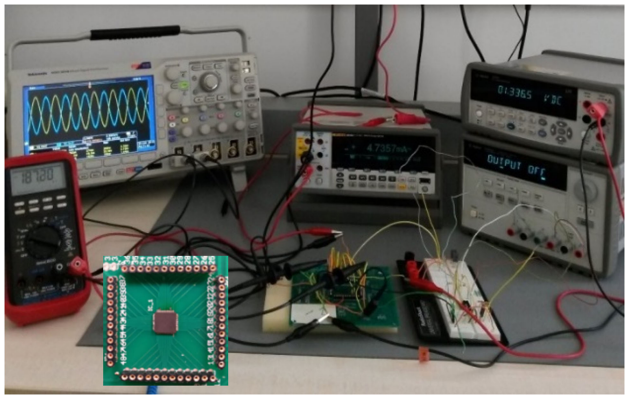

Fig. 11. Test bench for the chip.

design is implemented using UMC 180nm Technology and packaged in QFN 48 for characterization in laboratory environment. Prototype system testing is done using a 16 cm^2 TEG with 40 Ω output resistance. Since this version of the test chip did not have the LDO regulation integrated (although there is sufficient area to integrate it in the next version), this portion was prototyped on board, using an operational amplifier (LM741), and *N*-channel MOSFET (FQA46N15) to facilitate closed-loop testing as depicted in Fig. 11.

A. Validation of MPPT Algorithm

For $V_{\mathrm{TEG}} = 240$ mV, $R_L = 10$ kΩ, the 1 V target voltage is not initially achieved, as shown in Fig. 12, when the output is driven from stage 5. Therefore, the number of stages is decreased to four to achieve the output target voltage. The number of stages is then further decreased to find the minimum number of stages that can maintain output target voltage. Since with three stages the voltage drops below 1 V, the number of stages is increased back, and MPPT is deactivated by locking on stage 4. Fig. 13 demonstrates the results when $V_{\mathrm{TEG}} = 350$ mV with $R_L = 5$ kΩ. Stage 5 doesn't reach target 1V while both stages 4 and 3 can. The drop in number of stages from 5 to 4 is to reach target voltage while the drop from 4 to 3 and 2 is to minimize the number of stages. Finally stage 3 locks the MPPT search since the output voltage requirement is not met by 2-stage charge pump. Fig. 14 shows the validation results for

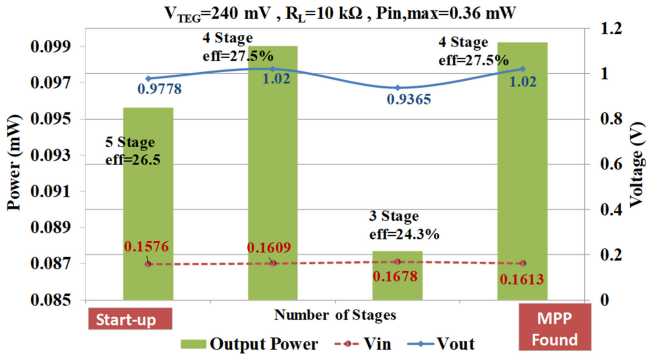

Fig. 12. Validation results for the autonomous system with $V_{\mathrm{TEG}} = 240$ mV and 10 kΩ load.

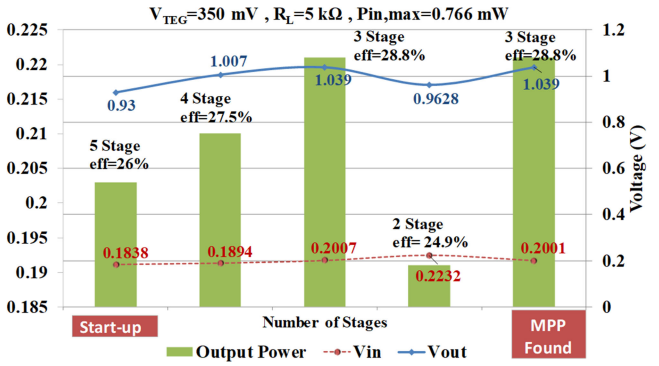

Fig. 13. Validation results for the autonomous system with $V_{\mathrm{TEG}} = 350$ mV and 5 kΩ load.

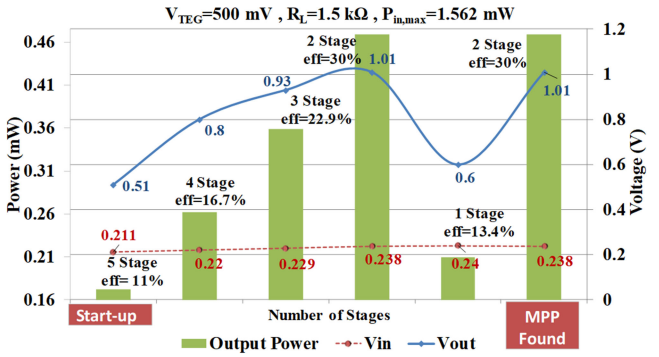

Fig. 14. Validation results for the autonomous system with $V_{\mathrm{TEG}} = 500$ mV and 1.5 kΩ load.

$V_{\mathrm{TEG}} = 500$ mV, $R_L = 1.5$ kΩ. 1 V target is not achieved with five stages. Therefore, 4, 3, 2, 1 stage options are sequentially scanned when the output voltage drops below 1 V, and MPPT is deactivated by locking on stage 2. At this stage a near-maximum output power of 0.469 mW is achieved. Fig. 15 illustrates the change in the number stages from 5 to 4 to maximize output power, when the load resistance decreases from 10 to 5 kΩ. Fig. 16 demonstrates the optimal number of stages drop from 4 to 3 to maximize efficiency as a result of increase in load. Fig. 17 shows the effect of change in V_{TEG} when regulator is not present. Voltages higher than 1 V will be regulated to 1 V.

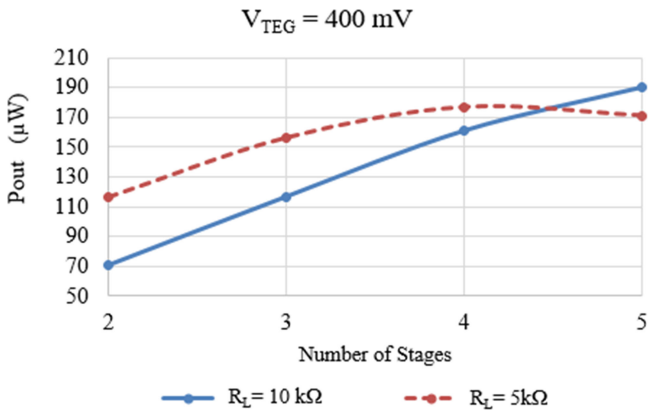

Fig. 15. Given a fixed $V_{\rm TEG}$ of 400 mV, output power is maximum with four stages for a 5 kΩ load but with five stages for a 10 kΩ load.

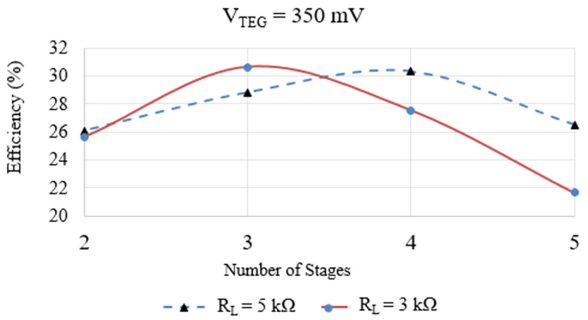

Fig. 16. Given a fixed $V_{\rm TEG}$ of 350 mV, efficiency is maximum with three stages for a 3 kΩ load, but with four stages for a 5 kΩ load.

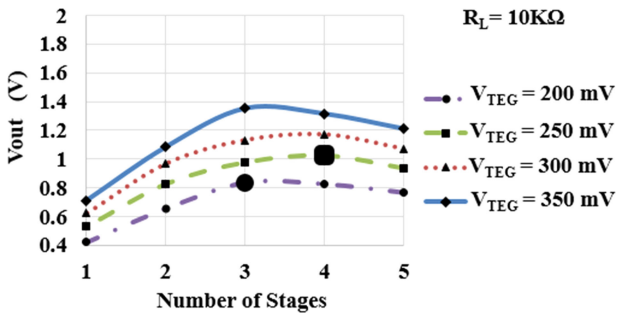

Fig. 17. Experimental results for nonregulated output.

MPPT for $V_{\rm TEG} = 200$ mV, $R_L = 10$ kΩ will keep searching since 1 V cannot be achieved by any of the stages. MPP for $V_{\rm TEG} = 250$, 300, and 350 mV will be 4, 3 and 2 stages, respectively, (see flowchart in Fig. 5). Fig. 18 illustrates validation results for MPP tracking accuracy which is defined as input power of the interface circuit over maximum deliverable power from TEG. Fig. 19 demonstrates the start-up condition signals at $V_{\rm in} = 170$ mV, when the IoT node is OFF and charge pump is not loaded.

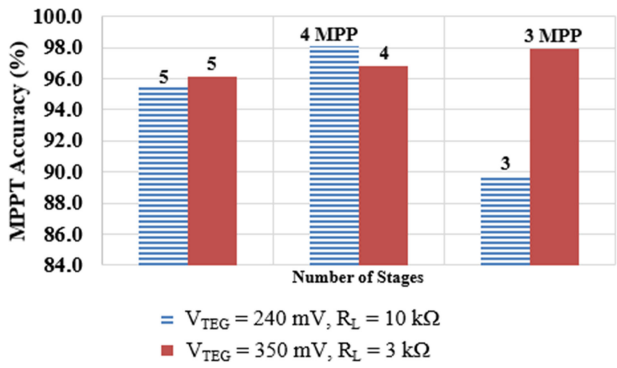

Fig. 18. MPPT efficiency validation results.

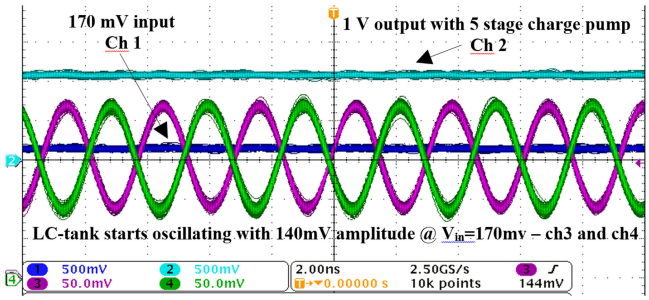

Fig. 19. Start-up condition (no-load) for $V_{\rm in} = 170$ mV.

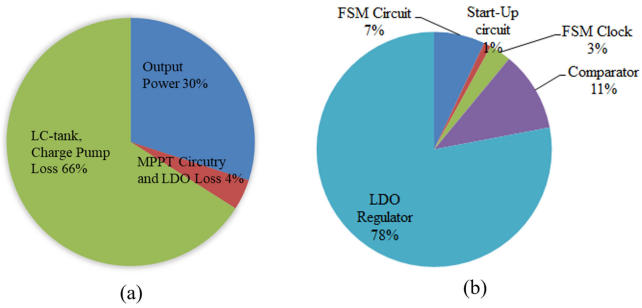

Fig. 20. (a) Contribution of MPPT to power losses. (b) Break-down of power consumption for different blocks within the MPPT circuitry and LDO regulator.

B. Power Losses in Power Management

Fig. 20(a) demonstrates the contribution of MPPT regulation circuitry to power budget is 4%. The highest share of this power consumption is in the LDO regulator as depicted in Fig. 20(b) due to the relatively high gain required to drive large PMOS switches. This can be expected to reduce after LDO integration in the next revision of the implementation.

C. Comparison Against Literature

Table I compares the proposed system with state of the art autonomous systems in the literature. Output power is significantly higher than the fully integrated (least size and cost) CMOS solutions in the table, and is comparable with the state of the art non-fully-integrated solutions. Our circuit does not require

TABLE I
COMPARISON OF THE PROPOSED CIRCUIT WITH STATE-OF-THE ART IN THE LITERATURE

Ref.	Process (nm)	Max. Output Current (µA)	Ext. Start Up Unit	Min V_{in} for start-up (mV)	Regulated V_{out} (V)	Fully Integrated	Off chip (L+C+R)	Chip Area (mm^2)	MPPT Mechanism
[25]	130	500	Yes	270	1	NO	0+1+2	0.835	N[1], F[2], C[3] OCM[4]
[29]	65	730	Yes	80	NO (0.7– 1)	NO	4+2+0	0.51	PWM Modulation
[30]	130	900	Yes	250	1.8	NO	0+7+2	NA	PWM Modulation
[21]	65	358	Yes	65	1.8	NO	1+2+0	1.96	PWM Modulation
[24]	65	> 1000	Yes	210	1	NO	1+0+0	0.54	N, F, C - OCM
[28]	180	5	No	140	NO (2.2 – 5.2)	YES	NA	0.86	NA
[31]	180	20	No	500	1.8	YES	NA	1.69	N - OCM
[13]	180	16	Yes	450	3.3	YES	NA	3.2	N - OCM
This Work	180	500	No	170	1	YES	NA	2.25	N - Continuous

1: Charge pump number of stages 2: Oscillation frequency 3: Charge pump capacitance 4: Open circuit voltage measurement

1: Charge pump number of stages 2: Oscillation frequency 3: Charge pump capacitance 4: Open circuit voltage measurement.

external startup, since the *LC*-tank oscillator can start oscillating from voltages as low as 170 mV, which is comparable to the literature, such as the one proposed in [28].

VI. CONCLUSION

A novel fully autonomous interface circuit for energy harvesting from TE modules is introduced, which provides considerably increased output power using MPPT at 1 V regulated voltage.

The circuit comprises of a dc–dc converter based on a dual-phase charge pump, an *LC*-tank oscillator, a digital MPPT Unit, and an LDO regulator. The proposed MPPT refrains from disconnecting the circuit from the TEG, and is compatible with varying harvesting efficiency in ultra-low voltage conditions. Low power design techniques have been employed, including a novel low frequency clock generator for the FSM. Based on validation results, the circuit start-up voltage is as low as 170 mV. The maximum output power is 500 μW, which is the highest in the literature to our knowledge for a fully integrated interface design. The circuit meets the real time power demand of various sensor nodes for measurement, signal processing and wireless data transmission in duty cycle mode and some GHz range. The peak efficiency is 30% based on the measurement results. Higher efficiency is in general not expected from such an ultra-low voltage solution with integrated inductors. The tested prototype used an external LDO regulator to validate the MPPT operation. The MPPT algorithm can reach up to 98% accuracy when the internal resistance of the TE generator is between 30 to 100 Ω, which is typical for a number of tiny TEGs connected in series for wearable applications. The circuit layout area is larger than other fully integrated solutions because of the use of inductors which are bulky on-chip elements, but leads to much lower cost compared to solutions with discrete components.

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