Design of a Grid-Tie Photovoltaic System With a Controlled Total Harmonic Distortion and Tri Maximum Power Point Tracking

Ala A. Hussein, *Senior Member, IEEE*, Xi Chen, *Student Member, IEEE*, Mahmood Alharbi, Anirudh Ashok Pise, and Issa Batarseh, *Fellow, IEEE*

***Abstract*—This article proposes an adaptive grid-tie photovoltaic system that maximizes the power injected to the grid while maintaining a predetermined power quality level. The proposed algorithm tracks the maximum power generated by the photovoltaic source, the maximum efficiency of the dc–dc converter, and the maximum efficiency of the inverter operating within a predefined total harmonic distortion limit. The tracked parameters that comprise the operating voltage of the photovoltaic source, the switching frequency of the dc–dc converter, and the switching frequency of the sinusoidal pulsewidth modulation inverter are updated, continuously, according to the generated photovoltaic power. The proposed method is fully adaptive, fast, and has a 100% convergence rate. Derivation of the proposed technique followed by the experimental verification and discussion are presented.**

***Index Terms*—DC–DC converter, efficiency, maximum power point tracking (MPPT), photovoltaic (PV), sinusoidal pulsewidth modulation (SPWM), switching frequency.**

Nomenclature

η	Efficiency.
AC	Alternating current.
ADC	Analogue-to-digital converter.
DC	Direct current.
DSP	Digital signal processor.
MEPT	Maximum efficiency point tracking.
MPPT	Maximum power point tracking.
PV	Photovoltaic.
PWM	Pulse width modulation.
SPWM	Sinusoidal pulsewidth modulation.
THD	Total harmonic distortion.
f_{ACme}	AC-side maximum-efficiency switching frequency.
f_{DCme}	DC-side maximum-efficiency switching frequency.
f_{sw}	Switching frequency.
V_{mp}	Photovoltaic maximum-power voltage.
P.I.	Performance index.

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A. A. Hussein is with the Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL 32816 USA, and also with the Department of Electrical Power Engineering, Yarmouk University, Irbid 21163, Jordan (e-mail: ahussein@ieee.org).

X. Chen, A. A. Pise, and I. Batarseh are with the Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL 32816 USA (e-mail: xi.chen@knights.ucf.edu; intelflux@knights.ucf.edu; issa.batarseh@ucf.edu).

M. Alharbi is with the Department of Electrical Engineering, Taibah University, Medina 42353, Saudi Arabia (e-mail: mahmood@knights.ucf.edu).

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I. Introduction

MOST of the research and development efforts in solar PV energy have focused on the materials used to manufacture PV cells for an ultimate goal of reducing the cost and improving the efficiency of PV modules. Recently, new efforts have been noticed on the integration side of the PV module and its power converters [1]. The concept of ac PV module—a fully integrated PV module that can be directly connected to the grid—has been proposed in [2]–[4]. This concept is interesting in the sense that PV modules can be used in a "plug and play" fashion, which is quite advantageous for allowing the full integration of the module with its power conversion circuits and control algorithms. This in turn allows for a modular and flexible design, and moreover, higher output power generation since each PV module has power converters that operate at a moving optimal operating point, unlike the traditional PV modules that are connected to a string or centralized inverter optimized at a fixed operating point.

The power generated by PV cells fluctuates widely on different time scales (minutes, hours, days, seasons, etc.). These fluctuations are due to many factors such as solar irradiance fluctuation, ambient temperature variation, shading, or dust accumulation. To enhance the operation of the PV module, the MPPT algorithms are implemented in the dc–dc converter to maximize the power generated by the PV source [5]–[9]. The trend in PV MPPT research, according to the reviewed literature, is in improving the performance of the algorithm by increasing its speed and accuracy [5], [10]–[13]. The MPPT algorithms found in literature optimize a single parameter, which is the operating voltage of the PV module. To date, the design of the PV power converters (dc–dc and dc–ac) is mainly optimized at a fixed operating point (a single-input power value). Yet, no work has been reported on maximizing the power injected to the grid by simultaneously tracking the PV converters optimal operating points when the input power varies, which is

very common in PV applications. In a PV system, where the generated power has a variable and sometimes unpredictable nature, optimizing the performance of each component in the system is advantageous for maximizing the output power at each instant. In a grid-tie PV system that consists of a number of power conversion stages, the power injected to the grid can be increased by optimizing the operation of the dc–dc and dc–ac conversion stages. The efficiency of a dc–dc converter directly correlates with the switching frequency [14], [15]. Many studies have presented the techniques to improve the efficiency of the dc–dc converters. The method proposed in [15] uses the steepest descent technique to track the switching frequency that provides maximum converter efficiency. Different approaches have been proposed in [16]–[20] to improve the light load converter's efficiency for general applications. In addition, the efficiency of an SPWM inverter has also shown a dependence on the SPWM's switching frequency (also known as the carrier frequency or frequency of modulation) [21], [22]. In the SPWM inverters, the switching frequency is usually set at a fixed value that optimizes the inverter's operation in terms of power quality and efficiency at a single-operating point (input power). However, as the power processed by the inverter varies, the efficiency and the THD of the inverter's output voltage and current will vary as well [22]. To improve the power generated by the inverter in terms of maximizing that power and at the same time maintaining a specific THD value, the switching frequency that maximizes the power while maintaining a specific THD must be tracked for any operating condition.

This article proposes a novel adaptive grid-tie PV system with an online tri-MPPT algorithm that maximizes the power injected to the grid and reduces the THD at the output by closely tracking the optimal operating points of both the PV source and the power converters. The proposed algorithm has several merits as follows.

1) It maximizes the output power of the system by optimizing three parameters, namely: the PV voltage, the converter, and the inverter efficiencies (unlike methods in literature where only a single parameter is optimized).
2) It has a 100% convergence rate and a fast convergence speed, since it uses an adaptive variable step-size algorithm.
3) It can be implemented at a low cost due to its simplicity.
4) It requires no tuning at all.

A high-level block diagram of the proposed system is demonstrated in Fig. 1. In this figure, three control loops are shown: the first is for controlling the PV panel operating voltage, which is similar to the traditional MPPT techniques where the PV panel is operated at the maximum-power voltage, while the second loop controls the switching frequency of the converter to yield a maximum possible efficiency at a specific input power condition. The third control loop is for operating the SPWM inverter at the maximum-efficiency switching frequency at a THD below a predetermined value (according to [23], the maximum allowed current THD is 5%). In this article, the THD value will be controlled under 4% (this control loop sets the SPWM switching frequency at a value at which the efficiency has a peak value while the THD is always under 4%).

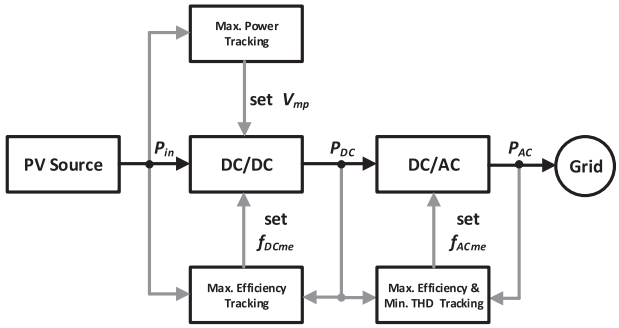

Fig. 1. Demonstration of the system with the control loops for the proposed tracking algorithm.

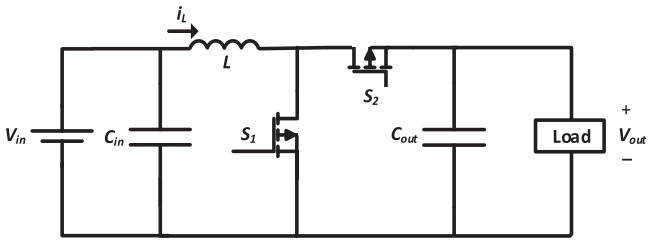

Fig. 2. Synchronous dc–dc boost converter circuit.

This article is organized as follows. Sections II and III represent the mathematical models and the design considerations of the dc–dc and dc–ac converters, respectively. Section IV presents the proposed algorithm, while Section V provides the experimental results and discussion. Section VI concludes this article.

II. DC–DC Stage

Typically in the grid-tie PV systems, a boost converter is used in the dc–dc stage. Fig. 2 shows a synchronous dc–dc boost converter that is used to mathematically model the dynamic losses in the dc–dc conversion stage. The synchronous dc–dc boost converter has the merit of higher efficiency at heavy load compared to the nonsynchronous dc–dc converter.

Generally, the total power losses in each switching cycle in a dc–dc converter is the sum of conduction losses, switching losses, gate-drive losses, and magnetic losses [15], [21], [24]. The conduction losses $(I_{\rm rms}^2 \times R)$ are a function of the parasitic resistances of all components and of the squared rms current in these resistances. The switching losses are a function of the switching frequency and parasitic capacitances of the switching devices. The gate-drive losses are due to the power consumption of the switching devices and are a function of the switching frequency. The magnetics losses consist of core loss and winding loss and both are the function of the switching frequency. Generally, the core loss density can be extracted from the datasheet and the winding losses (dc winding loss and ac winding loss) can be expressed by

$$\frac{R_{\rm ac}}{R_{\rm dc}} = \frac{(r_o/\delta)^2}{2\left[\frac{r_o}{\delta} + e^{-\frac{r_o}{\delta}} - 1\right]} \tag{1}$$

$$P_{\rm AC} = I_{pk}^2 \times R_{\rm ac} \tag{2}$$

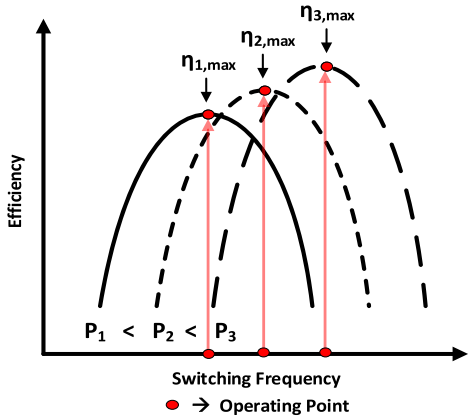

Fig. 3. Correlation between the efficiency and the switching frequency of the dc–dc converter at different power levels.

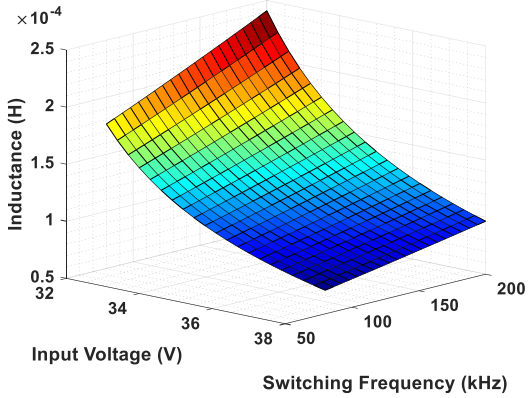

Fig. 4. Critical inductance to operate with the variable switching frequency.

$$P_{\mathrm{DC}} = I_{\mathrm{rms}}^2 \times R_{\mathrm{dc}} \tag{3}$$

where r_0 is the radius of the wire, δ is the skin depth, I_{pk} is the peak current, I_{rms} is the root-mean-square current, R_{dc} is the dc resistance, and R_{ac} is the ac resistance.

As the effective current I_{rms} in the components increases, the conduction losses increase. At low frequencies, the current ripple is large resulting in large I_{rms}, which in turn, makes the conduction losses higher at low frequencies. On the other hand, the switching losses are mainly due to the nonideal characteristics of the switch and gate driver. These components require finite time to turn ON and OFF. These finite times include rise time or turn-ON time (t_{on}) and fall time or turn-OFF time (t_{off}). Also, the switch needs some time to respond to the gate-driver signal known as the delay time (t_{delay}), which occurs when turning from OFF to ON or vice versa. As the switching frequency increases, these times become more significant and, hence, the switching losses get higher. Fig. 3 shows the generic efficiency curves of a dc–dc converter at different switching frequency and load conditions [14].

Since the dc–dc boost converter has a variable switching frequency and a variable input voltage, it is important to make sure that the selected inductor and capacitor values can operate over a wide range of the switching frequency. In addition, the switching frequency range needs to be limited, otherwise, if the upper bound of the frequency is too high, the switching loss will increase at light load, which will in turn decrease the efficiency, and if the lower bound of the frequency is too low, the current ripple will increase leading to the high conduction loss, which will again decrease the efficiency [25].

For a boost converter, the inductance L is given by [26]

$$L = \frac{V_{\mathrm{in}} \times (V_{\mathrm{out}} - V_{\mathrm{in}})}{\Delta I_L \times f_{\mathrm{sw}} \times V_{\mathrm{out}}} \tag{4}$$

where V_{in} is the input voltage coming from the PV source, V_{out} is the desired output voltage, ΔI_L is the inductor ripple current, and f_{sw} is the switching frequency.

Fig. 4 shows the minimum required inductance to allow the boost converter to operate with a variable switching frequency and input voltage with the prototype parameters provided in Section V. According to this figure, the inductance needs to be chosen at least at 242 μH to guarantee the operation over a switching frequency between 80 and 200 kHz and an input voltage range between 32 and 38 V.

Capacitance is required to maintain a regulated output voltage when the high-side MOSFET is OFF. Also, it is necessary to minimize the output voltage ripple. In addition, the transient load response capability of the output stage has to be considered since the output voltage will temporarily increase, which is known as the output voltage overshoot (V_{ov}), when the load current changes from high to low until the converter duty cycle is adjusted to return the output voltage to its regulated value [26]. The worst case occurs when the load current changes from maximum to zero, for which case the energy balance equation is shown as [27]

$$\frac{1}{2}LI_{\mathrm{pk}}^2 + \frac{1}{2}CV_{\mathrm{out}}^2 = \frac{1}{2}C(V_{\mathrm{ov}} + V_{\mathrm{out}})^2 \tag{5}$$

where I_{pk} is the peak current flowing through the inductor, and C is the capacitance.

Rearranging (5) yields

$$C = \frac{LI_{\mathrm{pk}}^2}{(V_{\mathrm{ov}} + V_{\mathrm{out}})^2 - V_{\mathrm{out}}^2}. \tag{6}$$

Fig. 5 demonstrates the minimum allowable capacitance to operate with the switching frequency between 80 and 200 kHz and an input voltage between 32 and 38 V. From this figure, the minimum capacitance must be 30 μF.

The minimum switching frequency step f_{step} depends on many parameters, such as the ADC resolution, sufficient changes in the input current made by minimum change in the switching frequency that the current sensor can detect, and so on [28]. In any converter, the following power balance equation must always be satisfied

$$P_{\mathrm{in}} = P_{\mathrm{out}} + P_{\mathrm{loss}} = V_{\mathrm{out}}I_{\mathrm{out}} + P_{\mathrm{loss}} \tag{7}$$

which yields

$$I_{\mathrm{in}} = \frac{V_{\mathrm{out}}I_{\mathrm{out}}}{V_{\mathrm{in}}} + \frac{P_{\mathrm{loss}}}{V_{\mathrm{in}}}. \tag{8}$$

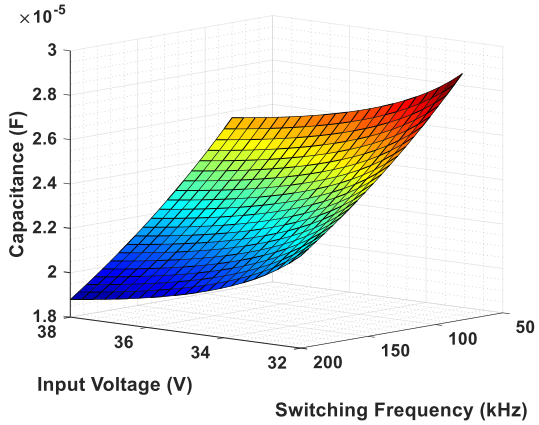

Fig. 5. Critical capacitance to operate with the variable switching frequency.

The input current gradient ∇I_{in} as a function of the switching frequency f_{sw} can be shown as [29]

$$\nabla I_{\text{in}} = \frac{\partial I_{\text{in}}}{\partial f_{\text{sw}}} = \frac{\partial\left(\frac{V_{\text{out}} I_{\text{out}}}{V_{\text{in}}}\right)}{\partial f_{\text{sw}}} + \frac{\partial\left(\frac{P_{\text{loss}}}{V_{\text{in}}}\right)}{\partial f_{\text{sw}}} = \frac{\partial\left(\frac{P_{\text{loss}}}{V_{\text{in}}}\right)}{\partial f_{\text{sw}}}. \tag{9}$$

The term $\frac{\partial(\frac{V_{\text{out}} I_{\text{out}}}{V_{\text{in}}})}{\partial f_{\text{sw}}}$ in (9) is eliminated since the output power at a specific load condition is constant and not a function of the input voltage or the switching frequency, and hence its gradient will be zero.

The minimum change the ADC can sense is

$$\Delta V_{\text{ADC}}^{\min} = \frac{V_{\text{ADC}}}{2^{N_{\text{bit}}}} \tag{10}$$

where $\Delta V_{\text{ADC}}^{\min}$ is the minimum voltage change ADC can sense, V_{ADC} is the typical ADC sensing voltage, and N_{bit} is the number of bits in the ADC.

For the prototype described in Section V, the input current is sensed by a 12-bit ADC with $V_{\text{ADC}} = 3.3$ V, therefore,

$$\Delta V_{\text{ADC}}^{\min} = \frac{V_{\text{ADC}}}{2^{N_{\text{bit}}}} = \frac{3.3}{2^{12}} = 8.057 \times 10^{-4} \text{ V}. \tag{11}$$

The current is sensed by a 2 mΩ sensing resistor with a current sensing op-amp gain set to 100 V/V, the minimum current change that will result in a 0.8057 mV voltage change can be calculated as

$$\Delta V_{\text{ADC}}^{\min} = I_{\text{in\_sense}} \times R_{\text{sense}} \times \text{gain} \tag{12}$$

yielding

$$I_{\text{in\_sense}} = 4.02 \times 10^{-3} \text{ A}.$$

Thus, the minimum switching frequency change that causes the minimum current change can be obtained by [30]

$$f_{\text{step}} = \frac{I_{\text{in\_sense}}}{\nabla I_{\text{in}}}. \tag{13}$$

Using (13), the switching frequency step size can be calculated. It shall be noted that since the proposed converter has a variable input voltage, the minimum step size will be different for the input-voltage value.

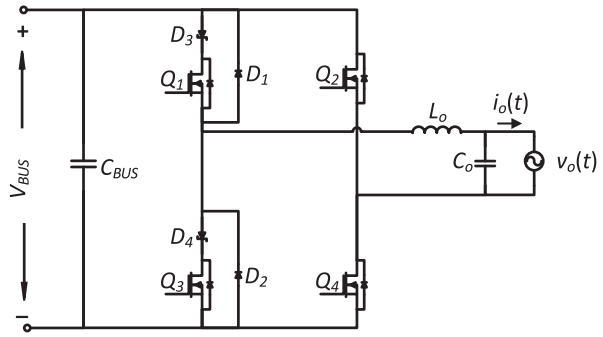

Fig. 6. H-bridge microinverter topology.

III. DC–AC Stage

The inverter used in the proposed system is a grid-tie, single-phase, H-bridge SPWM microinverter. In SPWM inverters, the pulsewidth is a sinusoidal function of the angular position, which is advantageous compared to the conventional (uniform) PWM in terms of reducing the lower order harmonics of the modulated voltage waveform [22]. A basic H-bridge inverter is shown in Fig. 6.

To accurately calculate the efficiency of the inverter stage, all losses of both active and passive devices must be calculated. As shown in Fig. 6, there are eight active and three passive devices, where each switch is driven by a single device.

The left-side leg of the inverter, which consists of Q_1, Q_3, D_1, D_2, D_3, and D_4, operates at high switching frequency (f_s). The right-side leg, which consists of Q_2 and Q_4, operates at frequencies as low as the fundamental frequency (f). Since the goal, here, is to model the correlation between the SPWM frequency and the inverter's output, the only passive component that will be considered in the calculation is the output filter inductor (L_o). According to the operation modes of the H-bridge inverter, both the positive and negative half-cycles have the same losses, since they run using the same type and the number of devices and components. So, calculating the losses during the positive half-cycle only will provide adequate results. Equation (14) represents the total instantaneous loss $(P_{\text{loss}_{\text{total}}})$ as a function of time. According to (14), there are three types of losses, namely: inductor losses, conduction losses, and switching losses. $P_{L_{\text{DC}}}$ and $P_{L_{\text{core}}}$ are defined as the inductor dc and core losses, respectively. The conduction losses are distributed among the two operation modes of the SPWM topology, where $P_{Q1_{\text{con}}}$ and $P_{D3_{\text{con}}}$ are calculated when Q_1 and D_3 are conducting, while $P'_{D2_{\text{con}}}$ and $P'_{Q4_{\text{con}}}$ are calculated when Q_4 and D_2 are conducting. $P_{Q1_{\text{sw}}}$ and $P_{Q4_{\text{sw}}}$ are defined as the switching losses for Q_1 and Q_4, respectively.

$$\begin{aligned} P_{\text{loss}_{\text{total}}}(t) = {} & P_{L_{\text{DC}}}(t) + P_{L_{\text{core}}} + P_{Q1_{\text{con}}}(t) + P_{D3_{\text{con}}}(t) \\ & + P'_{D2_{\text{con}}}(t) + P'_{Q4_{\text{con}}}(t) + P_{Q1_{\text{sw}}}(t) \\ & + P_{Q4_{\text{sw}}}(t). \end{aligned} \tag{14}$$

The instantaneous and averaged efficiencies are given in (15) and (16), respectively, where P_o is the average output power.

$$\eta(t) = \frac{P_o - P_{\text{loss}_{\text{total}}}(t)}{P_o} \times 100\% \tag{15}$$

$$\eta = \frac{2}{T}\int_0^{T/2} \eta\,(t)\,dt. \tag{16}$$

A commonly used parameter for evaluating the power quality and the performance of the grid-tie inverters is the THD. For a system that has a THD-based control strategy, low complexity and continuous measurement of the THD are required without interrupting the main operation of the microcontroller. A common method of measuring the THD is by using the quasi-synchronous sampling algorithm [31]. The periodic current signal can be expressed as the trigonometric Fourier series as in (17), where (18) and (19) are the Fourier coefficients, and the nth harmonic term and the phase angle of each term (fundamental and other harmonics) are expressed in (20) and (21).

$$i\,(t) = \frac{I_{a0}}{2} + \sum_{n=1}^{\infty}\left(i_{an}\cos\left(n\omega t\right) + i_{bn}\sin\left(n\omega t\right)\right) \tag{17}$$

$$i_{an} = \sqrt{2} I_n \sin\varphi_{\text{in}} \tag{18}$$

$$i_{bn} = \sqrt{2} I_n \cos\varphi_{\text{in}} \tag{19}$$

$$I_n = \frac{1}{\sqrt{2}} i_{cn} = \sqrt{\frac{i_{an}^2 + i_{bn}^2}{2}} \tag{20}$$

$$\varphi_{\text{in}} = \tan^{-1}\frac{i_{an}}{i_{bn}}. \tag{21}$$

The fundamental current and the current of other harmonics can be expressed as

$$\begin{aligned} I_n\,(t) &= i_{cn}\sin\left(n\omega t + \varphi_{\text{in}}\right) \\ &= i_{an}\cos\left(n\omega t\right) + i_{bn}\sin\left(n\omega t\right). \end{aligned} \tag{22}$$

The THD is defined as

$$\text{THD}_i = \frac{\sqrt{\sum_{n=2}^{N} I_n^2}}{I_1} \times 100\%. \tag{23}$$

The efficiency is measured by averaging the input and the output power of the H-bridge microinverter by monitoring the sampled signals for the input and output currents and voltages. The averaged sampled power over one-line period is

$$\bar{P} = \frac{1}{T}\sum_{t=0}^{T} i\,(t)\cdot v\,(t) \tag{24}$$

where

$$\begin{cases} i\,(t) = I_{pk}\sin\omega t \\ v\,(t) = V_{pk}\sin\omega t. \end{cases} \tag{25}$$

So, the efficiency is expressed as

$$\eta = \frac{\overline{P_o}}{\overline{P_{\text{in}}}} \times 100\% \tag{26}$$

where $\overline{P_o}$ and $\overline{P_{\text{in}}}$ are the averaged sampled output and input powers over one-line period, respectively.

The dependence of the THD and the efficiency of the inverters on its SPWM switching frequency are approximated, as shown in Fig. 7. In this figure, it was found that as the SPWM frequency increases, the THD tends to decrease and the efficiency tends to increase. However, if the frequency increases above a certain value at a specific load, the THD will go up while the efficiency will go down [22]. Hence, to optimize the inverter's operation, a search algorithm must be used to track the inverter's optimal operating point for peak efficiency with a specific THD value, as will be demonstrated in Section V.

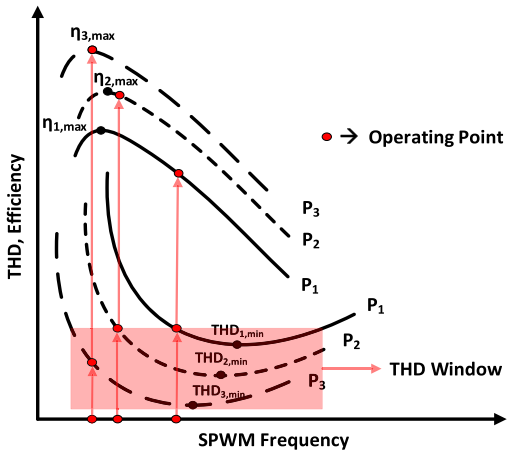

Fig. 7. Correlation between the THD, efficiency, and the SPWM switching frequency of the inverter at different power levels.

IV. Proposed Algorithm

The proposed technique employs a simple but powerful algorithm to allocate the optimal operating points of the PV module and the power converters to maximize the output power while maintaining a high-power quality (THD $< 4\%$). A flowchart of the proposed algorithm is shown in Fig. 8. The algorithm starts by setting an initial value for the controlled parameters (the PV panel voltage, and the converter's and inverter's switching frequencies).

In the first control loop, the algorithm searches for V_{mp} of the PV module. The initial value of V_{mp} and the initial step size are set at 35 V and 4 V, respectively. Each time a change in the sign of the slope, i.e., $\Delta P_{\text{in}}/\Delta V_{\text{mp}}$, is detected, the step size is divided by 2 and the search algorithm reverses its direction. The search loop is repeated until a termination criterion is met, at which instance the parameter V_{mp} is set at the value that corresponds to the maximum power.

The algorithm then searches for f_{DCme} of the dc–dc converter in the second control loop. The value of this frequency is initially set at 85 kHz, while the initial step size in this loop is set at 32 kHz. As the algorithm gets closer to the true value of f_{DCme}, the step size is divided by 2 every time the sign of the slope, i.e., $\Delta\eta_{\text{DC–DC}}/\Delta f_{\text{DCme}}$, changes and the search direction is reversed. The search loop is terminated when a termination criterion is met, and f_{DCme} is set at the value that corresponds to the maximum efficiency.

In a similar fashion, the optimal SPWM frequency at the ac side (f_{ACme}), which provides the maximum performance in terms of efficiency and power quality, is tracked. Initially, f_{ACme} is set at 20 kHz and the initial step size is set at 8 kHz. The

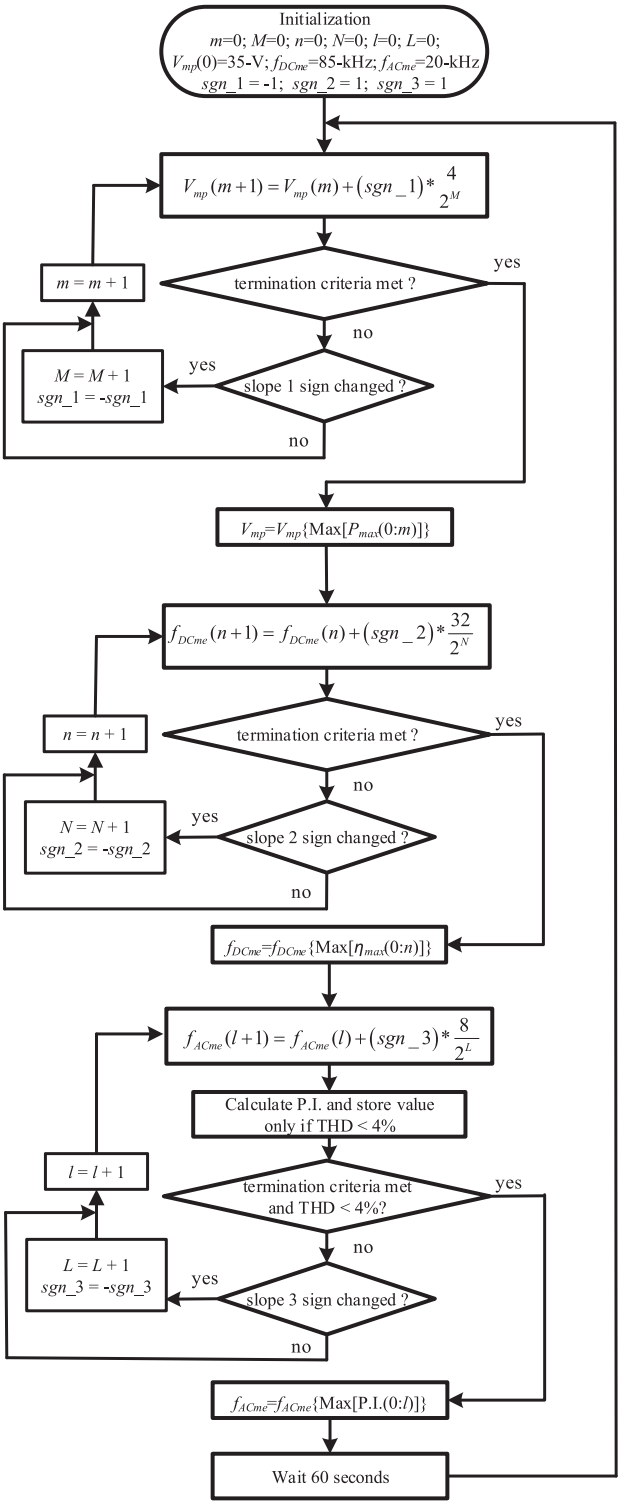

Fig. 8. Flowchart of the proposed adaptive tri-MPPT algorithm.

step size is divided by 2 each time the sign of the slope, i.e., $\Delta\eta_{\mathrm{DC-AC}}/\Delta f_{\mathrm{ACme}}$, is changed. This process continues until the value of f_{ACme} for maximum efficiency and THD below 4% is detected.

All search loops are terminated if any of the following is met.

TABLE I
TERMINATION CRITERIA BASED ON SLOPE

	Slope Termination Criteria
Control Loop 1	slope 1= $\Delta P_{in}/\Delta V_{mp}$ $(\text{slope 1})_{\min} = \pm 0.1$ W/V
Control Loop 2	slope 2 = $\Delta\eta_{DC\text{-}DC}/\Delta f_{DCme}$ $(\text{slope 2})_{\min} = \pm 0.01$ %
Control Loop 3	slope 3 = $\Delta\eta_{DC\text{-}AC}/\Delta f_{ACme}$ $(\text{slope 3})_{\min} = \pm 0.01$ %

TABLE II
SPECIFICATIONS OF THE DC–DC CONVERTER

Category	**Value**
Rated Power	200 W
Output Voltage	200 V
Input Voltage	32 – 38 V
Switching Frequency	80 – 200 kHz
Minimum Inductor	242 μH
Minimum Capacitor	30 μF
Maximum Inductor Current	8 A

1) The slope drops below a predefined value, as given in Table I.
2) The number of changes in the slope sign reaches three.
3) The number of iterations reaches ten.

In Table I, P_{in} is the PV power or the converter's input power, and η_1 and η_2 are the efficiencies of the converter and the inverter, respectively. It shall be noted that the second and third search loops must be fast enough to identify the optimal operating points while the input power stays unchanged. For both loops, the algorithm converges within less than ten iterations, as will be verified experimentally in Section V. Moreover, with a good initialization, the search speed can be further improved.

V. EXPERIMENTAL RESULTS

To evaluate the proposed system experimentally, a solar array simulator was used to generate the PV data. A synchronous dc–dc boost converter was built and run at different load and switching frequency conditions. Two STB20NM50FD MOSFETs (with fast diode) were used with a 250-μH Eaton inductor and 40 μF film capacitor. The ON-resistance of the MOSFET ($R_{\mathrm{DS,on}}$) is 220-mΩ, the turn-ON delay and the turn-OFF delay times are 22 ns and 6 ns, respectively, and the rise and fall times are 20-ns and 15-ns, respectively. A 200-W H-bridge SPWM microinverter prototype with 200-V dc-bus voltage is built as well. All the control is implemented using a 32-bit STM32F103C8T7 DSP. A counter is used with a 72-MHz fixed clock. The sampling frequency of the ADC is 12-MHz. To ensure converter stability, a rest period was introduced after setting the switching frequency to ensure accurate readings. The efficiency data were taken by Yokogawa Power Analyzer PZ4000. The specifications of the developed prototypes are given in Tables II and III. The system and experimental setups used are shown in Fig. 9.

To quantify the improvement in both the efficiency and the power quality of the proposed PV system achieved using the proposed technique, a performance index (P.I.) is defined in

TABLE III
SPECIFICATIONS OF THE SPWM H-BRIDGE INVERTER

Category	Value
Output Power	200 W
PV Voltage	24~45 V
Grid Voltage/ Frequency	~120 V/ 60 Hz
Nominal Bus Voltage	225 V

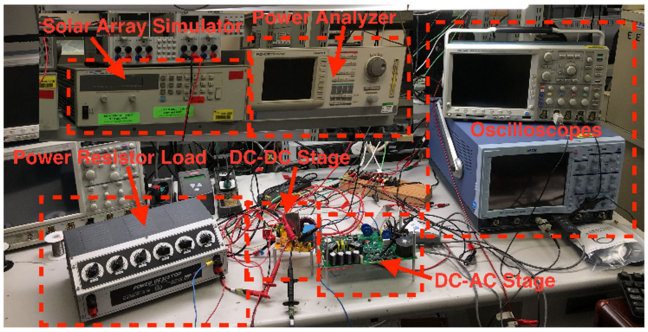

Fig. 9. Designed system and experimental setup used for testing.

TABLE IV
RESULTS AT 50-W LOAD POWER

Algorithm	THD (%)	P.I. (%)
Single MPPT (f_{s1} = 85 kHz & f_{s2} = 10 kHz)	11.19	84.58
Single MPPT (f_{s1} = 200 kHz & f_{s2} = 10 kHz)	11.19	85.99
Single MPPT (f_{s1} = 85 kHz & f_{s2} = 20 kHz)	6.10	89.34
Single MPPT (f_{s1} = 200 kHz & f_{s2} = 20 kHz)	6.10	90.82
Dual MPPT ($f_{s1} = f_{DCme}$ & f_{s2} = 10 kHz)	11.19	86.07
Dual MPPT ($f_{s1} = f_{DCme}$ & f_{s2} = 20 kHz)	6.10	90.91
Proposed Tri MPPT ($f_{s1} = f_{DCme}$ & $f_{s2} = f_{ACme}$)	3.81	92.82

TABLE V
RESULTS AT 100-W LOAD POWER

Algorithm	THD (%)	P.I. (%)
Single MPPT (f_{s1} = 85 kHz & f_{s2} = 10 kHz)	4.36	91.87
Single MPPT (f_{s1} = 200 kHz & f_{s2} = 10 kHz)	4.36	93.30
Single MPPT (f_{s1} = 85 kHz & f_{s2} = 20 kHz)	2.48	93.65
Single MPPT (f_{s1} = 200 kHz & f_{s2} = 20 kHz)	2.48	95.09
Dual MPPT ($f_{s1} = f_{DCme}$ & f_{s2} = 10 kHz)	4.36	93.48
Dual MPPT ($f_{s1} = f_{DCme}$ & f_{s2} = 20 kHz)	2.48	95.27
Proposed Tri MPPT ($f_{s1} = f_{DCme}$ & $f_{s2} = f_{ACme}$)	2.19	95.49

(27) and is used to evaluate the proposed tri-MPPT algorithm and compare it against the single and dual MPPT algorithms in [14] (see Tables IV–VI). The output voltage and the current waveforms for different loads and switching frequencies are shown in Figs. 10 and 11.

TABLE VI
RESULTS AT 200-W LOAD POWER

Algorithm	THD (%)	P.I. (%)
Single MPPT (f_{s1} = 85 kHz & f_{s2} = 10 kHz)	1.85	93.19
Single MPPT (f_{s1} = 200 kHz & f_{s2} = 10 kHz)	1.85	94.64
Single MPPT (f_{s1} = 85 kHz & f_{s2} = 20 kHz)	1.71	93.39
Single MPPT (f_{s1} = 200 kHz & f_{s2} = 20 kHz)	1.71	94.83
Dual MPPT ($f_{s1} = f_{DCme}$ & f_{s2} = 10 kHz)	1.85	94.83
Dual MPPT ($f_{s1} = f_{DCme}$ & f_{s2} = 20 kHz)	1.71	95.02
Proposed Tri MPPT ($f_{s1} = f_{DCme}$ & $f_{s2} = f_{ACme}$)	1.68	95.08

$$\text{P.I.} = \frac{P_{\text{out}}}{P_{\text{in}}}\,(1 - \text{THD}) \times 100\%. \tag{27}$$

According to the results, the proposed system not only increases the load power, but also reduces the generated THD. The last point is particularly important in the PV systems given the fact that PV power generation is consistently increasing and, hence, the issue of the THD injection is becoming more severe as a result. The improvement in both the efficiency and power quality can be controlled by adjusting the parameters of the search algorithm. However, it shall be noted that improving the efficiency and power quality by adjusting the algorithm parameters should not affect the speed of the algorithm, since increasing the delay between the loops may result in unreliable and inaccurate performance.

Another remark on the obtained results is that the improvement in the system's performance is more notable at light loads, as shown in Fig. 12, where the P.I. and the THD are shown for different scenarios. In this figure, the values for the P.I. and THD for the single- and dual-MPPT are shown at a 20 kHz SPWM frequency, while these values for the tri-MPPT are found at the optimal SPWM frequency, i.e., f_{Acme}. By optimizing the search algorithm parameters, the accuracy, reliability, and convergence rate can be improved.

The dc- and ac-stage optimization process using the proposed search algorithm is shown in Figs. 13 and 14, respectively. As shown, the algorithm was able to achieve convergence in less than ten iterations for each stage despite that the initial voltage of the PV source, the converter's switching frequency, and the SPWM frequency were purposefully wrong. According to the conducted experiments, the algorithm has a 100% convergence rate, which is achieved by employing the multiple termination criteria that prevent the algorithm from diverging after ten iterations or when no slope sign change is detected. Nonetheless, in all the conducted tests, the search process was terminated when the slope sign changed three times, which is occurred before the number of iterations reaches ten.

The sampling frequency of the ADC is selected based on the maximum and minimum switching frequency of the dc–dc

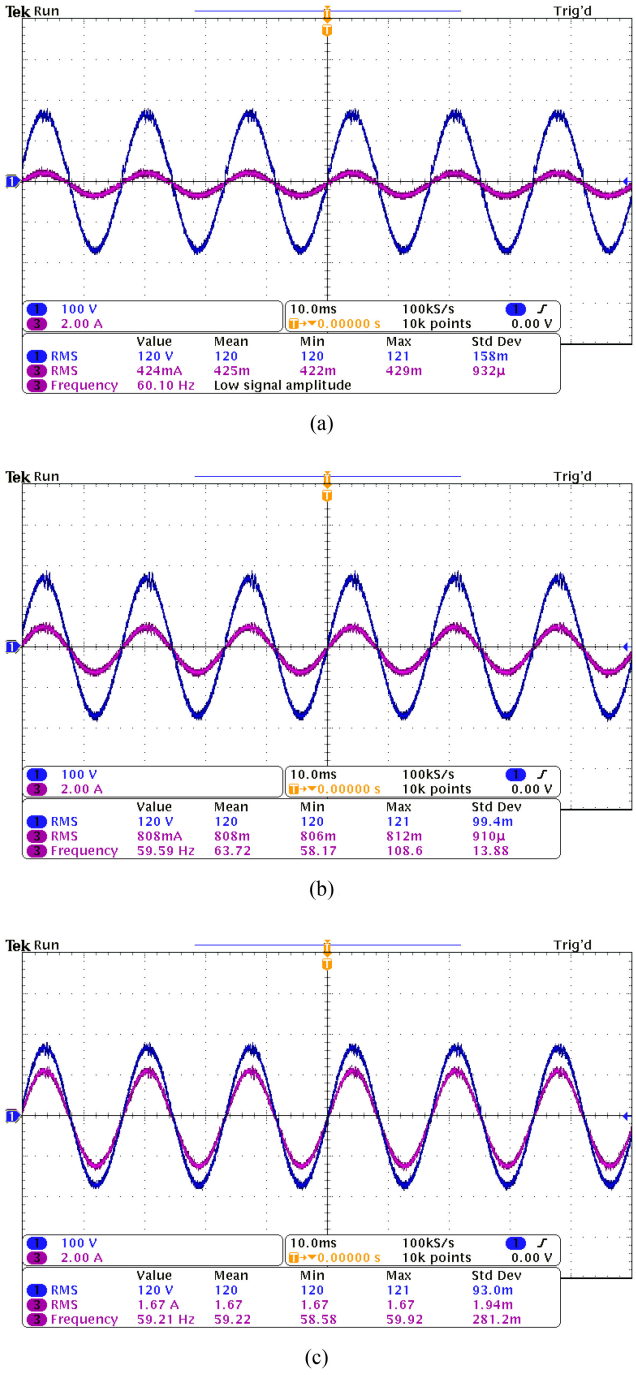

Fig. 10. Experimental output voltage and current waveforms of the proposed system at optimal operating point at different load conditions. (a) $P_{\mathrm{Load}} = 50.88$ W and $f_{\mathrm{ACme}} = 50$ kHz. (b) $P_{\mathrm{Load}} = 96.96$ W and $f_{\mathrm{ACme}} = 20$ kHz. (c) $P_{\mathrm{Load}} = 200.40$ W and $f_{\mathrm{ACme}} = 25$ kHz.

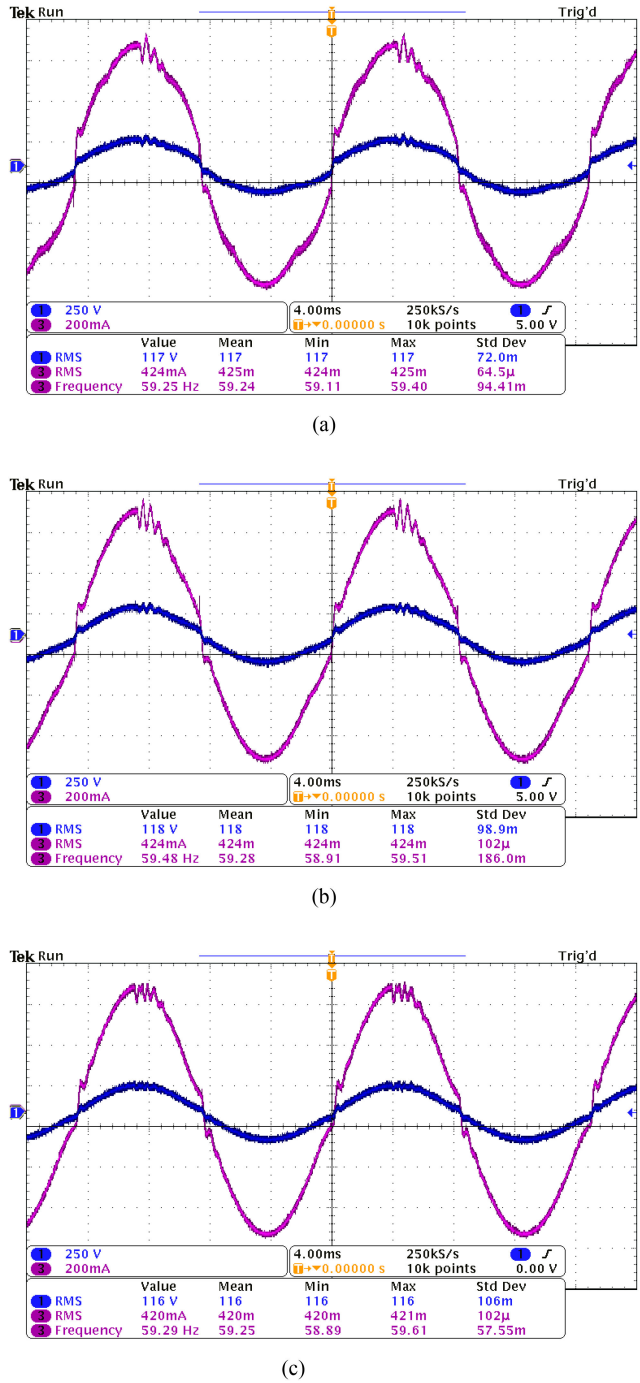

Fig. 11. Zoomed-in experimental output voltage and current waveforms of the proposed system at 50 W load (light load condition) at different SPWM frequencies. (a) $P_{\mathrm{Load}} = 49.61$ W and $f_{s2} = 10$ kHz. (b) $P_{\mathrm{Load}} = 50.03$ W and $f_{s2} = 20$ kHz. (c) $P_{\mathrm{Load}} = 48.72$ W and $f_{s2} = f_{\mathrm{ACme}} = 50$ kHz.

converter; the sampling frequency must be at least 140 kHz for the operating switching frequency range of the designed converter between 80 and 200 kHz. However, a much faster ADC was used in this article with a sampling frequency of 12 MHz. Theoretically, the time needed to complete each iteration is dictated mainly by the switching frequency of the converter, the sampling frequency of the ADC and the DSP speed assuming the converter's transients are negligible. Practically, however, the converter needs some time to stabilize when its frequency is changed. In the proposed system, an adequate wait time is introduced after the frequency is updated to ensure the converter stability. The selection of the wait time, however, can be optimized by addressing the correlation between the wait time and the operating frequency and/or the load power to achieve a faster convergence speed. For the proposed system, the frequency of the ADC and the DSP is much higher than the

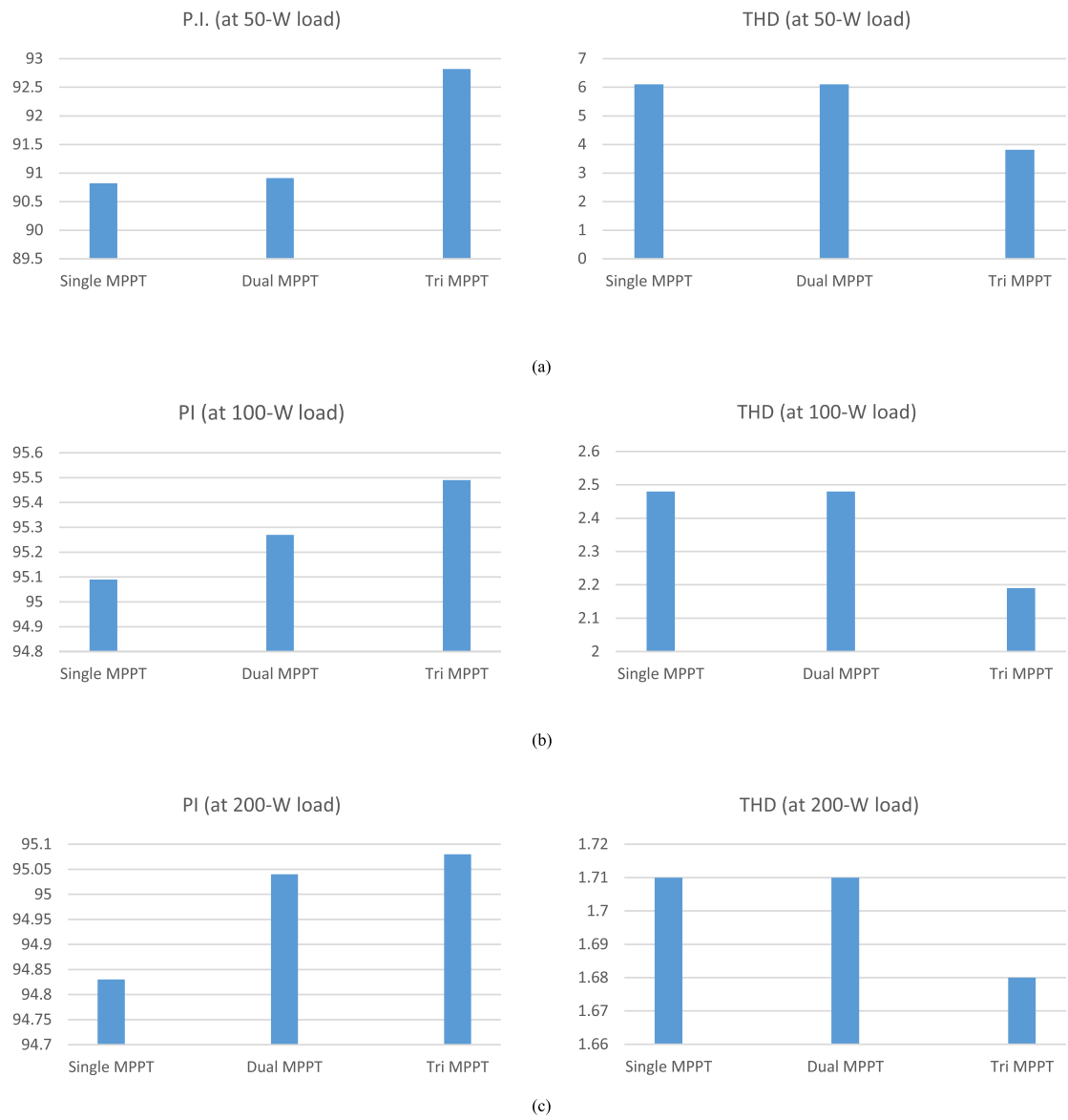

Fig. 12. Comparison of the THD and PI results for one-stage (PV alone), two-stage (PV + dc–dc), and three-stage (PV + dc–dc + dc–ac) optimization at 50-W load, 100-W load, and 200-W load. (a) Results at 50-W load for one-stage (single MPPT), two-stage (dual MPPT), and three-stage (tri-MPPT) optimization. (b) Results at 100-W load for one-stage (single MPPT), two-stage (dual MPPT), and three-stage (tri-MPPT) optimization. (c) Results at 200-W load for one-stage (single MPPT), two-stage (dual MPPT), and three-stage (tri-MPPT) optimization.

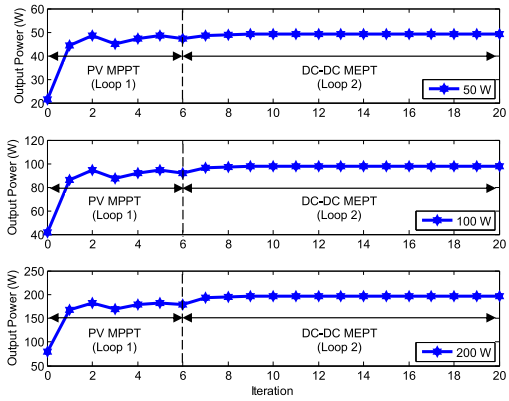

Fig. 13. DC stage optimization for the tested power conditions using the proposed algorithm (control loops 1 and 2).

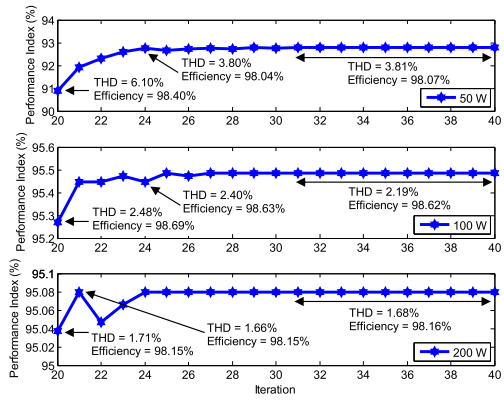

Fig. 14. AC stage optimization for the tested power conditions using the proposed algorithm (control loop 3).

converter's switching frequency, which means that a complete iteration can be achieved within one converter's switching cycle. In all the experiments conducted, the system converged within ten iterations or less for each optimization stage. Hence, with a carefully designed values for the converter's wait time and the ADC and DSP frequencies, the convergence speed of the tri-MPPT algorithm can be enhanced.

VI. Conclusion

A grid-tie PV system with a tri-MPPT algorithm is presented. The algorithm tracks the optimal operating points of the PV source and power converters (dc–dc and dc–ac stages). Results show that the proposed system is capable to reduce the generated THD and increase the efficiency, simultaneously, at any load value as verified experimentally at 25%, 50%, and 100% rated power. According to the results obtained, the improvement in both the power quality and efficiency is more notable at light loads, which is common in PV applications when the sun is covered by clouds or when dust accumulates over the PV panel. Although a basic prototype was built, the designed system has been successfully used to validate and prove the proposed technique. The designed dc–dc converter allows the switching frequency to vary between 80 and 200 kHz and the input voltage between 32 and 38 V, which is a reasonable range for a standard 200-W PV system. An SPWM-based inverter is selected as SPWM is capable to reduce lower order harmonics compared to the conventional (uniform) PWM.

Besides its high convergence speed and stability, the proposed technique avoids, to a great extent, wrong termination when the local maximum points are detected as it waits until the three slope-sign changes are detected. Future related research must investigate the possibility to implement the proposed search algorithm and control strategies using other power converter topologies.

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Ala A. Hussein (M'12–SM'18) received the B.S. degree from the Jordan University of Science and Technology, Irbid, Jordan, and the M.S. and Ph.D. degrees from the University of Central Florida, Orlando, FL, USA, all in electrical engineering, in 2005, 2008, and 2011, respectively.

He is an Expert in energy storage and conversion with over eight years of combined industrial, research, and teaching experience. He is an Associate Professor of electrical engineering with Yarmouk University, Irbid, Jordan. He also holds a joint appointment as a Research Associate with the Center of Florida Solar Energy and the Department of Electrical and Computer Engineering, Orlando, FL, USA. He has authored or coauthored more than 40 papers in leading refereed journals and conference proceedings.

Dr. Hussein was the recipient of multiple research excellence awards, and has successfully competed for a number of research grants totaling around $0.4 M.

Xi Chen (S'17) received the B.E. degree in photovoltaic and renewable energy engineering from the University of New South Wales, Sydney, NSW, Australia, in 2014, the B.S degree in applied physics from the South China University of Technology, Guangzhou, China, in 2014, the M.S. degree in electrical engineering from the University of Central Florida (UCF), Orlando, FL, USA, in 2016, and the joint graduate degree in electric drivetrain technology from the University of Colorado Colorado Springs, Colorado Springs, CO, USA, and the University of Colorado Boulder, Boulder, CO, USA, in 2018. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, UCF.

From 2015 to 2017, he was a Research Assistant with the Advanced Power Electronics Corporation, Orlando, FL, USA. He is currently with the Florida Power Electronics Center, UCF. His current research interests include efficiency optimization of dc–dc converters, soft-switching techniques, *LLC* resonant converter, digital controls, and magnetics design.

Mahmood Alharbi received the B.S. degree from Taibah University, Medina, Saudi Arabia, in 2010, the M.S. degree from the University of Colorado Colorado Springs, Colorado Springs, CO, USA, in 2014, and the Ph.D. degree from the University of Central Florida, Orlando, FL, USA, in 2018, all in electrical engineering.

He is a Faculty Member with the Department of Electrical Engineering, Taibah University. His research interests include power electronics application for renewable energy, energy storage, and power conversions.

Anirudh Ashok Pise received the B.E. degree in electrical and electronics engineering from Visvesvaraya Technological University, Belgaum, India, and the M.S. degree from the University of Central Florida (UCF), Orlando, FL, USA.

He is currently with the Florida Power Electronics Center, UCF. His current research interests include efficiency optimization of dc–dc converters, soft-switching techniques, *LLC* resonant converter, digital controls, and magnetics design.

Issa Batarseh (F'06) received the B.S.E.E. degree in electrical and computer engineering and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Chicago, IL, USA, in 1983, 1985, and 1990, respectively.

He is currently a Professor of electrical engineering with the Department of Electrical and Computer Engineering, University of Central Florida (UCF), Orlando, FL, USA. From 1989 to 1990, he was a Visiting Assistant Professor with Purdue University, Calumet, IN, USA, before joining the Department of Electrical and Computer Engineering, UCF, in 1991. He has authored or coauthored more than 80 refereed journals and 300 conference papers in addition to 31 U.S. patents. He is also the author of a textbook titled *Power Electronic Circuits* (Wiley, 2003) and a coauthor of the book titled *Power Electronics* (2nd ed., Springer). His research interests include power electronics and high frequency, smart grid-tied photovoltaic energy conversion systems. His team with the Florida Power Electronics Center has been leading the design, development, and commercialization of smart microinverters, and smart electric vehicle and industrial chargers. He is a member of the National Academy of Inventors and has been inducted into the Florida Inventors Hall of Fame. He served as a Chairman for the IEEE Power Electronics Specialists Conference, 2007, and was the Chair of the IEEE Power Engineering Chapter, the IEEE Orlando Section, and is currently serving as the Chair of the PELS Education Committee.

Dr. Batarseh is a Registered Professional Engineer in the State of Florida and a Fellow Member of the American Association for the Advancement of Science.