Design and Optimization of High-Failure-Current Dual-Direction SCR for Industrial-Level ESD Protection

Yang Wang, Xiangliang Jin, *Member, IEEE*, Yan Peng, Jun Luo, and Jun Yang

***Abstract*—In an industrial-grade bus, transient voltage suppressor (TVS) devices that need to withstand inrush currents ensure electrostatic discharge (ESD) reliability of the core chip. This article designs four types of dual-direction silicon-controlled rectifier (DDSCR) device structures based on the 0.5-μm CMOS process. The ESD performance of the TVS device is predicted and verified based on the basic principles of the device, two-dimensional device simulation, and transmission line pulse test results. Four DDSCR structures are embedded with floating N+ to adjust the device's holding voltage window. The results show that the current release capacity of DDSCR_1 is 81.93 mA/μm. The current release capability of DDSCR_2, which has a double-dummy-gate structure, is 82.37 mA/μm. The current release capability of DDSCR_3 of the gate-controlled structure is 86.68 mA/μm. The current release capability of DDSCR_4 of the double-dummy-gate structure and the gate-controlled structure is 86.25 mA/μm. Furthermore, the effect of the size of these devices on the ESD characteristics was studied. The ON-resistance of the device structure is calculated by the curve-fitting method. The influence of the dummy gate structure and the gate-controlled structure on the ESD characteristics is analyzed. Finally, the optimal device size to meet the window is found.**

***Index Terms*—Electrostatic devices, electrostatic discharges (ESDs), industrial electronics.**

I. Introduction

DUE TO the harsh working environment of the industrial-grade bus interface, high voltage and strong electromagnetic interference cause a serious robustness problem to the core chip. Accompanied by the continuous development of integrated circuits, the thickness of gate oxide of devices is getting thinner, and the electrostatic discharge (ESD) is becoming one of the main failure causes of electronic systems. Therefore, designing a high-performance transient voltage suppressor (TVS) device capable of on-chip integration against surge currents can help to reduce the manufacturing cost of industrial-grade chips. Usually, the bus interface requires bidirectional ESD protection to prevent forward and reverse ESD stress from damaging the core chip. The recently widely used diodes, bipolar junction transistor (BJT), and gate-grounded N-MOS devices do not have bidirectional conduction capability, and their protection capability does not satisfy the design requirements of the high-voltage resistance to surge current. However, taking advantage of a silicon-controlled rectifier (SCR), the device has deep snapback characteristics and is capable of conducting ESD currents higher than the aforementioned ESD devices. Through continuous optimization and the improvement of an SCR, an SCR device structure with the bidirectional release capability is designed. In order to solve the ESD problem of the industrial bus interface, the trigger surface is changed to adjust the device trigger voltage, and the device size is altered to adjust the device's holding voltage. According to the requirements of the ESD protection device design specific for the on-chip integrated industrial bus interface, the trigger voltage of the device should be lower than 24 V, the holding voltage should be higher than 14.4 V, the failure current should be greater than 10 A, and the human body model (HBM) level should be higher than 15 kV.

A waffle-type nLDMOS-SCR device fabricated by a 0.35-μm BCD process was proposed by Zheng *et al.*, and the device has achieved a failure current of 4.4 A. The waffle-type structure should be a promising layout for high-voltage ESD protection applications [1]. Ker and Chang proposed a new ESD protection scheme. The solution features an on-chip ESD bus and a high-voltage ESD clamp circuit for a 1.2-V/2.5-V mixed-voltage I/O interface, which is an excellent and cost-effective solution for protecting mixed-voltage I/O interfaces [2]. Dai and Ker used a 0.25-μm CDMOS process to design an SCR with a stacked high holding voltage. The proposed high-holding-voltage SCR structure can adapt to the ESD protection design window for the 60-V pins of the battery-monitoring IC and can successfully protect these 60-V pins from 7-kV human body ESD stress [3]. A novel SCR is fabricated using a 0.25-μm high-voltage BCD process. Dai and Ker studied the Joule heating effect of the device on the SCR path [4]. The design of [1]–[4] is difficult

Manuscript received May 3, 2019; revised September 4, 2019; accepted September 22, 2019. Date of publication September 25, 2019; date of current version February 11, 2020. This work was supported in part by the National Natural Science Foundation of China under Grant 61827812, Grant 61774129, and Grant 91648119, in part by the Hunan Science and Technology Department Huxiang High-level Talent Gathering Project under Grant 2019RS1037, in part by Changsha Science and Technology Plan Key Projects under Grant kq1801035, and in part by the Project of Shanghai Municipal Science and Technology Commission under Grant 17DZ1205000. Recommended for publication by Associate Editor M. Nawaz. *(Corresponding authors: Xiangliang Jin; Yan Peng.)*

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Digital Object Identifier 10.1109/TPEL.2019.2944073

to meet the failure window of industrial-grade ESD protection. Guan *et al.* proposed a novel embedded topology; significantly improving the holding voltage of SCR devices, the design can be applied to high-voltage ESD protection [5]. Lou and Liou proposed a new SCR with a 7-V trigger voltage and a current release capability of 60 mA/μm for a powerful ESD protection solution [6]. Liu *et al.* developed a novel SCR stack structure with an extremely high holding voltage, very small rebound, and acceptable failure current [7]. The design scheme for improving the holding voltage has been well applied [5]–[7]. However, how to effectively improve the device's holding voltage, meanwhile maintaining the high current-processing capability of the device, is a problem that needs to be solved for industrial-grade ESD protection.

In order to design a TVS device that meets industrial-grade ESD protection, four types of DDSCR structures are fabricated. A double-dummy-gate structure and a gate-controlled structure are used to improve the ESD characteristics of the device [8]. They are fabricated in a 0.5-μm CMOS process without any additional masking or process modifications. The important dimensions of the device to improve the holding voltage under the premise of maintaining the failure ability are found. The reasons why the double-dummy-gate structure affects the trigger voltage and voltage clamping capability of the device are discussed, and the high protection capability of the gate control device is verified. Therefore, the optimized device structure can be used for industrial-grade ESD protection and can ensure the normal operation of the core chip.

II. Design and Discussion of the DDSCR Structure

DDSCR_1, DDSCR_2, DDSCR_3, and DDSCR_4 are shown in Fig. 1(a)–(d), respectively. The four types of DDSCR structures use P+ and DN-Well to form the trigger surface and have a symmetrical two-way path meeting the trigger window requirements for industrial-grade ESD protection.

Fig. 2 shows the equivalent circuit diagram of the DDSCR structure. When the forward ESD current stress reaches the device anode, the P+ and DN-Well of the cathode generate an avalanche breakdown effect. A large number of avalanche carriers generate a voltage drop across the parasitic resistance R_p of the P-Well (cathode), and then, the parasitic transistor NPN (cathode N+/cathode P-Well/DN-Well) is turned on. With the similar latch-up effect of the SCR, the parasitic PNP (cathode P-Well/DN-Well/anode P-Well) is turned on; the positive feedback loop is formed such that the DDSCR is fully turned on, and thereby, the ESD current stress is discharged. The reverse conduction principle of the device is the same as the forward conduction principle. The four types of DDSCR structures are embedded with a floating N+ structure to increase the holding voltage of the DDSCR. Floating N+ increases the anode-to-cathode distance of the device, making the ESD release path longer. Moreover, the N+ structure increases the concentration of the base region of the parasitic PNP and reduces the emission efficiency of the parasitic transistor. Thereby, the holding voltage is significantly improved as compared to the conventional structure.

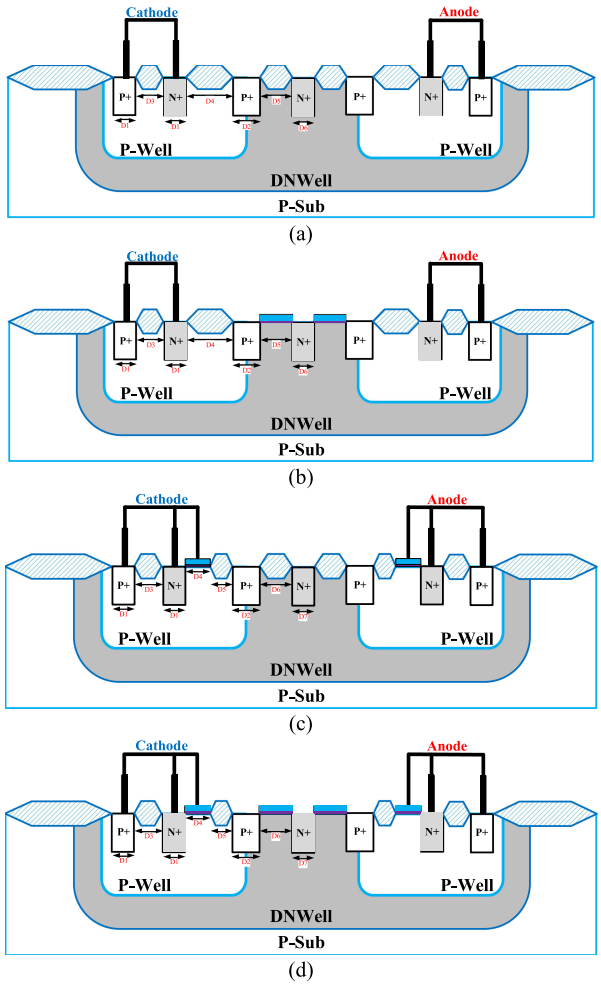

Fig. 1. (a) Cross section of the DDSCR_1 structure. (b) Cross section of the DDSCR_2 structure. (c) Cross section of the DDSCR_3 structure. (d) Cross section of the DDSCR_4 structure.

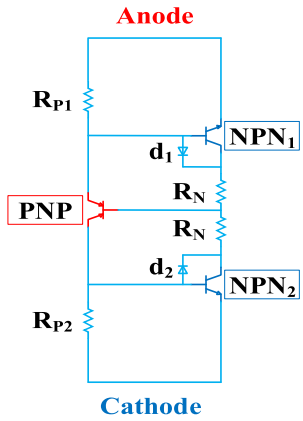

Fig. 2. Equivalent circuit of the DDSCR.

A. Double-Dummy-Gate Structure

DDSCR_2 uses a double-dummy-gate structure, which replaces the isolation layer on both sides of the floating N+ with a floating polysilicon gate. The floating polysilicon gate provides more ESD release path than the isolation layer, allowing part of the ESD current stress to flow from the device anode to

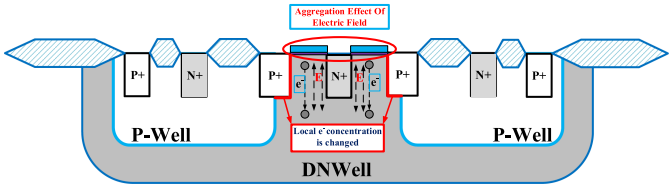

Fig. 3. Schematic diagram of the double-dummy-gate structure.

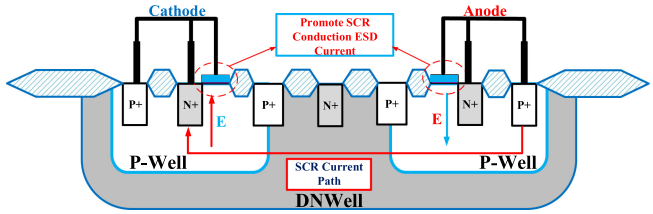

Fig. 4. Schematic diagram of the gate-controlled structure.

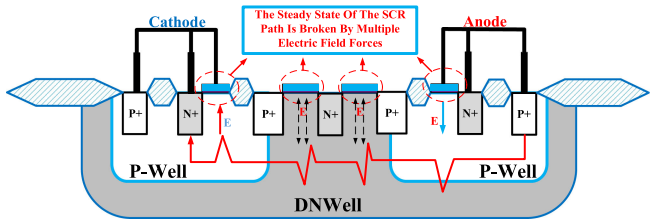

Fig. 5. Schematic diagram of the double-dummy-gate and gate-controlled structures.

the cathode without bypassing the isolation layer. The high concentration of floating N+ will promote more carriers to pass through the surface of the device. Floating N+ results in a DDSCR device having a higher voltage clamping speed and a shorter PNPN low resistance path formation time. The device can effectively protect the core chip from ESD stress damage. However, the inherent instability of the dummy gate structure is manifested by the concentration effect of the electric field. In the position, where the avalanche breakdown occurs in the device, a strong electric field force is collected under the dummy gate, which causes the local concentration of DN-Well to change significantly. This affects the avalanche breakdown voltage of the reverse-biased PN junction of DN-Well and P+, causing the shift of the forward and reverse trigger voltages of the DDSCR device. Moreover, since the two dummy gate structures can share a partially unstable electric field, the breakdown probability of the dummy gate structure at the time of conduction is greatly reduced. The reverse-biased PN junction formed by P+ and DN-Well is a P + N junction. It is known that the drift velocity of electrons is three times higher than that of holes. Changing the electron concentration on the side of the low-doped N region of the local PN junction causes a significant drift in the avalanche breakdown voltage of the PN junction. The amount of compensation for holes cannot compensate for the amount of electrons missing

$$U_B = \frac{1}{2}\left(\frac{\varepsilon_S \varepsilon_0}{q}\right)^{3/4}\left(\frac{8}{C_i}\right)^{1/4} N_D^{-3/4}. \tag{1}$$

The avalanche breakdown voltage of the PN junction is mainly affected by the concentration of the low-doping side. When the unstable electric field force generated by the dummy gate changes the local electron concentration of the DN-Well at the trigger surface, it directly causes a significant change in the trigger voltage of the DDSCR. The schematic diagram of the double-dummy-gate structure is shown in Fig. 3.

B. Gate-Controlled Structure

DDSCR_3 uses a gate-controlled structure. The device has a polysilicon gate that is shorted to the anode and cathode, and an isolation layer is used to block the channel ESD path under the gate of the device to improve the stability of the device. When the ESD is coming, the polysilicon gate of the device anode generates a vertical downward electric field force and the polysilicon gate of the device cathode generates a vertical upward electric field force, promoting carrier movement in the P-Well of the anode and cathode for the purpose of reducing the on-resistance. The PNPN path formed by the DDSCR is composed of P+, DN-Well, P-Well, and N+. When the device is turned on, the electric field force always remains in the same direction as the SCR current discharge path. Therefore, the formation of the SCR path can be promoted, and the voltage clamping capability of the device can be improved. The schematic diagram of the gate-controlled structure is shown in Fig. 4.

C. Double-Dummy-Gate and Gate-Controlled Structures

DDSCR_4 combines double-dummy-gate and gate-controlled structures. While combining the advantages of both types of structures, it also brings instability to the device. The unstable electric field effect generated by the double-dummy-gate structure and the electric field effect of the gate-controlled structure both affect the formation of the SCR path. Although the two structures will further reduce the ON-resistance of the DDSCR, the steady state of the SCR path is broken due to the influence of multiple electric fields. This causes a significant change in the ESD characteristics of the device. The design experience gained from the traditional DDSCR structure is not in line with DDSCR_4. A schematic diagram of the structure of this structure is shown in Fig. 5.

III. Two-Dimensional (2-D) Simulation and Discussion

The 2-D device simulation platform used in this article is Atlas, which can provide device-level dc simulation, ac simulation, and 2-D simulation. 2-D simulation of four types of devices using the technology computer-aided design (TCAD) software is applied to verify device principles and to improve device success. The concentration of P+ and N+ in DDSCR devices is the highest, and the concentration of P-Well is about three orders of magnitude lower. The concentration of DN-Well is about one order of magnitude lower than that of P-Well, and the concentration of P-Sub is the lowest. Fig. 6(a) and (b) shows the initial electric field distribution and impact ionization of

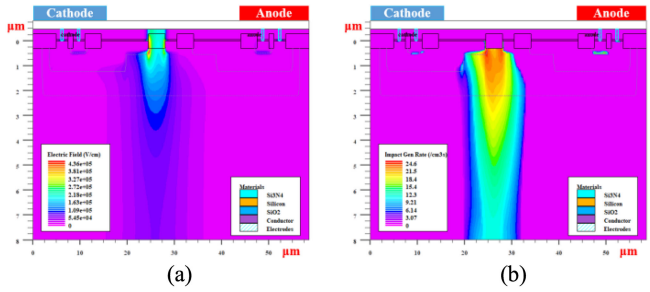

Fig. 6. (a) Electric field distribution of DDSCR_1. (b) Impact ionization of DDSCR_1.

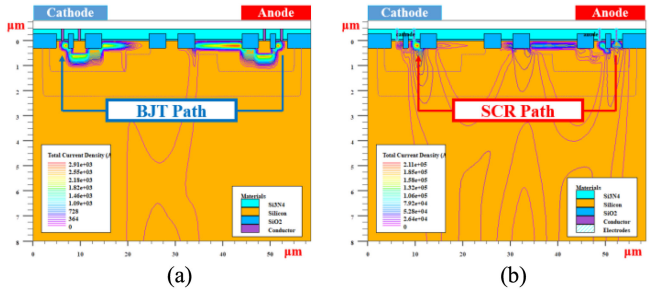

Fig. 7. (a) BJT path when DDSCR_1 is slightly turned on. (b) SCR path when DDSCR_1 is fully turned on.

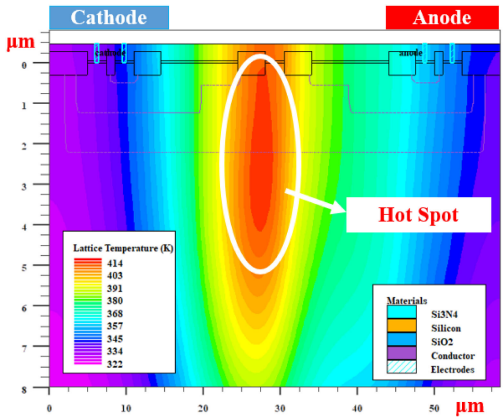

Fig. 8. Lattice temperature when DDSCR_1 is fully turned on.

DDSCR_1, respectively. The results show that there is a high-intensity electric field between the P+ and DN-Well reverse-bias PN junctions when the device is triggered and an avalanche breakdown effect occurs. Fig. 7(a) and (b) shows the current paths of the device at different time periods, and the conclusion can be clearly drawn. The DDSCR device is initially turned on as the BJT path (anode P+/DN-Well/cathode P+), at which point the SCR path is not fully formed. As the device is fully turned ON, the low-resistance PNPN path (anode P+/DN-Well/cathode P-Well/cathode N+) is gradually formed and the DDSCR is fully turned ON. Fig. 8 shows the lattice temperature distribution after the DDSCR is fully turned on. The peak temperature of the device is located inside the device, which effectively reduces the probability of thermal breakdown on the device surface and improves the stability of the device.

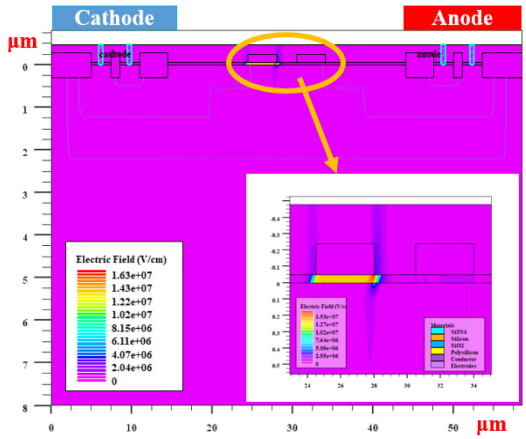

Fig. 9. Electric field distribution of DDSCR_2.

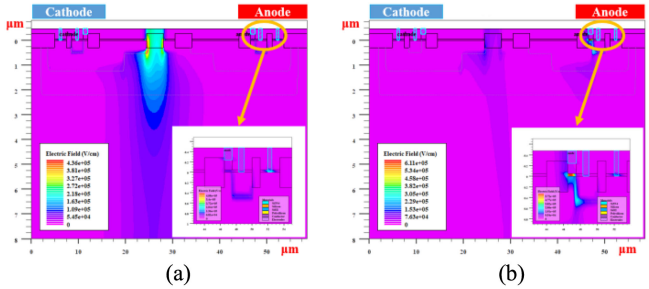

Fig. 10. (a) Electric field distribution when DDSCR_3 is slightly turned on. (b) Electric field distribution when DDSCR_3 is fully turned on.

Fig. 9 shows the electric field distribution after the opening of DDSCR_2. From the simulation results, it can be seen that there is a strong electric field force below the dummy gate near the cathode trigger surface of the device. This unstable electric field effect significantly changes the local carrier concentration of the DN-Well, causing a significant drift in the avalanche breakdown voltage of the device upon triggering. Moreover, there is also a small electric field effect below the dummy gate near the anode. The double-dummy-gate structure can share the electric field intensity generated by the electric field gathering effect, preventing the device from immediate failure after triggering. Therefore, the design of the double dummy gate structure ensures that the dummy gate structure is not directly destroyed by the strong electric field force and maintains the stability of the SCR path. Fig. 10(a) and (b) shows the electric field distribution results of DDSCR_3 in different time periods. With the gradual opening of the SCR, the electric field force generated by shorting the anode and cathode polysilicon gate is increasing, and the promotion of the SCR path is becoming more and more obvious. Moreover, one side of the polysilicon is an isolation layer, and the other side is a heavily doped region. It is impossible to form a MOS structure, which effectively avoids the source–drain breakdown problem caused by the voltage difference.

IV. Experimental Results and Discussion

The four types of two-finger DDSCR structures designed in this article are all implemented in a standard 0.5-μm CMOS

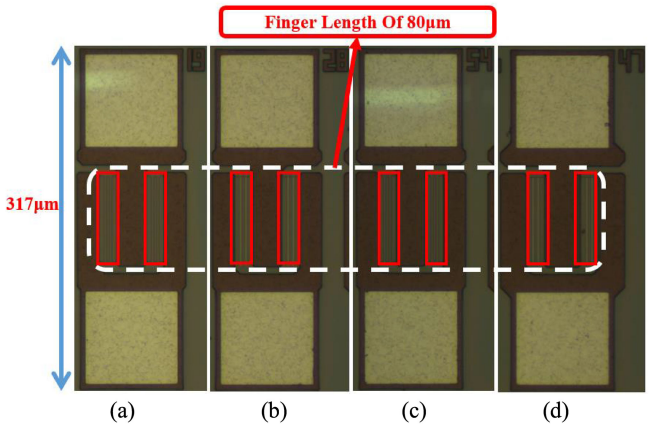

Fig. 11. (a) Microscope image of the DDSCR_1 structure. (b) Microscope image of the DDSCR_2 structure. (c) Microscope image of the DDSCR_3 structure. (d) Microscope image of the DDSCR_4 structure.

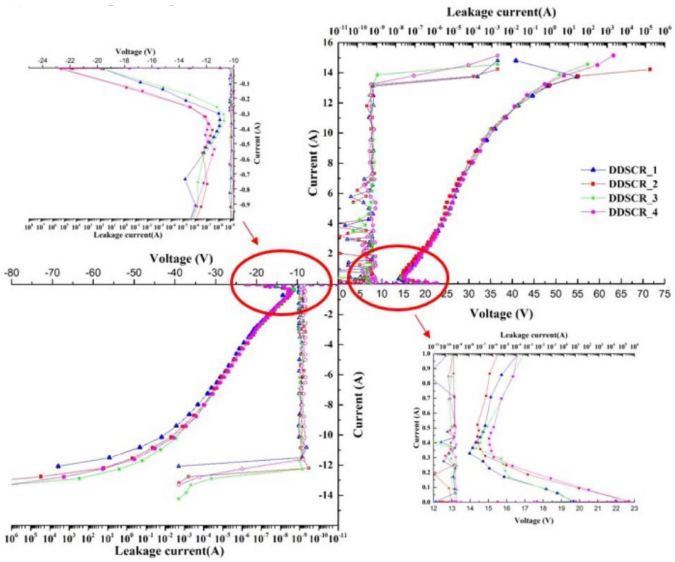

Fig. 12. TLP *I–V* curves of two-finger DDSCR_1 devices, two-finger DDSCR_2 devices, two-finger DDSCR_3 devices, and two-finger DDSCR_4 devices.

process. The finger length of the device is 80 μm. The transmission line pulse test system is used to detect the characteristics of the device under ESD strike and verify whether the trigger voltage, holding voltage, and failure current of the device meet the requirements of industrial-grade ESD protection.

A microscopic image of four types of DDSCR devices of the same size is shown in Fig. 11. Fig. 12 shows the forward and reverse transmission line pulse (TLP) test curves of the four types of device structures. Since the DDSCR structures have the same current path, the forward and reverse TLP curves have better symmetry. At the same size, DDSCR_1 has a trigger voltage of 19.58 V, a holding voltage of 13.97 V, and a failure current of 13.11 A. The trigger voltage of DDSCR_2 is 22.66 V, the holding voltage is 14.4 V, and the failure current is 13.18 A. Comparing the trigger voltages of DDSCR_2 with DDSCR_1, it can be found that the value of the trigger voltage produces a drift of 3 V due to the electric field concentration effect caused by the dummy gate. The reason why the dummy gate causes a change in the trigger voltage is verified. The trigger voltage of DDSCR_3 is 19.58 V, the holding voltage is 14.32 V, and the failure current is 13.87 A. The trigger voltage of DDSCR_4 is 22.67 V, the holding voltage is 15.04 V, and the failure current is 13.80 A. Using the linear fitting calculation method to estimate the ON-resistance of the four types of devices, only the data from the device maintenance point to the failure point are reserved for the calculation. The ON-resistances of the four types of devices are 0.437, 0.429, 0.427, and 0.426, respectively. The ON-resistance of a DDSCR device with a double-dummy-gate structure and a gate-controlled structure is slightly lower than that of DDSCR_1. However, the holding voltage of the four types of DDSCR structures of this size cannot meet the requirements of industrial-grade ESD protection. When the holding voltage is lower than the operating voltage of the core chip, the device is prone to latch-up and cannot be turned off normally until the chip is burned, which greatly reduces the robustness of the chip. In order to design an ESD device that meets the target ESD window, the device dimensions (D1, D2, D4, and D5/D6) will be changed in order to find an optimized size structure for industrial-grade ESD protection.

A. *Discuss the Effect of the Size of D1 on DDSCR Devices*

The D1 size of the four types of DDSCR devices is the region where the parasitic BJT emitter junction is located. Therefore, increasing the size of D1 will increase the BJT emission efficiency, and the failure capability of the four types of device structures can be significantly improved. The TLP test curves for different D1 sizes of the device are shown in Fig. 13(a)–(d). When the size of D1 is increased from 2.5 to 4.5 μm, the failure current of DDSCR_1 increases from 13.11 to 18.68 A, the failure current of DDSCR_2 increases from 13.18 to 18.59 A, and the failure current of DDSCR_3 increases from 13.87 to 18.58 A. The change of the failure current of DDSCR_4 does not conform to the change rule of the first three types of devices.

When D1 = 3.5 μm, the failure current reaches the highest (15.49 A). When D1 = 4.5 μm, the failure current decreases. Since the double-dummy-gate structure and the gate-controlled structure both have an electric field effect, the two structures interact with each other.

Although the device has the minimum ON-resistance, the conduction path of the DDSCR is difficult to maintain, and the influence of the dimensional change of the device on the ESD characteristic is weakened. The device's failure capability is significantly lower than the other three types of structures. The test data of the change in D1 size of the four types of devices are shown in Table I.

B. *Discuss the Effect of the Size of D2 on DDSCR Devices*

The TLP test curves for the different D2 sizes of the four types of DDSCR devices are shown in Fig. 14(a)–(d) respectively. Dimension D2 is the area where the device trigger surface P+ is located. According to the simulation diagram, the floating P+ is the main conduction path of the device and the ESD

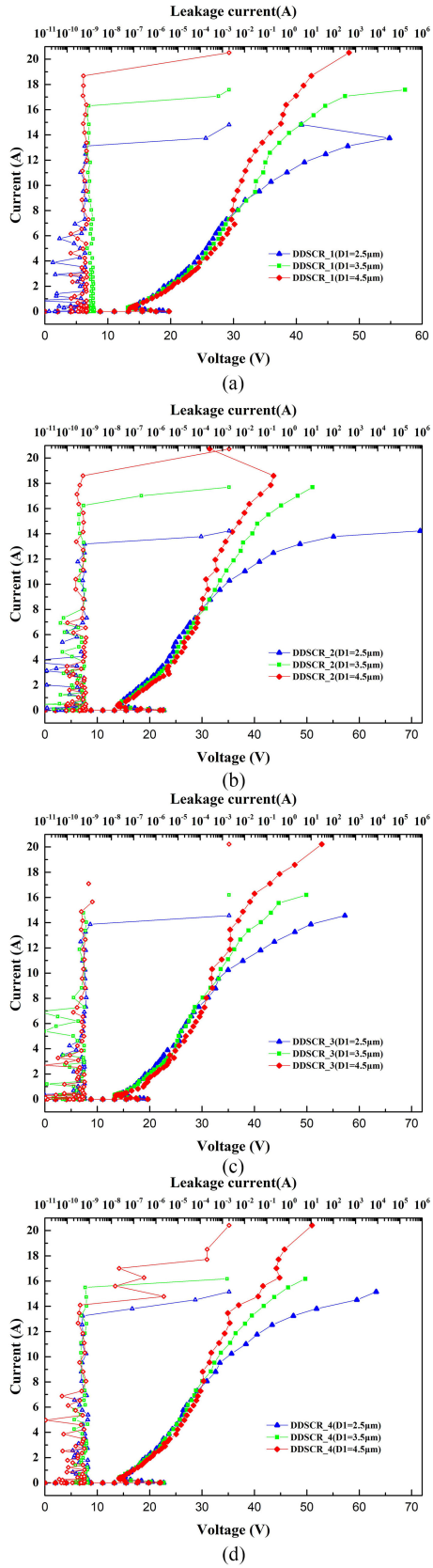

Fig. 13. (a) TLP *I–V* curves of two-finger DDSCR_1 devices (D1 = 2.5, 3.5, and 4.5 μm). (b) TLP *I–V* curves of two-finger DDSCR_2 devices (D1 = 2.5, 3.5, and 4.5 μm). (c) TLP *I–V* curves of two-finger DDSCR_3 devices (D1 = 2.5, 3.5, and 4.5 μm). (d) TLP *I–V* curves of two-finger DDSCR_4 devices (D1 = 2.5, 3.5, and 4.5 μm).

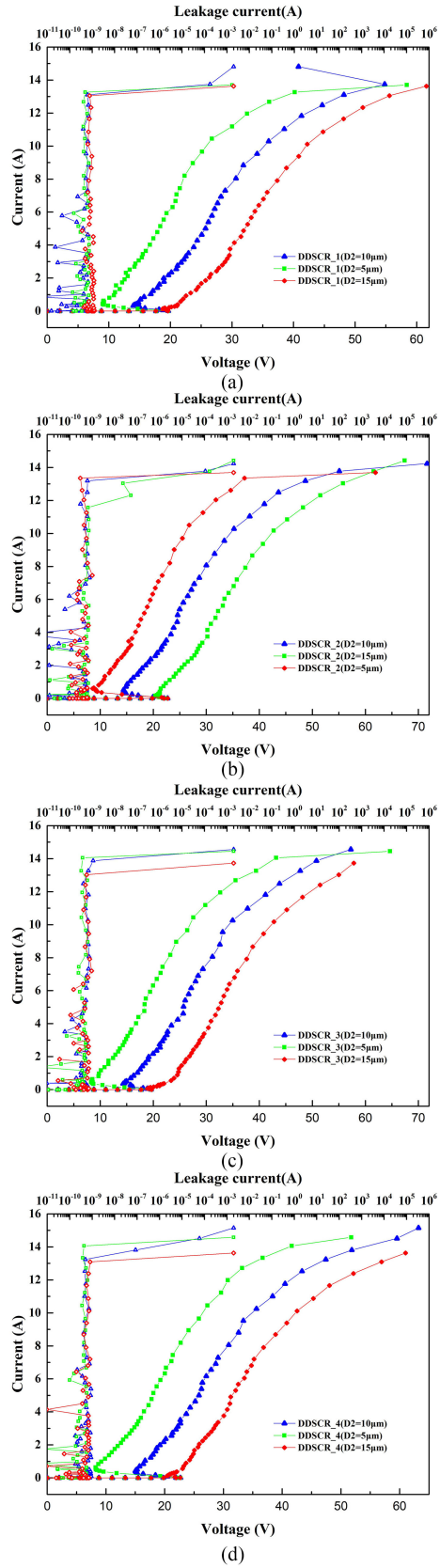

Fig. 14. (a) TLP *I–V* curves of two-finger DDSCR_1 devices (D2 = 5.0, 10, and 15 μm). (b) TLP *I–V* curves of two-finger DDSCR_2 devices (D2 = 5.0, 10, and 15 μm). (c) TLP *I–V* curves of two-finger DDSCR_3 devices (D2 = 5.0, 10, and 15 μm). (d) TLP *I–V* curves of two-finger DDSCR_4 devices (D2 = 5.0, 10, and 15 μm).

TABLE I
TEST RESULTS FOR THE D1 SIZE CHANGES FOR FOUR TYPES OF DEVICES

Device name	V_{t1}(V)	V_h(V)	I_{t2}(A)	HBM
DDSCR_1 (D1=2.5μm)	19.65	13.97	13.11	19.66
DDSCR_1 (D1=3.5μm)	19.69	13.20	16.30	24.45
DDSCR_1 (D1=4.5μm)	19.75	13.57	18.68	28.02
DDSCR_2 (D1=2.5μm)	22.71	14.40	13.18	19.77
DDSCR_2 (D1=3.5μm)	22.75	14.04	17.01	25.51
DDSCR_2 (D1=4.5μm)	22.50	13.92	18.59	27.88
DDSCR_3 (D1=2.5μm)	19.58	14.32	13.87	20.80
DDSCR_3 (D1=3.5μm)	19.67	13.30	15.55	23.32
DDSCR_3 (D1=4.5μm)	19.65	13.51	18.58	27.87
DDSCR_4 (D1=2.5μm)	22.67	15.04	13.80	20.70
DDSCR_4 (D1=3.5μm)	22.69	14.21	15.49	23.23
DDSCR_4 (D1=4.5μm)	22.11	14.17	14.09	21.13

TABLE II
TEST RESULTS FOR THE D2 SIZE CHANGES FOR FOUR TYPES OF DEVICES

Device name	V_{t1}(V)	V_h(V)	I_{t2}(A)	HBM
DDSCR_1 (D2=5.0μm)	19.66	8.99	13.26	19.89
DDSCR_1 (D2=10.0μm)	19.65	13.97	13.11	19.66
DDSCR_1 (D2=15.0μm)	19.61	18.74	13.05	19.57
DDSCR_2 (D2=5.0μm)	22.72	8.57	13.35	20.02
DDSCR_2 (D2=10.0μm)	22.71	14.40	13.18	19.77
DDSCR_2 (D2=15.0μm)	22.48	20.35	13.04	19.56
DDSCR_3 (D2=5.0μm)	19.63	8.27	14.04	21.06
DDSCR_3 (D2=10.0μm)	19.58	14.32	13.87	20.80
DDSCR_3 (D2=15.0μm)	19.65	18.93	13.02	19.53
DDSCR_4 (D2=5.0μm)	22.66	8.22	14.06	21.09
DDSCR_4 (D2=10.0μm)	22.67	15.04	13.80	20.70
DDSCR_4 (D2=15.0μm)	22.66	20.57	13.09	19.63

current stress flows from the anode of the device through the floating P+ to the cathode of the device. Therefore, increasing the length of the floating P+ can effectively lengthen the current conduction path of the device, so that the holding voltage of the device is significantly improved. When the D2 size is increased from 5 to 15 μm, the holding voltage of DDSCR_1 is changed from 8.99 to 18.74 V, the holding voltage of the DDSCR_2 is changed from 8.57 to 20.35 V, the holding voltage of DDSCR_3 is changed from 8.27 to 18.93 V, and the holding voltage of DDSCR_4 from 8.22 to 20.57 V. It can be seen that the holding voltage variations of the four types of device structures satisfy the theoretical derivation. However, the increase in the size of D2 will also cause the floating P+ to carry more carriers, which increases the probability of thermal breakdown on the surface of the device, and the failure capability is gradually reduced. When D2 = 15 μm, four types of devices have already met the industrial-grade ESD protection window. The test data of the D2 size change of the four types of devices are shown in Table II.

C. Discuss the Effect of the Size of D4 on DDSCR Devices

In DDSCR_1 and DDSCR_2, the D4 size is the isolation layer region (3.5 μm). The isolation layer is not located in the main release path of the device. The size of D4 is increased, which can effectively increase the holding voltage of the device, and the failure current of the device does not decrease significantly. In DDSCR_3 and DDSCR_4, the D4 size is a polysilicon gate region (1.0 μm), and the D5 size in both structures is set to 2.5 μm. Increasing the size of the polysilicon gate makes the range of the electric field effect larger. Therefore, compared with the DDSCR without the gate-controlled structure, the failure current is slightly higher than that of the first two types of DDSCR structures under the premise of ensuring the increase of the holding voltage. The TLP test curves for the four types of DDSCR structures at different D4 sizes are shown in Fig. 15(a)–(d). When D4 is increased from 3.5 to 7.0 μm, the holding voltage of DDSCR_1 increases from 13.97 to 18.18 V and the holding voltage of DDSCR_2 increases from 14.4 to 19.42 V. The failure currents of the two types of structures remain stable.

TABLE III
TEST RESULTS FOR THE D4 SIZE CHANGES FOR FOUR TYPES OF DEVICES

Device name	V_{t1}(V)	V_h(V)	I_{t2}(A)	HBM
DDSCR_1 (D4=3.5μm)	19.65	13.97	13.11	19.66
DDSCR_1 (D4=5.0μm)	19.77	15.82	13.82	20.73
DDSCR_1 (D4=7.0μm)	19.76	18.18	13.75	20.62
DDSCR_2 (D4=3.5μm)	22.71	14.40	13.18	19.77
DDSCR_2 (D4=5.0μm)	22.70	17.43	13.84	20.76
DDSCR_2 (D4=7.0μm)	22.73	19.42	13.81	20.71
DDSCR_3 (D4=1.0μm,D5=2.5μm)	19.58	14.32	13.87	20.80
DDSCR_3 (D4=2.5μm,D5=2.5μm)	19.70	16.64	13.87	20.80
DDSCR_3 (D4=4.5μm,D5=2.5μm)	20.51	19.46	13.87	20.80
DDSCR_4 (D4=1.0μm,D5=2.5μm)	22.67	15.04	13.80	20.70
DDSCR_4 (D4=2.5μm,D5=2.5μm)	22.70	17.33	13.87	20.80
DDSCR_4 (D4=4.5μm,D5=2.5μm)	23.39	20.44	14.51	21.76

When the size of the polysilicon gate is increased from 1.0 to 4.5 μm, the holding voltage of DDSCR_3 is increased from 14.32 to 19.46 V, and the failure current is maintained at 13.9 A. The holding voltage of DDSCR_4 is increased from 15.04 to 20.44 V, and the failure current is increased from 13.8 to 14.5 A. The test data of the D4 size change of the four types of devices are shown in Table III. It can be clearly seen from the test data that the D4 size change can obtain a higher holding voltage and the failure current is not significantly reduced compared to the D2 size change. The protection capability is stronger when applied to an industrial-grade ESD window.

D. Discuss the Effect of the Size of D6 on DDSCR_4

Since DDSCR_4 has a double-dummy-gate structure and a gate-controlled structure, attempts have been made to vary the size of the double-dummy-gate structure to obtain different characteristics of the device. The TLP test curves of two different D6 sizes of DDSCR_4 are shown in Fig. 16. It can be seen that as the size of the double-dummy-gate structure increases from 2.5 to 3.5 μm, the holding voltage of the device increases from 15.04 to 16.0 V, and the failure current remains steady. However, it can be clearly seen that when D6 = 3.5 μm, the voltage clamping speed of the device is significantly improved, which verifies that the double-dummy-gate structure can provide more ESD release paths. The SCR path is formed faster and the voltage clamping capability of the device is effectively improved.

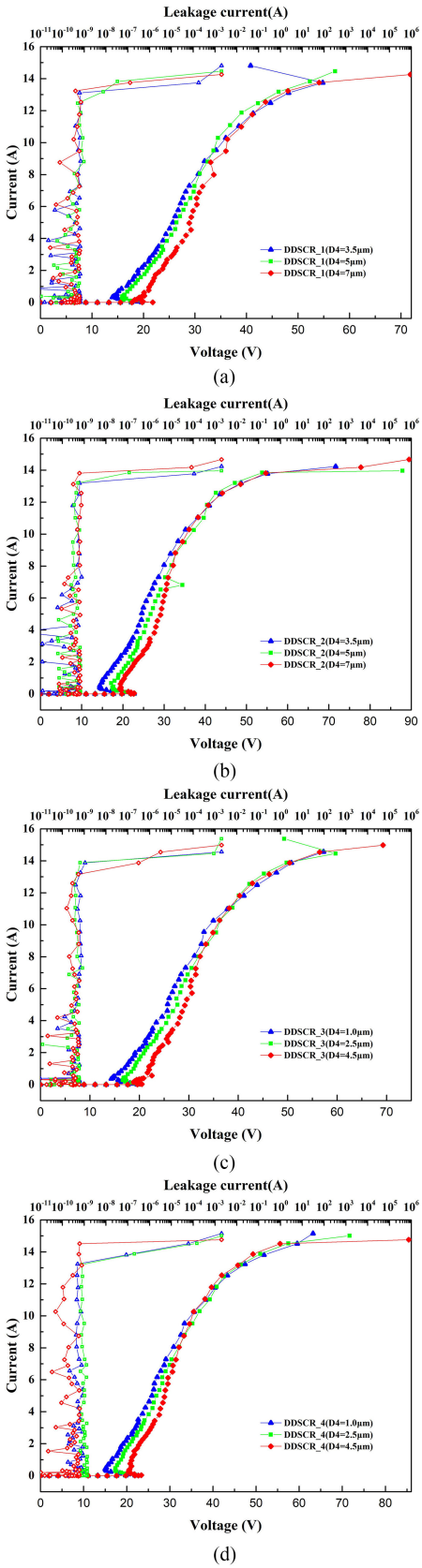

Fig. 15. (a) TLP *I–V* curves of two-finger DDSCR_1 devices (D4 = 3.5, 5.0, and 7.0 μm). (b) TLP *I–V* curves of two-finger DDSCR_2 devices (D4 = 3.5, 5.0, and 7.0 μm). (c) TLP *I–V* curves of two-finger DDSCR_3 devices (D4 = 1.0, 2.5, and 4.5 μm). (d) TLP *I–V* curves of two-finger DDSCR_4 devices. (D4 = 1.0, 2.5, and 4.5 μm).

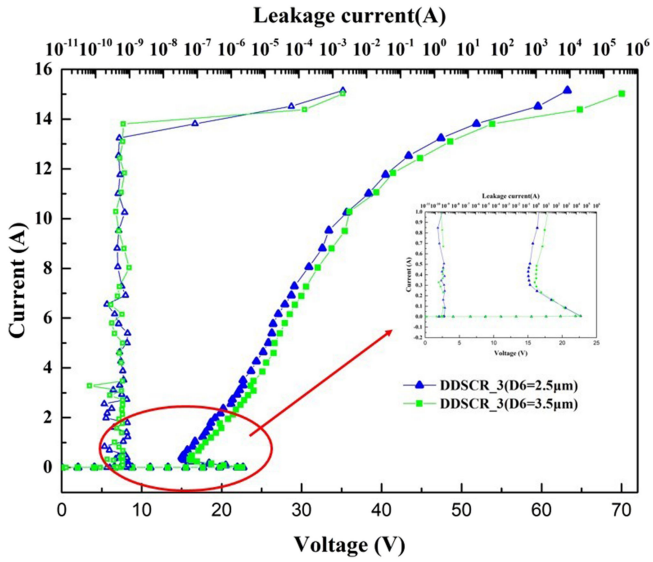

Fig. 16. TLP *I–V* curves of two-finger DDSCR_4 devices (D6 = 2.5, 3.5 μm).

In summary, the above four types of DDSCR structures are dimensionally changed to obtain device ESD characteristics at different sizes. The results show that changing the D1 size can effectively improve the failure current of the device, but changing the failure current of DDSCR_4 due to the various electric field effect does not meet the theoretical design results. The change in the size of D2 can greatly increase the holding voltage of the device and prevent the latch-up effect, but the failure current is significantly reduced. When D2 = 15 μm, the ESD specifications of the four types of devices meet the window requirements of industrial-grade ESD protection. The change of the D4 size can effectively ensure the stability of the failure current under the premise of increasing the holding voltage of the device, and the failure current of DDSCR_4 is obviously improved when D4 = 4.5 μm. Compared to the D2 size change, the D4 size is more helpful in optimizing the ESD characteristics of the device to meet the requirements of industrial-grade ESD protection. Finally, the influence of the double-dummy-gate structure in DDSCR_4 on the voltage clamping capability of the device is discussed. As the size of the double dummy gate increases, the ESD current path of the device increases, and the low-resistance PNPN path of DDSCR_4 is formed faster.

V. Conclusion

In this article, four types of DDSCR devices were fabricated in a 0.5-μm standard CMOS process. The ESD design window for this type of device was suitable for ESD protection of industrial bus interfaces. The TCAD simulation software was used to verify the working principle of the device, and the ESD characteristics of the device were measured based on the transmission line pulse test system. The test results showed that the double-dummy-gate structure can promote the voltage clamping capability of the ESD device. The gate-controlled structure can adjust the movement of the carrier and promote the current discharge of the SCR path. The DDSCR devices of

different sizes were discussed and analyzed. The HBM levels of the four types of devices were located at 16–28 kV, and the device structure that met the appropriate size of the target window was obtained. In summary, these four types of DDSCR devices provided a reference solution for high-voltage industrial-grade ESD protection.

ACKNOWLEDGMENT

The authors would like to thank Y. Ju from the Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong, B. Jiang, W. Xue, J. Tang, X. Zhang, J. Yang, F. Yan, and J. Xu from Hunan Normal University, Changsha, China, for their strong support and kind discussion on this article.

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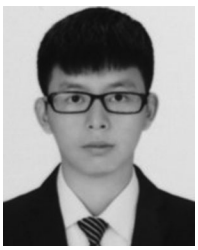

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