Design and Implementation of Half-Bridge Resonant Converter With Novel Primary-Side Control

Tsorng-Juu Liang, *Fellow, IEEE*, Chi-Hung Lin, Wei-Jing Tseng, and Yu-Meng Lin

***Abstract*—The opto-coupler is usually used for isolated resonant converter to feedback the secondary-side output information. However, the characteristics of the opto-coupler are easily affected by the operating conditions, which will cause higher standby power loss. In this article, a novel primary-side controlled isolated half-bridge resonant converter with output voltage and current estimation for LLC and series resonant converter (SRC) operations is presented. The output voltage is estimated by sampling the auxiliary winding voltage when the output diode current flows to zero, the output current is estimated by integrating the resonant current until the transformer decoupled. The operating principles of the half-bridge resonant converter and the design criteria of the key component parameters are addressed and analyzed. Also, the methods for estimating output voltage and output current are discussed in detail. Finally, an experimental prototype with rated power 100 W half-bridge resonant converter for input voltage 280–342 V and output voltage 24 V is built with microcontroller to validate the proposed primary-side regulation technique. Experimental results show the output voltage and current can be controlled with the error less than 1% and 8%, respectively. The highest efficiency of the system is 95.2%.**

***Index Terms*—Half bridge resonant converter, output voltage estimation, and output current estimation, primary side control.**

I. Introduction

THE primary-side regulation (PSR) technology has been widely applied to the flyback converter. To regulate the output voltage, the voltage across the auxiliary winding is sensed at zero current or fixed time point. Techniques used for output voltage estimation of the PSR flyback revealed in the lectures are knee point detector, adaptive blanking time, and zero slope detector [1]–[3]. To regulate the output current, the peak current flows through the main power switch and the conduction time of the output rectifier diode are detected. The propagation delay and input voltage compensation have been presented to estimate the output current [4]–[13]. However, there are seldom lectures of PSR half-bridge resonant converter are proposed [14], [15]. The approach proposed in [14] is only for the output voltage regulation, which obtains the voltage across the primary-side winding of the transformer when the voltage across the resonant inductor becomes zero. Then, the voltage across the secondary-side leakage inductor can be eliminated. Another PSR scheme for controlling the output voltage and current is integrated in control integrated circuit (IC) [15]. Inside the IC, there are two separated control loops to control the output voltage and current.

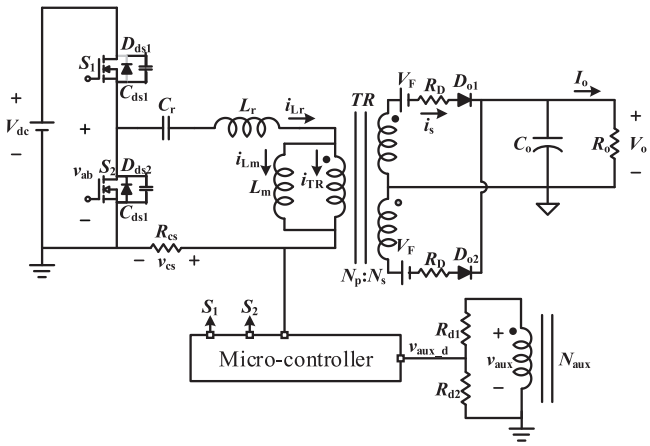

Fig. 1. Proposed primary-side controlled LLC converter with the equivalent circuit of output diode.

II. Analyses of Proposed PSR Control Scheme

For output voltage regulation, the output voltage can be estimated by the voltage across the auxiliary winding. Fig. 1 shows the proposed primary-side controlled LLC converter with the output diode modeled as an ideal diode with forward voltage V_F and a series resistance R_D. Therefore, the auxiliary winding voltage $v_{\rm aux}$ can be obtained as follows:

$$v_{\rm aux}(t) = \frac{N_{\rm aux}}{N_s}\left[V_o + V_F + i_s(t)\cdot R_D\right] \tag{1}$$

where the secondary-side current $i_s(t)$ is proportional to the primary-side current $i_p(t)$. From (1), the output voltage can be derived as follows:

$$V_o = v_{\rm aux}(t)\cdot\frac{N_s}{N_{\rm aux}} - V_F - i_s(t)\cdot R_D. \tag{2}$$

However, the current $i_s(t)$ is varied with time, which is needed to consider for output voltage calculation. Once the voltage $v_{\rm aux}$

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is sampled when the current $i_s(t)$ is equal to zero, the output voltage can be estimated without considering the current $i_s(t)$. The output voltage can be expressed as follows:

$$V_o = v_{\text{aux}}(t) \cdot \frac{N_s}{N_{\text{aux}}} - V_F. \tag{3}$$

For output current regulation, the current difference between i_{Lr} and i_{Lm} is transferred to the secondary-side of the transformer. The secondary-side current $i_s(t)$ is described as follows:

$$i_s(t) = n \cdot [i_{L_r}(t) - i_{L_m}(t)] \tag{4}$$

where n is the turn ratio between N_p and N_s. Since the output current I_o is equal to the average value of the current $i_s(t)$, the current I_o is expressed as follows:

$$I_o = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_s(t)\cdot dt = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} n\cdot[i_{L_r}(t) - i_{L_m}(t)]\cdot dt. \tag{5}$$

On the basis of (5), the current I_o of the converter operating above the first resonant frequency f_{r1} can be calculated as (6). Where ω_r is the resonant angular frequency, and φ is the phase angle between the resonant tank voltage v_{ab} and the resonant current i_{Lr}. However, transformer decoupled makes the calculation of the current I_o more complex when the converter operating below the frequency f_{r1}, which can be derived as (7). Where t_{de} is the transformer decoupled time, and t_r is the resonant period. As a result, the output current estimation based on (6) and (7), phase angle φ, peak resonant current $I_{\text{Lr\_pk}}$, and the transformer-decoupled time t_{de} should be sensed and calculated. Nevertheless, the complicated algorithm may cause the micro-control unit (MCU) hard to execute the calculation.

$$\begin{aligned} I_o &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} n\cdot[i_{L_r}(t) - i_{L_m}(t)]\cdot dt \\ &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} n\cdot\left[I_{L_r\_pk}\cdot sin(\omega_r t-\varphi) - \frac{nV_o}{L_m}\cdot\left(t-\frac{T_s}{4}\right)\right]\cdot dt \\ &= \frac{n\cdot f_s\cdot I_{L_r\_pk}}{\pi\cdot f_{r1}}\cdot\left[cos\varphi - cos\left(\pi\frac{f_{r1}}{f_s}-\varphi\right)\right] \end{aligned} \tag{6}$$

$$\begin{aligned} I_o &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} n\cdot[i_{L_r}(t) - i_{L_m}(t)]\cdot dt \\ &= \frac{2}{T_s}\int_0^{t_{de}} n\cdot\left[I_{L_r\_pk}\cdot sin(\omega_r t-\varphi) - I_{L_m}(t_0) - \frac{n\cdot V_o}{L_m}\cdot t\right]\cdot dt \\ &= \frac{2n}{T_s}\left\{\frac{I_{L_r\_pk}}{\omega_r}\left[cos\varphi - cos\left(2\pi\cdot\frac{t_{de}}{t_r}-\varphi\right)\right]\right. \\ &\qquad \left. - I_{L_m}(t_0)\cdot t_{de} - \frac{n\cdot V_o}{L_m}\cdot\frac{1}{2}t_{de}^2\right\} \end{aligned} \tag{7}$$

A. Output Voltage Regulation

Fig. 2 shows the block diagram of the output voltage control. Based on the mentioned algorithm, the knee point detector is used to detect the output current i_{Do} reaches zero, which determines the sensing instant of $v_{\text{aux\_d}}$. However, the *RC* delay circuit of the knee point detector will cause the sensing error. In order to eliminate the sensing error, the voltage holding circuit is adopted to ensure the sensing accuracy by keeping $v_{\text{aux\_d}}$ on the capacitor of the holding circuit.

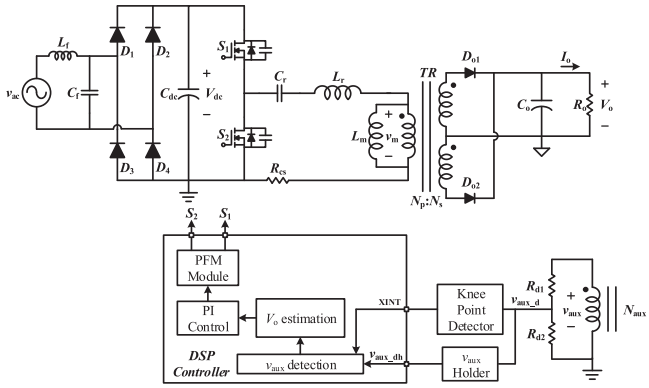

Fig. 2. Block diagram of output voltage control.

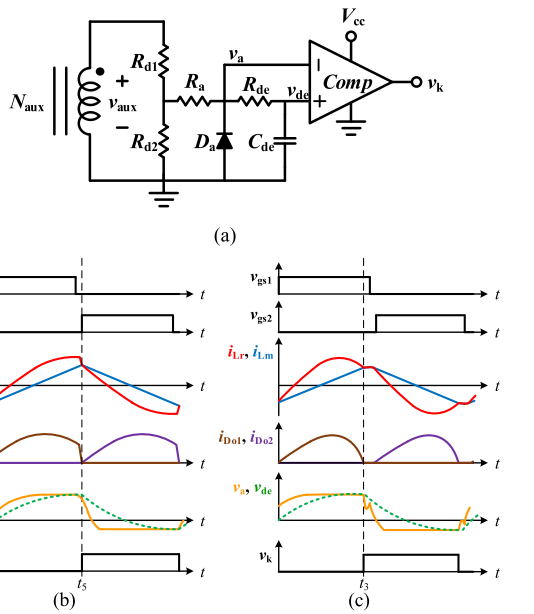

Fig. 3. Knee point detector. (a) Circuit, and waveforms in (b) SRC and (c) LLC region.

Fig. 3 shows the circuit and the key waveforms of the knee-point detector. Since the current difference between i_{Lr} and i_{Lm} is equal to zero, the output rectifier current i_{Do1} will reach zero and the voltage across the auxiliary winding v_{aux} will change rapidly. As shown, the comparator will become high when v_a is smaller than v_{de}, where v_{de} is obtained from v_a through the *RC* delay circuit. In the case of the voltage v_{aux} decreases rapidly, but v_{de} will not decrease promptly, and the output of the comparator v_k is pulled high. Hence, the zero-current timing can be detected. The voltage v_k is set as XINT for triggering the microcontroller to measure the voltage v_{aux}.

Fig. 4 shows the circuit and the key waveforms of the voltage holder. When the voltage v_k is pulled high, the microcontroller will measure the voltage $v_{\text{aux\_d}}$. However, the sensing error Δv_{aux} may lead to inaccurate output voltage regulation. As shown, the diode D_{vh} will be reverse biased when the voltage $v_{\text{aux\_d}}$ is lower than the voltage $v_{\text{aux\_dh}}$, then $v_{\text{aux\_dh}}$ will decrease

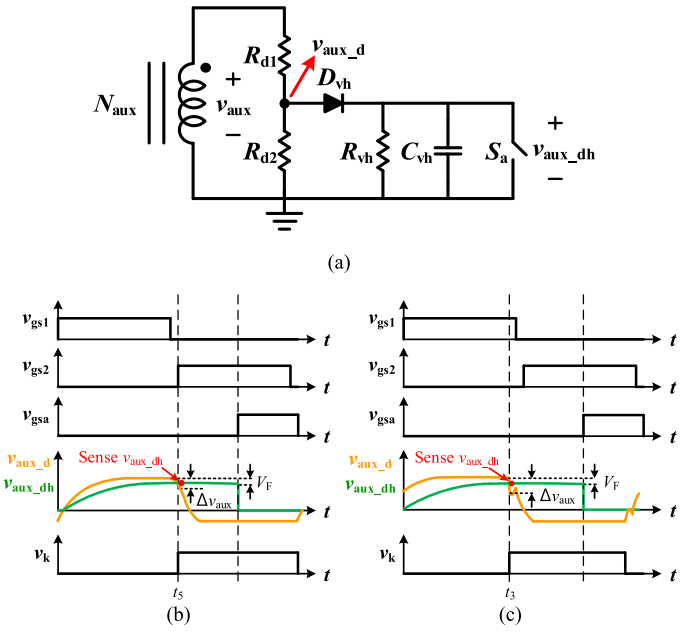

Fig. 4. Voltage holder. (a) Circuit, and waveforms in (b) SRC and (c) LLC region.

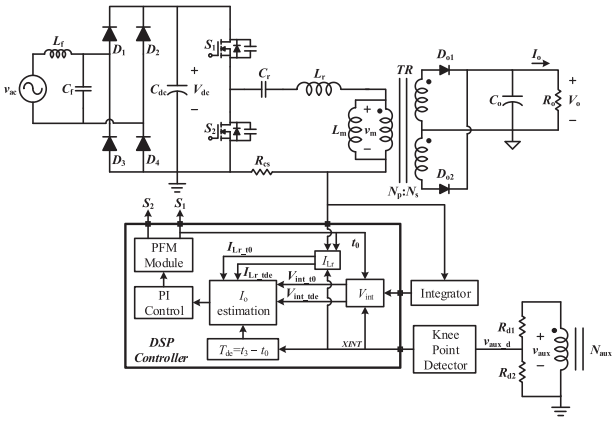

Fig. 5. Block diagram of output current control.

with a slow slope due to large resistance $R_{\rm vh}$. The gate signal $v_{\rm gsa}$ is used to reset the voltage $v_{\rm aux\_dh}$ before the switch S_1 is turned on. Therefore, the output voltage can be obtained as follows:

$$V_o = [v_{\rm aux\_dh}(t) + V_F] \cdot \frac{N_s}{N_{\rm aux}} - V_F. \tag{8}$$

B. Output Current Regulation

Fig. 5 shows the block diagram of the output current control. The integrator is adopted to calculate the energy transferred from the primary side for output current estimation. Fig. 6 shows the circuit and the key waveforms of the integrator, which is used to calculate the integral of the voltage across the current sensing resistor $R_{\rm cs}$. The output current I_o is equal to the average value of the secondary-side current i_s, which is determined by the current difference between $i_{\rm Lr}$ and $i_{\rm Lm}$. Based on the concept, the output current estimation can be expressed as follows. Since the positive and negative half-cycle is symmetrical, only positive half-cycle is calculated for output current estimation.

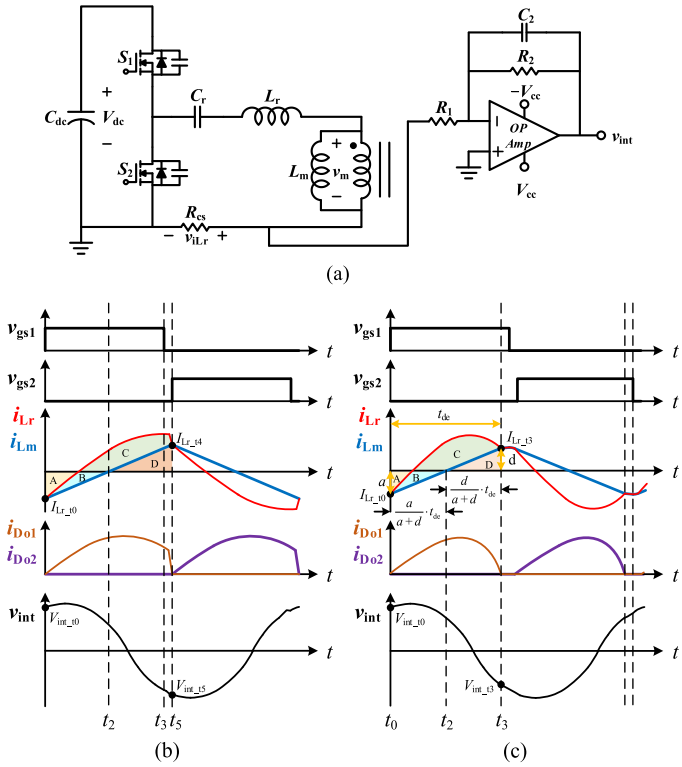

Fig. 6. Integrator. (a) Circuit, and waveforms in (b) SRC and (c) LLC region.

As shown in Fig. 6(b) that the converter is operated in series resonant converter (SRC) region. The output current I_o can be expressed as follows:

$$I_o = \frac{2}{T_s}\int_0^{t_5} [i_{\rm Lr}(t) - i_{\rm Lm}(t)] \cdot dt = \frac{2}{T_s} \cdot$$
$$Q_{\rm sec} = \frac{2}{T_s} \cdot [B + C]. \tag{9}$$

Because the magnetizing current $i_{\rm Lm}$ increases linearly with the same slope in half-switching cycle, the absolute value of $I_{{\rm Lr}\_t0}$ and $I_{{\rm Lr}\_t4}$ are the same. The equation can be expressed as follows:

$$\left|\int_0^{t_2} i_{\rm Lm}(t) \cdot dt\right| = A + B = \int_{t_2}^{t_5} i_{\rm Lm}(t) \cdot dt = D. \tag{10}$$

However, the result of the integrator can be expressed as follows:

$$\int_0^{t_5} i_{\rm Lr}(t) \cdot dt = Q_{\rm int} = -A + C + D. \tag{11}$$

By substituting (11) into (10), the output current I_o can be derived as follows:

$$I_o = \frac{2}{T_s} \cdot [B + C] = \frac{2}{T_s} \cdot [(-A + D) + C]$$
$$= \frac{2}{T_s}\int_0^{t_5} i_{\rm Lr}(t) \cdot dt = \frac{2}{T_s} \cdot Q_{\rm int} \tag{12}$$

where $Q_{\rm int}$ is obtained by the difference between $V_{{\rm int}\_t0}$ and $V_{{\rm int}\_t5}$.

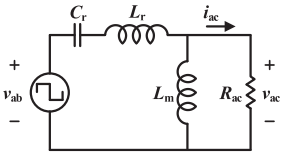

Fig. 7. Equivalent circuit of half-bridge LLC resonant converter.

As shown in Fig. 7(c) that the converter is operated in LLC region. The output current I_o can be expressed as follows:

$$I_o = \frac{2}{T_s}\int_0^{t_3} \left[i_{\rm Lr}(t) - i_{\rm Lm}(t)\right]\cdot dt = \frac{2}{T_s}\cdot Q_{\rm sec} = \frac{2}{T_s}\cdot [B+C]. \tag{13}$$

However, the result of the integrator can be expressed as follows:

$$\int_0^{t_3} i_{\rm Lr}(t)\cdot dt = Q_{\rm int} = -A + C + D. \tag{14}$$

Hence, the output current can be derived as follows:

$$I_o = \frac{2}{T_s}\cdot [B+C] = \frac{2}{T_s}\cdot [(-A+C+D)+(A+B-D)] = \frac{2}{T_s}\cdot [Q_{\rm int}+(A+B-D)]. \tag{15}$$

Furthermore, the area [A + B − D] can be calculated as follows:

$$A+B-D = \frac{1}{2}\cdot\frac{a}{a+d}\cdot t_{\rm de}\cdot a - \frac{1}{2}\cdot\frac{d}{a+d}\cdot t_{\rm de}\cdot d = \frac{1}{2}\cdot\frac{t_{\rm de}}{a+d}\cdot\left(a^2-d^2\right) = \frac{1}{2}\cdot t_{\rm de}\cdot(a-d). \tag{16}$$

where a and d are the absolute value of $I_{{\rm Lr}\_t0}$ and $I_{{\rm Lr}\_t3}$, respectively. As a result, the output current I_o can be expressed follows:

$$I_o = \frac{2}{T_s}\cdot\left[Q_{\rm int}+\frac{1}{2}\cdot t_{\rm de}\cdot(a-d)\right] = \frac{2}{T_s}\cdot\left[Q_{\rm int}+\frac{1}{2}\cdot t_{\rm de}\cdot|I_{{\rm Lr}\_t0}+I_{{\rm Lr}\_t3}|\right]. \tag{17}$$

III. Parameters Design

In order to verify the proposed control method, a prototype with output voltage and current control is realized by MCU. The digital signal processor (DSP) used for estimation is TMS320F28335 with the system clock speed of 150 MHz. The specifications of the proposed primary-side controlled half-bridge resonant converter is listed in Table I.

TABLE I
Specifications of Half-Bridge Resonant Converter

Parameters	Values
Input voltage ($V_{\rm in}$)	280 ~342 V
Output voltage ($V_{\rm o}$)	24 V
Maximum output current ($I_{\rm o}$)	4.17 A
Maximum output power ($P_{\rm o}$)	100 W
Operating frequency (f_s)	80 kHz ~ 130 kHz

A. Key Parameters Design

The sufficient dead time is necessary to avoid short circuit for the power switches S_1 and S_2, where the power switches are chosen as SSP7N60A. The output capacitance of the power switches $C_{\rm oss}$ is 130 pF that can be obtained from the datasheet. Assuming the dead time t_d is 200 ns and the highest operating frequency $f_{\rm s\_max}$ is 130 kHz that can be obtained from the specifications, thus, the limitation of the magnetizing inductance L_m is determined as follows:

$$L_m \le \frac{t_d\cdot T_{\rm s\_max}}{16C_{\rm oss}} = \frac{200\times10^{-9}\times\frac{1}{130\times10^3}}{16\times130\times10^{-12}} = 739.6\ \mu{\rm H}. \tag{18}$$

The maximum magnetizing inductance L_m should be designed smaller than 739.6 μH to ensure the ZVS under light load and highest input voltage condition. The maximum efficiency of the resonant converter can be obtained when the converter is operated at the first resonant frequency f_{r1} due to less circulating energy and soft-switching operation. As the normalized gain ($M_g = 1$) is set at the input voltage 310 V, the turn ratio of the transformer n can be calculated as follows:

$$n = \frac{N_p}{N_s} = \frac{V_{\rm in}}{2V_o} = \frac{310}{48} = 6.458. \tag{19}$$

By setting the turns-ratio n as 6.5, the requirement of the voltage-gain is from 0.912 to 1.114 according to the input voltage conditions, which makes the converter operate in both LLC region and SRC region. Fig. 7 shows the equivalent circuit of LLC resonant converter. Based on the Fourier analysis, the voltage $v_{\rm ac}$, current $i_{\rm ac}$ can be expressed as (20) and (21)

$$v_{\rm ac}(t) = \frac{4nV_o}{\pi}\sum_{i=1,3,5\ldots}^{\infty}\frac{1}{i}\cdot\sin(i2\pi f_s t-\varphi_v) \tag{20}$$

$$i_{\rm ac}(t) = \frac{\pi}{2}\cdot\frac{I_o}{n}\sum_{i=1,3,5\ldots}^{\infty}\frac{1}{i}\cdot\sin(i2\pi f_s t-\varphi_i). \tag{21}$$

If the Q_r is chosen as larger value, the higher order harmonics can be ignored that only fundamental component needs to be considered, and the equivalent resistor $R_{\rm ac}$ can be expressed as follows:

$$R_{\rm ac} = \frac{v_{\rm ac}}{i_{\rm ac}} = \frac{8}{\pi^2}n^2R_L. \tag{22}$$

According to Fig. 8, the voltage gain can be derived as follows:

$$M_g = \frac{v_{\rm ac}}{v_{\rm ab}} = \left|\frac{j\omega L_m//R_{\rm ac}}{j\omega L_r+\frac{1}{j\omega C_r}+j\omega L_m//R_{\rm ac}}\right| = \left|\frac{k\cdot f_n^2}{[(1+k)\cdot f_n^2-1]+j\cdot k\cdot Q_r\cdot f_n\cdot(f_n^2-1)}\right| \tag{23}$$

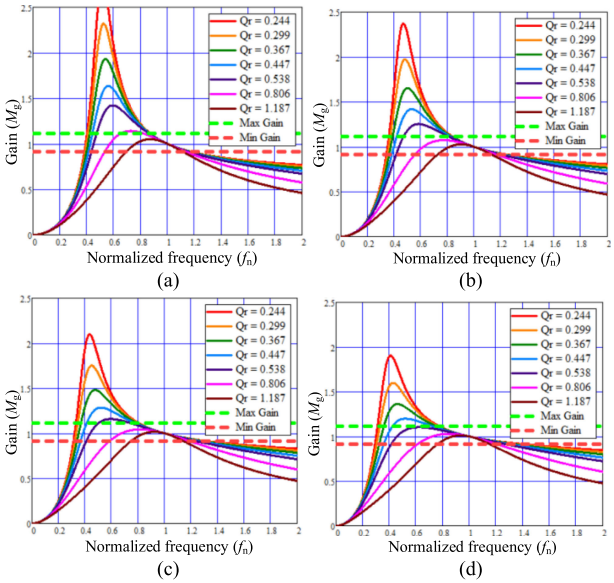

Fig. 8. Voltage-gain curves with different Q_r and k: (a) $k = 3$, (b) $k = 4$, (c) $k = 5$, and (d) $k = 6$.

TABLE II
KEY PARAMETERS OF CIRCUIT COMPONENTS

Parameters	Values
Magnetizing inductance (L_m)	680 μH/PQ3230
Turns ratio (N_p:N_s: N_{aux})	26 : 4 : 2
Resonant inductance (L_r)	170 μH/PQ2020
Resonant capacitance (C_r)	15 nF/630 V
Switches (S_1 and S_2)	SSP7N60A(600 V / 7 A / 1.2 Ω)
Output rectifier diode (D_{o1} and D_{o2})	MUR420
Output filter capacitance (C_o)	470 μF/50 V × 4 pcs

where $R_{\rm ac} = \frac{8}{\pi^2} \cdot n^2 R_L, Q_r = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{\rm ac}}, k = \frac{L_m}{L_r}, f_n = \frac{f}{f_{r1}}$, $f_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}, f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m) \cdot C_r}}$ Based on (23), the gain curves with different quality factor Q_r and the ratio between magnetizing inductance and leakage inductance k are shown in Fig. 8.

Considering the tradeoff between the resonant current and the operating frequency range, the values of Q_r and k are chosen as 0.538 and 4. Once the first resonant frequency f_{r1} is set to be 100 kHz, the value of the resonant components magnetizing inductance L_m, resonant inductance L_r, and resonant capacitors C_r can be calculated from (24) to (26), and the key parameters of the circuit components are listed in Table II.

$$C_r = \frac{1}{2\pi \cdot f_{r1} \cdot Q_r \cdot R_{\rm ac}} = \frac{1}{2\pi \times 100 \times 10^3 \times 0.538 \times 197.26} = 15 \text{ nF} \quad (24)$$

$$L_r = \frac{1}{4\pi^2 \cdot {f_{r1}}^2 \cdot C_r} = \frac{1}{4\pi^2 \times \left(100 \times 10^3\right)^2 \times 15 \times 10^{-9}} = 168.9\ \mu\text{H} \quad (25)$$

$$L_m = L_n \cdot L_r = 4 \times 168.9 \times 10^{-6} = 675.5\ \mu\text{H}. \quad (26)$$

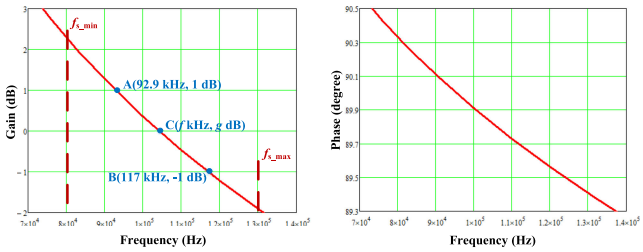

Fig. 9. Bode plot of integrator between 80 kHz and 130 kHz.

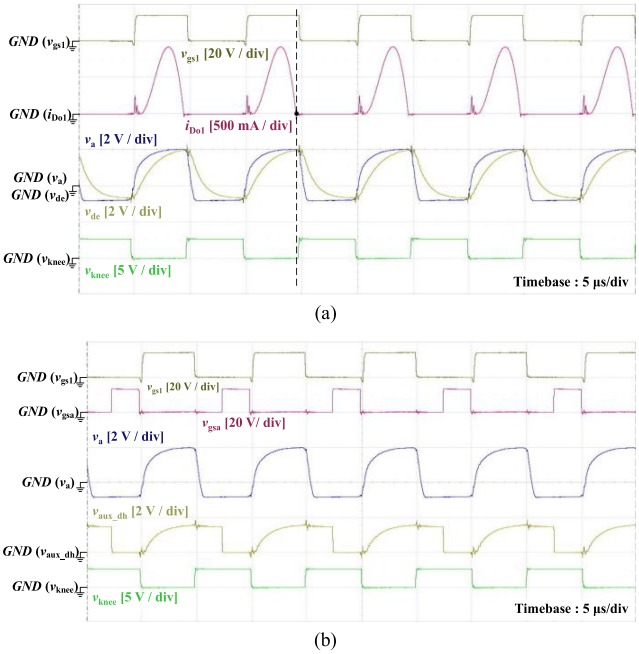

Fig. 10. Waveforms of (a) knee point detector and (b) voltage holder at $V_{\rm in}$ = 280 V and I_o = 0.417 A.

B. Integrator Design

Fig. 9 shows the bode plots of the integrator between 80 and 130 kHz in which the gain and phase are 0.38 dB and 89.91° at resonant frequency f_{r1} (100 kHz). Then, the linear formula of the gain curve in the range of $f_{\rm s\_min}$ and $f_{\rm s\_max}$ can be derived from

$$g(f_S) = 2 - 0.0095 f_S. \quad (27)$$

By setting the zero error reference point in 60% load condition with input voltage of 342 V, the error can be minimized under overall load conditions.

IV. EXPERIMENTAL RESULTS

A. Output Voltage Regulation

Figs. 10 and 11 show the waveforms of the knee point detector and the voltage holder at input voltage 280 V under 10% load and full load conditions, respectively. The $v_{\rm knee}$ is pulled high for sensing the voltage $v_{\rm aux}$ when the current $i_{\rm Do1}$ is equal to zero. However, the delay time caused by the *RC* delay circuit

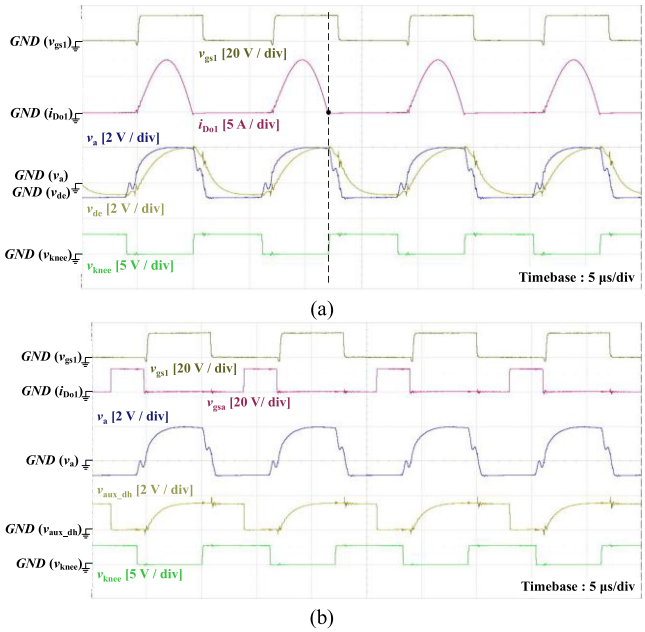

Fig. 11. Waveforms of (a) knee point detector and (b) voltage holder at $V_{\rm in}$ = 280 V and I_o = 4.17 A.

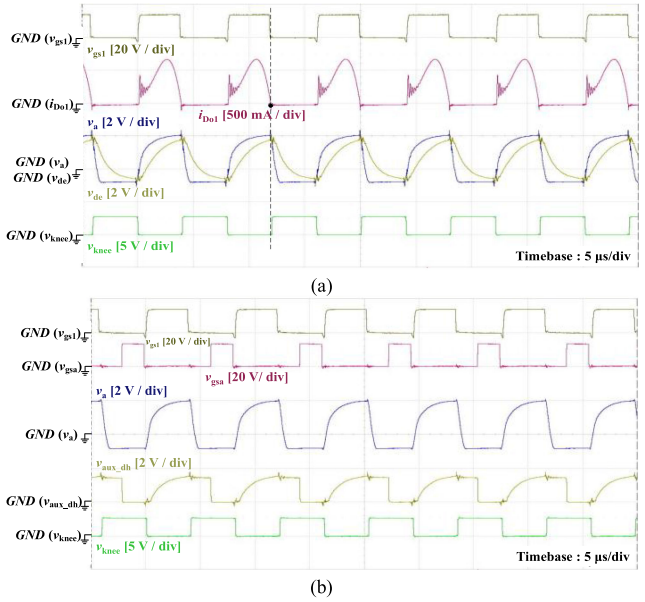

Fig. 12. Waveforms of (a) knee point detector and (b) voltage holder at $V_{\rm in}$ = 342 V and $I_{\rm o}$ = 0.417 A.

of the knee point detector makes $v_{\rm knee}$ may not be pulled high immediately. Therefore, the voltage holder is adopted for output voltage regulation. The auxiliary switch S_a will be turned on to reset the voltage $v_{\rm aux\_dh}$ after sensing by the MCU.

Figs. 12 and 13 show the waveforms of the knee point detector and the voltage holder at input voltage 342 V under 10% load and full load conditions, respectively. The output of the knee point detector $v_{\rm knee}$ is pulled high for sensing the voltage $v_{\rm aux}$ when the converter operation changes from positive half-cycle to negative half-cycle, where the current $i_{\rm Do1}$ will decrease

Fig. 13. Waveforms of (a) knee point detector and (b) voltage holder at $V_{\rm in}$ = 342 V and I_o = 4.17 A.

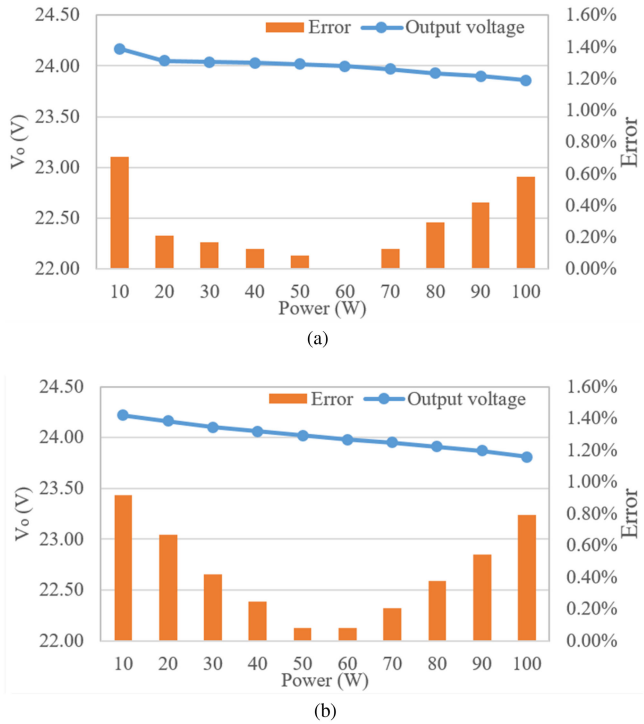

Fig. 14. Performance of output voltage regulation: (a) $V_{\rm in}$ = 280 V and (b) $V_{\rm in}$ = 342 V.

to zero. Fig. 14 shows the output voltage control performance at input voltage 280 and 342 V. The output voltage regulation is regulated within 1%. The voltage estimation error is mainly due to the sample and hold circuit, and knee point detector. By setting the reference point at 60% load, the estimation error can be minimized under overall load conditions. Fig. 15 show the transient response waveforms of the load step from 4 to 2 A and

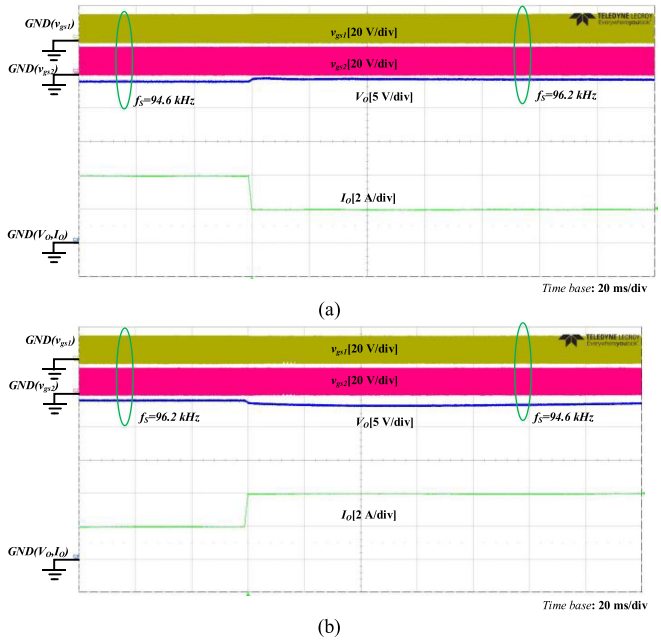

Fig. 15. Transient response waveforms of the load step from (a) 4 to 2 A and (b) 2 to 4 A load conditions at $V_{\rm in} = 312$ V.

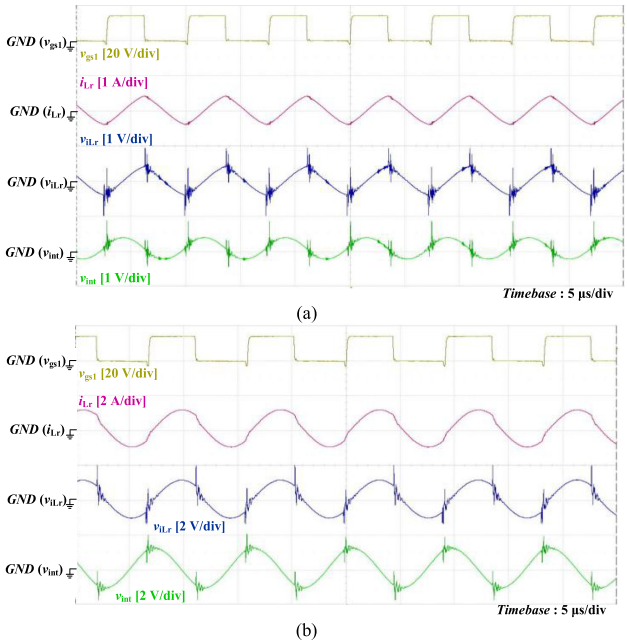

Fig. 17. Waveforms of integrator at $V_{\rm in} = 342$ V for (a) $I_o = 0.417$ A and (b) $I_o = 4.17$ A.

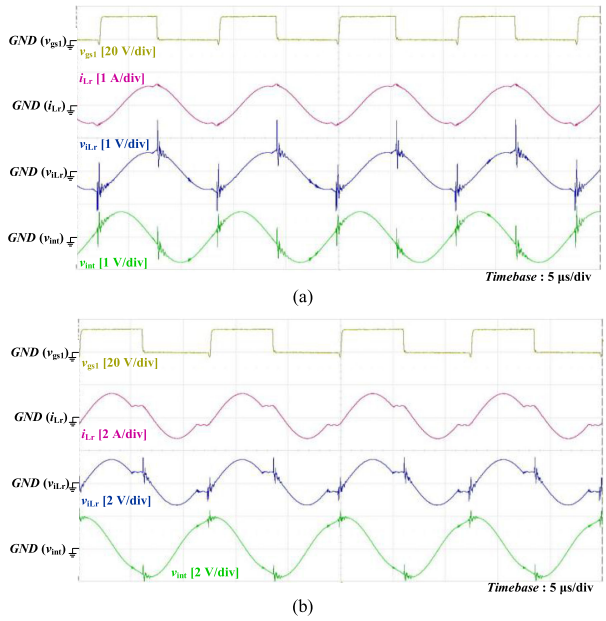

Fig. 16. Waveforms of integrator at $V_{\rm in} = 280$ V for (a) $I_o = 0.417$ A and (b) $I_o = 4.17$ A.

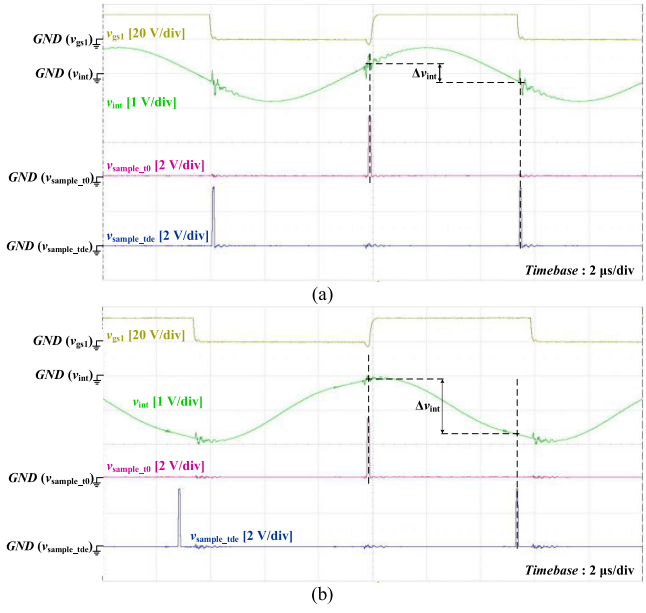

Fig. 18. Zoomed in waveforms of integrator at $V_{\rm in} = 280$ V for (a) $I_o = 0.417$ A and (b) $I_o = 4.17$ A.

2 to 4 A load conditions at $V_{\rm in} = 312$ V with the f_s variation between 94.6 and 96.2 kHz.

B. Output Current Regulation

Figs. 16 and 17 show the waveforms of the integrator at input voltage 280 and 342 V under 10% load and full load conditions, respectively. The voltage $v_{\rm iLr}$ is obtained by the resonant current flows through the current sensing resistor. The output of the integrator $v_{\rm int}$ is obtained by integrating the voltage across the sensing resistor $v_{\rm iLr}$, and the voltage $v_{\rm int}$ will lead 90° than the resonant current $i_{\rm Lr}$. Figs. 18 and 19 show the zoomed in waveforms, and the result for integrating the voltage $v_{\rm iLr}$ within half of switching cycle can be obtained by the difference between the voltage $v_{\rm int}$ sampled at t_0 and the timing that the current flows to zero, which is triggered by the MCU.

Fig. 20 shows the output current control performance at input voltage 280 and 342 V. The output current regulation is regulated

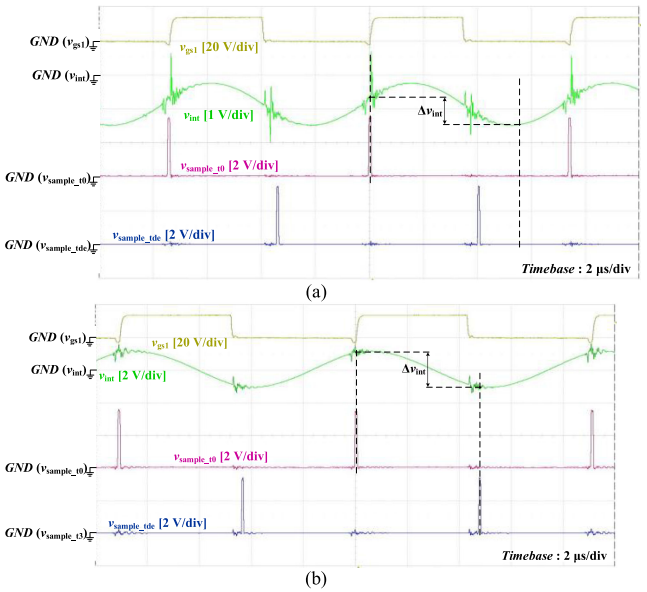

Fig. 19. Zoomed in waveforms of integrator at $V_{\text{in}} = 342$ V for (a) $I_o = 0.417$ A and (b) $I_o = 4.17$ A.

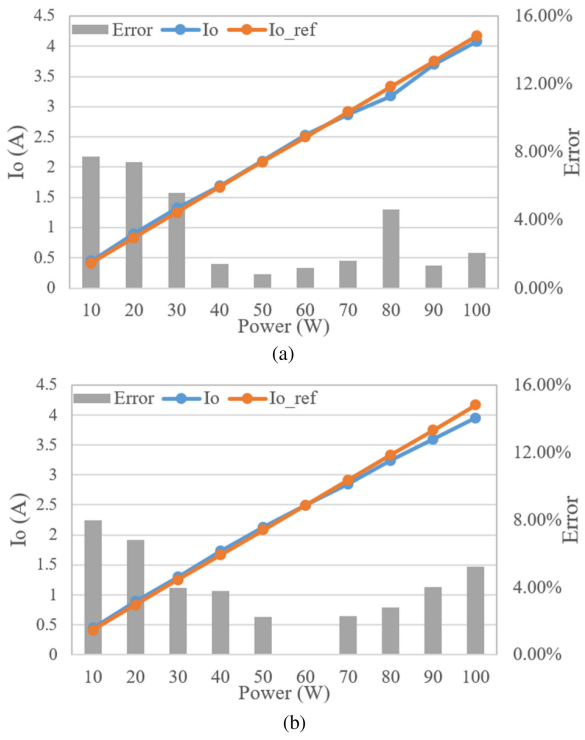

Fig. 20. Performance of output current regulation at $V_{\text{in}} =$ (a) 280 V and (b) 342 V.

within 8%. The current estimation error is due to the nonlinear characteristics of gain-to-frequency curves of integrator and resonant converter. By setting the reference point at 60% load, the estimation error can be minimized under overall load conditions. Fig. 21 shows the measured efficiency curves. Since the switching losses dominates under light load conditions, the efficiency increases as the output power increases. However, the

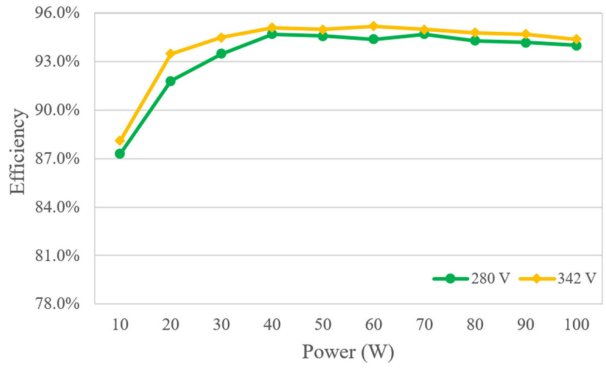

Fig. 21. Measured efficiency curves at rated output power.

efficiency decreases as the output power increases under heavy load conditions owing to the conduction losses dominates. The highest system efficiency is 95.2%.

V. Conclusion and Future Works

In this article, the half-bridge resonant converter with primary-side control schemes with output voltage control and output current control are proposed. To estimate the output voltage accurately, the auxiliary winding voltage is sampled and hold when the output diode current is equal to zero to reduce the effect of the voltage across the equivalent resistor of output diode. To estimate the output current, the resonant current is sampled and integrated by the integrator, then the current estimation algorithm is realized by the MCU. Finally, a 100 W laboratory prototype of primary-side controlled half-bridge resonant converter is implemented. The experimental results show the output voltage accuracy and the output current accuracy are less than 1% and 8%, respectively. The highest system efficiency is 95.2% under 60% load at input voltage 342 V.

The main contribution of this article is to propose the concept of a primary-side control methods for resonant converter with LLC and SRC operations. But many challenges and researches such as overload, short circuit, capacitive region condition, and transient response need to be continued to improve the performance of the primary-side controller of resonant converter for practical applications.

References

[1] Y. T. Lin and T. J. Liang, "IC design of primary-side control for flyback converter," in *Proc. IEEE Int. Future Energy Electron. Conf.*, 2013, pp. 449–453.

[2] P. C. Hsieh, C. J. Chang, and C. L. Chen, "A primary-side control quasi-resonant flyback converter with tight output voltage regulation and self-calibrated valley switching," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 3406–3412.

[3] Y. Bai, W. Chen, X. Yang, X. Yang, and J. Sun, "A novel constant current and constant voltage adaptive blanking regulation scheme for primary-side controlled flyback converter," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2016, pp. 1652–1659.

[4] C. N. Wu, Y. L. Chen, and Y. M. Chen, "Primary-side peak current measurement strategy for high-precision constant output current control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 967–975, Feb. 2015.

[5] X. Xie, J. Wang, C. Zhao, Q. Lu, and S. Liu, "A novel output current estimation and regulation circuit for primary side controlled high power factor single-stage flyback led driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4602–4612, Nov. 2012.
[6] Y. Leng, Y. Wang, J. Jiang, and L. He, "A primary-side controlled single-stage flyback LED driver with high power factor and high accuracy," in *Proc. IEEE Int. Future Energy Electron. Conf.*, 2013, pp. 293–298.
[7] H. H. Chou, Y. S. Hwang, and J. J. Chen, "An adaptive output current estimation circuit for a primary-side controlled LED driver," *IEEE Trans. Power Electron*., vol. 28, no. 10, pp. 4811–4819, Oct. 2013.
[8] J. S. Li, T. J. Liang, K. H. Chen, Y. J. Lu, and J. S. Li, "Primary-side controller IC design for quasi-resonant flyback LED driver," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 5308–5315.
[9] T. J. Liang, K. H. Chen, and J. F. Chen, "Primary side control for flyback converter operating in DCM and CCM," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3604–3612, May 2017.
[10] J. B. Lee, C. E. Kim, J. K. Kim, J. H. Kim, S. C. Moon, and G. W. Moon, "A novel accurate primary-side control (PSC) method for half-bridge (HB) LLC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1797–1803, Apr. 2015.
[11] REDiSEM, "RED2501 LED controller for LLC converters," 2016.
[12] Y. H. Huang, T. J. Liang, and W. J. Wu, "Analysis and implementation of half-bridge resonant capacitance LLC converter," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2016, pp. 1302–1307.
[13] H. Huang, "Design an LLC resonant half-bridge power converter," Texas Instruments Power Supply Design Seminar SEM1900, topic 3, TI literature no. SLUP263, 2010.
[14] Y. C. Chen, "Design and implementation of LLC resonant converter," M.S. thesis, Dept. Elect. Eng., National Cheng Kung Univ., Tainan, Taiwan, Jun. 2009.
[15] J. Hou, "Design procedure for LLC resonant converter," M.S. thesis, Dept. Elect. Eng., National Taiwan Univ., Taipei, Taiwan, Jun. 2009.

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