Characterization and Modeling of Frequency-Dependent On-Resistance for GaN Devices at High Frequencies

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***Abstract*—The switching frequencies of the GaN-based power converters have been pushed to several megahertz and even higher. At such high frequencies, the ON-resistances of the GaN devices might be much higher than their dc values, especially for the devices with low ON-resistances. The frequency-dependent characteristics of the ON-resistance are studied through the electrical and thermal experiments for the first time in this article. A device model for the finite element simulation is proposed to illustrate the mechanism. The results show that the frequency-dependent characteristics of the ON-resistance are closely related to the current distribution inside the GaN device and affected by the layout. A 4-depth ladder circuit model is proposed to describe the frequency-dependent ON-resistance of the GaN devices, and it proves a good accuracy in the frequency range of interest. Beside, two GaN-based 10 MHz dc–dc converters were designed, the only difference of which comes from the layout around GaN devices. The experimental results show that the efficiency of the converter with the optimized layout can be improved by around 2%.**

***Index Terms*—Frequency-dependent characteristics, gallium nitride (GaN), high-frequency power converter, layout, ON-resistance.**

I. Introduction

In RECENT years, gallium nitride (GaN) devices have attracted much attention in the high-frequency and high-efficiency power conversions due to their better figure of merit than the traditional Si MOSFETs [1]–[4]. With an excellent switching performance, the switching frequency of the GaN-based power converters has been pushed up to several megahertz and even higher to increase the power density of the converters [5]–[8].

Understanding the loss mechanism of GaN devices and accurately calculating their losses are important for optimizing megahertz GaN-based circuits. Switching losses are usually not negligible for GaN devices at a high frequency, especially for turn-ON losses in hard switching conditions. There has been a lot of research articles on the modeling and evaluation of the switching losses of GaN devices [9]–[12]. The reverse conduction loss of GaN devices could be significant at high frequencies due to their large reverse voltage drop. Some researchers have performed detailed analyses and proposed some optimization methods [13], [14]. In addition to these two well-known power losses, other power losses may be significant in GaN devices at high frequencies. Recent studies have found that even in zero voltage switching (ZVS) circuits, there could be significant losses in the output capacitance of GaN devices with large and fast voltage swing [7], [15], [16], which is also observed in super-junction Si devices and SiC devices [17]–[19]. This kind of loss is related to dv/dt, voltage amplitude, etc. The conduction losses of GaN devices may increase if an external magnetic field is applied to the GaN devices due to the eddy current effect [6]. The dynamic ON-state resistance effect can also cause an increase in the conduction loss, and it is more pronounced in the high-voltage applications [20]–[22]. In addition to the above-mentioned studies and findings, the research on the conduction loss of GaN devices at high frequencies is still insufficient. In [23] and [24], it is observed that the conduction loss of GaN devices is much more significant than the theoretical value at high frequencies. The researchers speculated that it was related to the dynamic resistance effect but did not conduct further research.

This article focuses on the ON-resistance characteristics of GaN devices at high frequencies and finds that the ON-resistance is frequency dependent. This characteristic is not caused by the dynamic resistance effect but is closely related to the current distribution inside the GaN device at high frequencies. In Section II, the frequency-dependent characteristics of the ON-resistance are studied through the electrical and thermal experiments. The variations of the ON-resistance with temperature and layout at high frequency are also analyzed. In Section III, a simplified device model for the finite element simulation is proposed, and the frequency-dependent mechanism of the ON-resistance is described. Then a 4-depth ladder circuit is presented to accurately

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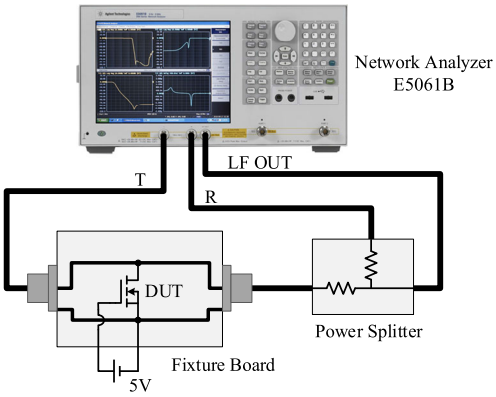

Fig. 1. Measurement of the high-frequency ON-resistance.

TABLE I
PARAMETERS OF GAN DUT

Part Number	EPC2023	EPC2021	EPC2001C	EPC2016C
V_{ds} (V)	30	80	100	100
Max R_{dson} @ V_{gs} = 5V & 25°C (mΩ)	1.45	2.5	7	16

model the frequency-dependent ON-resistance in the frequency range of interest. In Section IV, two GaN-based 10 MHz dc–dc converters are designed, and it proves that the efficiency of the converter with the optimized layout can be improved by 2% compared to that of the converter with the conventional layout. Section V concludes this article.

II. MEASUREMENTS OF ON-RESISTANCE AT HIGH FREQUENCIES

The ON-resistance of GaN devices at high frequencies is measured and analyzed, and then the effects of the layout and temperature on the high-frequency ON-resistance are investigated. To further confirm the frequency-dependent characteristics of the ON-resistance, thermal experiments are carried out. In the above-mentioned experiments, the GaN devices are kept on all the time, thus eliminating the effects of the dynamic ON-state resistance and output capacitance loss.

A. Electrical Measurement

The ON-resistance of several GaN devices are measured by a precise network analyzer at high frequencies, as shown in Fig. 1. The type of network analyzer is E5061B. The gain-phase/shunt-through method is adopted because it is capable of measuring the small resistance at high frequencies [25]. The measurement range with an accuracy of 10% is <1 mΩ–5 Ω at the frequency of 5 Hz–30 MHz.

Four types of GaN devices from Efficient Power Conversion Corporation are evaluated, and their parameters are listed in Table I. The ON-resistance of these four devices varies from 1.45 to 16 mΩ. During the measurement process, a 5 V dc voltage is applied between the gate and the source to ensure that the GaN devices are always ON. It should be noted that the measurement

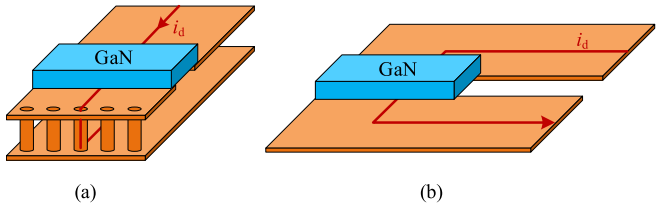

Fig. 2. Two typical layouts. (a) Layout A. (b) Layout B.

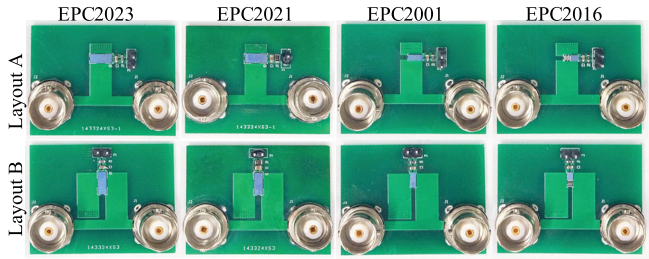

Fig. 3. Fixture boards with DUTs.

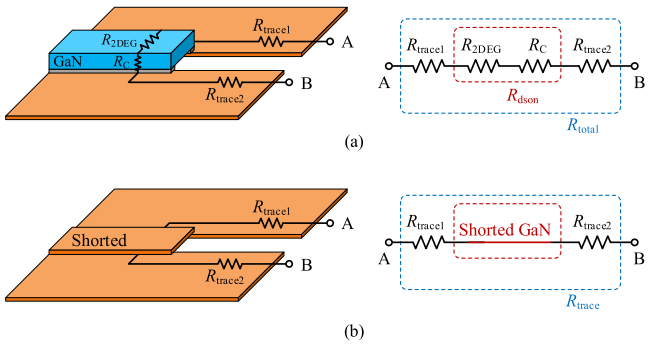

Fig. 4. Measurement of the ON-resistance R_{dson}. (a) Measuring the total resistance $R_{\rm total}$, which consists of the ON-resistance R_{dson} and the PCB trace resistance $R_{\rm trace}$. (b) Measuring the PCB trace resistance $R_{\rm trace}$.

results eliminate the effect of the dynamic ON-resistance and output capacitance loss because the drain–source voltage of the GaN devices is always kept at about zero.

Two typical layouts are evaluated, as shown in Fig. 2. In layout A, the current starts from the top copper layer, then flows through the GaN device and via holes, and finally returns by the bottom copper layer. In layout B, the current only flows through the top copper layer.

Fig. 3 shows the fixture boards of the four GaN devices under test (DUT). For each type of GaN devices, two fixture boards are fabricated based on layout A and layout B.

The printed circuit board (PCB) trace parasitic resistance $R_{\rm trace}$ will inevitably be introduced in the measurement of the ON-resistance if directly using the fixture board. The $R_{\rm trace}$ can be removed by multiple measurements, as shown in Fig. 4. The main steps of the measurements are as follows:

1) calibrate the network analyzer;
2) solder the DUT on the fixture boards, then measure the total resistance $R_{\rm total}$;
3) short the drain and source pads on the fixture boards without DUT, then measure the trace resistance $R_{\rm trace}$;

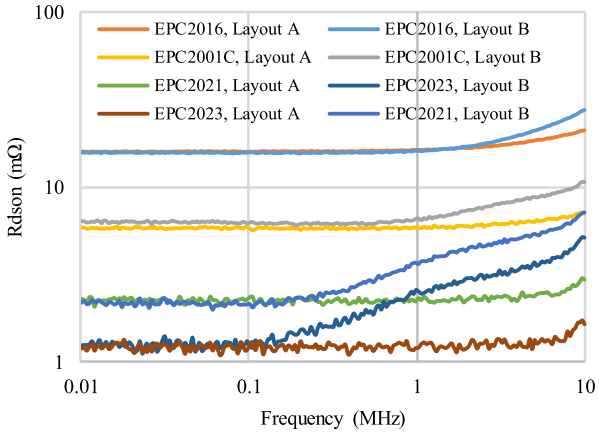

Fig. 5. Measured ON-resistance of GaN devices.

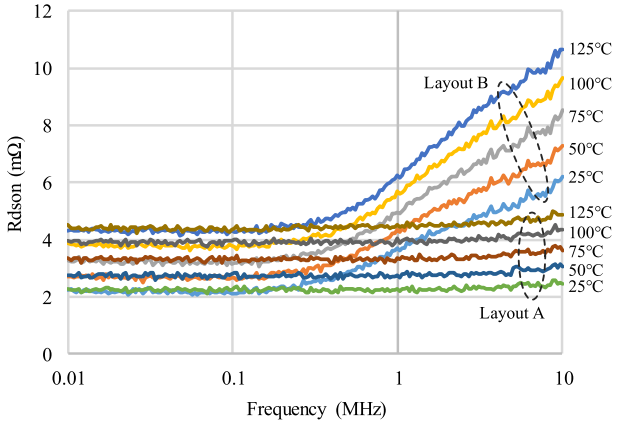

Fig. 6. Measured ON-resistance curves of GaN devices (EPC2021) at different temperatures.

4) calculate the ON-resistance R_{dson} by removing the trace resistance from the total resistance, namely $R_{dson} = R_{total} - R_{trace}$.

The final measured ON-resistance R_{total} includes the channel resistance $R_{2\text{-DEG}}$ and the interconnect resistance R_C inside the package. Fig. 5 shows the measured ON-resistance R_{dson} curves. At low frequencies, the ON-resistance remains almost unchanged and equals the dc value. There is no difference between layout A and layout B. At high frequencies, the ON-resistance of both layouts increases with frequency, and the increasing rate of the ON-resistance in layout A is much smaller than that in layout B. Taking EPC2023 as an example, its ON-resistance at 10 MHz is increased by about four times compared with its dc resistance. The results also show that the ON-resistance starts to grow at a lower frequency if the ON-resistance is smaller.

Furthermore, the influence of temperature on the high-frequency ON-resistance is studied. The GaN device was heated with a heat gun, and the temperature of the GaN device was observed using an infrared camera. The ON-resistance values were recorded when the temperature reached a steady state. The measured curves of the ON-resistance with frequency are shown in Fig. 6, where the temperature varies from 25 to 125 °C with an increment of 25 °C. The results show that the ON-resistance of

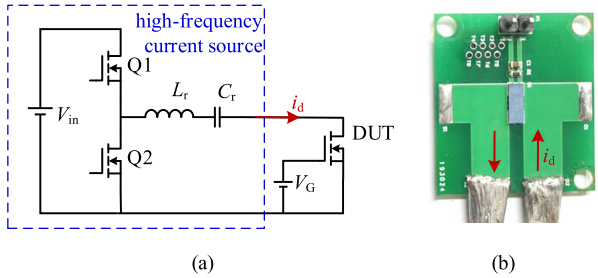

Fig. 7. (a) Thermal test circuit. (b) PCB board with a DUT.

the GaN devices increases with the temperature at high frequencies. In the layout A, the increase of the ON-resistance at high frequencies is almost the same as that at the low frequencies; in the layout B, the increase of the ON-resistance at high frequencies is more significant, which is about twice of that in the layout A at 10 MHz.

B. Thermal Measurement

To further confirm the frequency-dependent characteristics of the ON-resistance of GaN devices, a series of thermal test experiments was performed. The experiments were designed as follows. The GaN DUT remain in the ON-state by applying a 5 V dc voltage between the gate and source. A 10 A dc current and three high-frequencies (100 kHz, 1 MHz, and 5 MHz) 10 A rms ac currents are applied to flow through the drains of GaN devices, respectively. The high-frequency currents are generated by a half-bridge circuit with an *LC* series resonant tank. The switching frequency of the half-bridge is slightly higher than the *LC* resonant frequency to ensure that the half-bridge circuit can achieve ZVS and excite large current with a low input voltage. By adjusting the resonant components *L* and *C*, as well as the input voltage V_{in}, the current at different frequencies can be accurately controlled. In this experiment, the layout B is used. The test circuit and the PCB boards with DUT are shown in Fig. 7. An infrared camera was used to measure the temperature distribution. The type of infrared camera is Flir A320. The top of the entire board, including the GaN device, is coated with a thin layer of black material to improve the accuracy of the thermal measurements.

Since the rms currents are kept equal, the power losses of the GaN devices are only proportional to their ON-resistance. Under the same heat dissipation condition, the junction-ambient thermal resistance of the GaN device can be considered to be constant, so the power loss is approximately proportional to the temperature rise, i.e., the increase of the ON-resistance is approximately proportional to the temperature rise. Fig. 8 shows the experimental thermal images, and Fig. 9 shows the temperature rise of the GaN devices with frequencies. The trend of temperature rise with frequency is consistent with that of the ON-resistance increase with frequency, which further verifies the validity of the electrical measurements.

It can also be seen from Fig. 8 that the temperature distribution of the GaN device changes with the frequency. At low frequencies, such as dc and 100 kHz, the temperature distribution of the

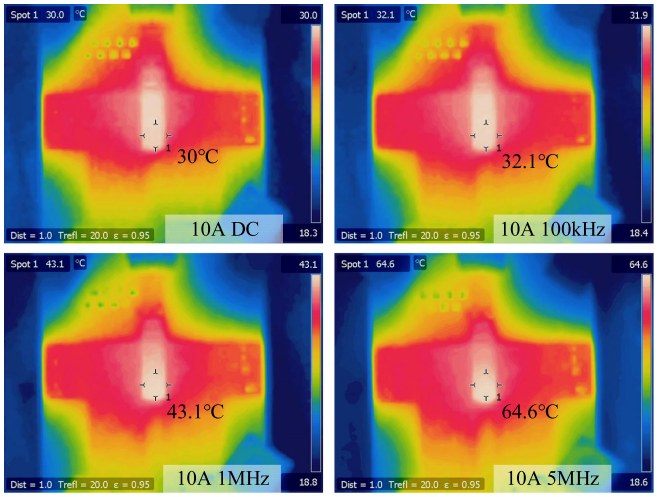

Fig. 8. Experimental thermal images at dc, 100 kHz, 1 MHz, and 5 MHz current excitation.

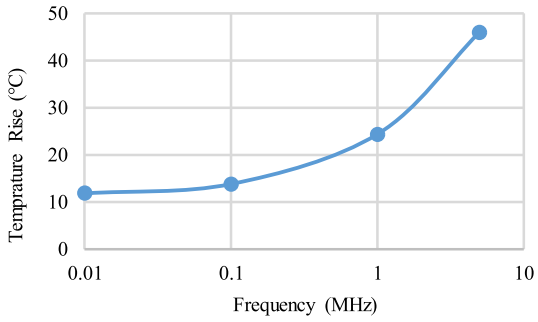

Fig. 9. Temperature rise of GaN devices at the same rms current excitation.

GaN devices is almost uniform. At 1 and 5 MHz, the temperature on one side of the GaN device is higher than the other side, and the uneven distribution becomes more remarkable as the frequency increases. This phenomenon is caused by the uneven current distribution inside the GaN devices at high frequencies, which will be explained and verified in Section III.

III. Modeling of Frequency-Dependent On-Resistance

To illustrate the mechanism of the frequency-dependent ON-resistance of GaN devices, a simplified device model for the finite element simulation is proposed. Additionally, to facilitate the spice circuit simulation, a 4-depth ladder circuit is proposed to model the frequency-dependent ON-resistance in the frequency range of interest.

A. Finite Element Analysis (FEA) Modeling

Fig. 10 shows the cross section of GaN devices with the major components of ON-resistance R_{dson}, namely the channel resistance $R_{2\text{-DEG}}$ and the interconnection resistance R_C [26]. The model of the GaN device is simplified into two parts to facilitate the simulation: a die and several pins. Considering that the GaN die is composed of many parallel connected cells,

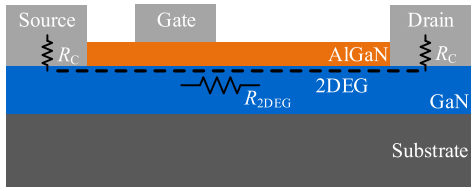

Fig. 10. Cross section of GaN devices with the major components of R_{dson}.

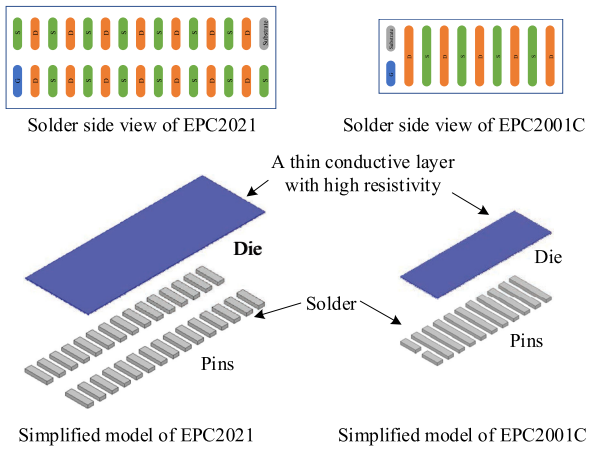

Fig. 11. Simplified model of GaN devices.

and the channel of the GaN die conducts current by a very thin two-dimensional electron gas (2-DEG), the die is simplified into a thin conductive layer with high resistivity. The resistivity of the conductive layer is adjusted to ensure that the dc ON-resistance of the GaN device is the same as the measured result. Taking EPC2021 and EPC2001C as an example, the thicknesses of the conductive layers are set to 20 nm, and the conductivities are set to 230 000 S/m and 150 000 S/m, respectively, as shown in Fig. 11. The pins and solder are set to Sn-37 Pb. The PCB trace is set to copper. The other materials are set to vacuum by default. The maximum element length is 0.2 mm as the initial mesh setting for all the conductors. The mesh of the rest is set by default.

The ON-resistances of the GaN devices are extracted using the proposed simplified model through Ansys software. Fig. 12 compares the simulation and measurement results. For both layout A and layout B, the variation of the ON-resistance with frequency is consistent with the measured results, which verifies the validity of the proposed model.

Fig. 13 shows the simulated current distribution in the GaN dies. At 10 kHz, the current distribution in the GaN device is uniform. At 10 MHz, the current distribution becomes uneven under the skin effect and proximity effect. Due to the uneven current distribution, the effective area of current conduction is reduced, resulting in an increase in the ON-resistance at high frequencies.

The results also show that the current distribution inside the GaN device is closely related to the layout of the GaN device at high frequencies. The current tends to flow through the path with the least impedance, which can lead to current concentration

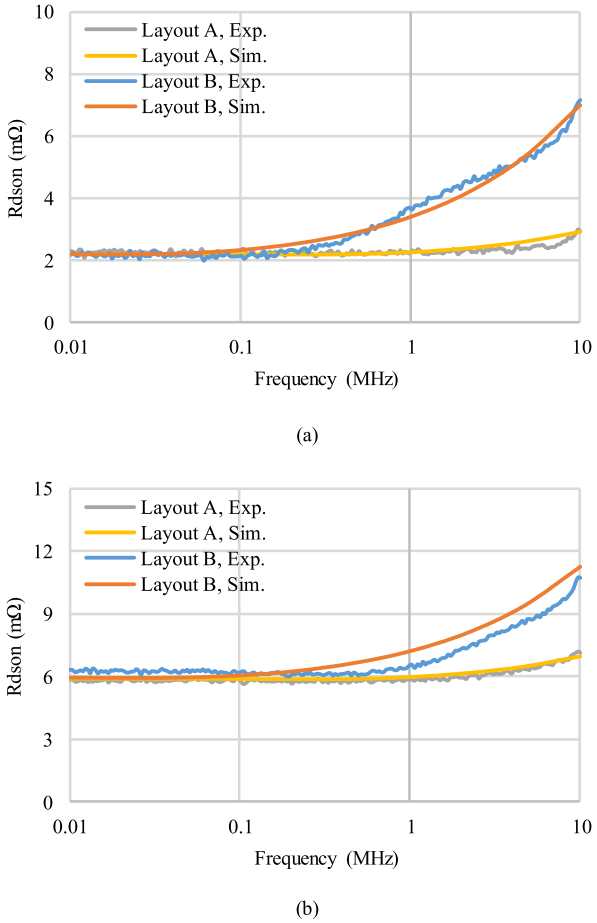

Fig. 12. Comparison of the simulation and measurement results. (a) EPC2021. (b) EPC2001C.

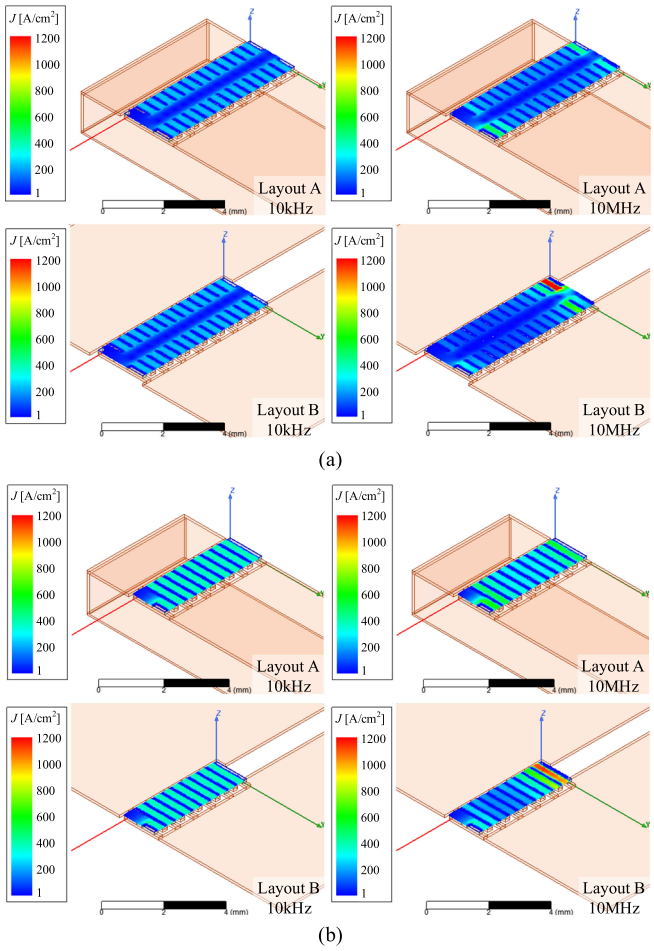

Fig. 13. Current density distribution in GaN devices. (a) EPC2021. (b) EPC2001C.

in the device at high frequencies. In layout B, the current is concentrated on one edge of the GaN device, resulting in a significant increase in the ON-resistance. However, in layout A, since the 2-DEG is very thin, the current distribution in the thickness direction of the 2-DEG is still uniform at 10 MHz. For layout B, there is a more concentrated current distribution in the device at high frequencies, resulting in a larger ON-resistance than that in layout A.

Furthermore, the validity of the simulated current distribution can be confirmed by thermal experimental results (see Fig. 8). In layout B, both the current distribution and the temperature distribution of the devices are uniform at low frequencies. At MHz frequencies, the temperature on one side of the GaN device is higher than the other side, which agrees well with the uneven current distribution in the GaN device.

Beside, the PCB trace resistance at high frequencies is much larger than its dc value due to the skin effect and proximity effect, and its loss is sometimes not negligible. Fig. 14 shows the current distribution in the PCB traces around the GaN device at 10 kHz and 10 MHz, respectively. It can be seen that the current distribution at 10 MHz is more concentrated than that at 10 kHz for both layouts A and B. Moreover, the PCB trace current distribution in layout B is more concentrated than that in layout A at 10 MHz, resulting in a larger PCB trace resistance.

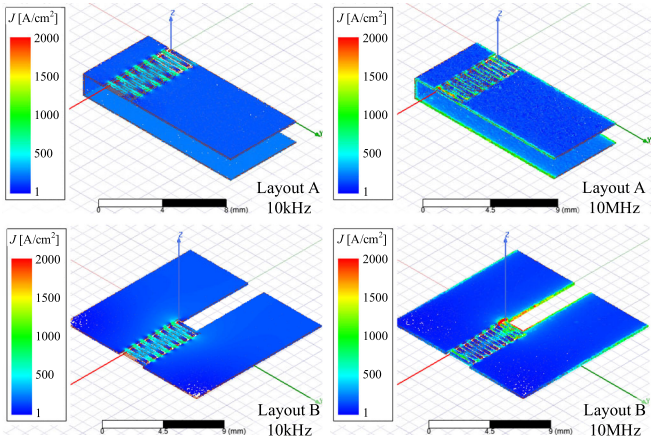

Fig. 14. Current density distribution in the PCB trace around GaN devices.

The main conclusions in this section can be applied to the other commercially available GaN devices, such as GITs and depletion-mode devices, because these devices are all in lateral structure and the basic cells are similar. Beside, it is necessary to pay attention to the packaging of GaN devices. The packaging of GaN devices from different manufacturers differs from

each other. The interconnections in the packaging could have a significant impact on R_{dson} because the interconnections are very close to the GaN dies.

B. Spice Circuit Model

Spice simulation is widely used in the design and optimization of the GaN-based circuits due to its fast simulation speed, ease of implementation, good accuracy, etc. The spice model of GaN devices is usually available from the device manufacturer. However, the ON-resistance in the model is not frequency dependent. The frequency-dependent characteristics of the ON-resistance should be included in the spice model to improve the simulation accuracy of the conduction loss.

It is well known that the conductor resistance is frequency dependent due to the skin and proximity effect, and it has been proven that the frequency-dependent resistance can be accurately modeled by a compact ladder circuit [27]. Inspired by this, a 4-depth ladder circuit is presented to model the frequency-dependent ON-resistance of GaN devices. The choice of the 4-depth ladder model is a tradeoff between accuracy and complexity. The lower depth ladder models have poorer accuracy, whereas the higher depth ladder models have more parameters, and the fitting process becomes more difficult. The 4-depth ladder circuit is shown in Fig. 15. At dc, $R_{dson} = R_1//R_2//R_3//R_4$. At very high frequencies, $R_{dson} \approx R_1$. This circuit can accurately model the R_{dson} from dc to the frequency of interest.

According to the circuit, the expression of the total impedance Z_1 can be derived as

$$\begin{cases} Z_3 = \dfrac{(sL_3 + R_4)\,R_3}{sL_3 + R_4 + R_3} \\ Z_2 = \dfrac{(sL_2 + Z_3)\,R_2}{sL_2 + Z_3 + R_2} \\ Z_1 = \dfrac{(sL_1 + Z_2)\,R_1}{sL_1 + Z_2 + R_1} \end{cases}. \tag{1}$$

Furthermore, R_{dson} and its equivalent series inductance L_{dson} can be solved from the total impedance Z_1

$$\begin{cases} R_{dson} = \mathrm{real}\,(Z_1) \\ L_{dson} = \dfrac{\mathrm{imag}\,(Z_1)}{\omega} \end{cases}. \tag{2}$$

The parameters of L_i ($i = 1, 2, 3$) and R_n ($n = 1, 2, 3, 4$) can be extracted from the curve fitting. The following fitting conditions should be guaranteed: $L_i/L_{i+1} < 1$, $R_n/R_{n+1} > 1$, and $R_1 > R_{dson@DC}$. The fitting process can be easily realized by the MATLAB software. Fig. 16 shows the comparisons between the fitted curves and the measured R_{dson} data. The fitted curves agree well with the measured R_{dson} data within the frequency range of interest. The fitted parameters are given in Table II.

An equivalent inductor L_{dson} is inevitably introduced in the presented model, and it is connected in series with R_{dson}. Fig. 17 shows the curves of the equivalent series inductance. In most cases, L_{dson} can be ignored because it is small enough. For example, L_{dson} is less than 0.02 nH above 100 MHz. In the GaN-based half-bridge circuit, the parasitic power loop inductance is usually above 0.4 nH [28], [29], which is much higher than L_{dson}.

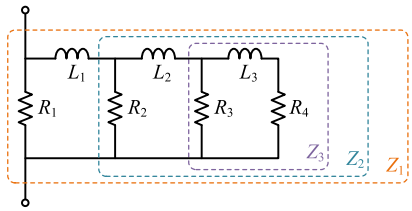

Fig. 15. Ladder circuit of 4-depth for modeling the frequency-dependent ON-resistance.

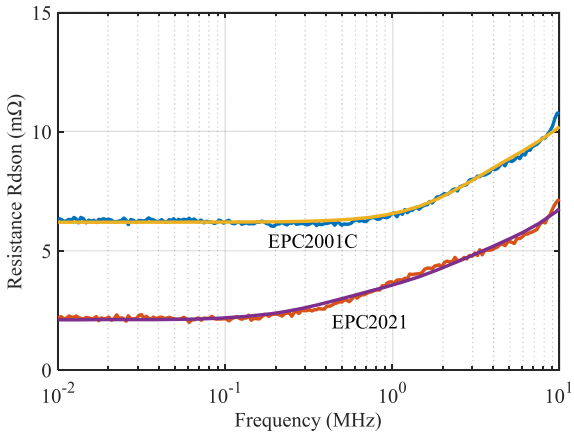

Fig. 16. Comparison of the fitted results and the measured results.

TABLE II
FITTED PARAMETERS OF FREQUENCY-DEPENDENT ON-RESISTANCE

	R_1 (mΩ)	R_2 (mΩ)	R_3 (mΩ)	R_4 (mΩ)	L_1 (nH)	L_2 (nH)	L_3 (nH)
EPC2021	12.24	8.284	7.417	7.237	0.172	0.877	3.638
EPC2001C	28.25	24.21	23.81	23.52	0.082	0.257	1.645

IV. EXPERIMENTAL VALIDATION IN HIGH-FREQUENCY CONVERTERS

As analyzed in the above-mentioned text, the layout has a significant effect on the ON-resistance of GaN devices at high frequencies. To verify the effect of the layouts on the efficiency of the GaN-based converters, two GaN-based 10 MHz dc–dc converters were designed. The main circuit is shown in Fig. 18. It consists of a class E inverter and two diode rectifier circuits. The main switch in the class E inverter is a GaN device. Through careful design, the GaN device can achieve soft switching with very low switching losses and, thus, can operate at very high switching frequencies.

Both converters have the same parameters and operate under the same conditions. The two converters share the same class E inverter and drive circuit for a fair comparison. The only difference comes from the layout around the GaN device. The

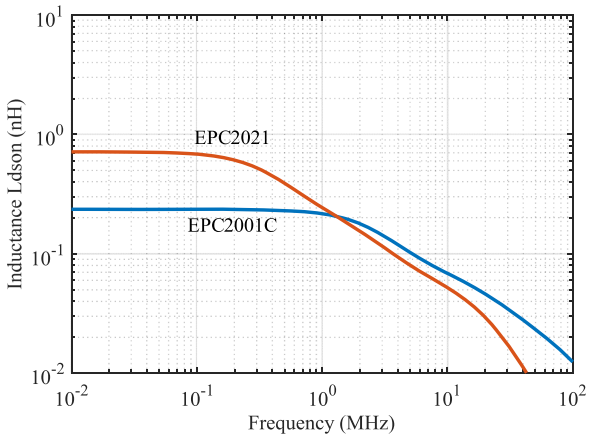

Fig. 17. Equivalent series inductance L_{dson} in the 4-depth ladder circuit.

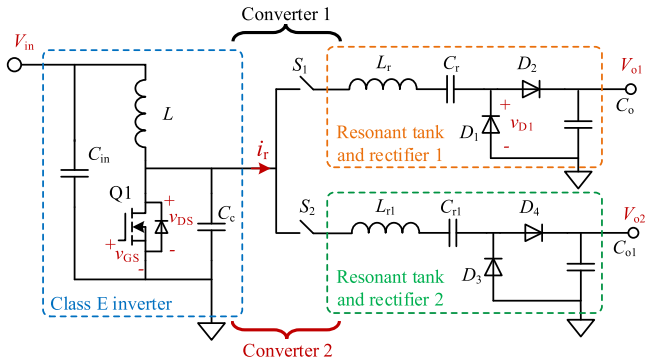

Fig. 18. Main circuit of 10 MHz dc–dc converters.

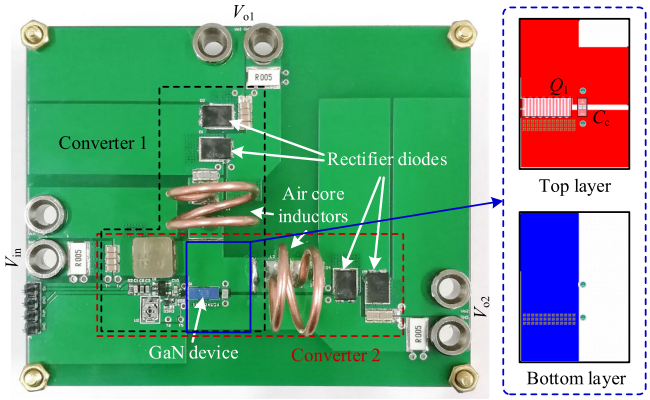

Fig. 19. Experimental prototype.

two converters are tested separately. When testing one of the converters, the other one is disabled by disconnecting the inductor from the drain of the GaN device. A two-layers PCB is used. The current i_r in converter 1 flows through both the top and bottom layers in a layout, as shown in Fig. 2(a). The current i_r in converter 2 flows only through the top layer in a layout, as shown in Fig. 2(b). The experimental prototype is shown in Fig. 19.

TABLE III
CIRCUIT PARAMETERS

Parameter	Value or Part Number
L	0.47 uH
L_r	57.5 nH
C_r	5.47 nF
C_c	3.3 nF
D_1 and D_2	SS12P3L (30 V)
GaN device	EPC2021 (80 V, 2.5 mΩ)
Driver	LMG1020

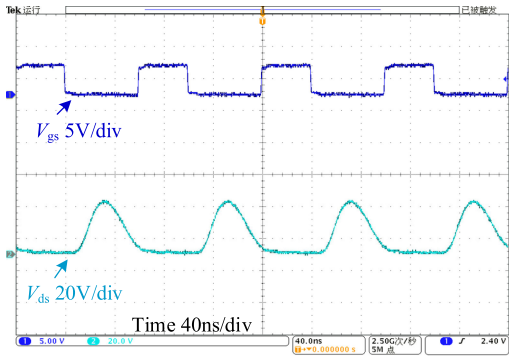

Fig. 20. Measured key waveforms.

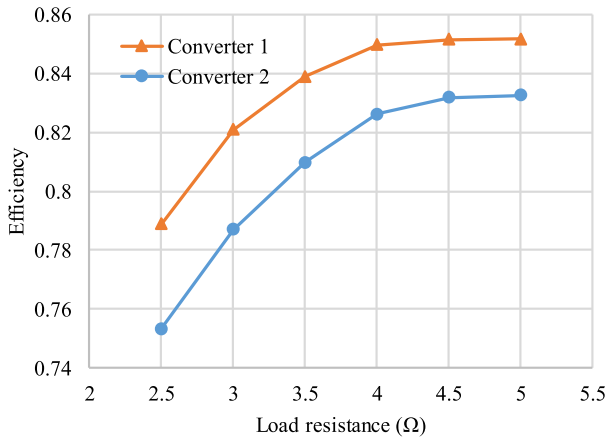

Fig. 21. Measured efficiency curves.

For the two converters, the input voltage is fixed at 10 V. The output voltage is not regulated and it varies with the load resistors. The output voltage is 13.6 V, and the output power is 46 W at a load of 4 Ω. The main circuit parameters and key components of the converters are listed in Table III.

The measured key waveforms are shown in Fig. 20. The gate-source voltage V_{gs} and the drain-source voltage V_{ds} are very clean due to the realization of soft switching.

High-precision 5 mΩ resistors are connected in series to the PCB traces at the input and output ports to detect the input and output currents. With four high-precision multimeters, the voltages and currents of the input and output can be measured simultaneously, and then the efficiency can be calculated. Fig. 21

compares the efficiency of the two converters under different loads. The result shows that the efficiency of the converter 1 is always higher than that of the converter 2. When the load resistance changes from 2.5 to 5 Ω, the efficiency of the converter 1 is 2%–3.3% higher than that of the converter 2. The increase in efficiency mainly results from the reduced ON-resistance of the GaN device and the PCB trace resistance at high frequencies.

V. Conclusion

In this article, the ON-resistances of several GaN devices are evaluated. The results show that the ON-resistance could increase significantly with frequencies above MHz, and it varies with the layouts of GaN devices. A simplified device model for the finite element simulation is proposed to illustrate the mechanism of the frequency-dependent ON-resistance. The simulation results show that the increase in the ON-resistance is caused by the uneven current distribution inside the GaN device at high frequencies. With the knowledge, layout optimizations are presented to reduce the conduction loss of GaN switches at high frequencies. The experimental results show that the efficiency of the converter with the optimized layout can be improved by around 2% compared to that with the conventional layout.

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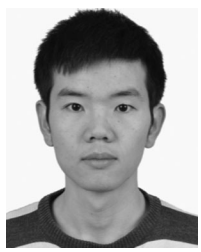

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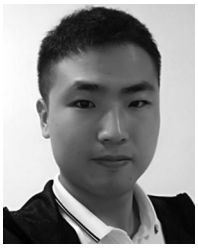

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