

# Bidirectional Buck–Boost Current-Fed Isolated DC–DC Converter and Its Modulation

Fengjiang Wu , Senior Member, IEEE, Shuai Fan, Xiaoguang Li , Student Member, IEEE, and Suhua Luo 

**Abstract**—In this article, a bidirectional buck–boost current-fed isolated dc–dc converter is proposed to realize the bidirectional and buck/boost voltage conversion and accordingly extend the operating range. The basic modulation is proposed and the operation principle is analyzed in detail. Furthermore, the voltage conversion ratio as the functions of the duty cycle ratio of the buck unit and shoot through ratio of the H-bridge converter is derived. The control rule of the two controllable variables is determined based on minimizing the average inductor current. In addition, the optimal starting moment of active period of the buck unit in the switching cycle is determined based on minimizing the inductor current ripple. The detailed experimental results verify the correctness and feasibility of the proposed topology and modulation.

**Index Terms**—Bidirectional boost–buck conversion, current-fed dc–dc converter, modulation optimization.

## I. INTRODUCTION

THE bidirectional isolated dc–dc converter has attracted more and more attentions and has a wide potential applications in the field of electrical vehicle charger, solid state transformer, energy storage system because of the advantages of good soft-switching operation and wide voltage conversion range, and so on [1]–[6].

The bidirectional isolated dc–dc converter mainly includes the following several typical topologies. The first one is the dual active bridge (DAB)-based dc–dc converter. In theory, this topology is capable of a wide voltage conversion and power transfer range and full soft-switching operation. However, its main shortcoming is the large current stress [7]–[10]. It results in a poor utilization rate of the current ratings of the power switches and other components and the system cost is high accordingly.

The second one is the DAB dc–dc converter with the inductor–capacitor resonant tank as the energy storage component. This kind of topology possesses a better electromagnetic characteristic because of the quasi-sinusoidal operating current waveform

and a better current ratio about 1.6 [11]–[16]. Due to these advantages relative to the DAB converter, the resonant-type dc–dc converter has been widely applied in the low-voltage and middle or small power systems. However, in the case of the high voltage, the voltage across the resonant capacitor is very high. In addition, with the increasing of the power rating, the capacitance of the resonant capacitor will increase accordingly [11]. However, it is also very difficult to manufacture, thus, nonpolar capacitor with so large capacitance and high voltage rating.

The third one is the current-fed isolated dc–dc converter (CFIDC) [17]–[26]. The configuration difference from the inductor-based DAB dc–dc converter leads to a quite different operating principle between these two topologies. In theory, the CFIDC possesses a quasi-unity ratio between the peak and averaged values of the transformer current. It results in a best utilization rate of the power rating of the hardware as compared to other two kinds of topologies. However, from the schematic of the CFIDC, it is essentially equivalent a standard boost dc–dc converter if neglecting the transformer current polarity reversion process. It means it can realize only the boost conversion. However, in many actual applications, i.e., the battery or the supercapacitors charging/discharging systems, the wide variation of the terminal voltage of the energy storage components requires that the charging/discharging system is capable of wide voltage conversion range. It is obvious that the feature of only boost conversion is not well suitable for thus application.

In order to preserve the advantages of quasi-unity current ratio of the CFIDC and extend its voltage conversion range, thus possessing a wide application fields, in this article, a bidirectional boost–buck CFIDC (B3CFIDC) is proposed. Furthermore, the control rule of the duty ratio cycle of the buck unit and the shoot through period of the H-bridge converter is determined based on minimizing the average inductor current. In addition, the optimal duration of the rising edge of the power switch of the buck unit relative to the starting moment of the switching cycle is determined based on minimizing the inductor current ripple. Finally, the proposed topology is compared with several popular dc–dc converters to highlight the advantages of the proposed topology.

## II. PRINCIPLE OF PROPOSED B3CFIDC

The proposed B3CFIDC is shown in Fig. 1, including one bridge arm composed of the switches  $S_{11}$  and  $S_{12}$ , inductor  $L$ , H-bridge converter ( $HB_1$ ), H-bridge converter ( $HB_2$ ), and a high

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F. Wu, S. Fan, and X. Li are with the Department of Electrical Engineering, Harbin Institute of Technology, Harbin 150001, China (e-mail: shimeng@hit.edu.cn; fanshuai@1995@163.com; xgli@hit.edu.cn).

S. Luo is with the Department of Physics, Harbin Institute of Technology, Harbin 150001, China (e-mail: shual@hit.edu.cn).

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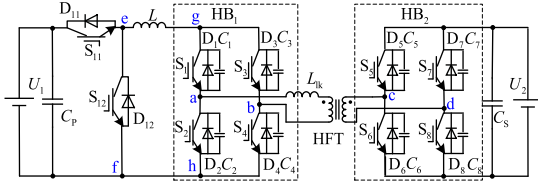
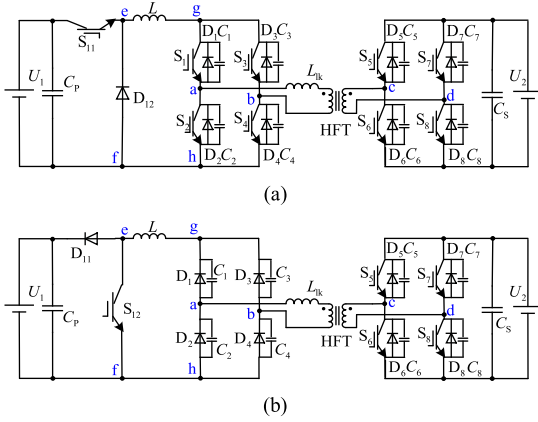


Fig. 1. Schematic of proposed B3CFIDC.


 Fig. 2. Equivalent circuits of proposed topology in two transfer directions. (a) From  $U_1$  to  $U_2$  (forward mode). (b) From  $U_2$  to  $U_1$  (reverse mode).

frequency isolation transformer (HFT).  $L_{lk}$  and  $n$  are the leakage inductor and winding ratio of HFT, respectively.  $L$ , HB<sub>1</sub>, HB<sub>2</sub>, and HFT constitute a standard CFIDC. From [19], it can only achieve boost operation when power is transferred from  $U_1$  to  $U_2$  and only achieve buck operation in reverse direction. For the proposed converter, when power is transferred from  $U_1$  to  $U_2$  (forward mode),  $S_{12}$  is turned OFF and its equivalent circuit is shown in Fig. 2(a). Besides the normal boost operation, it can achieve the buck operation by controlling the duty cycle  $d_{11}$  of  $S_{11}$  in forward mode. When power is transferred in reverse direction, switch  $S_{11}$  is turned OFF and its equivalent circuit is shown in Fig. 2(b). The proposed converter can achieve the boost operation by controlling the duty cycle  $d_{12}$  of  $S_{12}$  in reverse mode. According to the abovementioned analysis, by adding switches  $S_{11}$  and  $S_{12}$ , the proposed topology can realize a bidirectional power transfer and buck-boost operation.

In this section, the operating principle of proposed topology is analyzed to lay the foundation for the subsequent modulation strategy and optimization scheme. Considering that the operating process of the proposed topology in two power transmission directions is dual, in order to save page space, this article only analyses the working process of forward mode.

From [19] and Fig. 2(a), in forward mode, it needs to control the short through period of HB<sub>1</sub> to achieve the boost operation. At the same time, the diagonal switch pairs of HB<sub>2</sub> need to be turned ON for a short time in each switch cycle to control the transformer current actively. So that the transformer current can reach the inductor current actively before the converter becomes power transfer state, so as to avoid the sudden change of

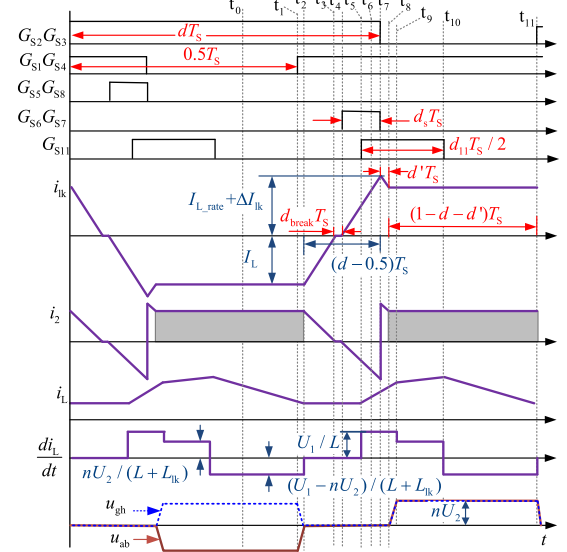


Fig. 3. General modulation waveforms of proposed converter.

transformer current and the voltage spike caused by the current mutation. The turn-ON time ratio of the diagonal switch pairs of HB<sub>2</sub> is defined as  $d_s$ . In addition, there is another controllable variable, which is the duty cycle  $d_{11}$  of  $S_{11}$ .

A general case of the modulation waveforms considering the abovementioned situation is shown in Fig. 3. Fig. 4 shows the corresponding equivalent circuits of the proposed converter during different intervals in Fig. 3. In the following analysis, assuming that the energy storage inductor  $L$  is large enough to maintain a constant average current  $I_L$  through it and the current ripple is small enough to be ignored. The exaggerated waveform of instantaneous current of energy storage inductor (denoted as  $i_L$ ) is also shown in Fig. 3 for the convenience of observation.

The control signals of  $S_2$ ,  $S_3$  of HB<sub>1</sub> lag those of  $S_1$ ,  $S_4$  in a half switching cycle. The simultaneous conduction period of diagonal power switches of HB<sub>1</sub> is defined as  $dT_S$ , then the short through period of HB<sub>1</sub> is

$$t_{shoot} = (d - 0.5)T_S \quad (1)$$

where  $T_S$  is the switching cycle.

The operating process of the proposed converter in each interval of the operating waveforms shown in Fig. 3 is analyzed as follows.

[ $t_0$ ,  $t_1$ ): In this interval,  $S_{11}$  keeps OFF state and  $i_L$  flows through  $D_{12}$ .  $S_2$  and  $S_3$  of HB<sub>1</sub> are under on state and the secondary current of HFT inputs to  $U_2$  through  $D_6$  and  $D_7$ .  $U_1$  does not output power, the inductor  $L$  can be seen as a current source transferring the power from the primary side to the secondary side of HFT. More accurately,  $i_L$  decreases gradually under the action of  $nU_2$ .

[ $t_1$ ,  $t_2$ ): At  $t_1$ ,  $S_1$  and  $S_4$  are turned ON, and  $C_1$  and  $C_4$  begin to discharge. The voltage  $u_{ab}$  rises from  $-U_2$  to zero in a very short time. When  $u_{ab}$  reaches zero at  $t_2$ , the transformer current rises under the action of  $U_2$ ,  $i_L$  and  $i_{lk}$  are no longer equal to

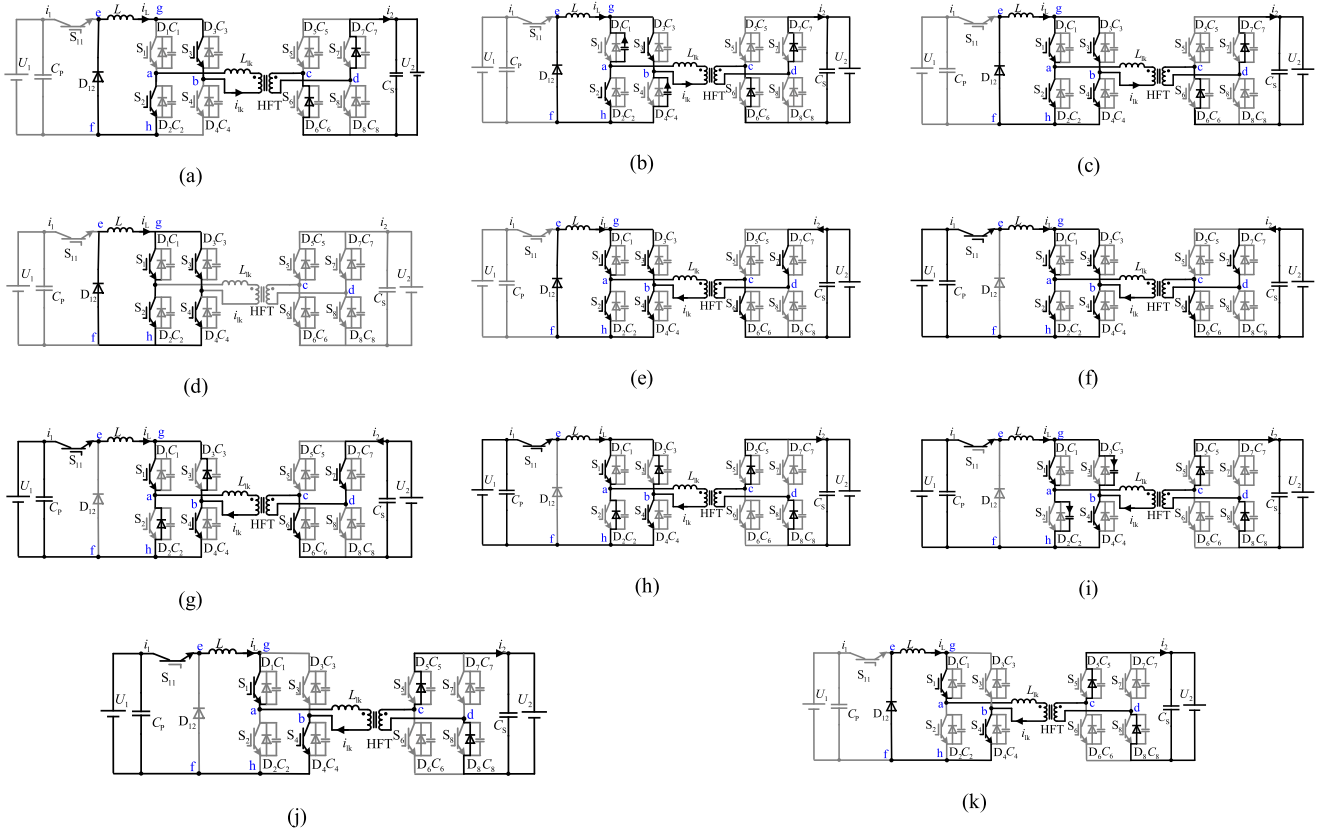


Fig. 4. Equivalent circuits of different intervals in Fig. 3. (a)  $[t_0, t_1)$ . (b)  $[t_1, t_2)$ . (c)  $[t_2, t_3)$ . (d)  $[t_3, t_4)$ . (e)  $[t_4, t_5)$ . (f)  $[t_5, t_6)$ . (g)  $[t_6, t_7)$ . (h)  $[t_7, t_8)$ . (i)  $[t_8, t_9)$ . (j)  $[t_9, t_{10})$ . (k)  $[t_{10}, t_{11})$ .

each other. From KCL law, the current flowing through  $S_{1-4}$  begins to increase from zero.

$[t_2, t_3)$ : At  $t_2$ ,  $S_{1-4}$  are all turned ON, the two bridge arms of HB<sub>1</sub> are both under shoot-through state.  $i_L$  flows through  $D_{12}$  and the two bridge arms of HB<sub>1</sub>.  $i_L$  remains constant because of zero voltage drop on  $L$ . The voltage across  $L_{lk}$  is

$$u_{lk} = u_{ab} - nU_2 \approx -nU_2. \quad (2)$$

So  $i_{lk}$  can be approximately expressed as

$$i_{lk} = -I_L + nU_2(t - t_2)/L_{lk}. \quad (3)$$

It begins to rise under the action of  $U_2$ . Starting from this interval, the current through the power switches of HB<sub>2</sub> are  $i_2 = i_{D7} = i_{D6} = -ni_{lk}$ . The current through  $S_1$  and  $S_4$  begin to rise from zero and the current through  $S_2$  and  $S_3$  begin to decrease from  $I_L$ . The instantaneous current of each switch of HB<sub>1</sub> can be expressed as

$$i_{S2} = i_{S3} = I_L - nU_2(t - t_2)/(2L_{lk}) \quad (4)$$

$$i_{S1} = i_{S4} = nU_2(t - t_2)/(2L_{lk}). \quad (5)$$

$[t_3, t_4)$ : At  $t_3$ ,  $i_{lk}$  reaches zero. The current through  $S_1$  and  $S_4$  rise to  $I_L/2$ , and the current through  $S_2$  and  $S_3$  decrease to  $I_L/2$ . Because all of the power switches of HB<sub>2</sub> are under OFF state,  $i_{lk}$  and the current through  $S_{1-4}$  remain constant.  $D_6$  and

$D_7$  of HB<sub>2</sub> are turned OFF softly because  $i_{lk}$  reached zero. This period is defined as  $d_{break}T_S$ , shown in Fig. 3.

$[t_4, t_5)$ : At  $t_4$ ,  $S_6$  and  $S_7$  are turned ON,  $U_2$  is applied to the secondary side of HFT. Because  $u_{ab} = 0$ ,  $i_{lk}$  begins to rise from zero under the action of  $U_2$ . It leads that the current through  $S_1$  and  $S_4$  begin to rise from  $I_L/2$ , and the current through  $S_2$  and  $S_3$  begin to decrease from  $I_L/2$ . Starting from this interval,  $i_2 = i_{S7} = i_{S6} = ni_{lk}$ .

$[t_5, t_6)$ : At  $t_5$ ,  $S_{11}$  is turned ON, then  $U_1$  is applied to the inductor  $L$ . Because  $u_{ab} = 0$ ,  $i_L$  is expressed as

$$i_L = i_L(t_5) + (U_1 - u_{ab})(t - t_5)/L = i_L(t_5) + U_1(t - t_5)/L. \quad (6)$$

Because  $L$  is much larger than  $L_{lk}$ , the rising rate of  $i_L$  is much less than the raising rate of  $i_{lk}$ . The energy is stored in  $L$  from  $U_1$ .

$[t_6, t_7)$ : At  $t_6$ ,  $i_{lk}$  rises to  $I_L$  and the current through  $S_1$  and  $S_4$  also rise to  $I_L$ , and the current through  $S_2$  and  $S_3$  decrease to zero. The current  $i_{lk}$  has two flowing paths: the first one is from  $S_1$  to  $D_3$ , and the other one is from  $D_2$  to  $S_4$ . The current through HB<sub>1</sub> are expressed as

$$i_{D2} = i_{D3} = 0.5(i_{lk} - I_L) \quad (7)$$

$$i_{S1} = i_{S4} = 0.5I_L + 0.5(i_{lk} - I_L) = 0.5i_{lk}. \quad (8)$$

$[t_7, t_8)$ : At  $t_7$ ,  $S_2$ ,  $S_3$ ,  $S_6$ , and  $S_7$  are turned OFF.  $S_2$  and  $S_3$  are under zero-current switching because no current flow through

them. Because  $u_{ab} = 0$ ,  $u_{lk} \approx -nU_2$ , and  $i_{lk}$  will decrease gradually. It means  $i_{lk}$  reaches its maximum at  $t = t_7$ , which is defined as  $i_{lk\_max}$ . In order to ensure there is no voltage spike in the entire power range,  $i_{lk\_max}$  should be designed based on the rated inductor current  $I_{L\_rate}$  and a current margin  $\Delta I_{lk}$  is considered. So  $i_{lk\_max}$  can be expressed as

$$i_{lk\_max} = I_{L\_rate} + \Delta I_{lk}. \quad (9)$$

Because  $i_{lk}$  begins to decrease, the current through  $S_1$ ,  $S_4$ ,  $D_2$ , and  $D_3$  also begin to decrease. Therefore, the current stress of each power switch can be obtained from (7) to (9).

$$i_{D1-4} = i_{S1-4} = I_{L\_rate} + 0.5\Delta I_{lk}. \quad (10)$$

[ $t_8, t_9$ ): At  $t_8$ ,  $i_{lk}$  reaches to  $I_L$ , and the current through  $D_2$  and  $D_3$  are zero.  $C_2$  and  $C_3$  are charged, and  $u_{ab}$  rises gradually. The flowing path of  $i_{lk}$  becomes from  $S_1$  to  $S_4$  and the secondary transformer current flows from  $D_5$  to  $U_2$  to  $D_8$ . It means the converter operates at the normal power transfer state. Furthermore, the period of [ $t_7, t_8$ ) is

$$d'T_S = (I_{L\_rate} + \Delta I_{lk} - I_L) L_{lk}/nU_2. \quad (11)$$

[ $t_9, t_{10}$ ): At  $t_9$ ,  $u_{ab}$  reaches to  $nU_2$  and  $i_L$  is expressed as

$$i_L = i_L(t_9) + (U_1 - nU_2)(t - t_9)/(L + L_{lk}). \quad (12)$$

[ $t_{10}, t_{11}$ ): At  $t_{10}$ ,  $S_{11}$  is turned OFF and  $i_L$  flows through  $D_{12}$ .  $i_L$  begins to decrease with the rate of  $(nU_2)/(L + L_{lk})$ .

Next, the relationship between the controllable variables  $d_{11}$ ,  $d$ ,  $d_s$ , the voltage conversion ratio  $k = nU_2/U_1$ , and  $I_L$  is analyzed. The average voltage between point e and f shown in Fig. 2 is defined as  $U_{ef}$  and the average voltage between point g and h shown in Fig. 2 is defined as  $U_{gh}$ . Obviously, the waveform of the instantaneous voltage between g and h can be obtained by rectifying the waveform of  $u_{ab}$  shown in Fig. 3, so  $U_{gh}$  can be obtained by calculating the average value of  $u_{ab}$  in a half switching cycle. The two average voltages can be expressed as

$$U_{ef} = d_{11}U_1 \quad (13)$$

$$U_{gh} = 2(1 - d - d')nU_2. \quad (14)$$

The volt-second product of  $L$  at the steady state is zero in the half switching cycle. It means

$$U_{ef} = U_{gh}. \quad (15)$$

Thus, the relationship between the voltage conversion ratio and the controllable variables can be obtained as

$$k = \frac{nU_2}{U_1} = \frac{d_{11}}{2(1 - d - d')}. \quad (16)$$

By substituting (11) into (16),  $k$  is expressed as

$$k = \frac{d_{11}}{2[1 - d - L_{lk}(I_{L\_rate} + \Delta I_{lk} - I_L)/(nU_2T_S)]}. \quad (17)$$

From (16), because of  $d > 0.5$  and  $d' > 0$ , the converter can achieve the boost and buck operation by varying  $d_{11}$  and  $d$  cooperatively.

### III. CONTROL RULE OF CONTROLLABLE VARIABLES

According to the abovementioned analysis, the voltage conversion ratio can be tuned by varying the controllable variables  $d_{11}$  and  $d$ . For a certain voltage conversion ratio,  $d_{11}$  and  $d$  have infinite combinations. So it is necessary to introduce some appropriate constraint to obtain the exact relationship between  $d_{11}$ ,  $d$ , and  $k$ . In addition, the variation of the position of  $S_{11}$  under on state in the entire control cycle does not affect the voltage conversion ratio, however, it will affect the current ripple of inductor. In this section, the position of  $S_{11}$  under on state relative to the control signal of  $HB_1$  will be obtained by minimizing the current ripple of inductor.

#### A. Control Rule of $d_s$ , $d_{11}$ and $d$ to Reduce Average Inductor Current

Following is an analysis of the design principle of the turn-ON time ratio  $d_s$  of the diagonal switch pairs of  $HB_2$ . The function of  $d_s$  is to make the transformer current to rise actively by adding the voltage  $nU_2$  at the leakage inductor  $L_{lk}$ , so that the voltage spike can be eliminated. Fig. 3 shows that during the turn-ON period of the diagonal switch pairs of  $HB_2$ ,  $U_1$  does not output power and the power flows to  $L_{lk}$  from  $U_2$ , which can be equivalent to the reactive power. Therefore, this period ( $d_sT_S$ ) should be as short as possible to avoid occupying too much effective power transfer time. The expression of primary transformer current is

$$i_{lk} = nU_2t/L_{lk}. \quad (18)$$

By substituting (9) into (18),  $d_s$  can be solved as

$$d_s = \frac{L_{lk}i_{lk\_max}}{nU_2} = \frac{L_{lk}}{nU_2} (I_{L\_rate} + \Delta I_{lk}). \quad (19)$$

Therefore, when the required  $i_{lk\_max}$  and  $U_2$  remain unchanged,  $d_s$  is mainly proportional to  $L_{lk}$ . The smaller  $L_{lk}$  is, the smaller  $d_s$  will be. In the actual system, it is necessary to consider the manufacturing process of the transformer, in order to avoid its design value too small to be realized in the actual production process. In order to simplify the control complexity, in the entire power range and voltage conversion range,  $d_s$  is always designed according to (19) and remain unchanged in this article.

Next, the control principle of  $d_{11}$  and  $d$  are analyzed. According to the principle of the converter, the relationship between the average input current  $I_1$  and  $I_L$  is

$$I_1 = d_{11}I_L. \quad (20)$$

From the waveform of the output current  $i_2$  shown in Fig. 3, the effective part of  $i_2$  is the area of the shadow part. The average value of  $i_2$  can be expressed as

$$I_2 = 2I_L(1 - d - d'). \quad (21)$$

From the abovementioned two equations, under the premise of transferring the same rated power, the larger  $d_{11}$  is, the smaller  $I_L$  will be. Reducing  $I_L$  is beneficial to reduce the loss of power devices, inductors  $L$  and HFT. Therefore, the larger  $d_{11}$  and the smaller  $d$  should be chosen as far as possible. Furthermore,

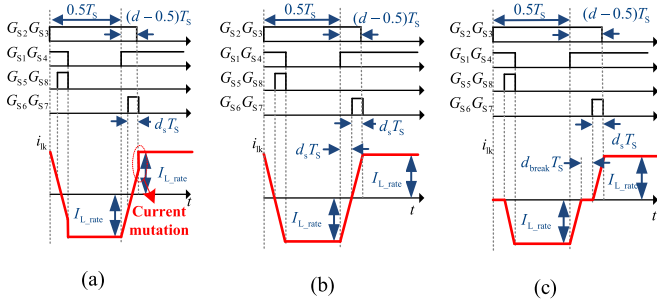


Fig. 5. Waveforms of polarity conversion process of the primary transformer current under different conditions. (a)  $(d - 0.5) < 2d_s$ . (b)  $(d - 0.5) = 2d_s$ . (c)  $(d - 0.5) > 2d_s$ .

from (16), in order to obtain the same voltage conversion ratio, if  $d_{11}$  is increased,  $d$  should be reduced accordingly.

Therefore, for a given  $k$ ,  $d_{11}$  should be as large as possible while  $d$  should be as small as possible to reduce  $I_L$ . Considering that  $k$  is proportional to  $d_{11}$  and inversely proportional to  $d$ , when the converter is under buck operation,  $d$  is taken as the minimum. When the converter is under boost operation,  $d_{11}$  is taken as 1 and various voltage conversion ratios can be achieved by adjusting  $d$ .

The principle of determining the minimum of  $d$  is analyzed as follows. According to the abovementioned analysis, in order to eliminate the voltage spike, HB<sub>2</sub> is required to provide the voltage actively for a short time in each half switching cycle so that the primary transformer current can rise as soon as possible and exceed  $I_L$ . In order to obtain the fastest variation rate of the primary transformer current, during the period when HB<sub>2</sub> provides the reverse voltage, the ac-side output voltage of HB<sub>1</sub>  $u_{ab}$  should be equal to zero.

Therefore, the short-through period of HB<sub>1</sub> should be greater than or equal to twice the period of HB<sub>2</sub> providing reverse voltage. So the constraint of  $d$  is

$$(d - 0.5) \geq 2d_s. \quad (22)$$

Fig. 5 shows the waveforms of polarity conversion process of the primary transformer current under different conditions. From Fig. 5(a), if  $(d - 0.5) < 2d_s$ , due to current transition time of transformer,  $L$  and  $L_{lk}$  are connected in series when the current through  $L_{lk}$  is not equal to the current through  $L$ , resulting in sudden change of current and the voltage spike.

As shown in Fig. 5(b), when the converter state varies, the primary transformer current is exactly equal to  $I_{L,rate}$  and it is in a critical continuous state. From Fig. 5(c), when the converter state varies, the primary transformer current also reach  $I_{L,rate}$ , so there will be no voltage spike. However, because the primary transformer current is discontinuous, in order to obtain the same power, the average inductor current will be larger than that in the critical continuous state, so additional power loss will be caused. In this article, in order to reduce the power loss as much as possible under the premise of eliminating the voltage spike, the minimum of  $d$  in buck operation is chosen as

$$d_{\min} = 0.5 + 2d_s. \quad (23)$$

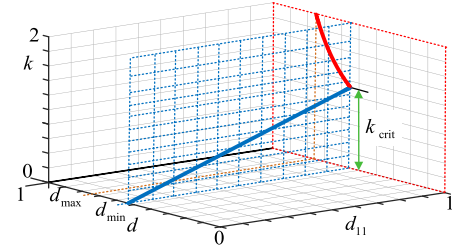


Fig. 6. 3-D spatial curves of  $k$  as the functions of  $d$ ,  $d_{11}$ .

By substituting (23) into (16) and ignoring the effect of  $d'$ , the relationship between  $k$  and  $d_{11}$  can be obtained as

$$k = \frac{nU_2}{U_1} = \frac{d_{11}}{2(1 - 0.5 - 2d_s - d')} \approx \frac{d_{11}}{2(0.5 - 2d_s)}. \quad (24)$$

When  $d_{11} = 1$ , the critical value of  $k$  is

$$k_{\text{crit}} = \frac{1}{2(1 - 0.5 - 2d_s - d')} \approx \frac{1}{2(0.5 - 2d_s)} > 1. \quad (25)$$

When  $k$  is larger than  $k_{\text{crit}}$ ,  $d_{11}$  is kept at 1, and  $k$  can be adjusted by adjusting the shoot-through period of HB<sub>1</sub>. In this situation,  $k$  can be expressed as

$$k = \frac{1}{2(1 - d - d')}. \quad (26)$$

In order to more intuitively and clearly explain the control rules of  $d$  and  $d_{11}$  in the entire voltage conversion range, the three-dimensional (3-D) curves of  $k$  as the functions of  $d$  and  $d_{11}$  are drawn and shown in Fig. 6. In Fig. 6, the blue solid line is from (24) and the red line is from (26). It can be clearly seen from Fig. 6 that, when  $k \leq k_{\text{crit}}$ ,  $d_{11}$  and  $k$  vary on the plane of  $d = d_{\min}$ . When  $k > k_{\text{crit}}$ ,  $d$  and  $k$  vary on the plane of  $d_{11} = 1$ . Besides, the adjustable range of  $d$  is  $[d_{\min}, d_{\max}]$ .  $d_{\max}$  can be calculated by setting  $k = 2$  in (26).

### B. Discussion and Optimization of Action Position of $G_{S11}$

From the principle of the proposed B3CFIDC, the position of S<sub>11</sub> under state in the switching cycle does not affect the voltage conversion ratio and the average inductor current. However, it will affect the inductor current ripple. In the following, the variation of the inductor current ripple  $\Delta i_L$  with different action position of  $G_{S11}$  is discussed and the optimal action position is determined to minimize the inductor current ripple.

Considering that the polarity of  $(U_1 - nU_2)$  determines the waveforms of  $i_L$ , the following analysis is divided into two cases:  $k \leq 1$  and  $1 \leq k < k_{\text{crit}}$ .

Taking the rising edge of  $G_{S2}$  as the starting moment, the operating waveforms of the B3CFIDC can be divided into six cases: a–f with the action interval of  $G_{S11}$  gradually moving backward along the time axis. As shown in Fig. 7(a), cases a–f correspond to  $1 < k < k_{\text{crit}}$ . As shown in Fig. 7(b), cases g–l correspond to  $k \leq 1$ . The time difference between the rising edge of  $G_{S11}$  and  $G_{S2}$  is expressed by  $\Delta d_{11} T_s$ . Considering that these cases only occur when  $d_{11}$  is in a certain range, the

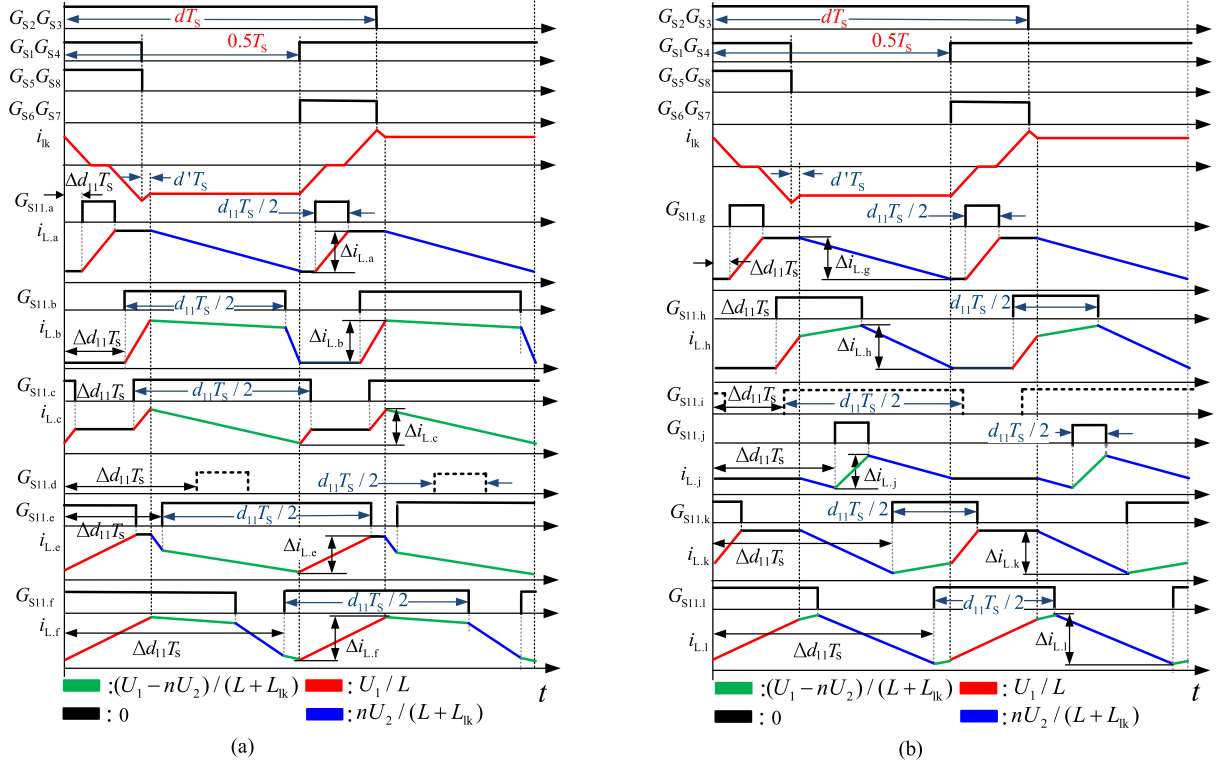


Fig. 7. Waveform of  $i_L$  with different action positions of  $G_{S11}$ . (a)  $1 < k < k_{crit}$ . (b)  $k \leq 1$ .

expressions of  $\Delta i_L$  in various cases and corresponding range of  $d_{11}$  are derived as follows.

1) *Case. a, g*: According to Fig. 7, the conditions of the edge moment of  $G_{S11.a}$  or  $G_{S11.g}$  is  $0 \leq \Delta d_{11} < (d + d' - 0.5)$ ,  $0 \leq (\Delta d_{11} + 0.5d_{11}) < (d + d' - 0.5)$ , and  $0.5d_{11}T_S$  should be less than the shoot-through period of HB<sub>1</sub>. The range of  $d_{11}$  can be obtained as

$$d_{11} < nU_2/(nU_2 + U_1). \quad (27)$$

From Fig. 7(a) and (b), the current ripple expressions of Case a and g can be obtained as

$$\Delta i_{L.a} = U_1(0.5d_{11})T_S/L \quad (28)$$

$$\Delta i_{L.g} = nU_2(1 - d - d')T_S/(L + L_{lk}). \quad (29)$$

2) *Case. b, h*: According to Fig. 7, when these two cases occur, the conditions of the edge moment of  $G_{S11.b}$  or  $G_{S11.h}$  is  $0 \leq \Delta d_{11} < (d + d' - 0.5)$ ,  $(d + d' - 0.5) \leq (\Delta d_{11} + 0.5d_{11}) < 0.5$ , and  $0.5d_{11}T_S$  should be less than  $(1 - 4d_s)kT_S$ . From Fig. 7(a) and (b), the current ripple expressions are

$$\Delta i_{L.b} = U_1(d + d' - 0.5 - \Delta d_{11})T_S/L \quad (30)$$

$$\Delta i_{L.h} = nU_2(0.5 - \Delta d_{11} - 0.5d_{11})T_S/(L + L_{lk}). \quad (31)$$

3) *Case. c, i*: According to Fig. 7, the conditions of edge moment is  $0 \leq \Delta d_{11} < (d + d' - 0.5)$ ,  $0.5 \leq (\Delta d_{11} + 0.5d_{11}) < (d + d')$ , and  $0.5d_{11}T_S$  must exceed the period when two diagonal switches of HB<sub>1</sub> are turned ON, which means  $(1 - d + d') < 0.5d_{11}$  and  $k > 1$  is obtained. So case c will occur as long as

$G_{S11.c}$  satisfies the conditions of edge moment when  $1 < k < k_{crit}$ , and case i does not exist when  $k \leq 1$ . From Fig. 7(a), the ripple current expressions are

$$\Delta i_{L.c} = U_1[d + d' - 0.5 - 0.5(1 - d_{11})]T_S/L \quad (32)$$

4) *Case. d, j*: According to Fig. 7, the conditions of the edge moment is  $(d + d' - 0.5) \leq \Delta d_{11} < 0.5$  and  $d_{11}$  must satisfy  $(1 - d + d') \geq 0.5d_{11}$ . According to the expression of  $k$ , case d does not exist when  $1 < k < k_{crit}$  and case j will occur as long as  $G_{S11.j}$  satisfies the conditions of edge moment when  $k \leq 1$ . From Fig. 7(b), the current ripple expressions of case j can be obtained as

$$\Delta i_{L.j} = nU_2(1 - d - d' - 0.5d_{11})T_S/(L + L_{lk}). \quad (33)$$

5) *Case. e, k*: The conditions of the edge moment is  $(d + d' - 0.5) \leq \Delta d_{11} < 0.5$ ,  $0.5 \leq (\Delta d_{11} + 0.5d_{11}) < (d + d')$ , and  $0.5d_{11}T_S$  should be less than  $(1 - 4d_s)kT_S$ . The current ripple expressions of cases e and k can be obtained as

$$\Delta i_{L.e} = U_1[\Delta d_{11} - 0.5(1 - d_{11})]T_S/L \quad (34)$$

$$\Delta i_{L.k} = nU_2(\Delta d_{11} - d - d' + 0.5)T_S/(L + L_{lk}). \quad (35)$$

6) *Case. f, l*: The conditions of the edge moment is  $(d + d' - 0.5) \leq \Delta d_{11} < 0.5$ ,  $(d + d') \leq (\Delta d_{11} + 0.5d_{11}) < 1$ , and  $d_{11}$  must satisfied  $(d + d' - 0.5) \leq 0.5d_{11}$ . The range of  $d_{11}$  can be obtained as

$$d_{11} \geq nU_2/(nU_2 + U_1). \quad (36)$$

TABLE I  
CONDITIONS AND CURRENT RIPPLE EXPRESSIONS UNDER  $1 < k < k_{\text{crit}}$

Case	Conditions of edge moment	Limitation of $d_{11}$	$\Delta i_L$
a	$0 \leq \Delta d_{11} < d + d' - 0.5, 0 \leq \Delta d_{11} + 0.5d_{11} < d + d' - 0.5$	$d_{11} < nU_2 / (nU_2 + U_1)$	$\Delta i_{L,a} = U_1(0.5d_{11})T_S / L$
b	$0 \leq \Delta d_{11} < d + d' - 0.5, d + d' - 0.5 \leq \Delta d_{11} + 0.5d_{11} < 0.5$	$d_{11} < (1 - 4d_s)k$	$\Delta i_{L,b} = U_1(d + d' - 0.5 - \Delta d_{11})T_S / L$
c	$d + d' - 0.5 \leq \Delta d_{11} < 0.5, 0.5 \leq \Delta d_{11} + 0.5d_{11} < d + d'$	$d_{11} < (1 - 4d_s)k$	$\Delta i_{L,c} = U_1[d + d' - 0.5 - 0.5(1 - d_{11})]T_S / L$
e	$d + d' - 0.5 \leq \Delta d_{11} < 0.5, 0.5 \leq \Delta d_{11} + 0.5d_{11} < d + d'$	$d_{11} < (1 - 4d_s)k$	$\Delta i_{L,e} = U_1[\Delta d_{11} - 0.5(1 - d_{11})]T_S / L$
f	$d + d' - 0.5 \leq \Delta d_{11} < 0.5, d + d' \leq \Delta d_{11} + 0.5d_{11} < 1$	$d_{11} \geq nU_2 / (nU_2 + U_1)$	$\Delta i_{L,f} = U_1(d + d' - 0.5)T_S / L$

TABLE II  
CONDITIONS AND CURRENT RIPPLE EXPRESSIONS UNDER  $k \leq 1$

Case	Conditions of edge moment	Limitation of $d_{11}$	$\Delta i_L$
g	$0 \leq \Delta d_{11} < d + d' - 0.5, 0 \leq \Delta d_{11} + 0.5d_{11} < d + d' - 0.5$	$d_{11} < nU_2 / (nU_2 + U_1)$	$\Delta i_{L,g} = nU_2(1 - d - d')T_S / (L + L_{lk})$
h	$0 \leq \Delta d_{11} < d + d' - 0.5, d + d' - 0.5 \leq \Delta d_{11} + 0.5d_{11} < 0.5$	$d_{11} < (1 - 4d_s)k$	$\Delta i_{L,h} = nU_2(0.5 - \Delta d_{11} - 0.5d_{11})T_S / (L + L_{lk})$
j	$d + d' - 0.5 \leq \Delta d_{11} < 0.5, 0.5 \leq \Delta d_{11} + 0.5d_{11} < d + d'$	$d_{11} < (1 - 4d_s)k$	$\Delta i_{L,j} = nU_2(1 - d - d' - 0.5d_{11})T_S / (L + L_{lk})$
k	$d + d' - 0.5 \leq \Delta d_{11} < 0.5, 0.5 \leq \Delta d_{11} + 0.5d_{11} < d + d'$	$d_{11} < (1 - 4d_s)k$	$\Delta i_{L,k} = nU_2(\Delta d_{11} - d - d' + 0.5)T_S / (L + L_{lk})$
l	$d + d' - 0.5 \leq \Delta d_{11} < 0.5, d + d' \leq \Delta d_{11} + 0.5d_{11} < 1$	$d_{11} \geq nU_2 / (nU_2 + U_1)$	$\Delta i_{L,l} = nU_2(0.5 - 0.5d_{11})T_S / (L + L_{lk})$

From Fig. 7(a) and (b), the current ripple expressions are

$$\Delta i_{L,f} = U_1(d + d' - 0.5)T_S / L \quad (37)$$

$$\Delta i_{L,l} = nU_2(1 - 0.5d_{11})T_S / (L + L_{lk}). \quad (38)$$

For sake of comparison, the edge moment conditions of  $G_{S11}$ , action width conditions of  $G_{S11}$  and current ripple expression of these cases above when  $1 < k < k_{\text{crit}}$  and  $k \leq 1$  are listed in Tables I and II, respectively.

From Table I, for cases b, c, and e, when  $1 < k < k_{\text{crit}}$ , no matter how much power the converter output, as long as the action position of  $G_{S11}$  varies, these three cases can all occur. But for cases a and f, these two cases may only occur within the partial power range. The current ripple in each case is compared as follows.

Compare cases b with c, because the conditions of the edge moment of case c is  $\Delta d_{11} + 0.5d_{11} \geq 0.5$ , by substituting it into (32),  $\Delta i_{L,c} \leq \Delta i_{L,b}$  can be obtained.

Compare case e with case c, because the conditions of the edge moment of case c is  $d + d' - 0.5 \leq \Delta d_{11}$ , by substituting it into (32),  $\Delta i_{L,c} \leq \Delta i_{L,e}$  can be obtained.

Compare case f with case c, because  $d_{11} < 1$ ,  $\Delta i_{L,c} < \Delta i_{L,f}$  can be obtained easily.

Compare case a with case c, because  $d + d' < 1$ ,  $\Delta i_{L,c} < \Delta i_{L,a}$  can be obtained easily. In summary, the current ripple of case c is the minimum, and when  $1 < k < k_{\text{crit}}$ , this case can occur in the entire power range.

Similar conclusions can be obtained by comparing the current ripple in Table II in the same way. In summary, the current ripple of case j is the minimum when  $k \leq 1$  and this case can occur in the entire power range.

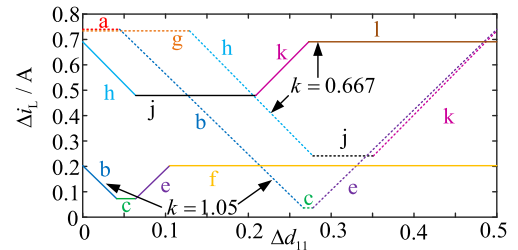


Fig. 8 Relation curve of current ripple of energy storage inductor with phase transformation of  $G_{S11}$ .

The curves of  $\Delta i_L$  as a function of  $\Delta d_{11}$  under various cases with a constant  $k$  are drawn and shown in Fig. 8. From Fig. 8, the current ripples corresponding to cases c and j are the smallest.

According to the abovementioned analysis, when  $1 < k < k_{\text{crit}}$ , the action position of  $G_{S11}$  is set according to case c. When  $k \leq 1$ , the action position of  $G_{S11}$  is set according to case j. Furthermore, according to the operating waveforms of the two cases shown in Fig. 7, the action position of  $G_{S11}$  should be as far as possible across the normal power transfer region in the switching cycle.

### C. Implementation of Optimized Modulation Strategy

From the principle of the proposed modulation strategy, the short-through time  $d$ , the turn-ON time of  $S_{11}$  ( $d_{11}$ ) and the action position of  $G_{S11}$  should be tuned in real time to obtain a smaller average inductor current and smaller current ripple under the premise of obtaining the required voltage conversion ratio. This article presents an implementation scheme based on the dual modulation waves and single carrier wave, as shown in Fig. 9. According to the principle of the converter, an entire

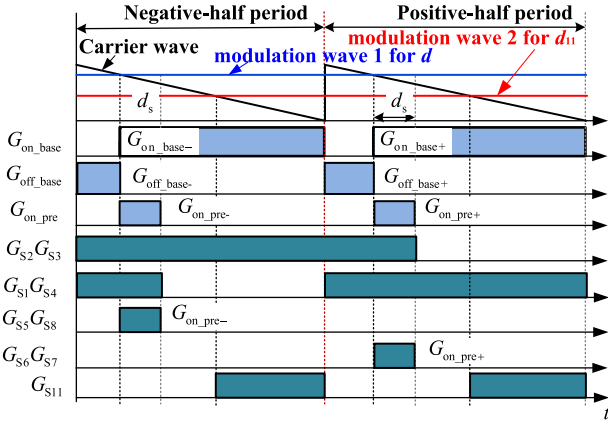


Fig. 9. Schematic of implementation of proposed modulation strategy.

control cycle contains two carrier periods, which are used to generate the positive and negative half-cycle transformer currents, respectively. The first modulation wave is used to generate the control signals of  $S_{1-8}$ , and the second modulation wave is used to generate the control signals of  $S_{11}$ . In the negative-half cycle of transformer current,  $S_2$  and  $S_3$  keep on state, and modulation wave 1 equals  $M_1 = (d - 0.5)T_S$ . When the carrier is greater than  $M_1$ , there is  $G_{on\_base} = 1$ ,  $G_{off\_base} = 0$ , otherwise  $G_{on\_base} = 0$ ,  $G_{off\_base} = 1$ . In addition, a control signal  $G_{on\_pre}$  is set, from the moment when the carrier wave is greater than  $M_1$ ,  $G_{on\_pre} = 1$ , and after time  $d_s T_S$ ,  $G_{on\_pre} = 0$ . Then, there is the following relationship between the control signals of  $S_{1-8}$  and  $G_{on\_base}$ ,  $G_{off\_base}$ , and  $G_{on\_pre}$ .

$$G_{S1,S4} = G_{off\_base} || G_{on\_pre}, G_{S5,S8} = G_{on\_pre}. \quad (39)$$

Similarly, during the positive-half cycle of the transformer current,  $S_1$  and  $S_4$  keep on state, there is the following relationship between the control signal of  $S_{1-8}$  and  $G_{on\_base}$ ,  $G_{off\_base}$ , and  $G_{on\_pre}$

$$G_{S2,S3} = G_{off\_base} || G_{on\_pre}, G_{S5,S8} = G_{on\_pre}. \quad (40)$$

As for the generation process of  $G_{S11}$ , from the above analysis, the conduction interval of  $S_{11}$  should be kept in the normal power transfer region. Therefore, a simple method is to align the falling edge of  $G_{S11}$  to the starting moment of the carrier wave. Thus the modulation wave 2 can be set as  $M_2 = d_{11} T_S$ . When the carrier wave is greater than  $M_2$ , there is  $G_{S11} = 0$ , otherwise  $G_{S11} = 1$ .

#### IV. EXPERIMENTAL VERIFICATION AND DISCUSSION

In order to verify the basic performance of the proposed B3CFIDC and the optimized modulation strategy, an experimental platform based on DSP+FPGA is built, as shown in Fig. 10. The two dc sides of the B3CFIDC are connected with a dc voltage source and an adjustable resistor as the load, respectively. The experimental parameters are listed in Table III. All experiments were carried out under open-loop conditions.

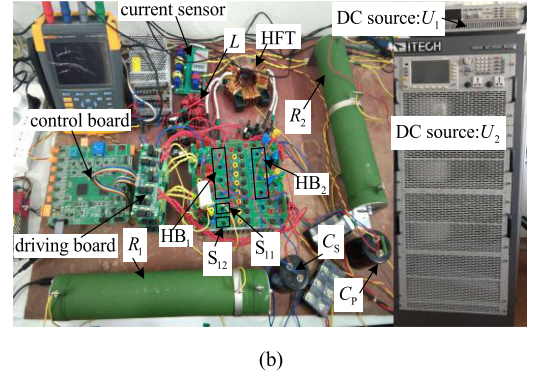
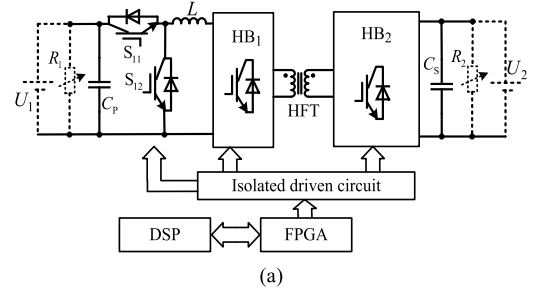


Fig. 10. Schematic of (a) experimental platform and (b) photograph.

TABLE III  
VALUES OF EXPERIMENTAL PLATFORM PARAMETERS

Parameter	Value	Parameter	Value
$U_2$	200 V	$d_s$	0.025
Range of $U_1$	50 V-150 V	$k_{crit}$	1.111
$n$	0.5	$I_{L\_rate}$	8 A
$L_{lk}$	5 $\mu$ H	$\Delta I_{lk}$	2 A
$T_s$ ( $f_s$ )	20 $\mu$ s (50 kHz)	$L$	600 $\mu$ H
Part number of power switch		IGBT, K30T60	

First, the buck and boost operation functions of the proposed topology under forward mode and the correctness of the derived voltage conversion ratio expression are verified. The optimal control scheme is adopted for the modulation strategy. In order to verify the performance is a wide voltage conversion range,  $U_1$  is set to 50 V and 150 V, respectively. Another dc side is connected with a pure resistor as a load, and the expected value of  $U_2$  is set to 200 V. Furthermore, two different reference powers are set to verify the proposed topology and theoretical analysis under boost and buck operation conditions and under different power conditions.

First,  $U_1$  is set to 150 V and the expected power is  $P = 437$  W. The resistance  $R_2$  is adjusted to the corresponding value, so that when the output power equals the reference power, there will be  $U_2 = 200$  V in theory. Because it is in buck operation,  $d$  should be the minimum value, which is  $d = 0.55$ , and  $d_{11}$  should be  $d_{11} = 0.5835$  calculated by the voltage conversion ratio expression.

Similarly,  $U_1$  is further set to 50 V and the expected power is  $P = 300$  W and the expected  $U_2$  is still 200 V. The system

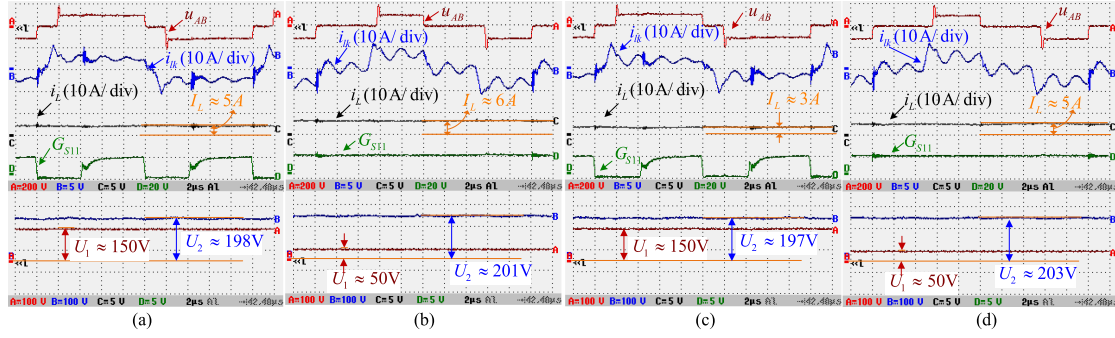


Fig. 11. Experimental results of forward mode using optimized modulation. (a)  $U_1 = 150$  V and  $P = 437$  W and  $d = 0.55$ ,  $d_{11} = 0.5835$ . (b)  $U_1 = 50$  V and  $P = 300$  W and  $d = 0.74$ ,  $d_{11} = 1$ . (c)  $U_1 = 150$  V and  $P = 260$  W and  $d = 0.55$ ,  $d_{11} = 0.5766$ . (d)  $U_1 = 50$  V and  $P = 250$  W and  $d = 0.737$ ,  $d_{11} = 1$ .

is under boost conditions.  $d = 0.74$ ,  $d_{11} = 1$  can be calculated from the set voltages and power. Furthermore,  $U_1$  is set to 150 V and the expected power is set as

$P = 260$  W,  $d = 0.55$ ,  $d_{11} = 0.5766$  can be calculated. And  $U_1$  is set to 50 V, the expected power is set as  $d = 0.737$ ,  $d_{11} = 1$ ,  $P = 250$  W can be calculated.

The corresponding experimental results are shown in Fig. 11(a)–(d). In the four cases mentioned above, the average value of  $i_L$  remains unchanged, indicating that the voltage–second balance is obtained, while  $U_2$  is approximately equal to the expected value of 200 V, indicating that the proposed topology has realized the buck and boost operation, and the derived voltage conversion ratio expression is correct.

Furthermore, in the four cases, the waveforms of  $u_{ab}$  contain only some transient resonant voltage overshoot and there is no significant voltage spike inside. It verifies the ability of the proposed modulation strategy to eliminate the voltage spike. The waveforms of  $i_{lk}$  are basically consistent with the theoretical waveforms. The reason of existing the oscillations in the transformer current is that the junction capacitor of the power switch resonates with the leakage inductor.

Second, the performance of the optimized control rule of  $d$  and  $d_{11}$  to reduce the average inductor current is verified. Taking the experimental results of Fig. 11(a) and (b) as reference, and on the premise of the same input and output voltage and power, two groups of different nonoptimal values of  $d$  and  $d_{11}$  were set as follows:  $d = 0.722$ ,  $d_{11} = 0.364$ , and  $d = 0.805$ ,  $d_{11} = 0.75$ . The experimental results are shown in Fig. 12(a) and (b). In the optimization scheme,  $I_L$  equals 5 A and 6 A, respectively. For the cases in Fig. 12,  $I_L$  equals to 8 A, which is much larger than the optimal cases in Fig. 11. The reasons are described as follows. According to the expression of voltage conversion ratio, for a certain  $k$ ,  $d$  should be set as small as possible while  $d_{11}$  should be set as large as possible to reduce the average inductor current. The values of  $d_{11}$  in Fig. 12 are less than those in Fig. 11 while the values of  $d$  in Fig. 12 are larger than those in Fig. 11. Reducing  $d_{11}$  means the period of outputting power of  $U_1$  decreases in a control cycle. Increasing  $d$  means the effective period of transferring power from HB<sub>1</sub> to HB<sub>2</sub> decreases. The both factors lead  $I_L$  needs to be larger with the same  $P$ . The experimental results show that the proposed control rule of  $d$  and  $d_{11}$  achieves the operation with the minimum inductor current.

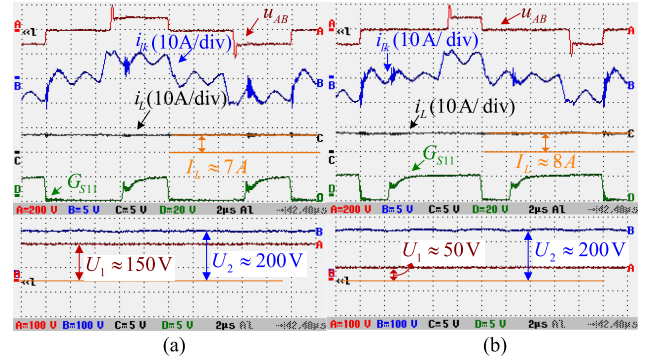


Fig. 12. Experimental results using nonoptimized  $d$  and  $d_{11}$ . (a)  $U_1 = 150$  V and  $P = 437$  W and  $d = 0.722$ ,  $d_{11} = 0.364$ . (b)  $U_1 = 50$  V and  $P = 300$  W and  $d = 0.805$ ,  $d_{11} = 0.75$ .

The third, the optimization scheme of action position of  $G_{S11}$  is verified. The comparison is performed under the same input, output voltages, and transfer power. The inductor current ripple  $\Delta i_L$  and other key experimental waveforms of the optimized scheme are shown in Fig. 13(a). In addition, cases k and l are selected as the compared objects. For case k, the rising edge of  $G_{S11}$  is lags 5.4  $\mu$ s ( $\Delta d_{11} = 0.27$ ) behind the start moment (the rising edge of  $G_{S2}$ ).

The corresponding experimental results are shown in Fig. 13(b). For case l, the rising edge of  $G_{S11}$  lags 9.2  $\mu$ s ( $\Delta d_{11} = 0.46$ ) behind the starting moment. The corresponding experimental results are shown in Fig. 13(c). From these figures, under the optimized scheme,  $\Delta i_L \approx 0.45$  A, however,  $\Delta i_L \approx 0.64$  A in case k and  $\Delta i_L \approx 0.7$  A in case l. The experimental results show that the inductor current ripple under the optimized scheme is much smaller than those under the other two cases, which shows that the proposed optimization scheme for the position of  $G_{S11}$  has obtained a smaller inductance current ripple.

Finally, the performance of the proposed topology in reverse mode is experimentally verified. In this mode,  $S_{11}$  keeps OFF state because the current flows through its body diode. In the boost mode,  $S_{12}$  is controlled with the pulsewidth modulation-control signal of  $G_{S12}$ .  $S_{12}$  keeps OFF in the buck mode. In this mode,  $U_2$  is the source and it is set as 200 V. The desired  $U_1$  are

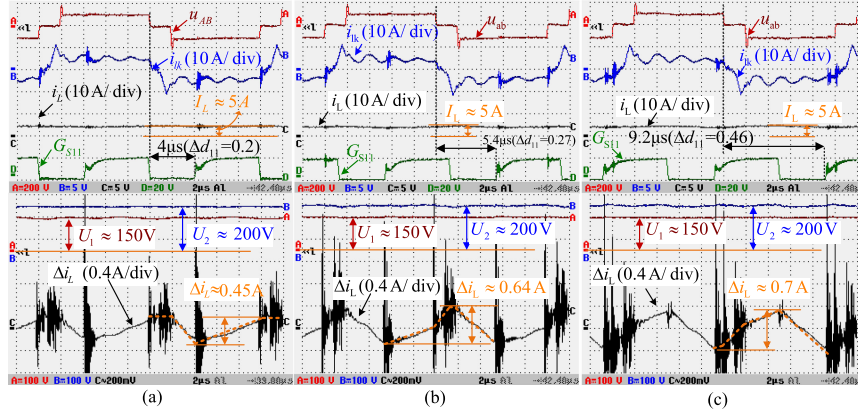


Fig. 13. Experimental results with different action positions of  $G_{S11}$ . (a) Optimal case. (b) Case k. (c) Case l.

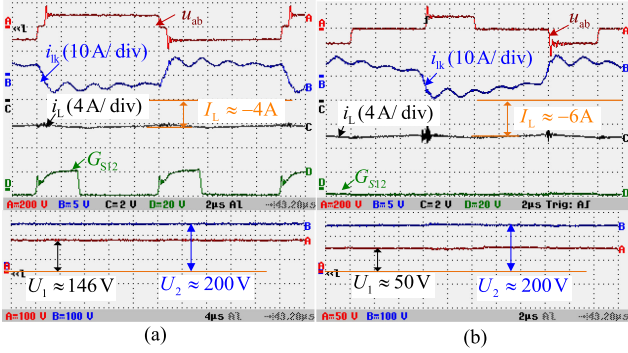


Fig. 14. Experimental results of proposed topology under reverse mode. (a)  $U_1 = 146$  V and  $P = 410$  W. (b)  $U_1 = 50$  V and  $P = 300$  W.

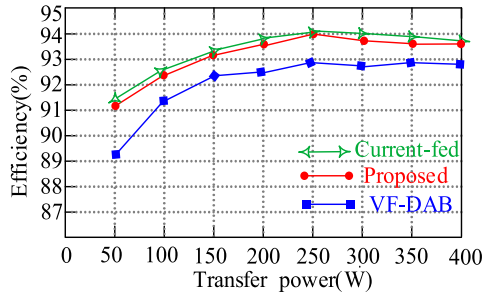


Fig. 15 Efficiency of three isolated dc-dc converter.

150 V and 50 V, and the desired power is 437 W and 300 W, respectively. The corresponding experimental waveforms are shown in Fig. 14. From Fig. 14, the actual  $U_1$  in both cases are approximately equal to the expected values, thus realizing the reverse buck and boost operation and power control.

In addition, the efficiency of the proposed topology is measured at the input voltage of 50 V and the output voltage of 200 V by experiment. The efficiency of the proposed topology is compared with that of VF-DAB and boost-current-fed converter [19], as shown in Fig. 15. Because the proposed topology has more conduction loss on the switch  $S_{11}$  than the boost-current-fed converter, its efficiency is slightly lower. Because the current

TABLE IV  
DATA OF SEVERAL BIDIRECTIONAL DC-DC CONVERTERS

	DAB	Resonant	Current-fed	Proposed
Voltage conv. range	Buck-boost, wide	Buck-boost, wide	Boost, narrow	Buck-boost, wide
Current stress ratio	2	1.6	1	1
Number of switch	8	8	8	10
Number of equivalent switch	16	12.8	8	10
Cost ratio of switch	1.6	1.28	0.8	1

stress of the proposed topology is much smaller than that of VF-DAB, its conduction loss is less than that of VF-DAB, and its efficiency is slightly higher than that of VF-DAB.

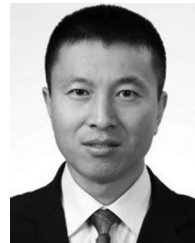
Furthermore, in order to further verify the advantages of the proposed topology in terms of the voltage conversion range, current stress and cost, it is compared with the typical voltage-type DAB-based dc-dc converter, LC series resonant dc-dc converter, and the boost CFIDC in [19]. The corresponding comparative data are shown in Table IV. According to the existing literature, the ratio of peak to average current in DAB converter is about 2, the ratio of peak to average current in LC resonant converter is 1.6, and the ratio of peak to average current in current-fed converter is about 1. The number of equivalent power switches is defined as the product of the current stress ratio and the actual number of switching devices. Under the same transfer power, in order to simplify the comparison, the number of equivalent power switches and cost ratio are calculated according to the approximately proportional relationship of the current rating. From Table IV, at the same power, the number of equivalent power switches of the proposed topology is reduced by 50% and 28% compared with DAB and LC resonant dc-dc converters, respectively. The voltage conversion range is significantly extended compared with the boost current-fed dc-dc converter. Therefore, the proposed topology has excellent comprehensive performance.

## V. CONCLUSION

The proposed B3CFIDC realizes the bidirectional boost and buck operation. The proposed modulation strategy and the cooperative control scheme of shoot-through duty cycle and buck duty cycle achieve a low average inductor current and current ripple and the voltage spike is avoided in the entire operation range. The comparison between the proposed topology and several typical dc–dc converters shows that the proposed topology has lower cost ratio under the premise of realizing the bidirectional boost and buck operation. The cost of the proposed topology is 40% lower than that of the DAB dc–dc converter and 22% lower than that of the resonant converter, respectively. The proposed topology has better practical value.

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**Fengjiang Wu** (M'15–SM'17) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology (HIT), Harbin, China, in 2002, 2004, and 2007, respectively.

Since 2007, he has been with the Department of Electrical Engineering, HIT, where he is currently an Associate Professor. He has authored or coauthored more than 40 top-tier journal papers. His research interests include renewable energy generation, solid state transformer, and microgrid.

Dr. Wu is currently an Associate Editor for the *IEEE ACCESS* and *IET Power Electronics*.



**Shuai Fan** received the B.S. degree in electrical engineering in 2018 from Zhengzhou University, Zhengzhou, China. He is currently working toward the M.S. degree in electrical engineering with the Harbin Institute of Technology (HIT), Harbin, China.

His research interests include the field of dc–dc power conversion.



**Xiaoguang Li** (S'19) received the B.S. degree in electrical engineering in 2015 from the Harbin Institute of Technology, Harbin, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include the field of grid-connected inverters for renewable energy generation system and microgrid.

**Suhua Luo**, photograph and biography not available at the time of publication.