

# Active Gate Delay Time Control of Si/SiC Hybrid Switch for Junction Temperature Balance Over a Wide Power Range

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**Abstract**—The optimal gate delay time control between the two internal devices to achieve excellent electrical and thermal performance of the Si/SiC hybrid switch is considerably affected by several factors and requires careful adjustment to suit the different operation conditions of power converters. However, the conventional gate control solution for the hybrid switch applies a fixed delay time to achieve the minimum switching loss at a specific load current, resulting in disparities in junction temperature of internal devices over a wide load range. This effectively reduces the safe operating area by risking one internal switch subjected to overrated junction temperature in a wide range operation with regard to power handling condition. To avoid such a serious risk of reliability degradation or thermal breakdown, a novel active gate delay time control strategy based on the electro-thermal coupling loss model is proposed. The gate delay time was dynamically adjusted and optimized according to the operation conditions of power converters so that the operation junction temperature difference of the two internal devices can be minimized. Experimental results demonstrate that the junction temperature of the hybrid switch decreases by 20 °C at 8-kW load condition and its maximum power handling capability increases by 18%, without compromising the power converter's efficiency in a 20 kHz Si/SiC hybrid switch-based dc/dc buck converter compared with the conventional approach.

**Index Terms**—Control, hybrid switch, insulated-gate bipolar transistor (IGBT), junction temperature, SiC MOSFET.

## I. INTRODUCTION

SiC power MOSFETs have been the center of attention in the race to medium-voltage device innovation to displace silicon insulated-gate bipolar transistors (IGBTs) because of low specific on-resistance, fast switching speed, and high switching

frequency capability in recent years [1]–[4]. However, their significantly high cost/ampere (\$/A) is the major roadblocks for the SiC MOSFET's widespread employment in the commercial mainstream power electronics systems [5], [6]. In recent years, the Si/SiC hybrid switch of paralleling a high-current Si IGBT and a low-current SiC MOSFET was reported to achieve an improved cost/performance tradeoff [7]–[9], which is a promising solution to address the high-cost issue of SiC devices [10]–[13].

The Si/SiC hybrid switch needs optimal gate delay time control between its two internal switches to achieve improved electrical and thermal performance because its gate configuration is different from conventional discrete power semiconductor devices [14]–[21]. When the internal IGBT's turn-OFF is prior to SiC MOSFET's turn-OFF for an appropriate gate delay time, zero voltage switching (ZVS) OFF operation of the internal IGBT and the minimum total turn-OFF switching loss of the hybrid switch can be achieved [14]–[17]. When the IGBT's turn-ON is prior to SiC MOSFET's turn-ON for a very short gate delay time, the hybrid switch can achieve a minimum turn-ON switching loss because of the high di/dt during the switching ON transient [18]–[19]. To improve the over current capability of the hybrid switch, the main IGBT turn-ON shortly prior and turn-OFF shortly after the auxiliary SiC MOSFET for a carefully chosen gate control delay time under the heavy load condition is proposed in [20], [21]. In [22], the gate control delay time strongly influences the junction temperatures of the two internal devices in converter applications. And even a minor variation of the gate control delay time would induce significant fluctuation of their junction temperatures, which may result in a severe junction unbalance between the two internal devices or a serious risk of thermal breakdown of one internal devices of the hybrid switch under heavy-load conditions [23]–[26].

The optimal gate control delay time of the hybrid switch is influenced by several limiting factors, such as the internal switches' junction temperatures [22], sizing selection [13], packaging choice, and parasitic inductance [19], etc. Moreover, it also varies with operation conditions of power converters, such as the load condition and ambient temperature of the hybrid switch-based converter [20], [21]. The main reason is that adjustment of the gate delay time control can change the distribution of power losses and junction temperatures of the IGBT and SiC MOSFET inside the hybrid switch, and achieve

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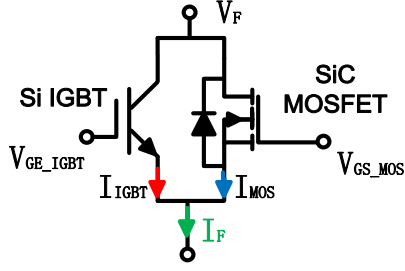


Fig. 1. Schematic of a hybrid switch.

the minimum total power loss or junction temperatures under different operation conditions [22]. However, any gate delay time control determined for the specified load current only provides a sole and fixed value in these previous works, which cannot adapt to the requirement of different operating conditions in a real power converter operation and therefore put the device at risk of over temperature or temperature dependent catastrophic failures.

In order to solve this problem, an active gate delay time control strategy with real-time optimized gate delay time adjustment based on the electro-thermal coupling power loss model of the hybrid switch is proposed. The control algorithm aims to achieve the minimum operating junction temperature difference of the hybrid switch's two internal devices without compromising the power conversion efficiency within a wide load condition. The thermoelectric coupling power loss model of the hybrid switch for the dc/dc buck converter is developed and analyzed in Section II. In Section III, the active gate delay time control strategy is introduced. Then the experimental results using the conventional fixed gate delay time control and the active gate delay time control are compared and analyzed. Section IV concludes the article.

## II. ELECTRO-THERMAL COUPLING POWER LOSS OF Si/SiC HYBRID SWITCH

The basic schematic of the Si/SiC hybrid switch is shown in Fig. 1. The cost-effective Si/SiC hybrid switch combines the advantages of the high current Si IGBT and the low current SiC MOSFET, and offers smaller conduction loss because most of the load current flows through the SiC MOSFET at a low current level and the Si IGBT at a high current level.

The specific gate control pattern is preferred for the hybrid switch to reduce the switching loss of the hybrid switch, as shown in Fig. 2.  $T_{on\_delay}$  and  $T_{off\_delay}$  are the turn-ON gate delay time and turn-OFF gate delay time between the IGBT and SiC MOSFET inside the hybrid switch, respectively. The ZVS OFF operation of the IGBT is achieved by turning OFF the IGBT prior to the SiC MOSFET, which can greatly reduce the IGBT's turn-OFF switching loss induced by tail current. Because the IGBT's turn-ON speed is slower than that of the SiC MOSFET, the SiC MOSFET undertakes the hard switching ON action and the IGBT is ZVS switching ON when the gate turn-ON delay time of the hybrid switch is zero.

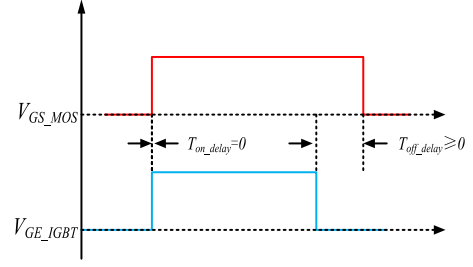


Fig. 2. Gate control pattern of the hybrid switch.

In order to achieve the real-time optimized gate turn-OFF delay time adjustment varying with the load conditions of the hybrid switch converter, the Si/SiC hybrid switch's electro-thermal coupling power loss model associated with its gate turn-OFF delay time for the dc/dc buck converter applications is built and analyzed in this article.

### A. Conduction Loss of the Hybrid Switch

When the forward voltage drop of the hybrid switch is smaller than the knee voltage of the Si IGBT, the forward current fully flows through the SiC MOSFET, and the critical forward current can be derived as

$$I_{MOS} = I_{knee} = \frac{V_{knee}}{R_{ds}} \quad (1)$$

where  $V_{knee}$  is the knee voltage of the IGBT,  $R_{ds}$  is the specific ON resistance of the SiC MOSFET,  $I_{knee}$  is the critical forward current of the SiC MOSFET when the forward voltage drop of the hybrid switch is the  $V_{knee}$  voltage. When the forward voltage of the hybrid switch larger than the knee voltage of the IGBT, the forward current flows through both the SiC MOSFET and the IGBT. Approximating the ON-state characteristic of the IGBT with an equivalent straight line with an intercept of  $V_{knee}$  and a slope of  $R_{ce}$ , the current distribution between the SiC MOSFET and the IGBT can be derived as

$$I_{MOS} = \frac{R_{ce}}{R_{ce} + R_{ds}} I_F + \frac{V_{knee}}{R_{ce} + R_{ds}} \quad (2)$$

$$I_{IGBT} = \frac{R_{ds}}{R_{ce} + R_{ds}} I_F - \frac{V_{knee}}{R_{ce} + R_{ds}} \quad (3)$$

where  $R_{ce}$  is the equivalent differential ON-state resistance of the IGBT,  $I_F$  is the total forward current of the hybrid switch. Considering the temperature coefficient of the ON-state characteristics of the IGBT and SiC MOSFET,  $V_{knee}$  and  $R_{ce}$  of the IGBT, and  $R_{ds}$  of the SiC MOSFET are functions of the junction temperature, respectively, as given by

$$R_{ds}(T_{j\_MOS}) = R_{ds}(25^\circ\text{C}) + T_{CR\_MOS}(T_{j\_MOS} - 25^\circ\text{C}) \quad (4)$$

$$R_{ce}(T_{j\_IGBT}) = R_{ce}(25^\circ\text{C}) + T_{CR\_IGBT}(T_{j\_IGBT} - 25^\circ\text{C}) \quad (5)$$

$$V_{knee}(T_{j\_IGBT}) = V_{knee}(25^\circ\text{C}) + T_{CV\_IGBT}(T_{j\_IGBT} - 25^\circ\text{C}) \quad (6)$$

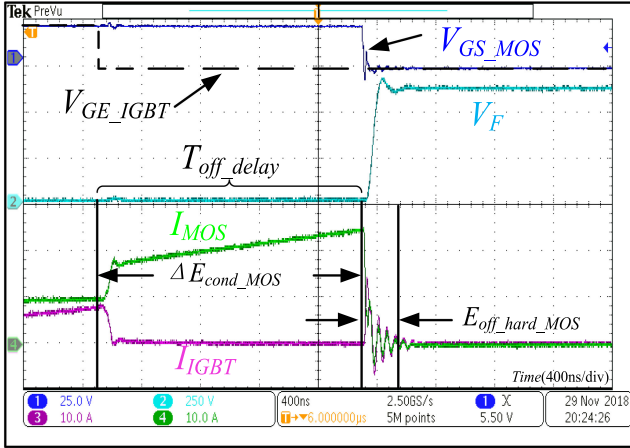


Fig. 3. Turn-OFF process of Si/SiC hybrid switch.

where  $T_{j\_MOS}$  and  $T_{j\_IGBT}$  are the junction temperatures of the SiC MOSFET and the IGBT, respectively.  $T_{CR\_IGBT}$  and  $T_{CV\_IGBT}$  are the temperature coefficients of the IGBT's knee voltage and equivalent ON-state resistance, respectively, and  $T_{CR\_MOS}$  is the temperature coefficient of the SiC MOSFET's specific ON resistance. The temperature coefficient of the ON-state characteristic can be calculated from the 25 °C and the hot values from the datasheets of the IGBT and SiC MOSFET, e.g., for  $T_{CR\_MOS}$  applies

$$T_{CR\_MOS} = \frac{R_{ds}(150^\circ\text{C}) - R_{ds}(25^\circ\text{C})}{150^\circ\text{C} - 25^\circ\text{C}}. \quad (7)$$

Therefore, the conduction loss of the SiC MOSFET and the IGBT at a given operating point can be derived as

$$E_{\text{cond\_MOS}}(I_F, T_{j\_MOS}) = \begin{cases} I_{\text{MOS}}^2 \cdot R_{ds}; & I_F < I_{\text{knee}} \\ \left( \frac{R_{ce}}{R_{ce} + R_{ds}} I_F + \frac{V_{\text{knee}}}{R_{ce} + R_{ds}} \right)^2 \cdot R_{ds}; & I_F \geq I_{\text{knee}} \end{cases} \quad (8)$$

$$E_{\text{cond\_IGBT}}(I_F, T_{j\_IGBT}) = \begin{cases} 0; & I_F < I_{\text{knee}} \\ \left( \frac{R_{ds}}{R_{ce} + R_{ds}} I_F - \frac{V_{\text{knee}}}{R_{ce} + R_{ds}} \right) \times \left[ V_{\text{knee}} + \left( \frac{R_{ds}}{R_{ce} + R_{ds}} I_F - \frac{V_{\text{knee}}}{R_{ce} + R_{ds}} \right) \cdot R_{ce} \right]; & I_F \geq I_{\text{knee}}. \end{cases} \quad (9)$$

### B. Switching Loss of the Hybrid Switch

The IGBT's turn-OFF prior to the SiC MOSFET is preferred to achieve the ZVS operation of the IGBT inside the hybrid switch. The typical waveforms of the turn-OFF process of the hybrid switch consisting of a 1200 V/25 A IGBT and a 1200 V/12.5 A SiC MOSFET at  $T_{\text{off\_delay}} = 1.6 \mu\text{s}$  are shown in Fig. 3. When the IGBT is turned OFF prior to the SiC MOSFET, the SiC MOSFET is conducted 100% of the load current during the short gate turn-OFF delay time, and then undertakes hard switching OFF operation.

The total turn-OFF switching loss ( $E_{\text{off\_MOS}}$ ) of the SiC MOSFET consists of the hard switching OFF loss ( $E_{\text{off\_hard\_MOS}}$ ) and the additional conduction loss ( $\Delta E_{\text{cond\_MOS}}$ ) during the short gate turn-OFF delay time, which can be expressed as

$$E_{\text{off\_MOS}} = E_{\text{off\_hard\_MOS}} + \Delta E_{\text{cond\_MOS}}. \quad (10)$$

The hard switching OFF loss ( $E_{\text{off\_hard\_MOS}}$ ) of the SiC MOSFET is related to the forward current, dc-link voltage, and junction temperature in power converter applications. An empirical formula of the turn-OFF switching loss of the SiC MOSFET based on a nonlinear approximation is given as [26]

$$E_{\text{off\_hard\_MOS}}(I_F, T_j) = E_{\text{off\_MOS\_ref}} \left( \frac{I_F}{I_{\text{ref}}} \right)^{a_{I\_MOS}} \times \left( \frac{V_{\text{DC}}}{V_{\text{ref}}} \right)^{b_{V\_MOS}} \times (1 + T_{CS\_off\_MOS}(T_{j\_MOS} - T_{j\_ref})) \quad (11)$$

where  $V_{\text{DC}}$  is the dc-link voltage of the converter.  $I_{\text{ref}}$ ,  $V_{\text{ref}}$ , and  $T_{j\_ref}$  are the reference forward current, dc-link voltage, and SiC MOSFET's junction temperature taken from the datasheet.  $a_{I\_MOS}$  and  $b_{V\_MOS}$  are the exponents for the current dependency and dc-link voltage dependency of the SiC MOSFET's switching OFF loss, respectively.  $T_{cs\_off\_MOS}$  is the temperature coefficient of the SiC MOSFET's switching OFF loss.  $E_{\text{off\_MOS\_ref}}$  is the turn-OFF switching loss of the SiC MOSFET at a specific operating condition in the datasheet.

As show in Fig. 3, the SiC MOSFET undertakes 100% of the load current during the gate turn-OFF delay time. The additional conduction loss  $\Delta E_{\text{cond\_MOS}}$  during the gate turn-OFF delay time could be modeled as a linear function of the gate turn-OFF delay time  $T_{\text{off\_delay}}$  at the certain forward current condition, which is expressed in the following:

$$\Delta E_{\text{cond\_MOS}}(I_F, T_{j\_MOS}) = [I_F^2 \cdot R_{ds}(T_{j\_MOS})] \cdot T_{\text{off\_delay}}. \quad (12)$$

When the turn-OFF gate signal is applied, the MOS channel current in IGBT rapidly decreases to zero and all load current is commutated to the SiC MOSFET. The IGBT is turned OFF without undertaking high voltage since the SiC MOSFET is still conducted, as shown in Fig. 3. The large amount of stored charge in N-base region of the IGBT decreases exponentially due to the minority carrier recombination during the gate turn-OFF delay time [10]. The turn-OFF switching loss of the IGBT can be modeled as

$$E_{\text{off\_IGBT}} = (E_{\text{off\_hard\_IGBT}} - E_{\text{res}}) \cdot e^{-\tau \cdot T_{\text{off\_delay}}} + E_{\text{res}} \quad (13)$$

where  $E_{\text{res}}$  is the residual turn-OFF switching loss of the IGBT, and  $\tau$  is the exponential time constant for the dependency of the IGBT's switching OFF loss on the gate turn-OFF delay time, respectively. Their values can be obtained from the double-pulse test at the same condition with the converter applications. Fig. 4 shows the typical dependency of the IGBT's turn-OFF switching loss on its gate signal's turn-OFF delay time.

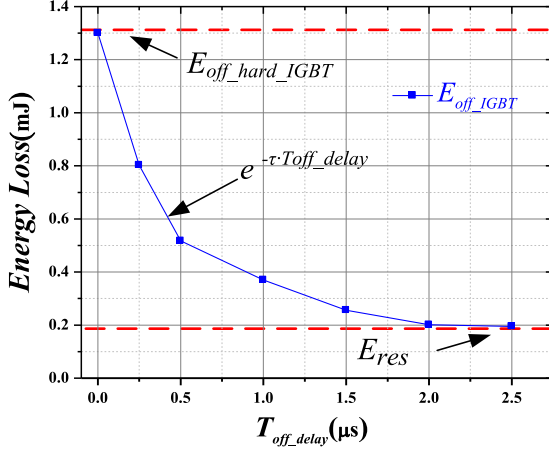


Fig. 4. Dependency of the IGBT's turn-OFF switching loss on its gate signal's turn-OFF delay time.

The  $E_{res}$  is caused by which the IGBT has to undertake the dc-link voltage and remove the remaining plasma when the SiC MOSFET is hard switching OFF [27]. The magnitude of  $E_{res}$  is mainly influenced by the dc-link voltage. When the gate turn-OFF delay time between the IGBT and the SiC MOSFET is long enough, the magnitude of  $E_{res}$  is almost constant at the certain dc-link voltage.  $E_{off\_hard\_IGBT}$  is the hard switching OFF loss of the IGBT at a certain forward current. When the gate turn-OFF delay time is zero or negative, the IGBT undertakes the hard switching OFF operation, and the SiC MOSFET is ZVS switching OFF. The hard switching OFF loss of the IGBT can be extracted from the IGBT manufacture's datasheet with the nonlinear approximation as shown in the following:

$$E_{off\_hard\_IGBT}(I_F, T_j) = E_{off\_hard\_IGBT\_ref} \left( \frac{I_F}{I_{ref}} \right)^{a_{I\_IGBT}} \times \left( \frac{V_{DC}}{V_{ref}} \right)^{b_{V\_IGBT}} (1 + T_{CS\_off\_IGBT} \times (T_{j\_IGBT} - T_{j\_ref})) \quad (14)$$

where  $a_{I\_IGBT}$  and  $b_{V\_IGBT}$  are the coefficients for the power dependency of the IGBT's switching OFF loss on the current dependency and dc-link voltage, respectively.  $T_{CS\_off\_IGBT}$  is the temperature coefficient of the IGBT's switching OFF loss.  $E_{off\_hard\_IGBT\_ref}$  is the turn-OFF switching loss of the IGBT extracted from the datasheet at the specific operating condition.

The gate turn-ON delay time between the SiC MOSFET and the IGBT inside the hybrid switch is selected to be zero in order to simplify the loss model of the hybrid switch. The measured waveforms of the turn-ON process of the hybrid switch at  $T_{on\_delay} = 0 \mu s$  are shown in Fig. 5.

Because the IGBT's turn-ON speed is slower than that of SiC MOSFET, the SiC MOSFET undertakes the hard switching ON action, and the IGBT is ZCS switching ON when the gate turn-ON delay time of the hybrid switch is zero. The hard switching ON loss of the SiC MOSFET can be extracted from the manufacture's datasheet with the nonlinear approximation

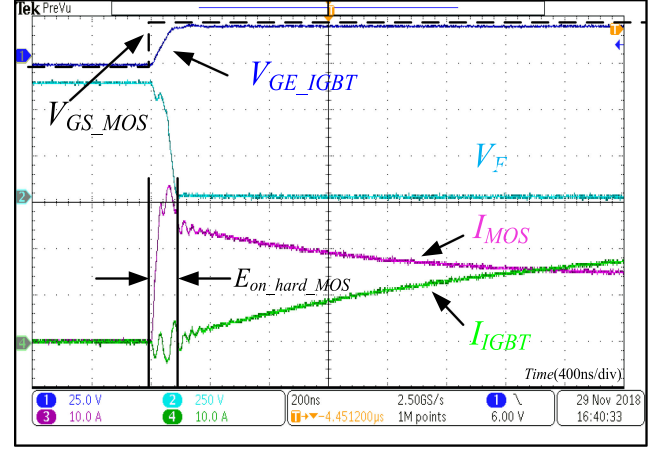


Fig. 5. Turn-ON process of Si/SiC hybrid switch.

as shown in the following:

$$E_{on\_MOS}(I_F, T_j) = E_{on\_MOS\_ref} \left( \frac{I_F}{I_{ref}} \right)^{c_{I\_MOS}} \left( \frac{V_{DC}}{V_{ref}} \right)^{d_{V\_MOS}} \times (1 + T_{CS\_on\_MOS}(T_{j\_MOS} - T_{j\_ref})) \quad (15)$$

where  $c_{I\_MOS}$  and  $d_{V\_MOS}$  are the coefficients for the power dependency of the SiC MOSFET's turn-ON switching loss on the load current and dc-link voltage, respectively.  $T_{CS\_on\_MOS}$  is the temperature coefficient of the SiC MOSFET's switching ON loss.  $E_{on\_MOS\_ref}$  is the switching ON loss of the SiC MOSFET taken from the datasheet at the reference operating point.

Therefore, neglecting the load current ripple, the total power loss of the SiC MOSFET, and the IGBT inside the hybrid switch could be expressed as

$$P_{loss\_MOS}(I_F, T_{j\_MOS}) = (D - f_{sw} \cdot T_{off\_delay}) E_{cond\_MOS} + f_{sw} (E_{off\_MOS} + E_{on\_MOS}) \quad (16)$$

$$P_{loss\_IGBT}(I_F, T_{j\_IGBT}) = (D - f_{sw} \cdot T_{off\_delay}) E_{cond\_IGBT} + f_{sw} \cdot E_{off\_IGBT} \quad (17)$$

where  $D$  is the duty cycle of the dc/dc buck converter, the  $f_{sw}$  is the switching frequency. The (16) and (17) show that the power losses of the SiC MOSFET and IGBT inside the hybrid switch are functions of the gate turn-OFF delay time. Because the junction temperature of the power device is dependent on its power loss and the two internal switches' junction temperatures inside the hybrid switch are strongly affected by its gate turn-OFF delay time.

### C. Loss Model Verification

In this article, a 20-kHz hybrid switch-based dc/dc buck converter prototype is built, as shown in Fig. 6.

The CREE 1200 V/12.5 A SiC MOSFET (C2M0160120D) and Infineon 1200 V/25 A Si IGBT (IGW25N120H3) are selected to constitute the hybrid switch. The CREE 1200 V/12.5 A SiC MOSFET (C2M0160120D) and the CREE 1200 V/15 A SiC Schottky diode (C4D15120D) are parallel connected as the freewheeling diode to achieve the synchronous rectification

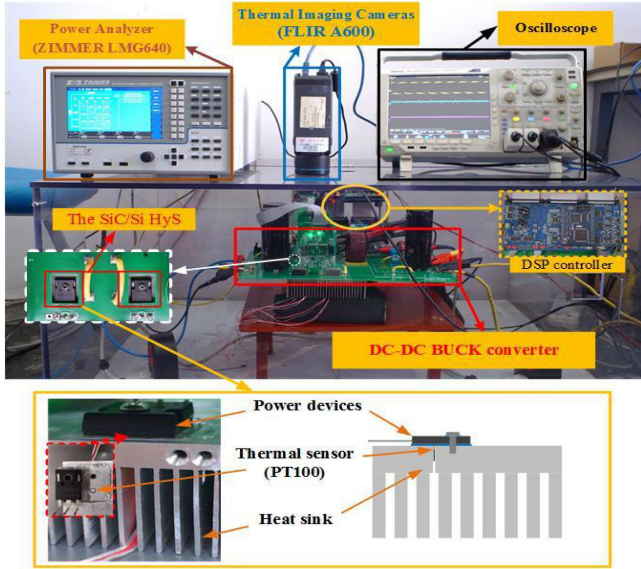


Fig. 6. Buck converter prototype based on Si/SiC hybrid switch.

TABLE I  
PARAMETERS OF THE HYBRID SWITCH BUCK CONVERTER

No.	Parameters	Values
1	Supply voltage	600 V
2	Output voltage	300 V
3	Power rating	1~9.5 kW
4	Switching frequency	20 kHz
5	Inductor	1 mH
6	Output capacitor	2200 $\mu$ F

operation. They are assembled on a heat sink, and a designed gate driver is used to achieve the specific gate control patterns of the hybrid switch. The case temperature of the hybrid switch is measured by the temperature sensor PT100 from the bottom side as show in Fig. 6. The parameters of the buck converter are shown in Table I.

In the steady-state operation of the buck converter, the average junction temperature of the hybrid switch's two internal devices can be calculated with the aid of their thermal resistances  $R_{th}$ . Therefore, the simplified thermal equivalent circuit diagrams of the hybrid switch can be expressed as shown in Fig. 7.

The  $R_{th(j-c)}_{MOS}$  and  $R_{th(j-c)}_{IGBT}$  are the junction to case thermal resistance of the SiC MOSFET and IGBT, respectively. As given in the manufacturer's datasheets, they are 0.9 and 0.46 K/W, respectively.  $R_{th(c-s)}_{MOS}$  and  $R_{th(c-s)}_{IGBT}$  are the case to heat sink thermal resistance of the SiC MOSFET and IGBT, respectively, which are determined by the cooling strategy adopted by the hybrid switch-based converter.  $R_{th(s-a)}$  is the heat sink to ambient thermal resistance, which is dependent on the geometry of the heat sink and the heat dissipation way of the hybrid switch-based converter. Because the package of

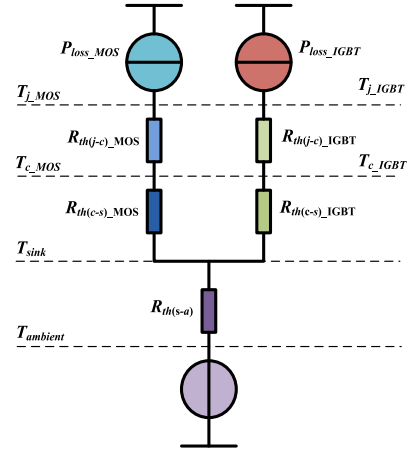


Fig. 7. Simplified thermal equivalent circuit diagram of the hybrid switch.

both the internal SiC MOSFET and the IGBT are TO-247 in this experiment, and they are assembled on the same heat sink, the  $R_{th(c-s)}$  of the SiC MOSFET and IGBT are considered the same. The relationship between the average junction temperature and the power loss of the power device in the steady state can be expressed as

$$T_j = T_c + R_{th(j-c)} \cdot P_{loss}. \quad (18)$$

The power losses of the hybrid switch are temperature-dependent in the loss model. In order to obtain the precise power loss and junction temperature of the hybrid switch, the losses based on the power loss model can be determined iteratively at the calculated junction temperature. In the first duty cycle, the starting value is the power dissipation at the case temperature measured by the temperature sensor PT100, and then a new and more precise loss value is generated. After several iterations, the final power loss value and junction temperature will be reached. In the following duty cycle, the loss and junction temperature can be obtained recursively. The dependency of the power loss and the junction temperature of the hybrid switch on the gate turn-OFF delay time at 6-kW output power rating is shown in Figs. 8 and 9, respectively.  $P_{loss\_IGBT\_m}$  and  $P_{loss\_MOS\_m}$  are the measured power losses of the internal IGBT and the SiC MOSFET, respectively, which are calculated by the integral of the measured voltage and current waveforms over the period of a duty cycle in the steady state.  $T_{j\_MOS\_m}$  and  $T_{j\_IGBT\_m}$  are the calculated junction temperature of the internal IGBT and the SiC MOSFET using (18) based on the  $P_{loss\_IGBT\_m}$  and  $P_{loss\_MOS\_m}$ , respectively.  $P_{loss\_IGBT\_c}$  and  $P_{loss\_MOS\_c}$  are the calculated power loss of the IGBT and the SiC MOSFET based on the loss model, respectively.  $T_{j\_MOS\_c}$  and  $T_{j\_IGBT\_c}$  are the estimated junction temperature of the internal IGBT and the SiC MOSFET based on  $P_{loss\_IGBT\_c}$  and  $P_{loss\_MOS\_c}$ , respectively. The calculated power loss and junction temperature of the hybrid switch based on the loss model are consistent with those of the measured power loss and junction temperature.

When the gate turn-OFF delay time of the hybrid switch is very short, the IGBT's large power loss makes its junction

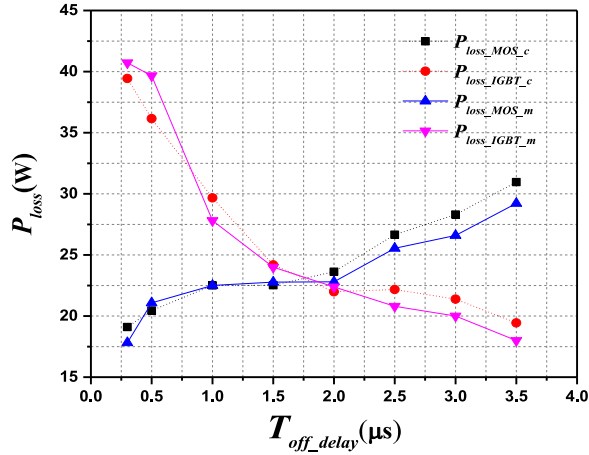


Fig. 8. Comparison of the measured power loss and calculated power loss.

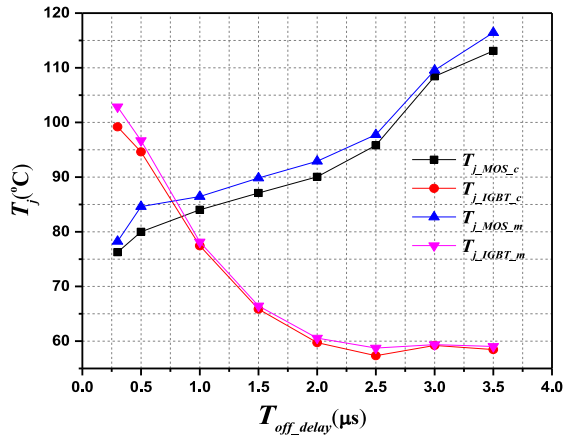
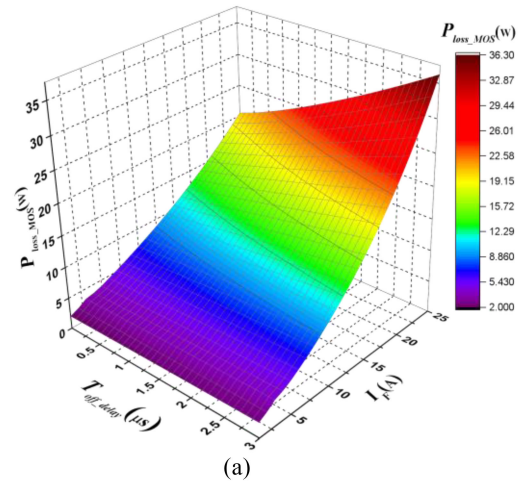


Fig. 9. Comparison of the measured and junction temperature calculated junction temperature.

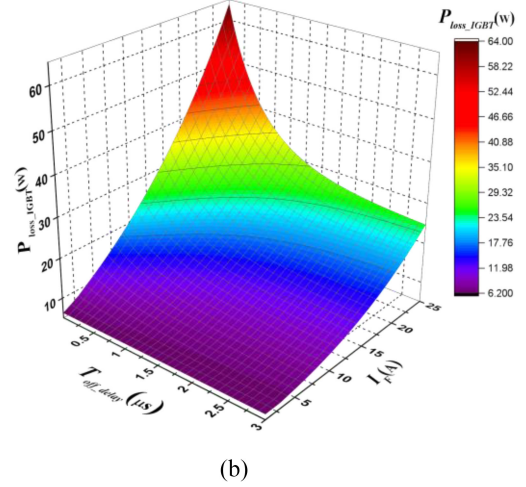
temperature much higher than that of the SiC MOSFET. When the gate turn-OFF delay time of the hybrid switch is too long, the large additional conduction loss of SiC MOSFET makes its junction temperature much higher than that of the IGBT. For example, the junction temperature of the SiC MOSFET is 50 °C higher than that of the IGBT at  $T_{off\_delay} = 3.5 \mu s$ . The power losses of the SiC MOSFET and IGBT are evenly distributed when the gate turn-OFF delay time at  $T_{off\_delay} = 1.8 \mu s$ . Because the thermal resistance of the two internal devices are different, their junction temperature are balanced at  $T_{off\_delay} = 0.8 \mu s$ .

#### D. Loss Distribution and Junction Temperature Unbalance Discussion

The losses and junction temperatures of the hybrid switch's two internal devices are strongly dependent on its gate turn-OFF delay time and the load conditions of the hybrid switch-based converter. In order to illustrate the dependency of the loss and junction temperature distribution of the hybrid switch on its gate turn-OFF delay time and operation current, the case to heat sink thermal resistance  $R_{th(c-s)}$  and the heat sink to ambient thermal resistance  $R_{th(s-a)}$  are set to be 0.25 and 2 K/W, respectively



(a)



(b)

Fig. 10. Dependency of the hybrid switch's power loss on gate turn-OFF delay time and operation current. (a) SiC MOSFET. (b) IGBT.

and the ambient temperature is set to be 27 °C. The power loss dependency of the SiC MOSFET and IGBT on the gate turn-OFF delay time and forward current rating are show in Fig. 10. The x-axis and y-axis represent the gate turn-OFF delay time and the operation current rating, respectively. And the z-axis is the total power loss of the SiC MOSFET or the IGBT.

Because the conduction loss and switching loss of the SiC MOSFET and the IGBT inside the hybrid switch at the small operation current is small, the dependency of the loss distribution between the two devices on the gate signal's delay time is weak. When the load current is large, the loss distribution between the two devices is strongly influenced by the gate signal's delay time. When the gate turn-OFF delay time increases, the power loss of the SiC MOSFET increases, while the power loss of the IGBT decreases. The dependency of the total power loss of the hybrid switch on the gate signal's turn-OFF delay time and operation current are shown in Fig. 11. When the operation current of the hybrid switch is 25 A, the minimum total power loss of the hybrid switch can be achieved if the gate turn-OFF delay time is around 1.5  $\mu s$ . And the minimum total power loss of the hybrid switch under a load current of 11 A can be achieved if the gate turn-OFF delay time is around 2  $\mu s$ . In one word, the optimal

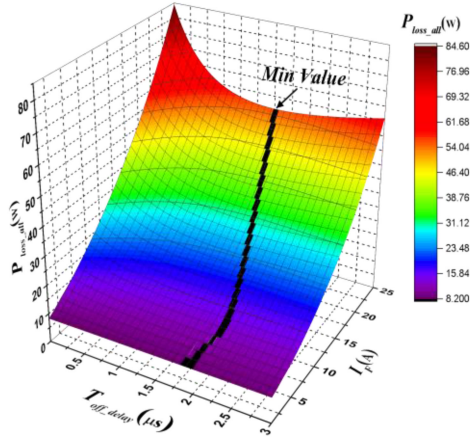


Fig. 11. Dependency of the hybrid switch's total power on gate turn-OFF delay time and operation current.

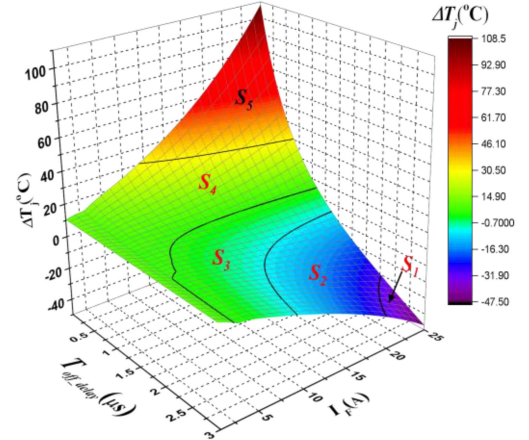


Fig. 13. Dependence of the hybrid switch's junction temperature difference on gate turn-OFF delay time and operation current.

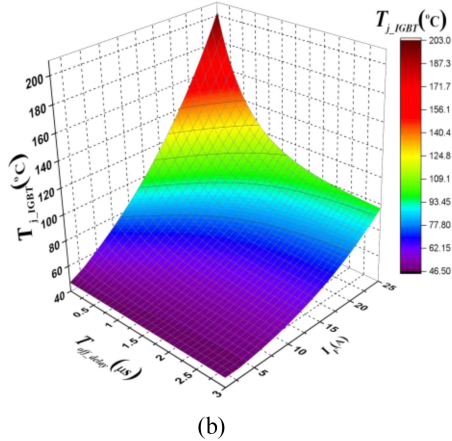
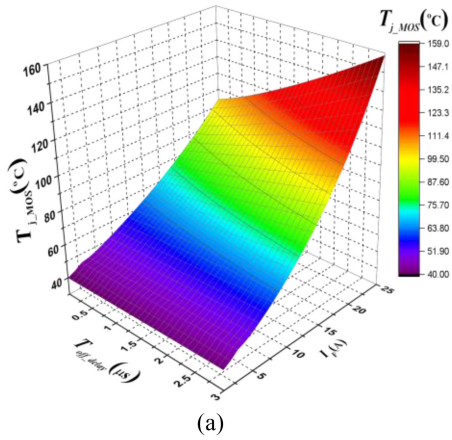


Fig. 12. Dependency of the hybrid switch's junction temperature on gate turn-OFF delay time and operation current. (a) SiC MOSFET. (b) IGBT.

gate turn-OFF delay time to achieve the converter's minimum total power loss is varying with the operation current.

The junction temperature dependency of the SiC MOSFET and IGBT on the gate signal's turn-OFF delay time and forward current rating are shown in Fig. 12. The junction temperature distribution of the hybrid switch is similar to its loss distribution.

TABLE II  
JUNCTION TEMPERATURE DIFFERENCE AND SMALLEST  
JUNCTION TEMPERATURE SAFETY MARGIN

Area	Boundary Lines of Areas	Minimum $T_{j\_margin}$
$S_1$	$\Delta T_j \leq -30\text{ }^\circ\text{C}$	SiC MOSFET overheating
$S_2$	$-30\text{ }^\circ\text{C} < \Delta T_j \leq -5\text{ }^\circ\text{C}$	$T_{j\_margin} > 5\text{ }^\circ\text{C}$
$S_3$	$-5\text{ }^\circ\text{C} < \Delta T_j < 5\text{ }^\circ\text{C}$	$T_{j\_margin} > 25\text{ }^\circ\text{C}$
$S_4$	$5\text{ }^\circ\text{C} \leq \Delta T_j < 30\text{ }^\circ\text{C}$	$T_{j\_margin} > 7\text{ }^\circ\text{C}$
$S_5$	$\Delta T_j \geq 30\text{ }^\circ\text{C}$	IGBT overheating

It is because the junction temperature is strongly dependent on the loss of the power device. When the operation current is large, too small or too large gate turn-OFF delay time induce the severe junction temperature unbalance between the two internal devices. The severe junction temperature unbalance may make the IGBT or SiC MOSFET's junction temperature reach its junction temperature limit more easily and reduce the hybrid switch's safe junction temperature margin.

The junction temperature difference of the two internal switches of the hybrid switch is defined as

$$\Delta T_j = T_{j\_MOS} - T_{j\_IGBT} \quad (19)$$

where  $T_{j\_MOS}$  and  $T_{j\_IGBT}$  is the estimated junction temperature of the SiC MOSFET and the IGBT, respectively. The dependence of  $\Delta T_j$  on the gate turn-OFF delay time and operation current is shown in Fig. 13. The z-axis is the  $\Delta T_j$  between the SiC MOSFET and the IGBT. According to the degree of the junction temperature difference between the two internal devices, the  $\Delta T_j$  is divided into six areas.

The boundary lines of these six areas and the minimum  $T_{j\_margin}$  within these areas are shown in Table II. The  $T_{j\_margin}$  is the junction temperature safety margin of the hybrid switch at a certain forward current rating and gate turn-OFF delay time,

which is defined as

$$T_{j\_margin}(T_{off\_delay}, I_F) = T_{j\_limit} - \max[T_{j\_MOS}(T_{off\_delay}, I_F), T_{j\_IGBT}(T_{off\_delay}, I_F)] \quad (20)$$

where  $T_{j\_limit}$  is the upper maximum operation junction temperature limit of the hybrid switch. The minimum  $T_{j\_margin}$  is the smallest junction temperature safety margin within the operation areas. Therefore, the larger minimum  $T_{j\_margin}$ , the more reliable operation condition of the hybrid switch can be achieved within this area.

When the hybrid switch is operated within the area S1 and S5, the absolute junction temperature difference between its internal device is more than 30 °C, which may easily make the junction temperature of its one internal device be close to or even over its maximum operation junction temperature limit. Therefore, the S1 and S5 are not the preferred operation areas for the hybrid switch.

When the hybrid switch is operated within the area S2 or S4, the absolute junction temperature difference between its internal devices is between 5 °C and 30 °C. The high junction temperature unbalance inside the hybrid switch reduces the operation junction temperature safety margin of the hybrid switch. The minimum  $T_{j\_margin}$  is higher than 5 °C and 7 °C within the operation area S2 and S4, respectively.

The junction temperature difference of the hybrid switch is smaller than 5 °C when the hybrid switch is operated within S3 operation area. Benefiting from the almost balanced junction temperature of the hybrid switch, the largest junction temperature safety margin is achieved during the S3 area. The minimum  $T_{j\_margin}$  is higher than 25 °C within the area S3. The large junction temperature safety margin of the hybrid switch improves the maximum output power capability and over load capability of the hybrid switch-based converter. The optimal gate turn-OFF delay time to achieve the hybrid switch's operation within the S3 area is varying with the operation current.

### III. ACTIVE THERMAL CONTROL OF HYBRID SWITCH

In the previous reported studies, the fixed gate control delay time of the hybrid switch is commonly used to reduce the total switching loss of the hybrid switch. However, the optimal gate control delay time of the hybrid switch needs adjustment according to the varied operation conditions of power converters because its total power loss, junction temperatures, and junction temperature difference are strongly dependent on the gate turn-OFF delay time and operation current. The inappropriate fixed gate control delay time risks one internal device's junction temperature subjected to its operation junction temperature upper limit within a wide-load condition, which endangers the safe operation of the hybrid-switch-based converter under certain extreme operation conditions.

#### A. Fixed Gate Turn-OFF Delay Time Control

When the output power of the dc/dc buck converter varying with the load condition variation, the junction temperatures of

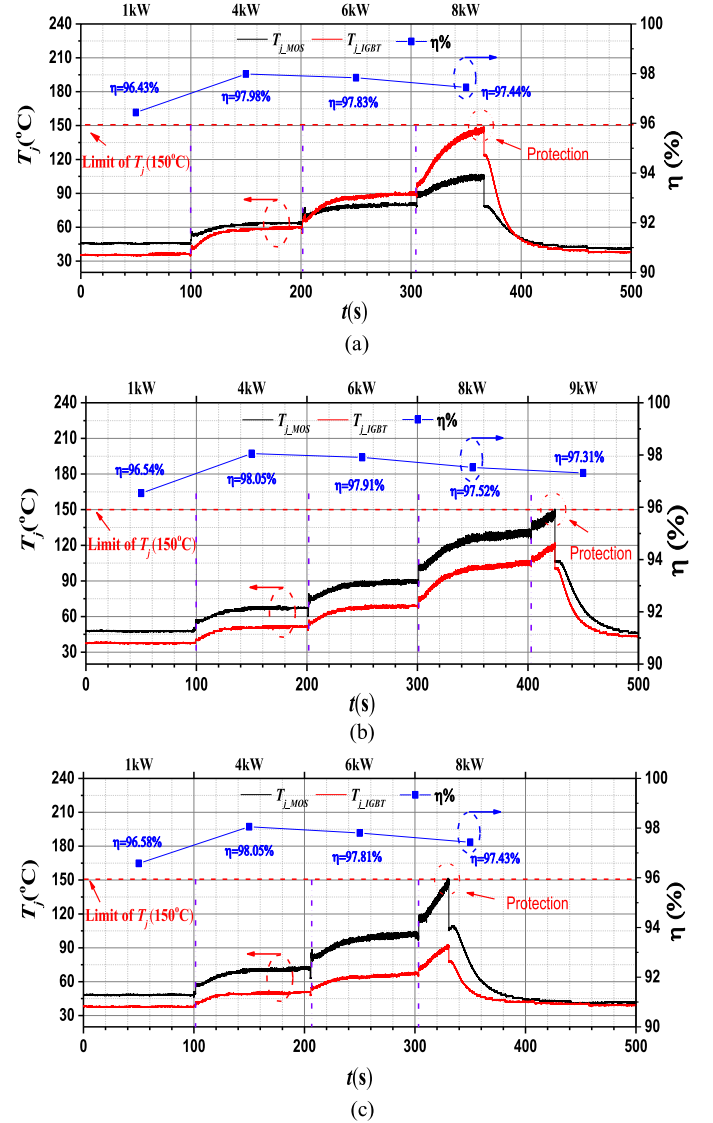


Fig. 14.  $T_j$  of the hybrid switch at several fixed gate turn-OFF delay time. (a)  $T_{off\_delay} = 0.6 \mu s$ . (b)  $T_{off\_delay} = 1.8 \mu s$ . (c)  $T_{off\_delay} = 3 \mu s$ .

the SiC MOSFET and the IGBT inside the hybrid switch and the measured efficiency of the dc/dc converter at three types fixed gate turn-OFF delay times are shown in Fig. 14. The conversion efficiency of the hybrid switch measured by the power analyzer ZIMMER LMG640.

When the output power is 1 kW, the 96.58% conversion efficiency of the converter is achieved at  $T_{off\_delay} = 3 \mu s$ , which is higher than those at  $T_{off\_delay} = 0.6 \mu s$  and  $T_{off\_delay} = 1.8 \mu s$ . This is because the large gate turn-OFF delay time reduces the total power loss of the hybrid switch under the light-load condition. When the output power is 6 kW, the highest 97.91% conversion efficiency of the converter is achieved at  $T_{off\_delay} = 1.8 \mu s$  among these three types fixed gate delay time control mode, which is 0.1% higher than that at  $T_{off\_delay} = 3 \mu s$ . The reason is that the large switching OFF loss of the IGBT at  $T_{off\_delay} = 0.6 \mu s$  and large additional conduction loss of the SiC MOSFET at  $T_{off\_delay} = 3 \mu s$  reduce the conversion efficiency of the hybrid-switch-based converter.

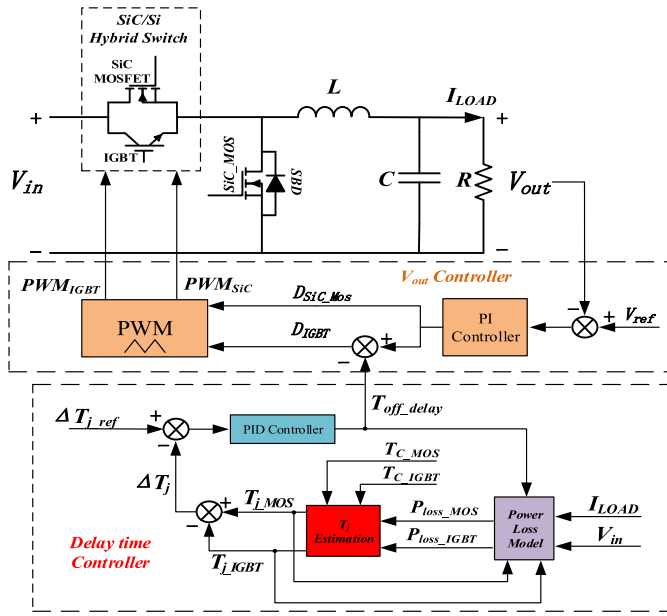


Fig. 15. Block diagram of the active gate turn-OFF delay time controller.

When the output power of the hybrid switch converter is smaller than 6 kW, the junction temperature of the SiC MOSFET and the IGBT are below their operation junction temperature limits at these three types gate delay time control mode. When the output power is increased to 8 kW, the junction temperature of the SiC MOSFET and IGBT is 132 °C and 101 °C, respectively, at  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$ . However, the junction temperature of the IGBT or the SiC MOSFET is higher than its operation junction temperature limit (150 °C) and triggers the over temperature protection at  $T_{\text{off\_delay}} = 0.6 \mu\text{s}$  or  $T_{\text{off\_delay}} = 3 \mu\text{s}$ , while the junction temperature of the corresponding SiC MOSFET or the IGBT is only 100 °C and 91 °C when triggering the protection.

When the output power is increased by 9 kW, the junction temperature of the SiC MOSFET is higher than its operation junction temperature limit at  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$ , which those of the corresponding IGBT is only 120 °C. The severe junction temperature unbalance caused by the fixed gate turn-OFF delay time restricts the full utilization of the two internal devices of the hybrid switch in converter applications. And the maximum output power handling capability of the hybrid-switch-based converter is reduced because one of the internal devices reaches its operation junction temperature limit much earlier than another device under the unbalance junction temperature condition.

### B. Active Gate Delay Time Control

In order to avoid a serious risk of overheating of the hybrid switch's internal device within a wide-load condition, the active gate delay time control strategy based on the electro-thermal coupling loss model is proposed as shown in Fig. 15. The basic control diagram of the Si/SiC hybrid switch buck converter is consisted of the active gate delay time controller and the output

voltage controller. These two controllers are implemented on the TMS320F28335 digital signal processor.

The duty cycle of the buck converter is calculated by the output voltage controller at first. The output voltage controller is realized with a single output voltage control loop to keep the output voltage stable of the hybrid switch buck converter. When using the gate control pattern as shown in Fig. 2, the equivalent duty cycle of the buck converter is determined by the duty cycle of the auxiliary SiC MOSFET. And appropriate reducing the duty cycle of the IGBT could realize the gate turn-OFF delay time of the hybrid switch. Therefore, the output voltage controller determines the duty cycle of the auxiliary SiC MOSFET. And the duty cycle of the IGBT is calculated by the active gate delay time controller to achieve the appropriate gate turn-OFF delay time.

The active gate delay time controller consists of the Si/SiC hybrid switch power loss model, junction temperature estimation unit, and the delay time close loop controller.

First, the power loss of the hybrid switch are calculated based on the electro-thermal coupling loss model calibrated with the measured dc voltage and load current.

Second, the average junction temperatures of the two internal devices under the steady state are estimated based on (18) with the calculated power loss, measured case temperature, and the extracted thermal resistance from the device datasheet.

Then the junction temperature difference  $\Delta T_j$  between the two internal devices is compared to the junction temperature difference reference  $\Delta T_{j\_ref}$ . And the junction temperature difference error as the input of the PID controller to adjust the gate turn-OFF delay time. When the  $\Delta T_j$  between the SiC MOSFET and the IGBT is higher/lower than the reference junction temperature difference  $\Delta T_{j\_ref}$ , the PID controller will adjust the duty cycle of the IGBT to change the gate turn-OFF delay time between the two devices to achieve their junction temperature balance. The parameters of the PID controller can be calculated by the basic Ziegler—Nichols tuning rules, or empirical-based method.

Finally, the gate turn-OFF delay time is used to calibrate the duty cycle of the IGBT to achieve its ZVS turn-OFF while keep the SiC MOSFET's duty cycle unchanged simultaneously.

Because of the duty cycle of the buck converter without change when the active gate delay time controller adjusts the gate turn-OFF delay time, the active gate delay time controller is independent from the output voltage controller and has no effect on the dynamic response and stability of the buck converter.

When the  $\Delta T_{j\_ref}$  is set as the 0 °C, the junction temperatures of the hybrid switch with the active gate turn-OFF delay time control strategy at various load conditions are shown in Fig. 16.

When the output power is 1 kW, the junction temperature of the IGBT is a little smaller than that of the SiC MOSFET. It is because the SiC MOSFET undertakes the most conduction loss and switching loss under the small operation current condition.

When the output power changes from 2 to 8 kW, the junction temperature between the two devices inside the hybrid switch is balanced during the load varying condition. Using the active gate turn-OFF delay time control strategy, the maximum junction temperature of the hybrid switch is about 112 °C under 8-kW

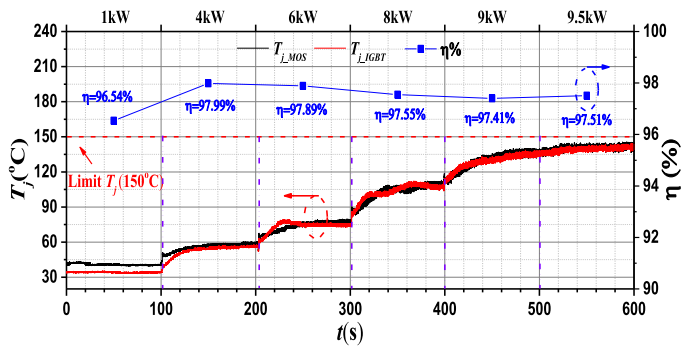


Fig. 16.  $T_j$  of the hybrid switch with the active junction temperature balance control.

load condition, which is 20 °C smaller than that at the fixed  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$  under the same load condition.

When the junction temperature of the hybrid switch reaches the operation junction temperature limit, the maximum output power handling capability is 9.5 kW using the active gate turn-OFF delay time control strategy, which is 1.5 kW larger than that at the  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$  fixed gate turn-OFF delay time control mode.

When using the active gate turn-OFF delay time control, the conversion efficiency of the buck converter increases by 0.03% compared to the fixed  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$  control mode under 8 kW output power condition. When the output power is 6 kW, the conversion efficiency with the active gate delay time control decreases by 0.02% compared to at the fixed  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$ , and increases by 0.06% and 0.08% compared to the at the  $T_{\text{off\_delay}} = 0.6 \mu\text{s}$  or at the  $T_{\text{off\_delay}} = 3 \mu\text{s}$ , respectively. Therefore, achieving the balanced junction temperature between the two internal devices inside the hybrid switch is without obvious compromising on the conversion efficiency of the hybrid switch converter within a wide load range. Furthermore, the hybrid switch with the active gate turn-OFF delay time control achieves the larger safe operation junction temperature margin, more reliable working condition, and larger maximum output power capability within a wide-load condition compared to the fixed gate turn-OFF delay time control mode.

### C. Reduction of the Junction Temperature Swing

As the power loss's magnitude of the SiC MOSFET and the IGBT inside the hybrid switch depends on the gate turn-OFF delay time and the load condition, the invoked magnitude of the junction temperature swings also varies. Usually, the transient junction temperature swing of the power device caused by the switching and conduction losses during a PWM period is small magnitude and most of them are filtered out by device thermal capacitances [25]. On the other hand, the average junction temperature swing of the device caused by the converter's load variation is in large magnitude and creates cyclic heating and cooling process of power device, also called thermal cycles [24]. The thermal cycles are the main cause of failures and destruction of the power devices over long-term operation. Therefore, the hybrid switch's average junction temperature swing difference between using the fixed gate turn-OFF delay time control and

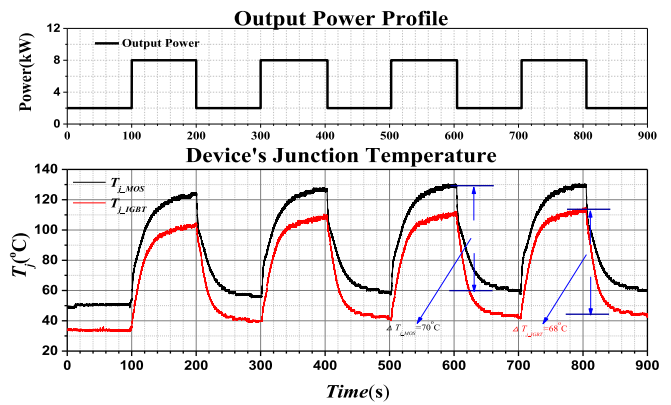


Fig. 17. Average junction temperature swing of the hybrid switch with fixed gate turn-OFF delay time.

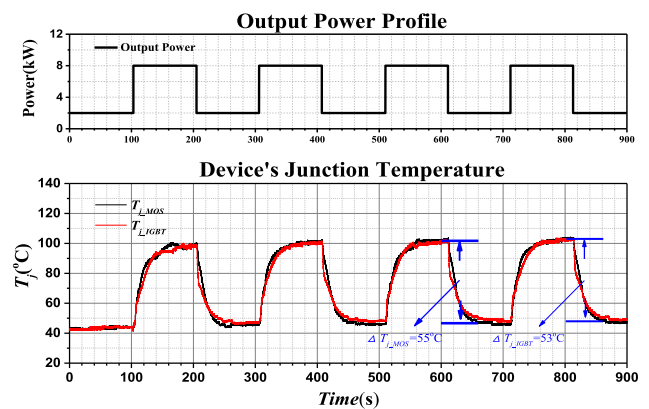


Fig. 18. Average junction temperature swing of the hybrid switch using the active gate turn-OFF delay time control.

the active gate turn-OFF delay time control are analyzed and compared.

When the load condition of the hybrid switch buck converter cycles between 2 and 8 kW, the junction temperatures of the hybrid switch at fixed  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$  and using the active gate turn-OFF delay time control are shown in Figs. 17 and 18, respectively.

The severe junction temperature unbalance at the conventional fixed gate control delay strategy induces a large junction temperature swing of the hybrid switch during the load condition fluctuations. The junction temperature swing of the SiC MOSFET and the IGBT is 70 °C and 66 °C during the load fluctuation, respectively. When using the active gate delay time control, the junction temperatures are balanced between the two internal devices during the load fluctuation. Therefore, the same junction temperature swings of the two internal devices are achieved, which avoids the accelerating aging of one internal device caused by its larger junction temperature swing during the load fluctuation condition. Moreover, because of the balance junction temperature leading to a smaller junction temperatures compared to the fixed  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$  gate control mode under the same load condition, the SiC MOSFET and the IGBT inside the hybrid switch has smaller magnitude of the junction temperature swing under the same cyclic load conditions. As shown in Fig. 18, the

junction temperature swings of the SiC MOSFET and the IGBT are 55 °C and 54 °C during the load fluctuation, respectively. The maximum junction temperature swing of the hybrid switch with the active gate turn-OFF delay time control is 15 °C smaller than that at the fixed  $T_{\text{off\_delay}} = 1.8 \mu\text{s}$ . It means that the active gate delay time control strategy is helpful to improve the long-term reliability of the hybrid switch.

#### IV. CONCLUSION

In this article, a novel active gate delay time control method based on the electro-thermal coupling loss model of the Si/SiC hybrid switch is proposed to achieve the minimum operation junction temperature difference of the hybrid switch's two internal devices within a wide load range. Different from the conventional fixed gate delay time control, the proposed method continuously adjusts the optimized gate control delay time of the hybrid switch according to the operation conditions of the converter, which helps improve the maximum operation junction temperature margin, and reduce the junction temperature swing during the cyclic load condition of the hybrid switch. The active gate turn-OFF delay time controller is independent to the converter's output voltage controller and does not affect the dynamic performance and stability of the hybrid switch converter. Using the active gate delay time control method, the hybrid switch achieves the 18% rise in maximum power handling capability, 20 °C reduction in maximum junction temperature under the 8 kW power rating and 15 °C reduction in maximum junction temperature swing during the same load cyclic compared with the conventional approach in the 20 kHz dc/dc buck converter applications.

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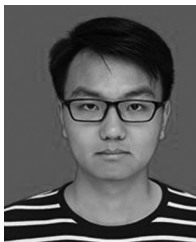
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